New front end board for ILD Si-W ECAL

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CALICE WEEK 24-26/03/2021

Electrical long SLAB

Success of assembly of 8 boards chained 2017-2018

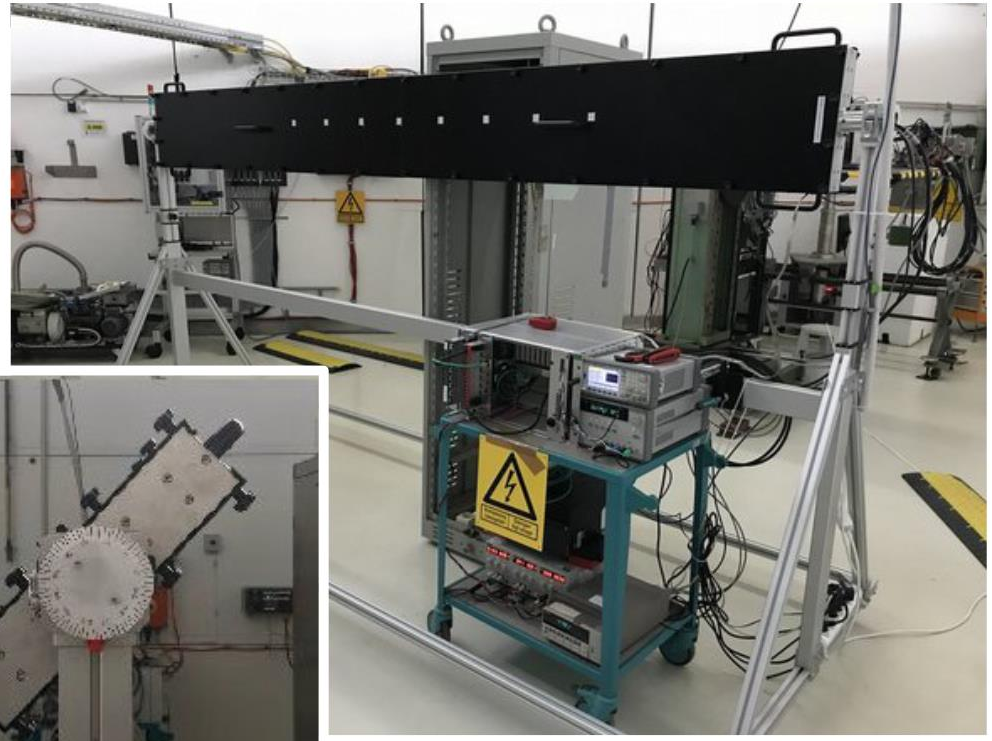
- Test beam @DESY 2018
- Results (see presentation @ LCWS 2018)

Confirm measure after TB

- Voltage drop cross with bandgap distribution

Feedback

- **Important voltage drop (5%)**
- Need extra electronics to configure more than 4 boards
- Need too many manipulations to move or replace board
- Mini wafers not adapted to observe cumulative effect

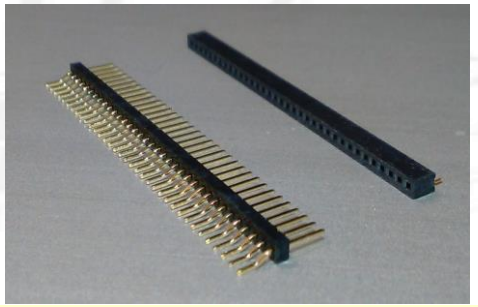


For final project, we need new board & new mechanics

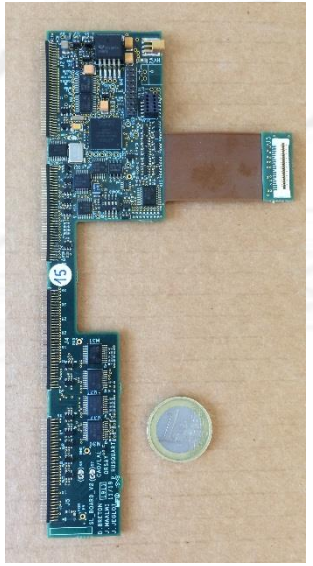
→ Move to physics long SLAB (fully equipped of 6’’ Si wafers

Compact Readout electronics

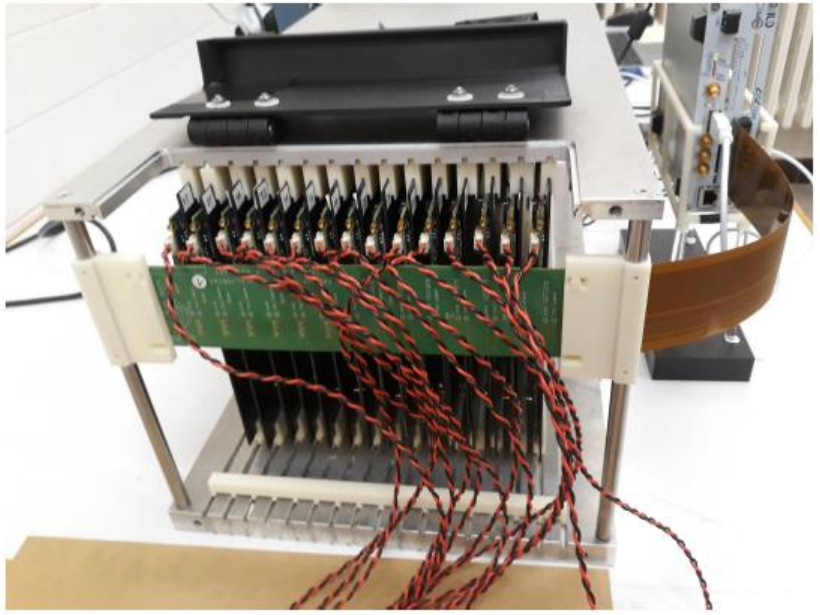
- In the last 3 years, a new compact readout electronics have been developed by IJCLab. These electronics are composed by:
- The **SL-Board** :
  - It is interfaced to the Front-End board via flat connectors : GradConn (1,5 mm high)
  - Its **size** is compatible with the final detector requirements.
  - It **limits the current delivered to the Slab** to ~ **100 mA :**
    - Need **capacitors** on the Front-End board to store the charge during the **power pulsing**
  - Configuration (slow control) and readout through 2 partitions (< Fev12 like)
- The C**ORE-Kapton** and **CORE-Module** :
  - It permits to **synchronise** and **readout** up to 15 x 2 Layers (~30 k channels)



Gradconn connectors (1,5 mm high)



SL – Board V2



15-Layer prototype with SL-Board, CORE kapton and CORE module (~ 15 000 channels)

- Collaboration between IJCLab and LLR to develop a new Si-W Ecal Front End Board :
  - Compatible with the new compact readout electronics
  - Benefits from experience of the long Slabs developed by LLR.

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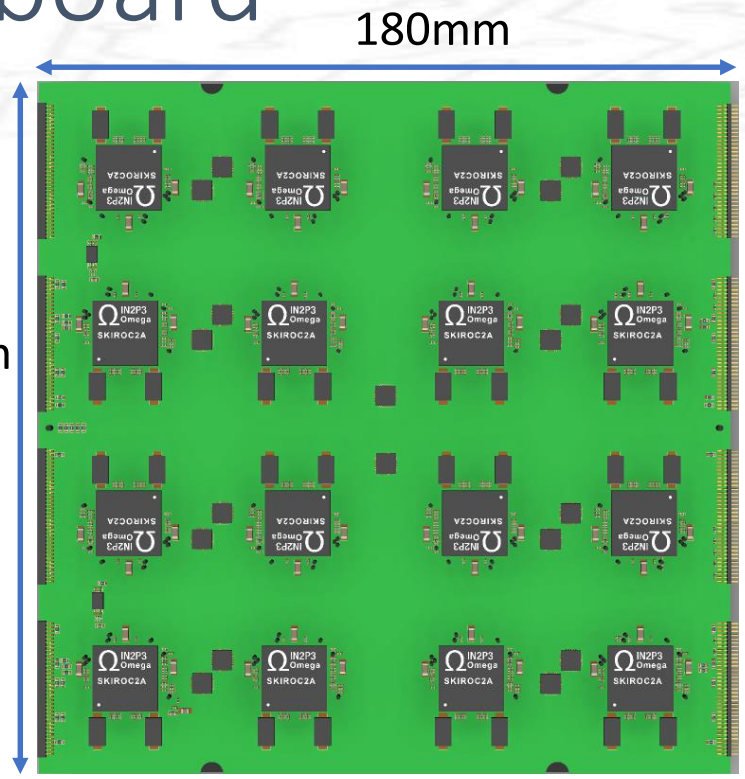
Challenges of the new Front End Board

- **Optimise Power Pulsing Mode:**
  - The new philosophy is to **limit the current** through the Slab (current limiter present on the SL Board). This will permit to :
    - Avoid driving high currents through the connectors and makes the current peaks local around the SKIROCs chips.
    - Avoid voltage drop along the slab.
    - Temperature uniformity
- **Clean clock distribution** all over the slab :
  - For slow control and readout.
- Parallel configuration and readout over 2 partitions. (< Fev12 like)
- Easy disassembly and full individual test for ASUs
  - Use of flat connectors for connexion between boards.
- Drive high voltage up to 350V for 750µm wafer (through the connectors)

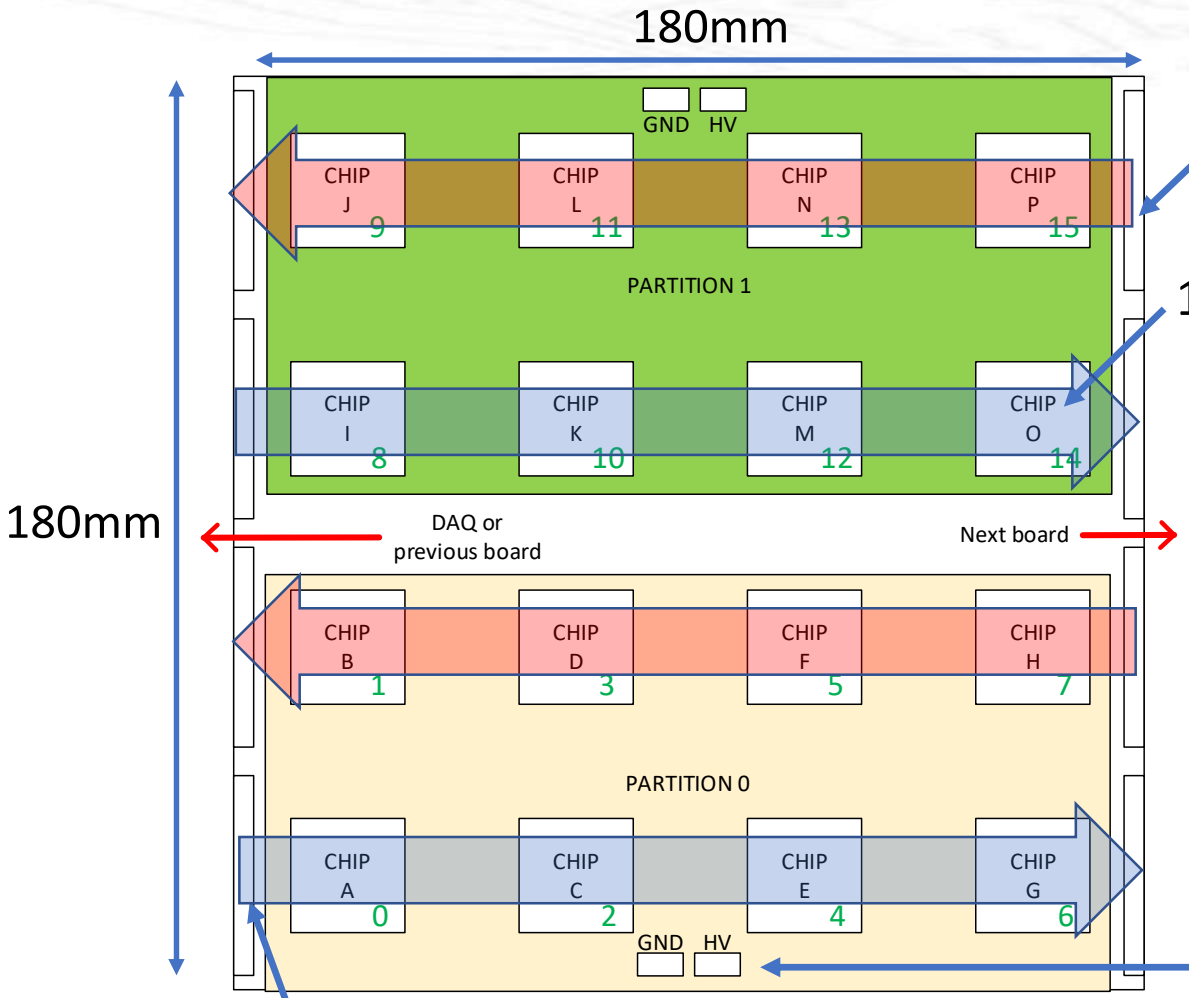
Properties of the new front end board

- 16 chips Ωmega SK2A to read pixels
- 2 power supply AVDD and DVDD
  - Generate local analog power per chip
  - Generate local digital power per partition
- 1024 pixels on bottom side to glue 4 x 6’’ Si wafers
- Up to 10 boards configured
- Keep or improve performances (ex: S/N of 20)
- Precision on flatness, dimensions, … ±25µm



3D view from Cadence Allegro

Board synoptic



4x 35 pins female connector

Gradconn BB02-WF352-K03-000000

16 chips Ωmega SK2A

2 partitions for slowcontrol and data flow.

→ Could be link or bypass with 0Ω resistor

→ Test mode for 1 chip only per partition

Stand-alone HV distribution

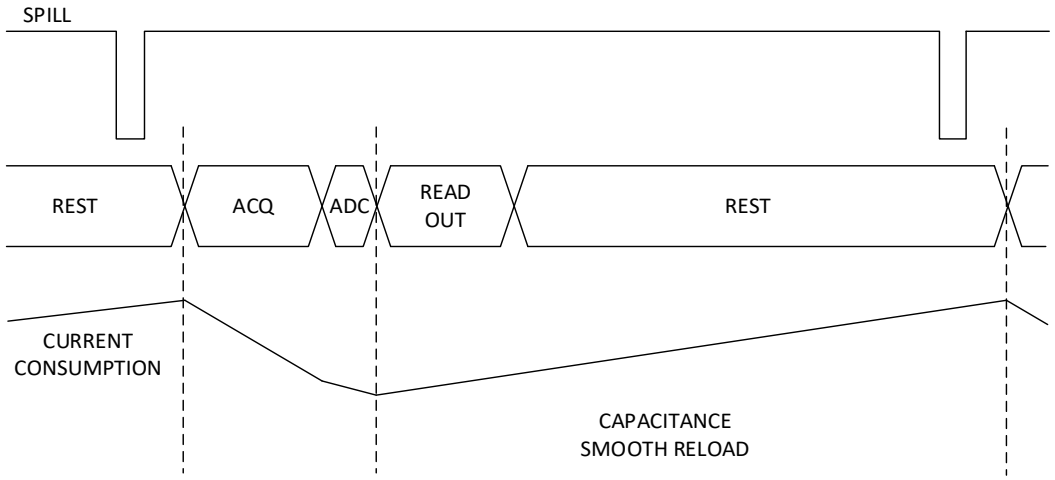
→ More flexibility: testing & set-ups

Choose solution for HV connexion

4x 35 pins male connector

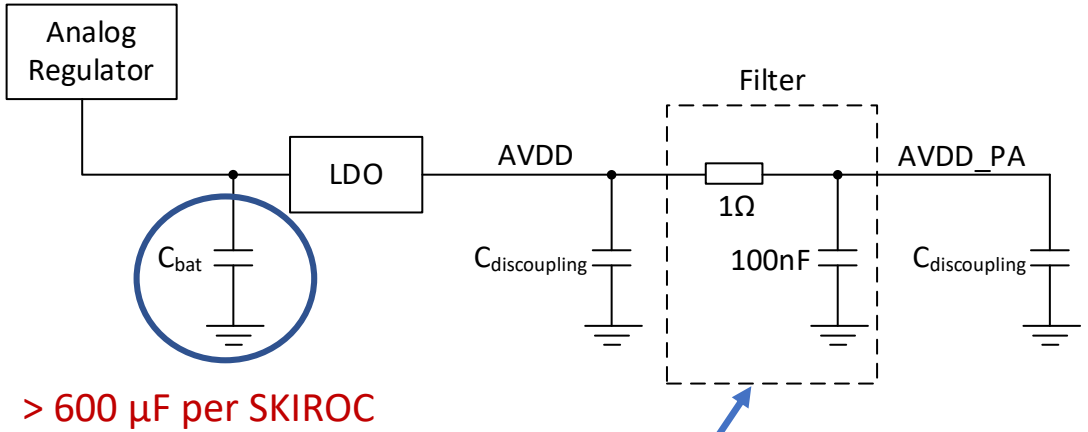
Antelec AM1C100352GCMSH1BA

Power distribution and power pulsing



On the electrical long slab (8 boards chained), we measure important voltage drop (5%) due to:

- 50%: Resistivity of vdda layer
  - **Propagation of high current to the power supply (300mA / board in acquisition)**
- 50%: Ωmega SKIROC 2 Bandgap distribution



> 600 µF per SKIROC

Add filter to generate local preamplifier power supply

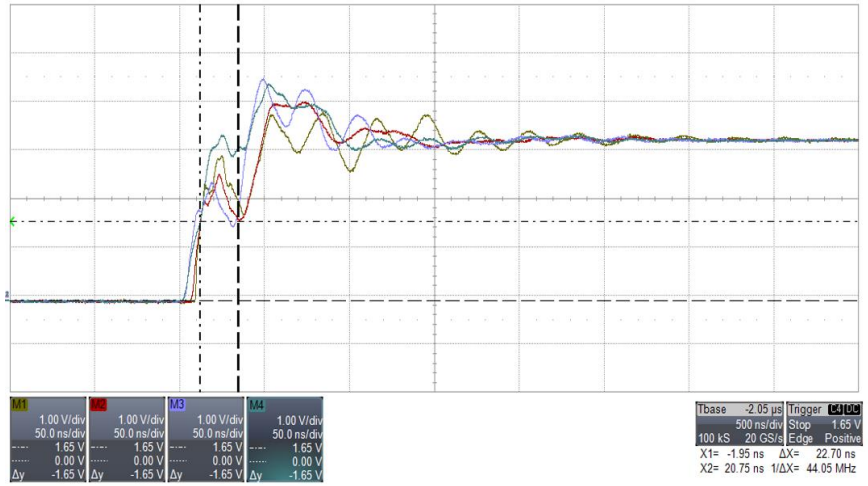
We decide to :

- **Limit the current** through the slab.
- Add **large capacitors with low ESR** for local **energy storage** (around each SKIROC chip)
- Generate local power supply with **LDO** (Low Drop Out) to remove **voltage variations**

Configuration lines (1/2)

In the electrical long SLAB, we have some difficulties to configure more than 4 boards. Configuration clock line is not design for variable number of boards chained.

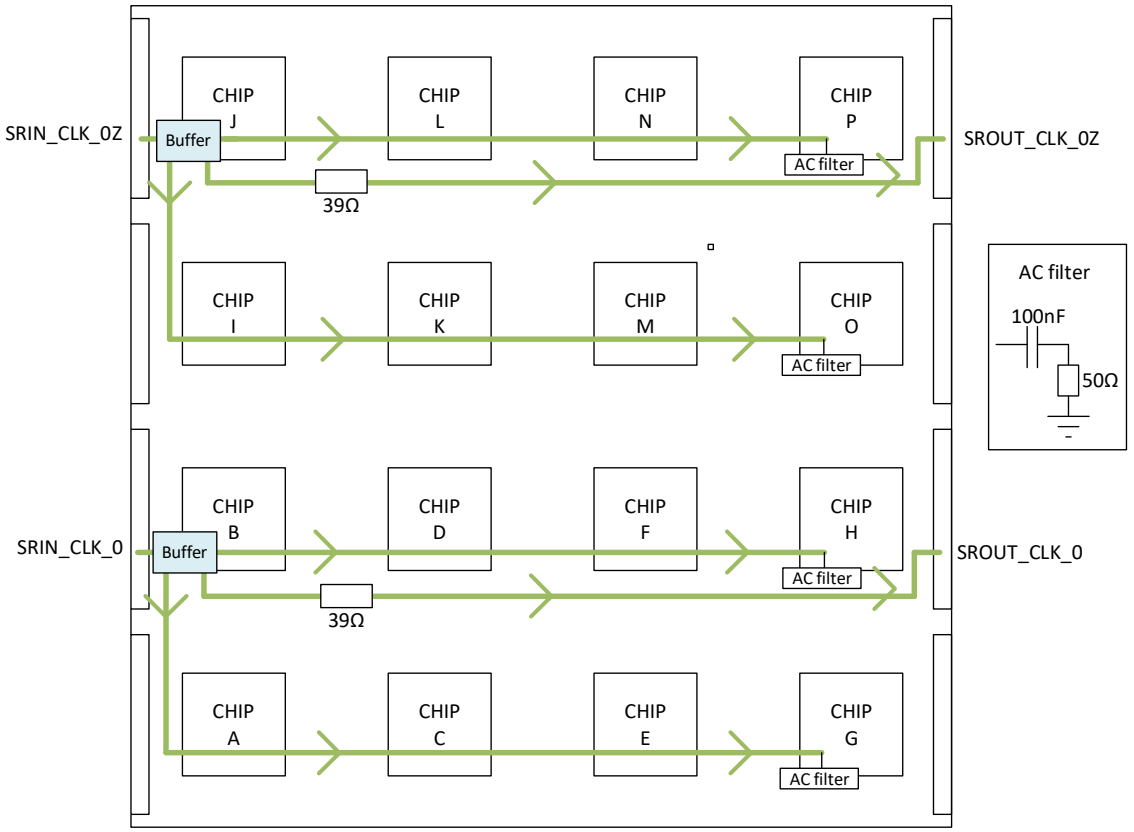
→ Only 1 buffer upstream drive all readout chips, not adapted for variable wire length.



→ Need long studies to find solution with hardware

- Make simulations with Sigrity
- Place filter to shift the reflection effect on the configuration clock

Configuration lines (2/2)



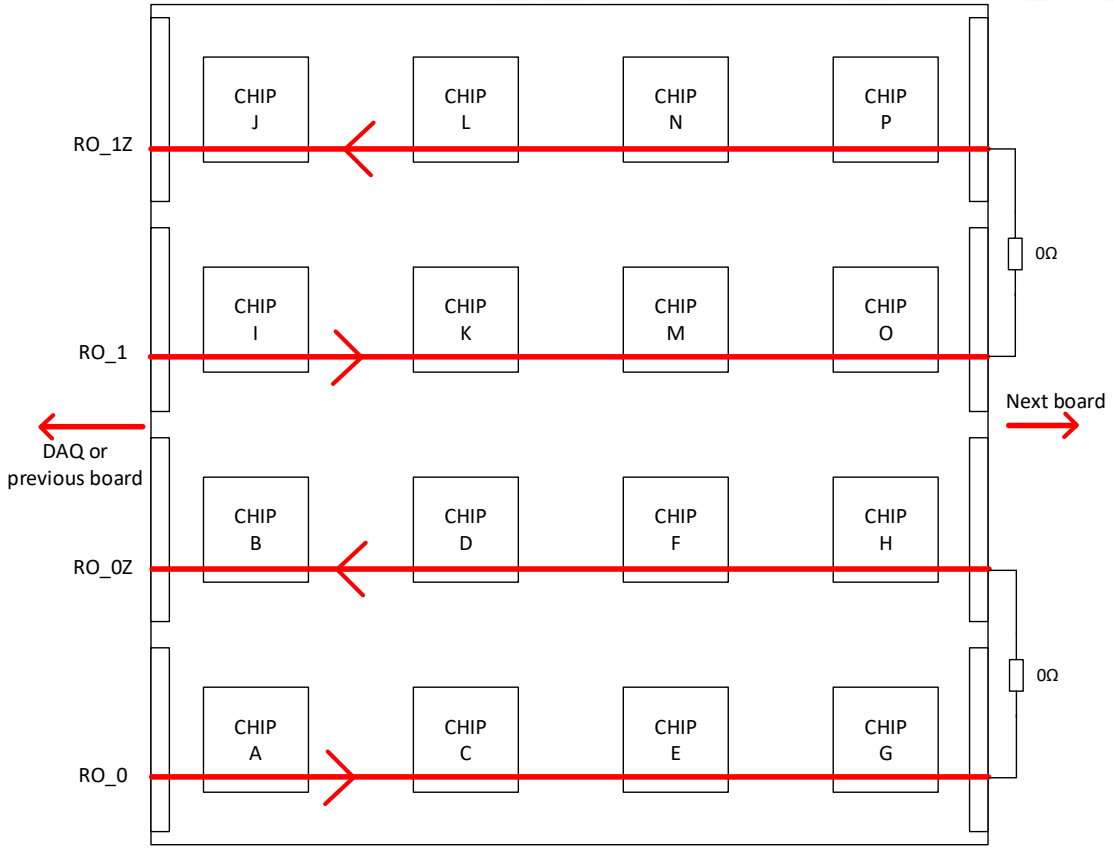
Need system to reduce length of clock line and load capacitors.

→ Add buffer or logic gates, dedicated per local partition and for next board

→ Add AC filter to reduce reflection effect on each partition.

→ Configuration clock is drawing to limit stub and reflection

Data lines



Each chip is chained in coil per partition.

Ωmega SK2A chips are not design to drive signal on 180 cm (10 boards).

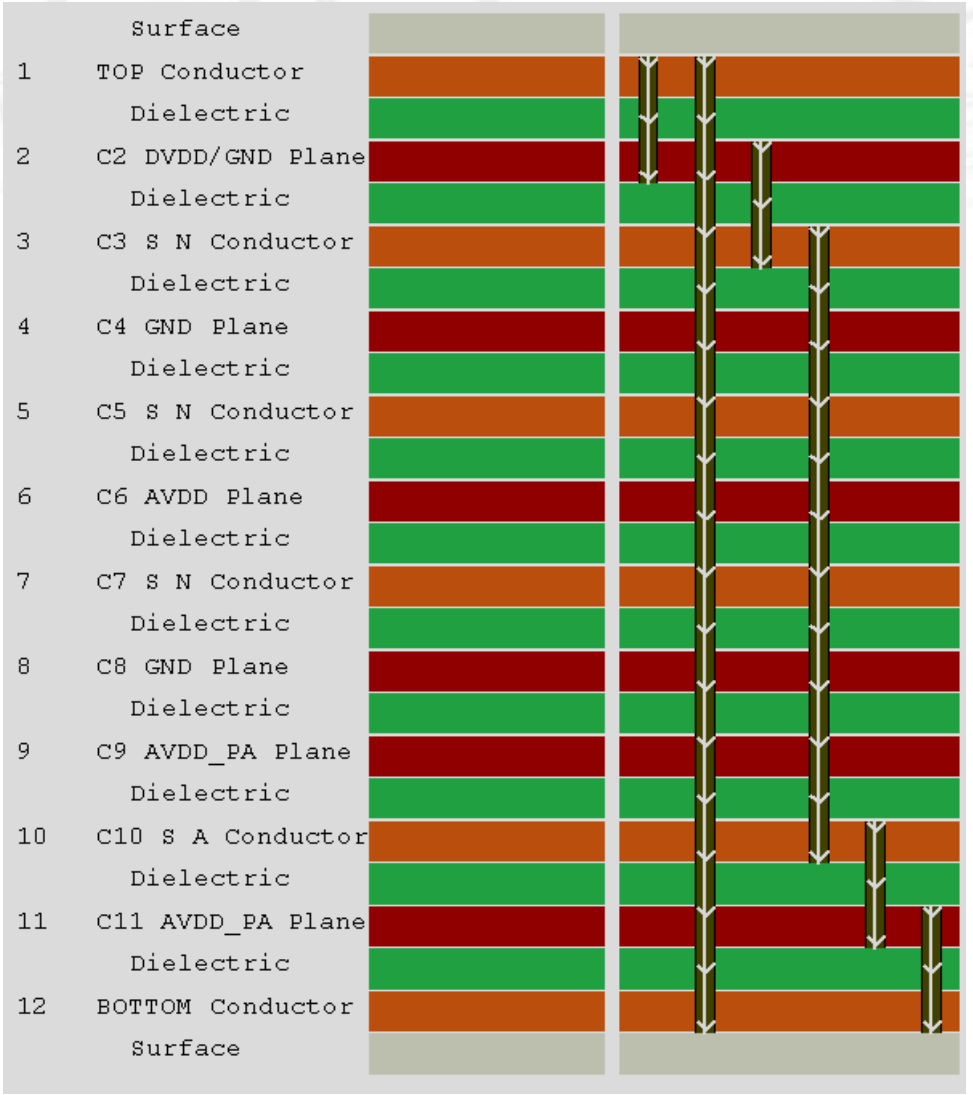
Possibility to bypass chip if necessary with slowcontrol or shunt resistors.

→ The last chip of each partition must be the closest of DAQ.

→ Board is divided in 2 partitions to reduce readout time

Stack-up board

- Keep layer for power
  - 2 x GND
  - 2 x AVDD_PA
  - 1 x AVDD
  - 1 x DVDD
- Minimize crosstalk
- Keep shielding mush as possible
  - AVDD_PA for preamplifier signals
  - GND for analog and digital signals
- Move away digital from preamplifier line
- Adaptation lines
  - 50Ω for single ended
  - 100Ω for ddifferential lines

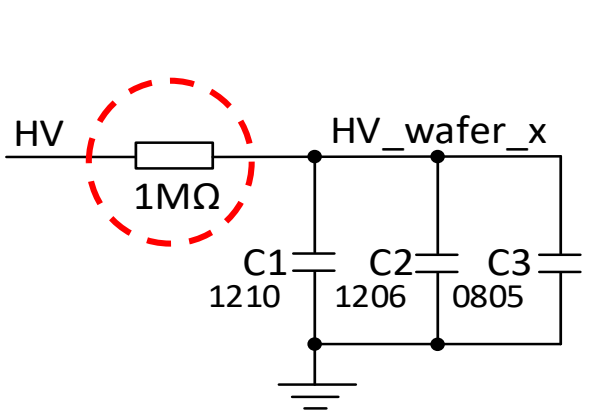


High voltage proposition

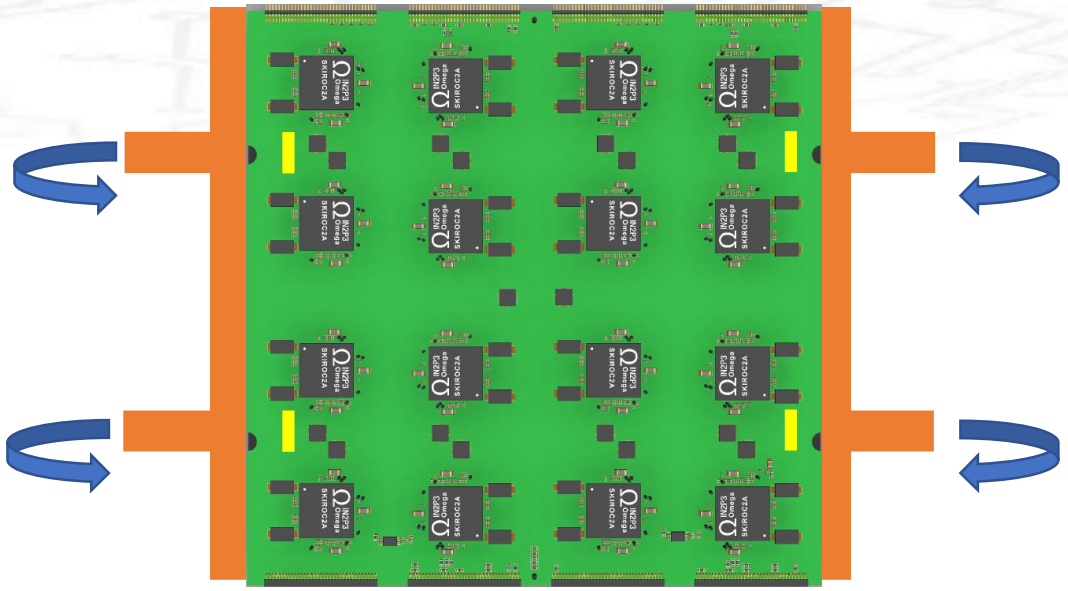
We have no idea of cumulative effect on HV for 10 boards

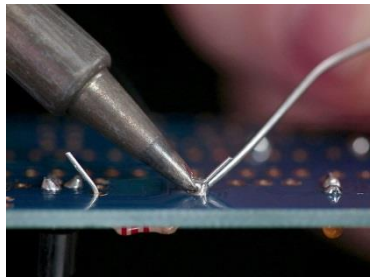
- 40 wafers connected on the same HV
- Leakage current <1nA / wafer in average
- Noise effect ?

→ Add a filter for each wafer and **limit the current** in case of **wafer failure.**

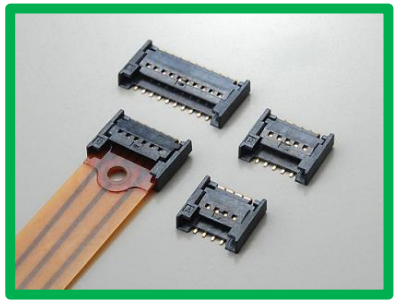


How to connect kapton to board ?

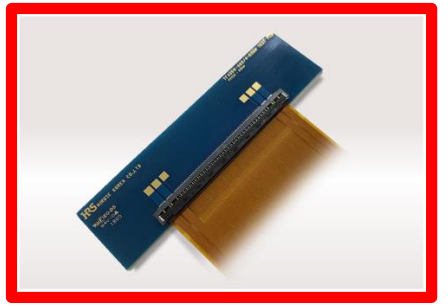




JAE FA10 series



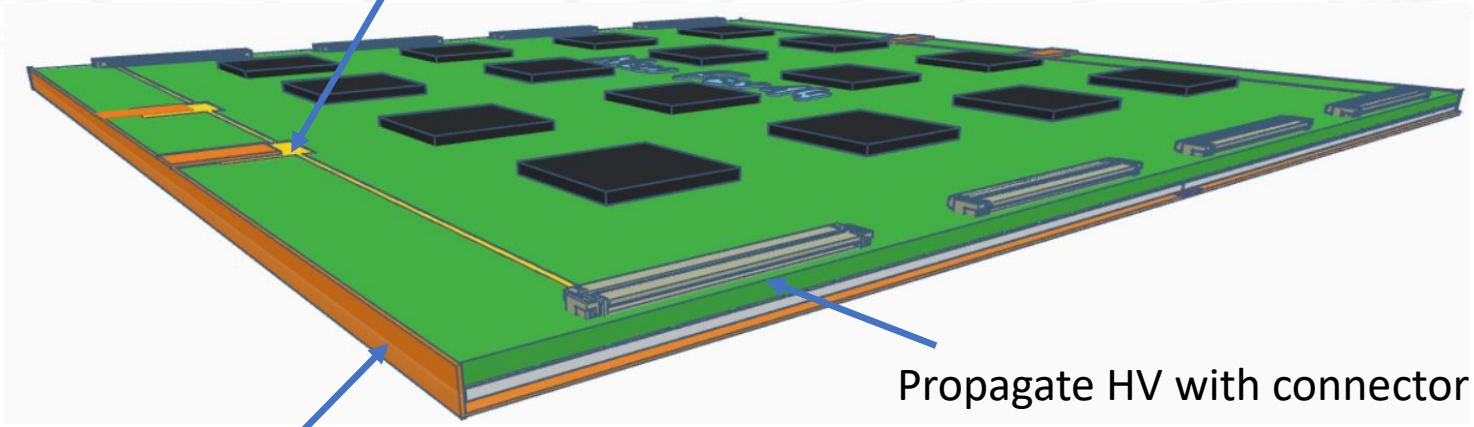
HIROSE TF443SW series

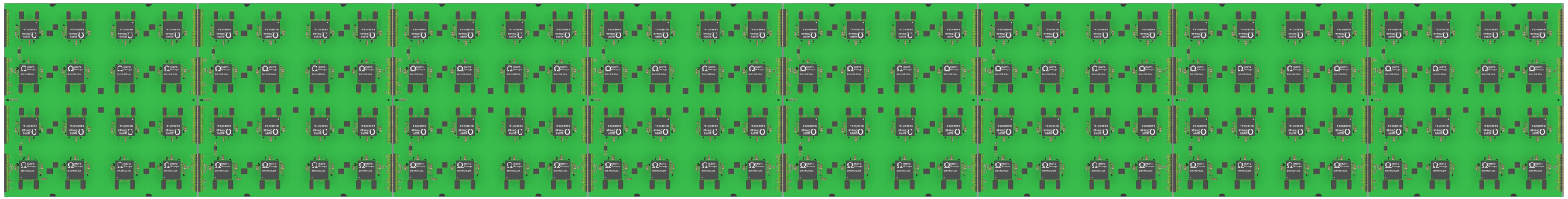


Request samples to test connectors solutions

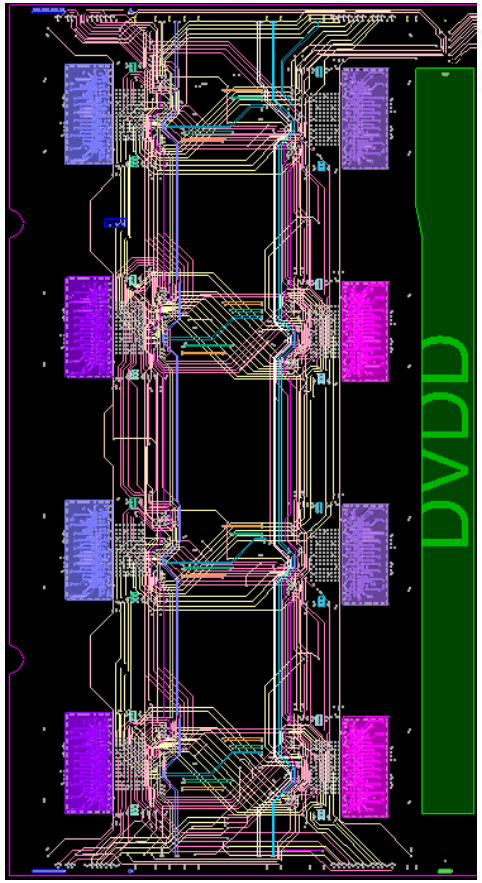
Mechanics propositions

- Kapton is enlarge to protect 2 sides of the system during insertion or slice in the support.
- High voltage is driven by the board instead of the kapton for assembly, maintenance and costs reductions.

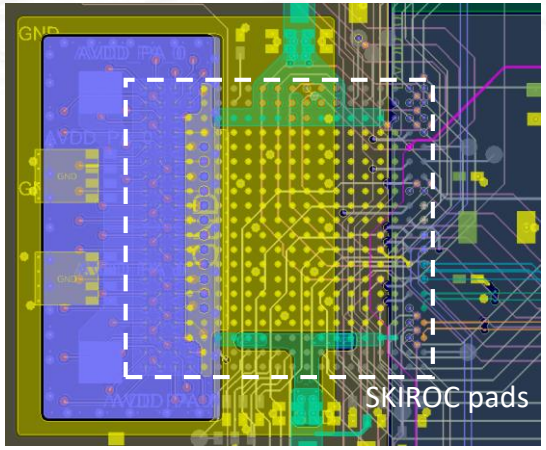




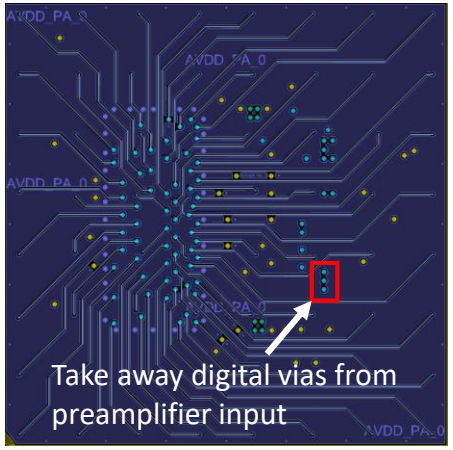
Layout optimizations



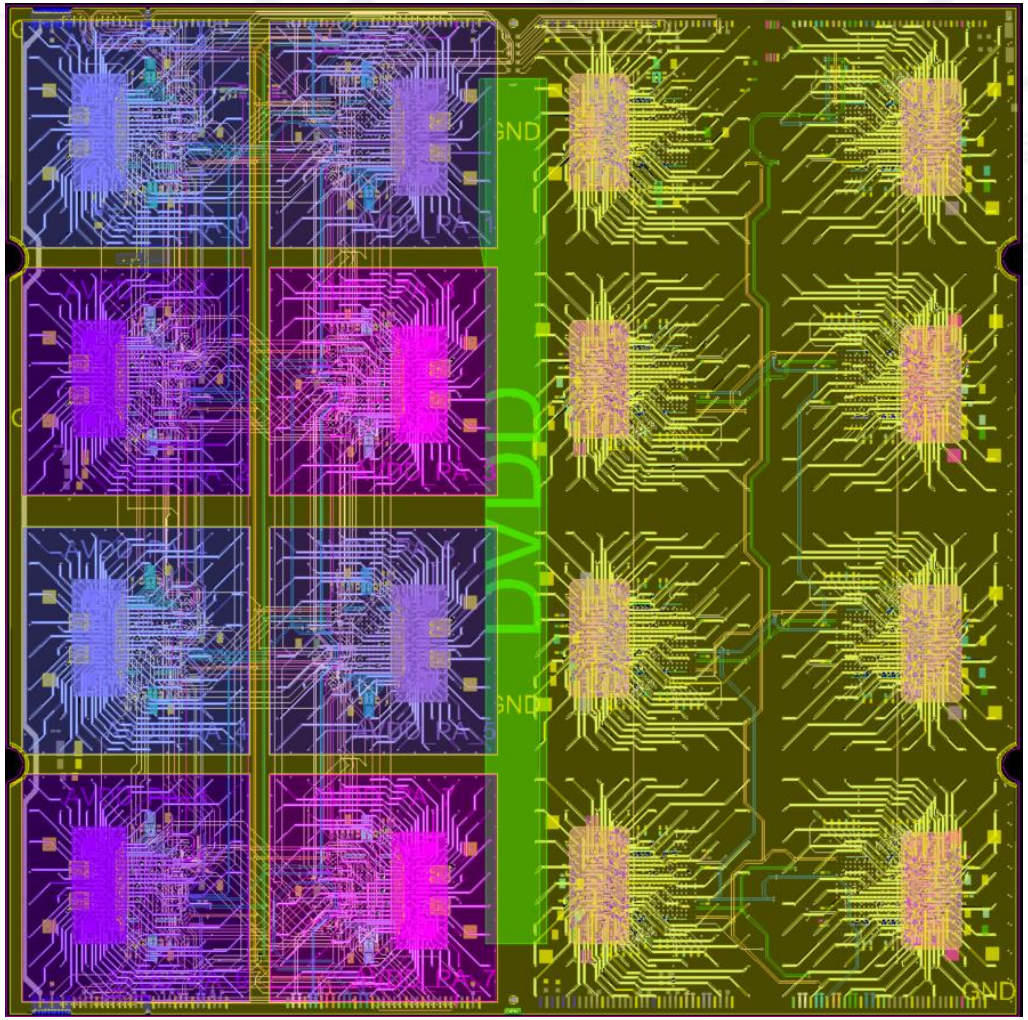
Digital lines optimize for long SLAB



Insulate input signals with GND ring



Each pattern of input signal are identical



Board finished 45%

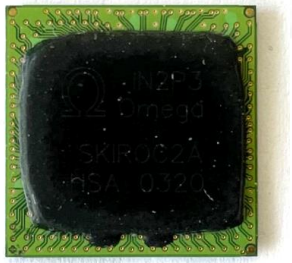
- 5% for LDO power
- 50% for partition duplication

New packaging for SKIROC2A chips

- Previous company **Novapack stop BGA activities**
- Very difficult to find a company for BGA encapsulation.
- Test a new company Aptasic

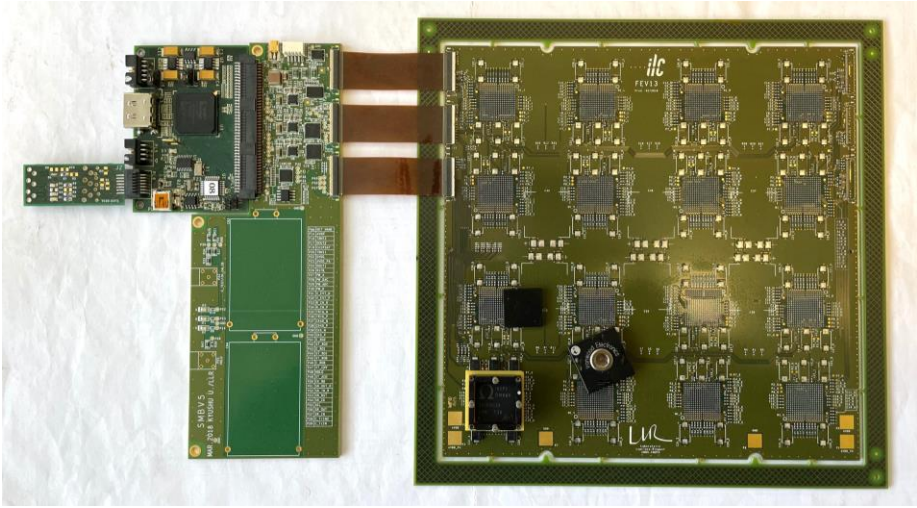
  → No conclusive results
- Contact with a new Chinese company (recommend by Ωmega) **NCAP**
  - Package BGA size: 17mm x 17 mm
  - Thickness: 1,2mm

I receive quotation today !



Aptasic solution

Awaited solution

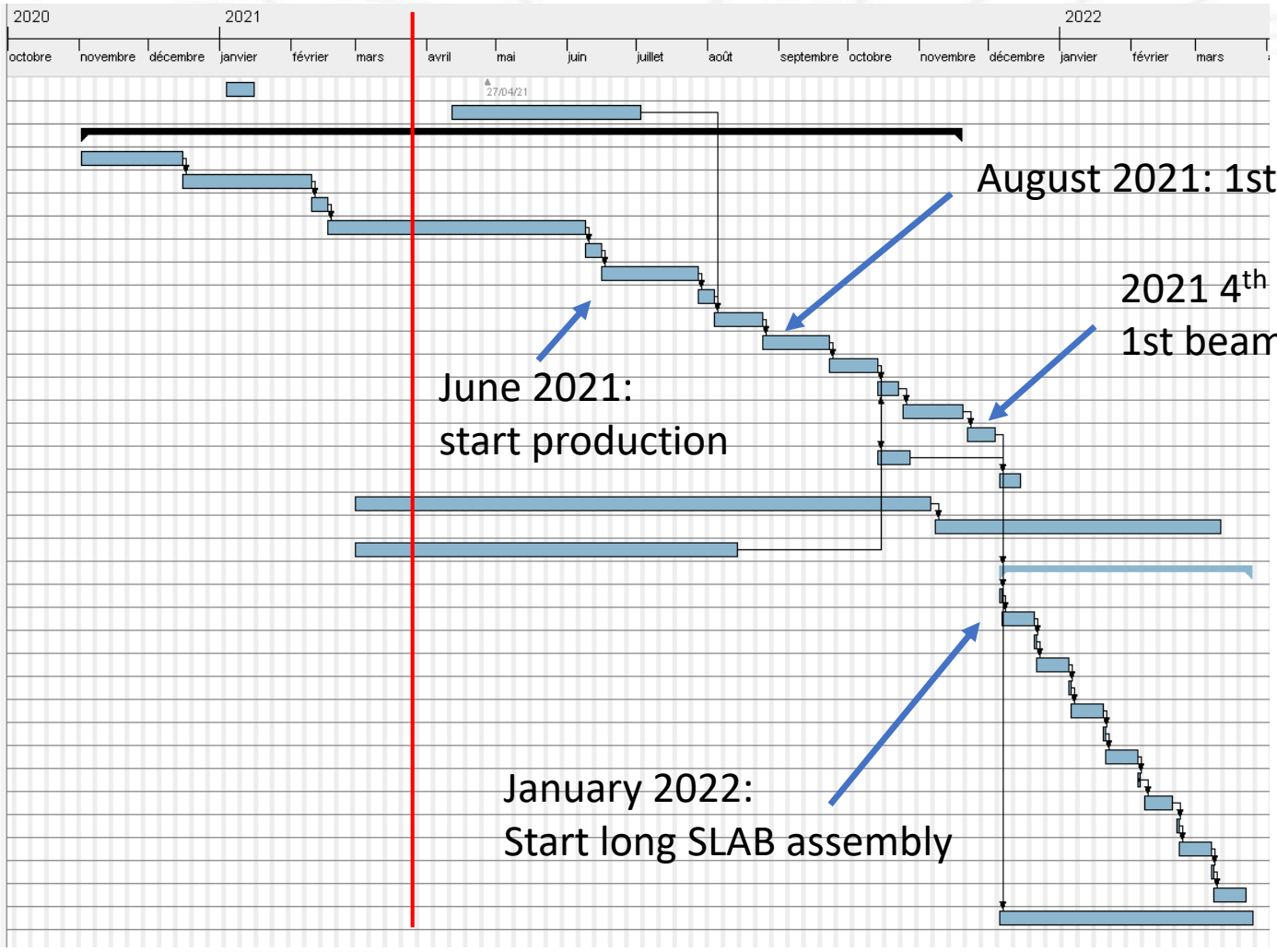


Upgrade bench of unique chip

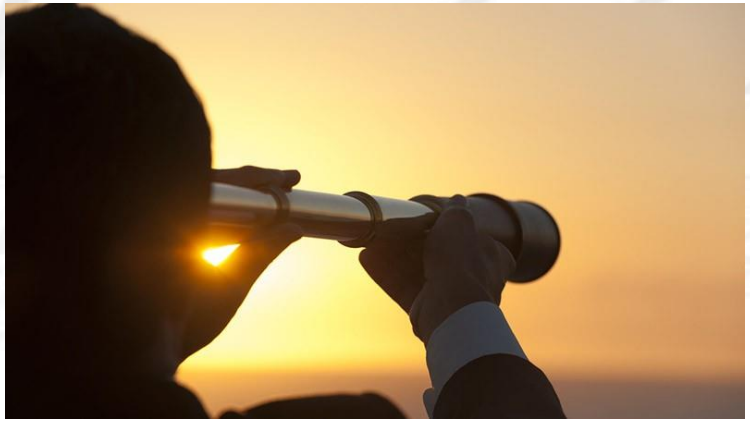
Planning for 2021

Today March 24

Nom	Date de début	Date de fin
Measure wafers i(V)	04/01/21	15/01/21
Packaging SKIROC 2A by NCAP	12/04/21	02/07/21
FEB conception	02/11/20	19/11/21
Cahier des charges	02/11/20	15/12/20
Schematic	16/12/20	09/02/21
Review schematic	10/02/21	16/02/21
Drawing board	17/02/21	08/06/21
Review drawing	09/06/21	15/06/21
Production of 15 boards	16/06/21	27/07/21
Metrology	28/07/21	03/08/21
Solders componants for 1+4 boards	04/08/21	24/08/21
Fonctionnal tests	25/08/21	22/09/21
Tests with wafers (not glued)	23/09/21	13/10/21
Gluing wafers on 1+4 boards	14/10/21	22/10/21
Calibration + cosmic tests	25/10/21	19/11/21
Beam tests	22/11/21	03/12/21
Solder componants for 5 boards	14/10/21	27/10/21
Gluing wafers on 2 boards	06/12/21	14/12/21
Study mechanical support for long slab	01/03/21	05/11/21
Mechanical production	08/11/21	11/03/22
HV kapton study and production	01/03/21	13/08/21
Long SLAB assembly v2	06/12/21	25/03/22
Assemble 2 boards	06/12/21	06/12/21
Measure & analysis	07/12/21	20/12/21
Assemble 3 boards	21/12/21	21/12/21
Measure & analysis	22/12/21	04/01/22
Assemble 4 boards	05/01/22	05/01/22
Measure & analysis	06/01/22	19/01/22
Assemble 5 boards	20/01/22	20/01/22
Measure & analysis	21/01/22	03/02/22
Assemble 6 boards	04/02/22	04/02/22
Measure & analysis	07/02/22	18/02/22
Assemble 7 boards	21/02/22	21/02/22
Measure & analysis	22/02/22	07/03/22
Assemble 8 boards	08/03/22	08/03/22
Measure & analysis	09/03/22	22/03/22
Calibration / tests / source	06/12/21	25/03/22



Conclusion/planning



Design of new front end board (Collaboration between LLR and IJCLab) :

- Optimisation of the power pulsing (compatible with the SL Board and the new philosophy of current limitation over the slab)
- Reduce voltage drop on power supply
- Clean clock distribution over the slab.
- Change high voltage distribution through the board (HV distribution over connectors)
- Add solutions to simplify manipulation and protect wafers

- June: production of 15 new front end boards
- September: 1st electrical test
- End of 2021: beam test @ DESY (COVID ?)
- 2022: start long slab assembly

→ Be ready in 2023, with new long slab design for ILD schedule

Any
Questions