



Updates of Timing electronics for T-SDHCAL

Weihao Wu, On behalf of SDHCAL Group

Shanghai Jiao Tong University

29/09/2023

饮水思源•爱国荣校





Introduction

- > 2nd version of FEB prototype
- >Timing performance evaluation
- Double-FEB setup for cosmic ray test
- DAQ development
- Conclusion & plans





Semi-Digital Hadronic CALorimeter

- SDHCAL is one of high granularity PFA (Particle Flow Algorithm) calorimeter
 - Connect first hits and then their clusters using distance and orientation information
 - The energy information helps to optimize the connections of hits belongs to the same shower.
- A SDHCAL prototype built based on Glass RPC
- Semi-digital readout: hits associated to three different thresholds
 - Ist threshold = 110fC
 - 2nd threshold = 5pC
 - > 3rd threshold = 15pC
- > 48 layers with GRPC as sensitive medium
- Dimensions: 1m×1m×1.3m





SDHCAL prototype at testbeam in 2015

CALOR2022 Conference

Introduction of Timing Electronics

- Timing information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.
- Method: Adding some mRPC layers in the SDHCAL
- Front-End Electronics for mRPC readout
 High resolution timing measurement
 - Time measurement with 10 bits TDC interpolating 40MHz clock
 - Timing resolution below 40 ps
 - ➤ 32 input channels
 - Power consumption: ~6mW/channel





2023/9/28

Timing Electronics at SDHCAL







- ➢ A 32-channel front-end ASIC designed for SiPMs readout (mRPCs as well).
- Charge and timing measurement
- 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line
- Dynamic Range 0-480 pC i.e. 3000
 - photoelectrons @ 10^6 SiPM gain
- Fast fixed gain (40) inverting voltage preamplifier
- Slow shaper with adjustable shaping time from 25 to 100 ns
- Charge measurements by Track&Hold
- Power consumption 6mW/channel





Overview



2023/9/28

- A small FEB prototype
 - Timing performance validation
 - Readout scheme with mRPC detectors
- 2nd-version of FEB has been designed and fabricated
 - 2 Petirocs on-board
 - ➤ On-board power rails
 - ≻64-channel input pads
 - SMAs to inject signals
 - Crosstalk issue in injection test has been fixed





FEB v2





Injected Test

- Injection Test has been performed and verified.
- Timing performance has been evaluated based injection test

Setup:

- Setup 1: inject signal to one channel of one chip. For timing between neighbor hits
- Setup 2: inject signal to two channels from two chips. For timing between two chips





Calorimeter for ILC

Signal profile:

- Negative pulse
- *freq*: 10kHz (period of 100 μs)
 or 25kHz (period of 40μs)
- ➢ 95% duty
- 1Vpp amplitude
- leading of 1us
- trailing of 2ns



Timing Electronics at SDHCAL

2023/9/28

Timing performance tests



- > To test the timing performance, two experiments are implemented:
 - timing tests for single chip, between neighbor hits
 - If Petiroc2B is working properly, every two neighbor hits should have the same time gap (when inject signal is uniform). So analyzing the time gaps can get us the timing performance.

ILA Status: Idle				A #			Λ.+	Т							<u>65, 536</u>
Name	Value	0	5,000	10, 000	$\Delta l_4 \Delta l_5$ 15,000	Δι ₆ Δι 20, 000	25, 000	30, 000	35, 000	40, 000	45, 000	50, 000	55, 000	60, 000	6 <mark>5, 000</mark>
₿ asic1_dout_diff	0														
<pre>asic2_dout_diff</pre>	0														
╏ asic1_trans_onb_IBUF	1														
asic2_trans_onb_IBUF	0														

timing tests for single hit, between two chips

Because two chips share one clock source, the phase difference should be fixed, which means that for the same single hit, the time gap between two chips should be fixed.

ILA Status: Idle							Т							65. 536	
Name	Value	0 5, 000	10, 000	15, 000	20, 000	25, 000	30, 000	35, 000	40, 000	45, 000	50, 000	55, 000	60, 000	5, 000	
lasic1_dout_diff	0														
🔓 asic2_dout_diff	0	$\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{$	t ₃ ↓ ∆t ₄ ↓ ∆	$t_5 \bullet \Delta t_6$	$\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{\mathbf{$	1t ₈ ↓	•••								
<pre>asic1_trans_onb_IBUF</pre>	0														
asic2_trans_onb_IBUF	0														$\left \bigcap \right $
											/	/ 11			JI IL
			Timing	Flectr	ronics	at SDI	ICAL						2	022/9/	28

Timing between neighbor hits



2023/9/28

ILA Status: Idle			$\Lambda t_1 \Lambda t_2$	Λt _o	Λt , Λt_{-}	$\Lambda t_{\star} = \Lambda t$	$-\Lambda t_{0}$	Т							65, 536
Name	Value	0	5, 000	10,000	15, 000	20,000	25, 000	30, 000	35, 000	40, 000	45, 000	50, 000	55, 000	60, 000	65, 000
<pre>asic1_dout_diff</pre>	0														
<pre>asic2_dout_diff</pre>	0														
<mark>™</mark> asic1_trans_onb_IBUF	1														
asic2_trans_onb_IBUF	0														

- Inject signal into one chip.
- ➤ Calculate the timing differences (Δt) between every two neighbor hits.
- \succ Check if Δt is consistent.

Results: ✓ The std of Δt is 45.8ps ✓ Δt is consistent











ILA Status: Idle Value Name 15,000 5,000 10,000 ,20, 000 ,25,000 ,30, 000 ,35,000 40,000 45,000 ,50,000 ,55, 000 60,000 65,000 asic1_dout_diff 0 lasic2_dout_diff 0 asic1_trans_onb_IBUF 0 asic2_trans_onb_IBUF 0

- Inject the same signal into two chips (with a double-pass).
- > Calculate the Δt between two Petiroc2B chips of each hit.
- \succ Check if Δt is consistent.

Results:
✓ The std of Δt is 53.6ps
✓ Δt is consistent







Timing Electronics at SDHCAL



Setup for Cosmic Test

The objective is to detect cosmic ray signals by both FEBs that corresponds to each other, including time and channel number (location information).





Injection tests for double-FEB system

- ➤ the signal is injected from the same channel of the function generator, with a bi-pass, and the cables are of equal length so that the signals can reach two boards simultaneously
 ➤ calculate Δt of each instance between two FEB
- \succ repeat the test one hour later, to see if the Δt are consistent

Results:
✓ The std of Δt is 54.6ps
✓ Δt is consistent

两板事例时间差平均值为2.3294us (mean) 两板事例时间差方差为2981.3778ps^2 (variance) 两板事例时间差标准差为54.602ps (std)

mRPC Test

mRPC detector

- The test conditions are:
 - ➢ voltage: 7500V
 - ➤ gas: 10% C4H10, 12% SF6, 18.9% F134a

Preliminary Test

- Use a readout pad with copper strips, and observe the signal from an oscilloscope
- > Can capture something, but probably noises only.
- Still working on the mRPC test, with our colleagues' help

* · /	网络调试助手 (CⅢ精装版 V3.8)	\ ×	× ▲ IEDHAR CLAM - □ ×
网络沉里	网络教课物版		THU BER DE CONSTRUCTION OF THE CONSTRUCTION OF THE OFF
「日本社会社会社会社会社会社会社会社会社会社会社会社会社会社会社会社会社会社会社会	P PRESENTERS		
(1) 助収英望	37 30 33 37 63 37 33 33 30 30 37 65 33 37 37 36 33 37 63	37 36 00 ^	▲ 【▲ 泉州里奈は諸藩 → K001-2)
UDP 👤	33 37 38 33 30 33 36 63 37 37 33 37 63 37 33 33 37 63 37	30 33 65	Nn. Time Source Destination Protocol Length Info
(2) 本 #up#h#i	30 33 33 37 63 37 65 33 33 00 63 37 36 33 66 38 33 30 33	37 63 37	1114 193.091113 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
	37 33 36 30 37 33 33 66 63 37 30 33 37 38 37 37 33 66 38	37 36 33	9467 1139.663585 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
192.168.1 .100	66 38 37 30 33 66 63 37 37 33 66 63 37 36 33 63 63 37 30	33 66 38	9468 1139.663585 192.168.1.10 192.168.1.100 UDP 286 62510 + 5001 Len=244
(3) 本地端口号	37 33 33 37 63 37 30 33 64 63 37 37 33 64 38 37 33 33 66	38 37 30	9469 1159.665585 192.168.1.10 192.168.1.100 UDP 286.65510 + 5001 Len-244
5001	33 66 63 37 66 33 66 63 37 33 37 66 64 64 66 37 66 64 66	66 37 66	94/8 [199.605365] 192.106.1.10 192.106.1.10 UUP 280 62516 3901 [eff]244
10001	64 66 66 37 66 64 66 66 37 66 64 66 66 37 66 64 66 66 37	66 64 66	001 1141 01405 101 102 100 110 102 100 110 007 100 007 100 0014 000 100 000
	66 37 66 64 66 66 37 66 64 66 66 37 66 64 66 66 37 66 64	66 66 37	9451 1141-024605 152-106-1.10 152-106-1.10 00F 280 0210 9 3601 EEE/244
🖲 断开	66 64 66 66 37 66 64 66 66 37 66 64 66 66 37 66 64 66 66	37 66 64	9588 1143, 988368 192, 168, 1, 10 192, 168, 1, 100 UDP 286 62510 + 5001 Len=244
	66 66		9520 1145.058596 192.168.1.10 192.168.1.100 UDP 286 62510 + 5001 Len=244
橡胶区设置	FF FF FF FF 33 66 38 37 37 33 65 30 37 37 33 37 30 37 65	33 36 63	9531 1146-136616 192-168-1.10 192-168-1.100 UDP 286 62510 → 5001 Len=244
	37 30 33 37 63 37 33 33 30 30 37 65 33 37 37 36 33 37 63	37 36 00	9546 1147.219025 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
1 摄明(19610])(1+	33 37 38 33 30 33 36 63 37 37 33 37 63 37 33 33 37 63 37	30 33 65	9551 1148.297214 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len-244
✓ 自动执行显示	30 33 33 37 63 37 65 33 33 00 63 37 36 33 66 38 33 30 33	37 63 37	9559 1149.375384 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
▼ 十六进制显示	37 33 36 30 37 33 33 66 63 37 30 33 37 38 37 37 33 66 38	37 36 33	9564 1150.453439 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
匚 新信体游员子		33 66 38	9568 1151.531612 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
I BINTROCLEVIN	27 22 23 27 63 27 20 23 64 63 27 27 27 23 64 29 27 23 23 66	29 27 20	9574 1152.609687 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
保存数据 遺除显示	20 66 60 07 66 00 66 60 07 00 07 66 64 66 07 66 64 66	66 37 66	9584 1153.692142 192.168.1.10 192.168.1.100 UDP 286 62510 → 5001 Len=244
		00 31 00	9593 1154.770257 192.168.1.10 192.168.1.100 UDP 286 62510 + 5001 Len=244
发送区设置	04 00 00 J/ 00 04 00 00 J/ 00 04 00 00 J/ 00 04 00 00 J/	66 64 66	9599 1155.848596 192.168.1.10 192.188.1.100 UDP 286 67510 + 5001 Len-244
	00 37 00 04 00 00 37 00 04 00 00 37 00 04 00 00 37 00 04	66 66 37	9613 1156 926548 192,108,1.10 192,108,1.100 UDP 286 62510 + 3001 Len 244
启用义计数据源…	05 64 65 65 37 65 64 66 65 37 65 64 66 65 37 65 64 66 65	37 66 64	3014 1136.004049 132.106.1.10 132.106.1.100 UDF 200.02310 7 3001 Lei 244
□ 自动发送附加位	66 66		2020 1123 00 2001 125 100 112 100 1120 100 100 100 200 0230 4 3001 Filin 544
□ 发送完自动清空			
□ 按十六进制发送		~	Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E780980-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits) on interface (Device Nev(E78090-0560-4/81-8462-A88ADEF/2F15), 10 (Frame 1114: 286 bytes on wire (2288 bits), 286 bytes captured (2288 bits), 286 bytes (288 bytes (288 bits), 286 bytes (288 bytes (288 bits), 286 bytes (288 bits), 286
10170203002		_	 Element In Ster Alling de Sole (00 del 55 del 102 (00 del 55 del 102 del
1 数据流幅外友医	目标主机: 192.168.1.10 目标满口: 62510		Littlering Friddows Friddows Strephone (1991) 1921 1921 1921 1921 1921 1921
发送间隔 1000 豪秒	1		> Data (244 bytes)
1000 800	http://www.omsort.cm.ww.iuoo5600	生涯	Data: ffffffff313230336331363033531313433633133383337313334333533313833643131
文件载入 遺跡輸入		~ 14	[Length: 244]
	1		
of brite	发送: 256 接收: 59780	复位计数	

Ethernet data test - read from DMA

MainWindow

Mask disci charge			
0	8	16	24
1	9	17	25
2	10	18	26
3	11	19	27
4	12	20	28
5	13	21	29
6	14	22	30
7	15	23	31
Mask disci time			
		16	24
		17	25
	10	18	26
3	□ 11	19	
4	12	20	28
5	13	21	29
6	14	22	30
7	15	23	31
ADC ramp compensation	charge 300	Cin	CI
	tina 500	(1. 25pF	() 100fF
External start ADC	cime 500	○ 2. 5pF	() 200fF
LatchDiscri no latch 🗸	DAC dummy 0	○ 3.75pF	() 300fF
		◯ 5pF	○ 400fF
Polarity Negative ~	DAC delay 0	τ =25ns	τ =25ns

- > The DAQ software is a Python GUI application.
- The GUI is designed via QT designer, which is set of crossplatform C++ libraries that implement high-level APIs.
- PyQt5 modules binding with QT v5.
- > The data is read from a DMA configured in PL (FPGA)
- The ethernet transfer function is realized through PS (ARM core) of ZYNQ, using LWIP protocol
- Counter data has been tested and verified

. <u>n</u> 8

Conclusion

- The timing performance of a small FEB prototype has been validated, with a resolution under 100ps.
- Double-FEB system has been validated through injection tests.
- DAQ through ethernet has been preliminarily validated.

Further plans

- Build a customized test platform to operate mRPCs properly
- Validate the FEBs with mRPCs, by observing signals from cosmic rays
- Complete DAQ system development
- Build large-sized modules

Thank you for your attention

