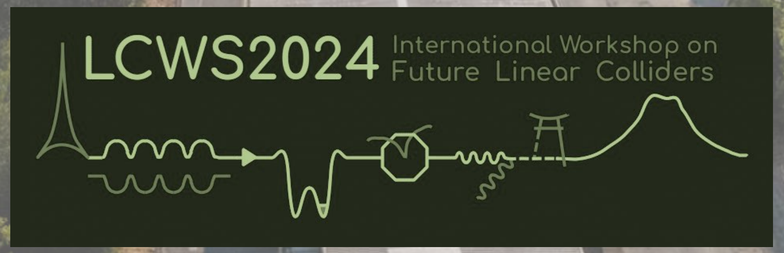
(towards) Nanosecond timing MAPS

Caterina Vernieri on behalf of
Christos Bakalis, James E. Brau, Martin Breidenbach, Angelo Dragone, Christopher Kenney, Lorenzo Rota, Julie Segal, Mirella Vassilev



SLAC NATIONAL ACCELERATOR LABORATORY

Stanford University | U.S. DEPARTMENT OF ENERGY

Current benchmarks and next steps

The goal of measuring Higgs properties with sub-% precision translates into ambitious requirements for detectors at e+e-

Initial state	Physics goal	Detector	Requirement
e^+e^-	hZZ sub-%	Tracker	σ_{p_T}/p_T=0.2% for $p_T < 100$ GeV $\sigma_{p_T}/p_T^2 = 2 \cdot 10^{-5}$/ GeV for $p_T > 100$ GeV
		Calorimeter	4% particle flow jet resolution EM cells 0.5×0.5 cm^2, HAD cells 1×1 cm^2 EM $\sigma_E/E = 10\%/\sqrt{E} \oplus 1\%$ shower timing resolution 10 ps
	$hb\bar{b}/hc\bar{c}$	Tracker	$\sigma_{r\phi} = 5 \oplus 15(p \sin\theta^{\frac{3}{2}})^{-1} \mu$m 5$\mu$m single hit resolution

Arxiv:2209.14111 Arxiv:2211.11084 DOE Basic Research Needs Study on Instrumentation

Current benchmarks and next steps

The goal of measuring Higgs properties with sub-% precision translates into ambitious requirements for detectors at e+e-

Initial state	Physics goal	Detector	Requirement
e^+e^-	hZZ sub-%	Tracker	σ_{p_T}/p_T=0.2% for $p_T < 100$ GeV $\sigma_{p_T}/p_T^2 = 2 \cdot 10^{-5}$/ GeV for $p_T > 100$ GeV
		Calorimeter	4% particle flow jet resolution EM cells 0.5×0.5 cm^2, HAD cells 1×1 cm^2 EM $\sigma_E/E = 10\%/\sqrt{E} \oplus 1\%$ shower timing resolution 10 ps
	$hb\bar{b}/hc\bar{c}$	Tracker	$\sigma_{r\phi} = 5 \oplus 15(p \sin\theta^{\frac{3}{2}})^{-1} \mu$m 5$\mu$m single hit resolution

Arxiv:2209.14111 Arxiv:2211.11084 DOE Basic Research Needs Study on Instrumentation

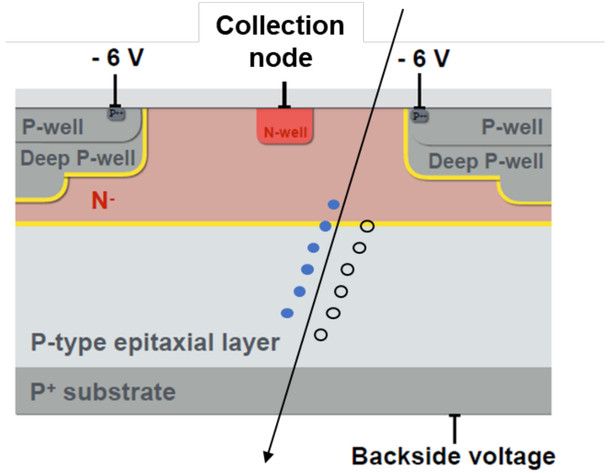
- Requirements mostly driven by (Higgs) specific benchmarks
- Technological advances can open new opportunities and additional physics benchmarks (i.e. H→ss) can add more stringent requirements

Focus topics for the ECFA study on Higgs / Top / EW factories *should* provide further detector design guidelines (2401.07564) by Spring 2025

Monolithic Active Pixel Sensors - MAPS

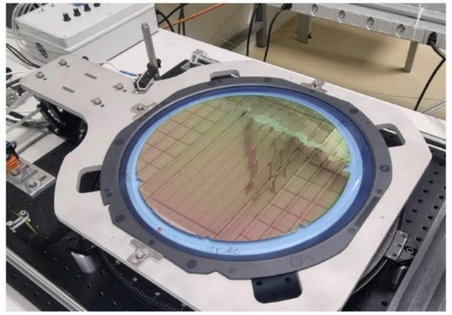
A suitable technology for high precision tracker and high granularity calorimetry

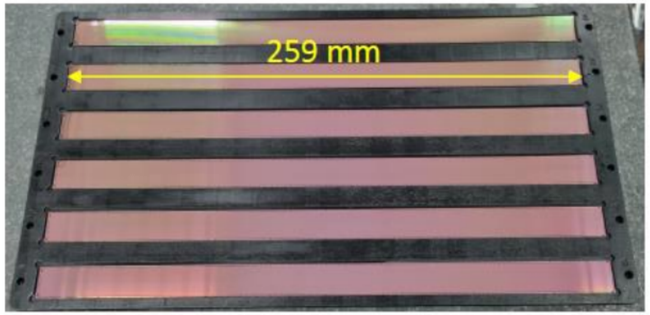
- Monolithic technologies can yield to higher granularity, thinner, intelligent detectors at lower overall cost
- Significantly lower material budget: sensors and readout electronics are integrated on the same chip
  - Eliminate the need for bump bonding : thinned to less to 50μm
  - Smaller pixel size, not limited by bump bonding (<25μm)
  - Lower costs : implemented in standard commercial CMOS processes technologies with small feature size (65-110 nm)
    - Either reduce power consumption or add more features
- Target big sensors (up to wafer size) through use of “stitching” (step-and-repeat of reticles) to reduce further the overall material budget



Current sensor optimization in TJ180/TJ65 nm process
Effort to identify US foundry on going

M. Winter, 2024





Snowmass White Paper 2203.07626
Common US R&D initiative for future Higgs Factories 2306.13567

Current effort

Co-design approach: close interaction between physics studies and technology R&D [4]

- Novel CMOS process for MAPS has recently become available, CERN (WP1.2 Collaboration) provides access to scientific community: TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
    - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS → **potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade is the main driver of CERN WP1.2 efforts
  - SLAC is the only US institute involved in Enginering Runs fabrication
- Several challenges towards wafer-scale devices → **large international effort needed to address all of them**
  - Large collaboration is interested in designing solutions for power distribution compatible with stitching and enabling O(ns) timing precision

[1] M. van Rijnbach *et al., Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al., Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,* 2019 *JINST* 14C05013
[3] S. Bugiel *et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

Large area MAPS – Highlights & Next Steps

Approach:

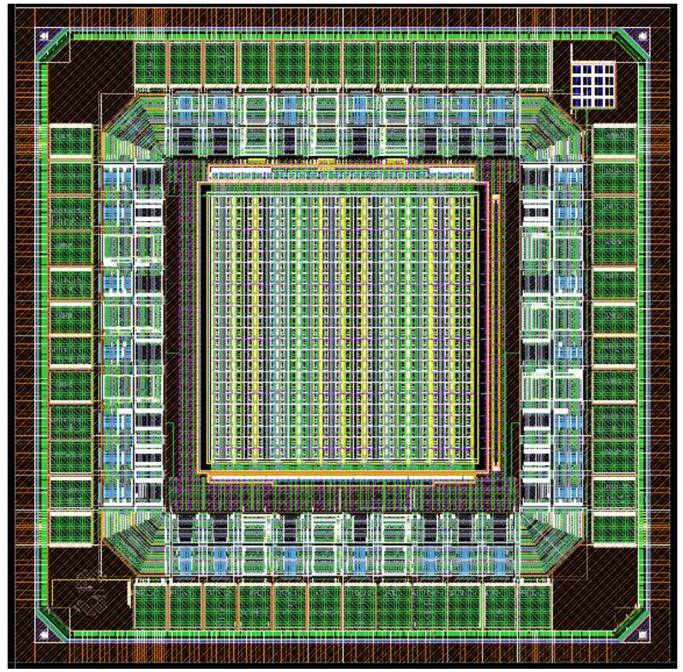
- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

- Designed pixel architecture with binary readout
- Submitted a small pixel matrix for fabrication on CERN WP1.2 shared run
- Architecture will allow us to evaluate technology in terms of defects and RTS

Next steps:

- Evaluation performance of 1st SLAC prototype on TJ65nm (2023).
- New design combining O(ns) timing precision and low-power (2024/2025).
- **Stretch Goals:** design of a wafer-scale ASIC (2025/2026, design only)



Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm

Beam induced backgrounds at future HF

D. Ntounis (2023)
G. Marchiori (2023)
TDAQ@Annecy2024

Same tools and methodology between ILC & FCC within Key4HEP

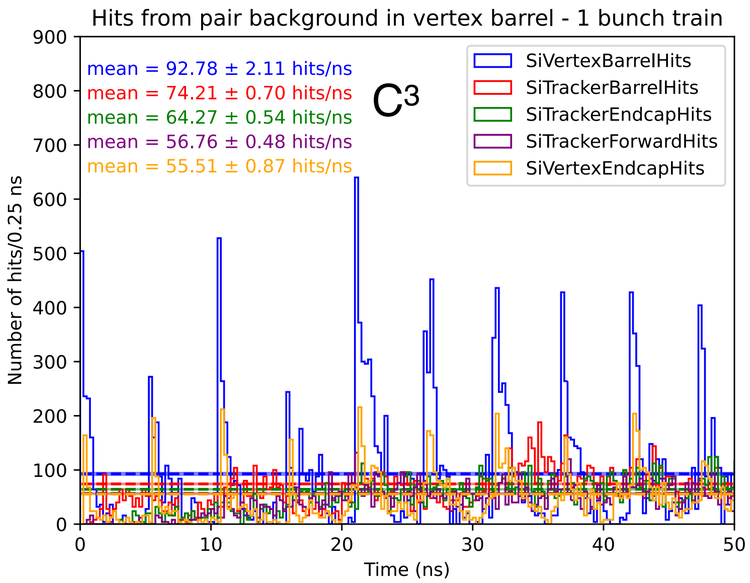
- ILC physics studies are based on full simulation data and some have been recently repeated for C³
  - Time distribution of hits per unit time and area on 1st layer ~ $4.4 \cdot 10^{-3}$ hits/(ns·mm²) ≃ 0.03 hits/mm² /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole
  - assuming 10μs integration time

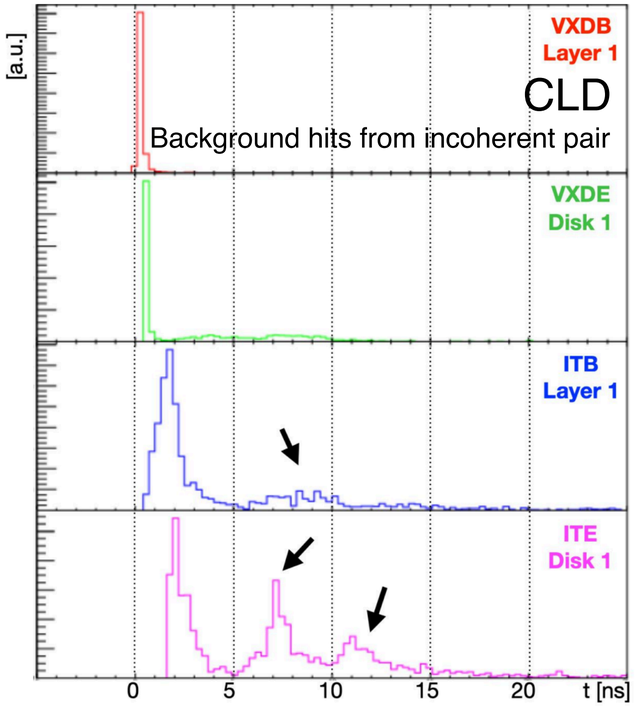
$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m\ (pixel)}{1mm \times 0.05mm\ (strip)} \qquad size_{cluster} = \frac{5\ (pixel)}{2.5\ (strip)} \qquad safety = 3$$

	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

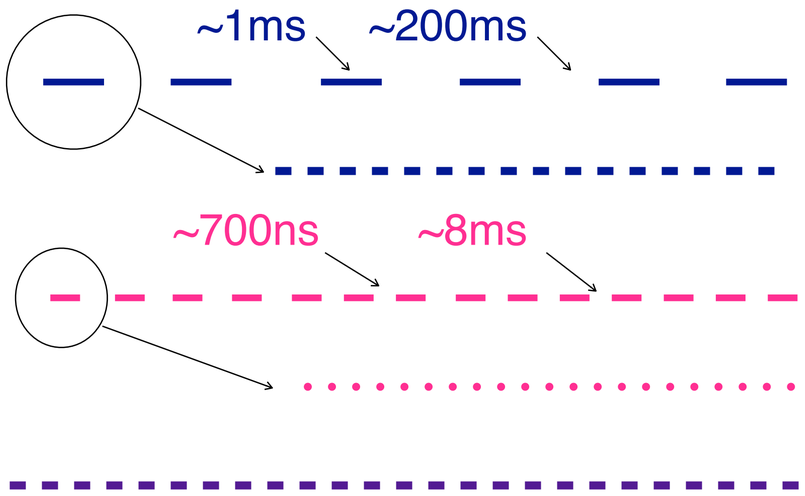
Occupancy in readout window (10μs)





Beam Format and Detector Design Requirements

arXiv:2003.01116
FCC Mid Term Report



ILC Trains at 5Hz, 1 train 1312 bunches
Bunches are 369 ns apart

C³ Trains at 120Hz, 1 train 133 bunches
Bunches are 5 ns apart

FCC@ZH Bunches 1 μs apart
FCC@Z Bunches 20 ns apart

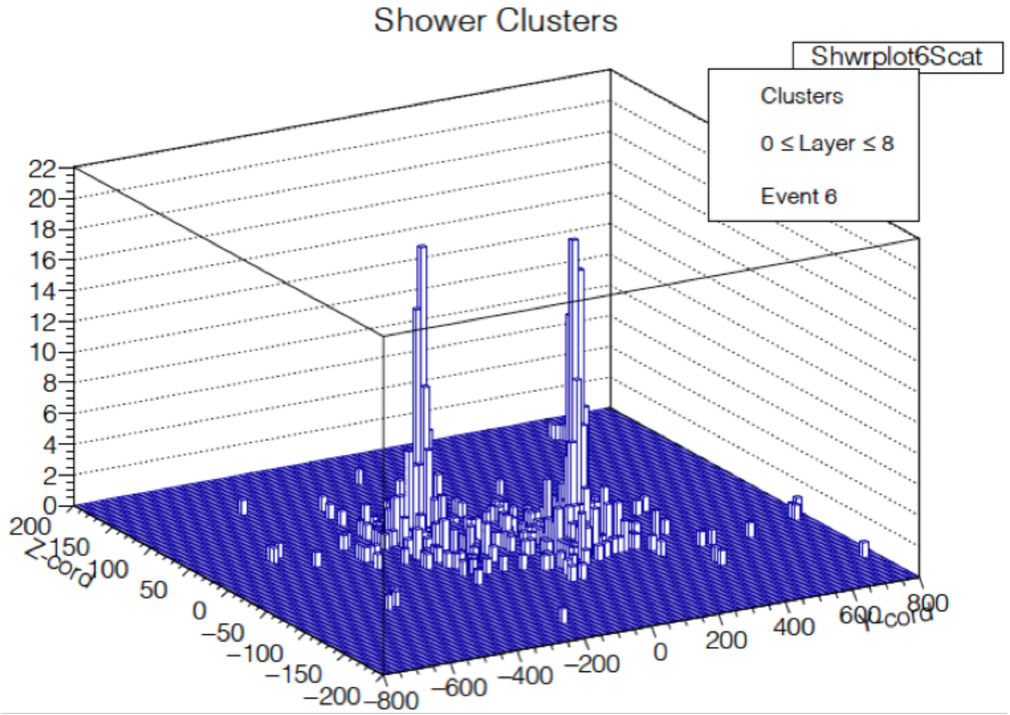
- Very low duty cycle at LC (0.5% ILC, 0.03% C³) allows for trigger-less readout and power pulsing
  - Factor of 100 power saving for front-end analog power
  - **O(1-100) ns bunch identification capabilities**
- Impact of beam-induced background to be mitigated through MDI and detector design
  - Timing resolution of O(ns) can further suppress beam-backgrounds and keep occupancy low
  - **O(1-10) ns for beam background rejection and/or trigger decision before reading out the detector**
  - Tracking detectors need to achieve good resolution while mitigating power consumption

Instruments 2022, 6(4), 51

MAPS for ECal

Fine granularity allows for identification of two showers down to the mm scale of separation

- SiD detector configuration with 25x100 μm^2 pixel in the calorimeter at ILC
  - With no degradation of the energy resolution
- ***The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR***
- The 5T magnetic field degrades the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower
- Future planned studies include the reconstruction of showers and π^0 within jets, and their impact on jet energy resolution



GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

see Jim's talk

Time resolution vs. power

JINST 19 (2024) 04, C04033

O(ns) time resolution for beam-background suppression requires dedicated optimizations

Current designs that can achieve ns or sub-ns time resolutions compensate with higher power consumption

- Target power consumption is less than 20 mW/cm^2

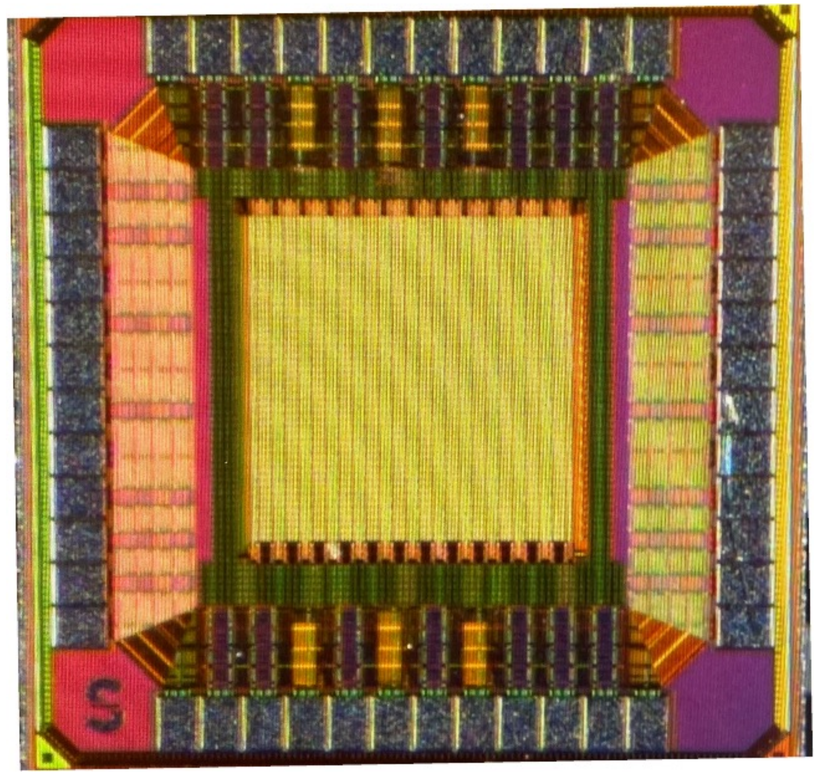
Chip name	Experiment	Subsystem	Technology	Pixel pitch [μm]	Time resolution [ns]	Power Density [mW/cm^2]
ALPIDE	ALICE-ITS2	Vtx, Trk	Tower 180 nm	28	< 2000	5
Mosaic	ALICE-ITS3	Vtx	Tower 65 nm	25x100	100-2000	<40
FastPix	HL-LHC		Tower 180 nm	10 - 20	0.122 – 0.135	>1500
DPTS	ALICE-ITS3		Tower 65 nm	15	6.3	112
NAPA	SiD	Trk, Calo	Tower 65 nm	25x100	<1	< 20
Cactus	FCC/EIC	Timing	LF 150 nm	1000	0.1-0.5	145
MiniCactus	FCC/EIC	Timing	LF 150 nm	1000	0.088	300
Monolith	FCC/Idea	Trk	IHP SiGe 130 nm	100	0.077 – 0.02	40 - 2700
Malta	LHC, ..	Trk	Tower 180 nm	36	25	> 100
Arcadia	FCC/Idea	Trk	LF 110 nm	25	-	30

Our ongoing effort to target O(ns) resolution with Napa
First prototype (Napa-p1) produced in TJ 65 nm process 5x5 mm^2, 25 µm pitch

NAPA_p1: **NA**nosecond **P**ixel for large **A**rea sensors – **P**rototype **1**

First prototype in TJ 65nm

- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 μm x 25 μm, to serve as a baseline for sensor and pixel performance.
- Design motivation ➔ simple architecture with minimum global signals to reduce failure risk in a large area implementation.
- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies



Picture of NAPA-p1 prototype from WP1.2 shared submission

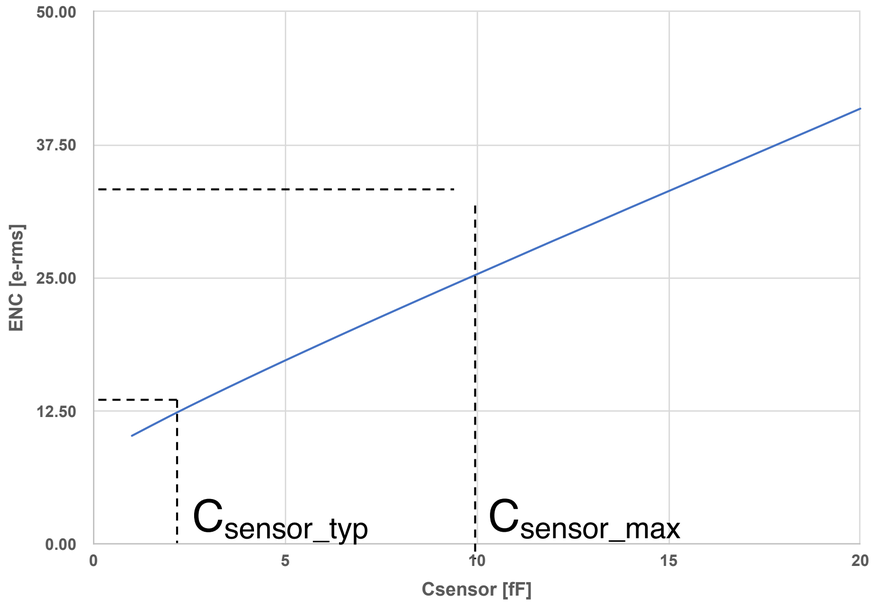
JINST 19 (2024) 04, C04033

Summary of NAPA-p1 Performance

JINST 19 (2024) 04, C04033

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 μm	7 μm ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓

ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF

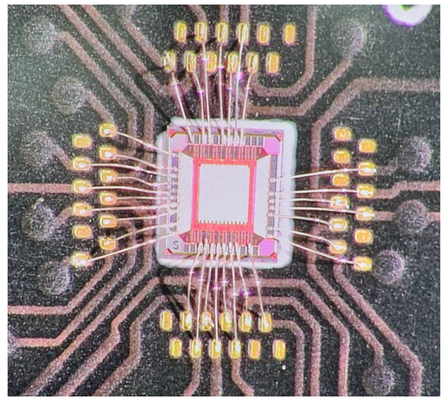


Acknowledgement: to CERN WP 1.2 for the excellent cooperation.
NAPA-p1 uses the pixel masked developed and optimized by CERN, and was fabricated in a MLR led by CERN

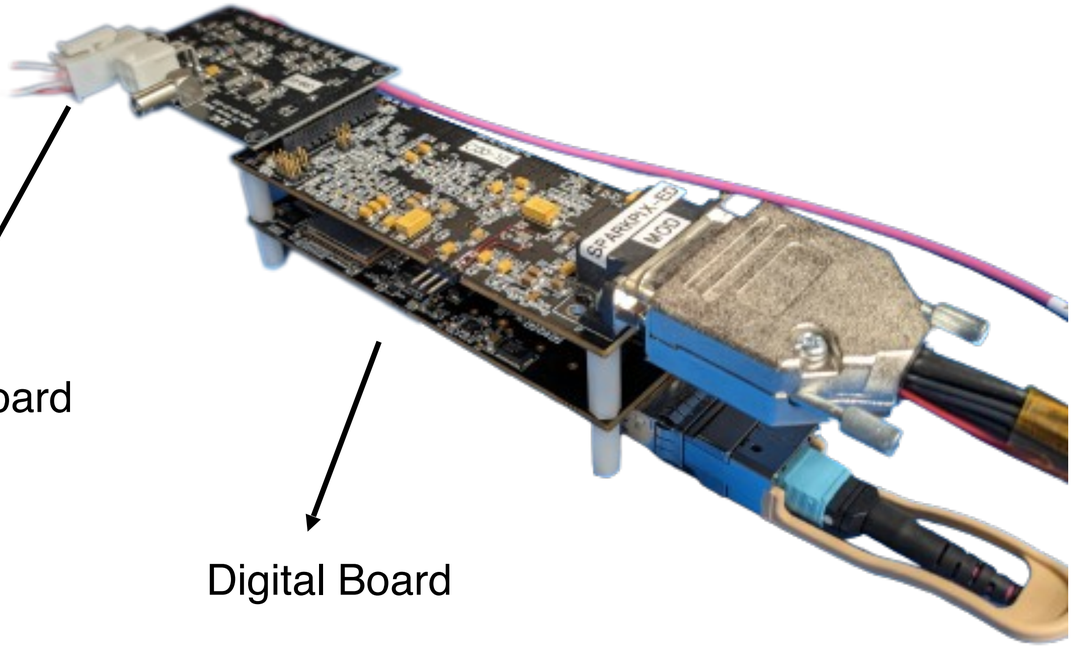
Test Setup for NAPA-p1

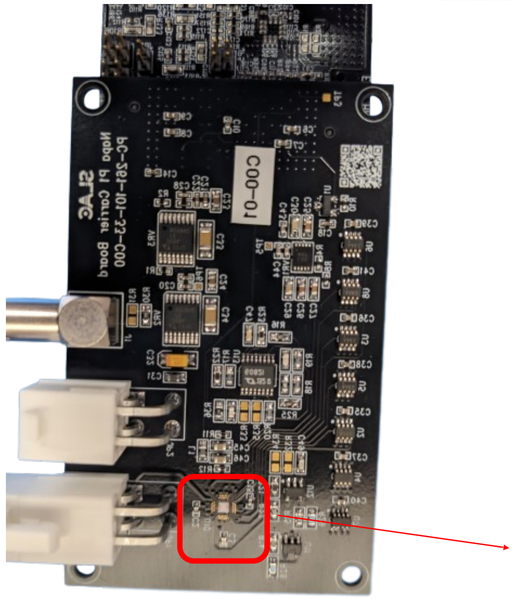
Chips were received in September 2023

- A custom carrier was designed at SLAC for the NAPA-p1 chip providing all analog references
- The chip was wire-bonded at SLAC
- The carrier boards connects to a digital board containing an FPGA and several DAC's



Napa-p1





Carrie Board

Characterization Results

Preliminary results match simulation

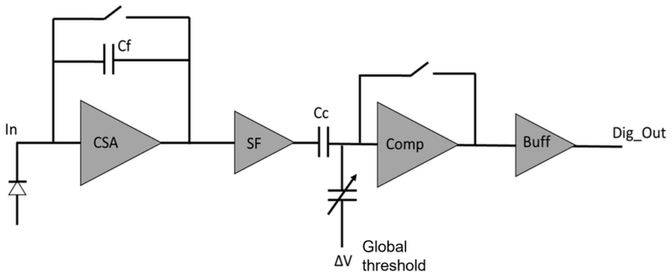
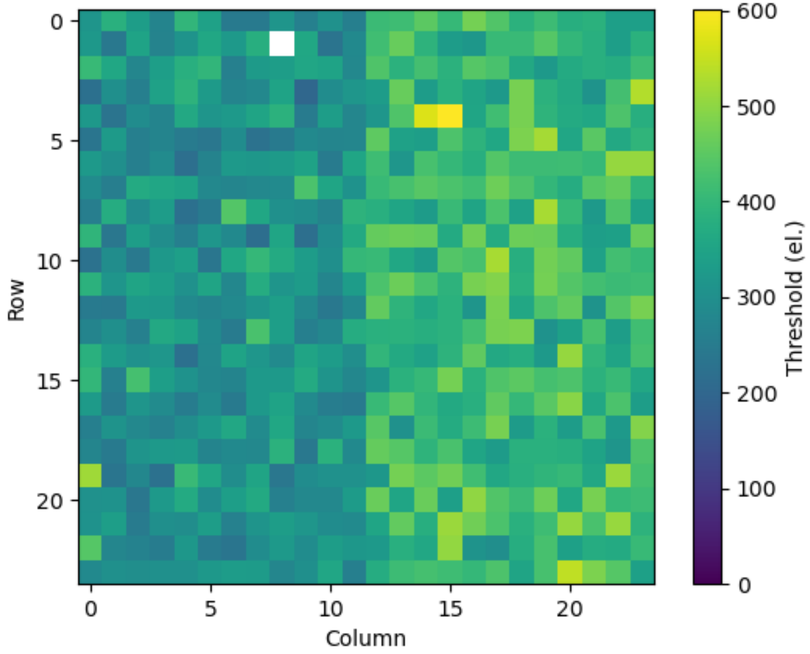
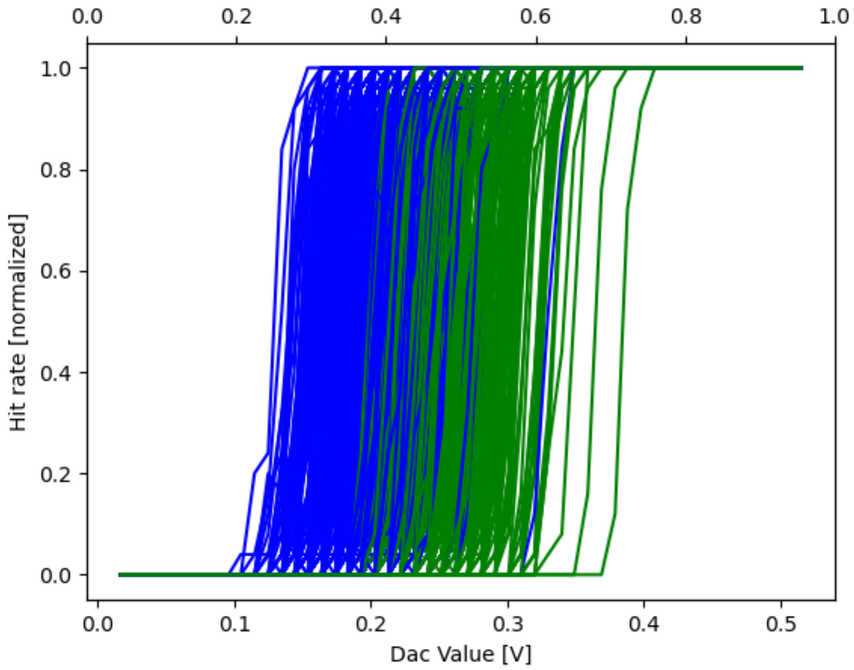
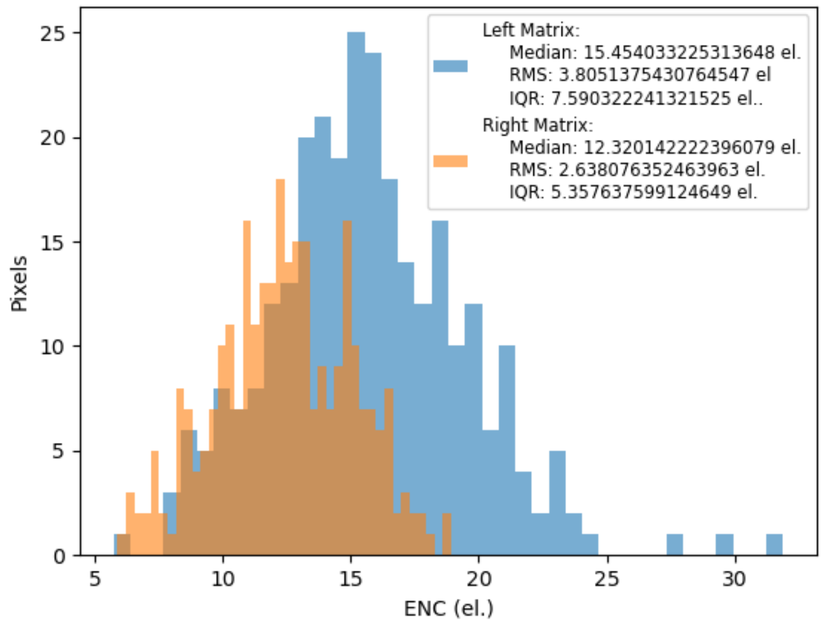


Figure 1: NAPA-p1 pixel general architecture.







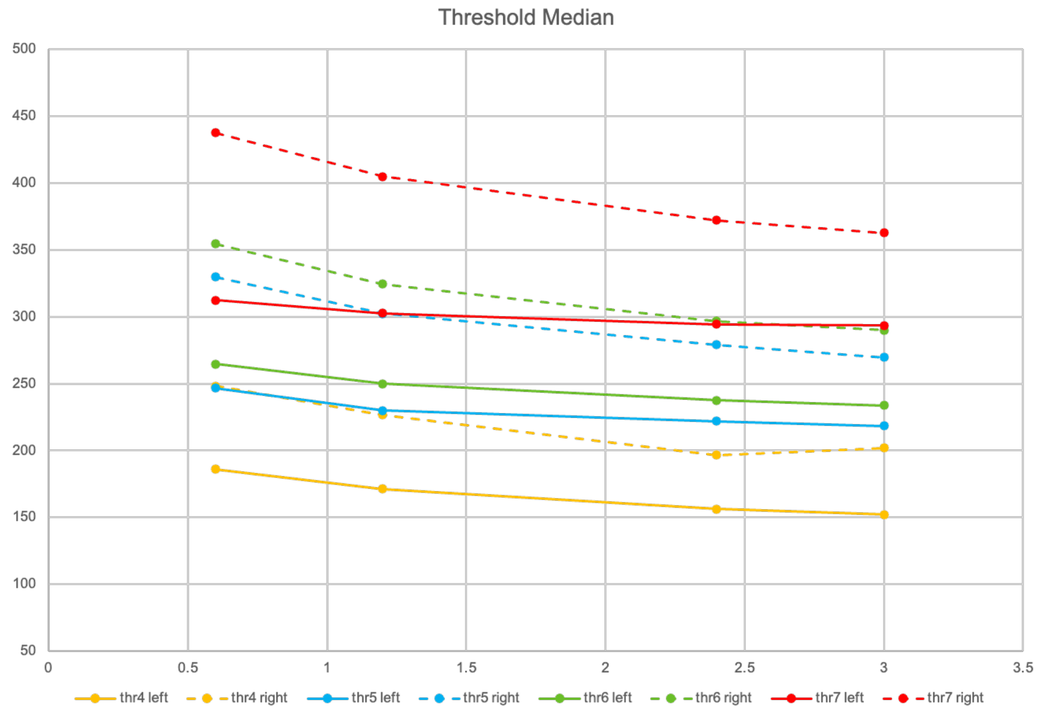
Left Matrix:
Nominal Pixel Variant

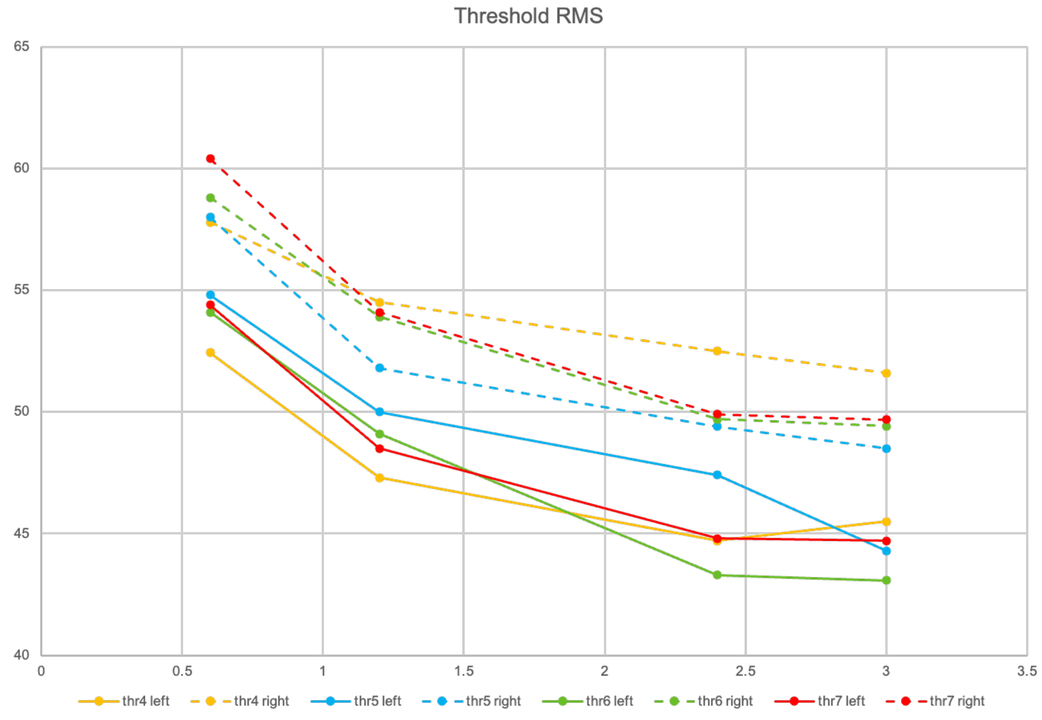
Right Matrix:
Pixel Variant with DC leakage current compensation

DC leakage current variant has less nosie

Threshold/ENC as a function of voltage and threshold

Left
Right





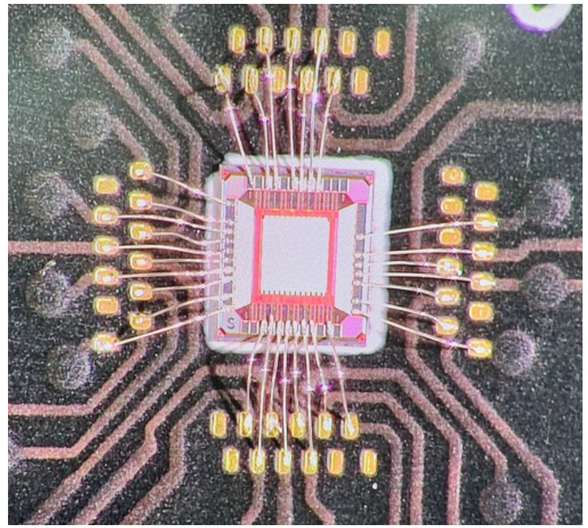
Threshold/ENC median and rms decreases with reverse bias.
In particular, left matrix ENC median and rms decrease more dramatically.

Conclusions and next steps

First MAPS prototype within CERN WP1.2 collaboration targeting e^+e^- requirements is being tested

- MAPS technology is being investigated for applications at future e^+e^- colliders for both tracking and calorimetry applications
- Developed first prototype within CERN WP1.2 based on TJ 65nm processing
  - First characterization of Napa-p1 is promising - more ongoing
  - Design of NAPA-p2 has started to tackle large sensor challenges and timing resolution of ~ns
    - NAPA-p2 will serve as a system proof of concept

NAPA-p1



Thank you!

Enabling technical capabilities at SLAC

Microwave Annealing & Device modeling and simulations

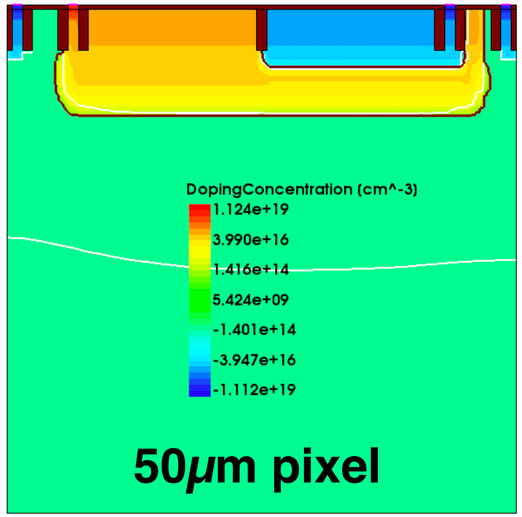
AXOM Microwave Annealing System in SLAC cleanroom

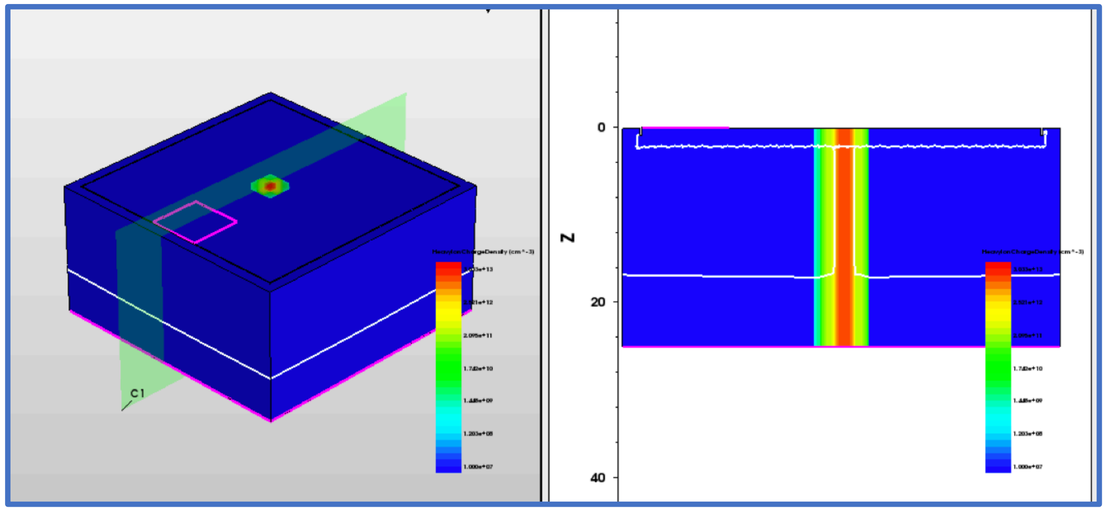
- Optimization of material to obtain desired properties (semiconductors, ceramics, polymers) often requires annealing (heat)
  - Heat may change, damage or destroy other elements of a structure
  - Heating materials is energy intensive process
- Microwave annealing (MWA) is a non-equilibrium annealing technique which selectively transfers energy to defects, dopants, interfaces or impurities
  - Tool facilitates development of novel device structures for sensors, ASICs
  - SLAC has developed several HEP applications using microwave annealing
  - MWA is compatible with CMOS processing, allowing advanced integration
- Experience in Device modeling and simulations
  - TCAD full characterization of new processes

MAPS on novel CMOS technologies

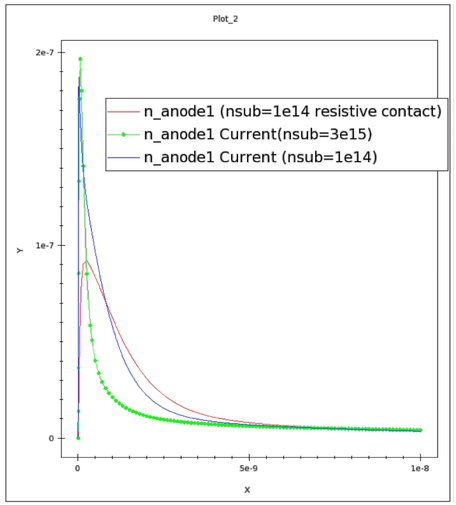
Blue-sky R&D on CMOS 22nm FDSOI

- Fully-Depleted Silicon-On-Insulator process enables implementation of sensor in substrate
- Promising CMOS process with excellent mixed-signal performance
- TCAD simulations and initial pixel design to evaluate key performance parameters:
  - Detector capacitance
  - Charge collection time
  - Cross-talk





3D Charge collection simulations (MIP)

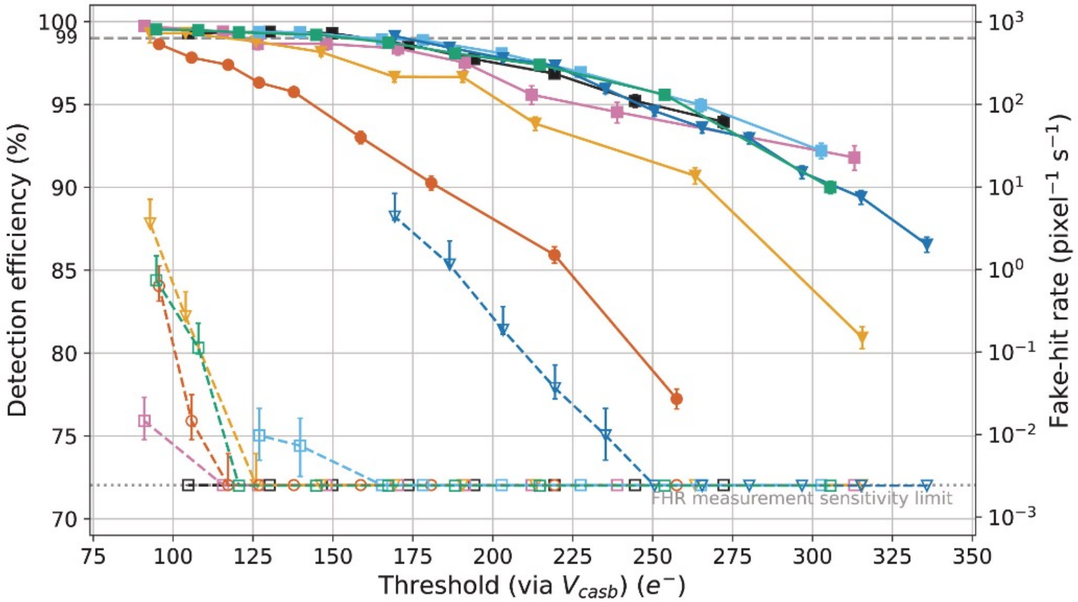


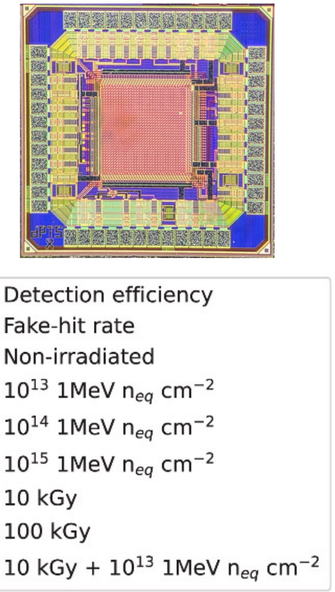
Read-out current:
compare three process options

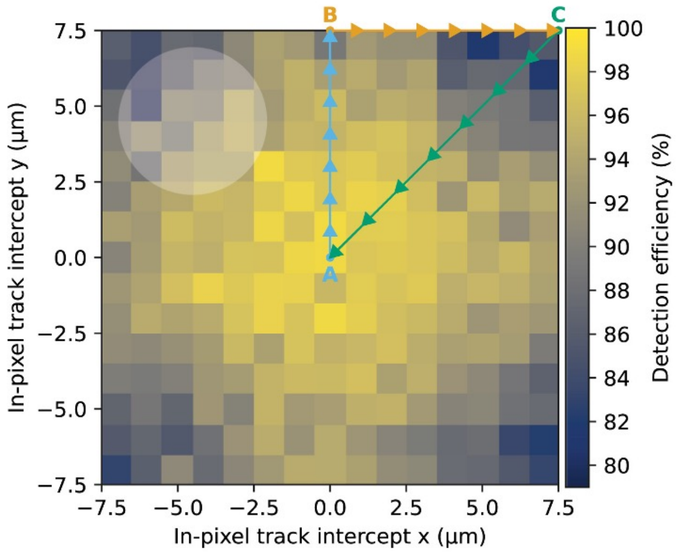
Recent results with Digital Pixel Test Structures

Synergies with DPTS characterization at CERN test beam facility within ALICE Collaboration

Characterization done up to 10^{15} 1 MeV n_{eq} cm^{-2}







Digital pixel test structures implemented in a 65 nm CMOS process
A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology

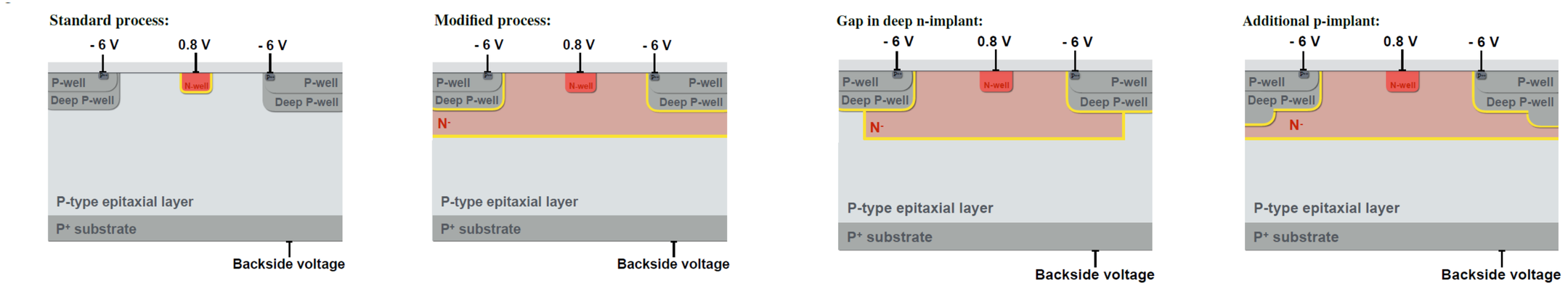
Design Approach

For a constant SNR and Q_{in} ➔ $Power \propto (C_{sensor})^m \quad with\ 2 \leq m \leq 4$ as shown in [11]

➔ **Aim for smallest possible sensor capacitance**

- Thanks to CERN WP1.2 effort on sensor optimization in TowerSemi 180 nm and 65 nm technologies [12] [13]
  - ➔ C_{sensor} of 2-3 fF is achievable while maintaining high collection efficiency

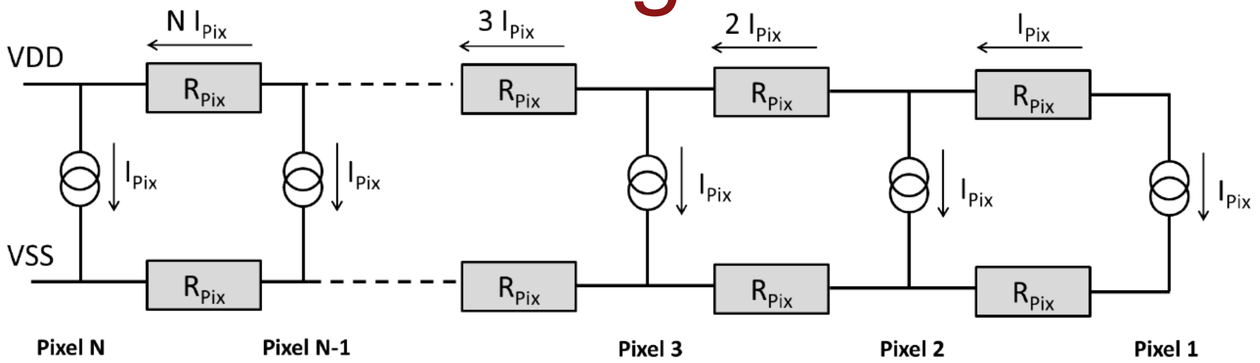
Jitter $\propto \frac{Cload}{\sqrt[n]{I}}$ with $1 \leq n \leq 2$ ➔ **Keep C_{load} to a minimum and increase the current if needed.**



Sensor optimization in TowerSemi 180 nm process from [12] and [13]

Going Towards a Large Sensor → Challenge

$$\Delta V = I_{pix} \times R_{Pix} + 2 \times I_{Pix} \times R_{Pix} + 3 I_{Pix} \times R_{Pix} + ... + N \times I_{Pix} \times R_{Pix}$$
$$\Delta V = I_{Pix} \times R_{Pix}(1 + 2 + 3 + ... + N)$$
$$\Delta V = I_{Pix} \times R_{Pix} \times \frac{N(N+1)}{2}$$



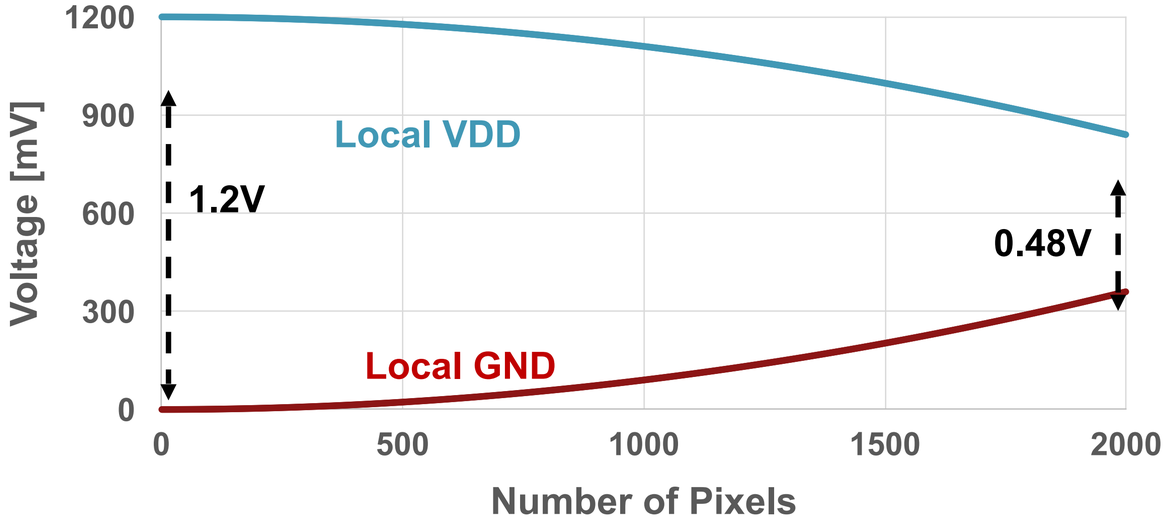
Assuming :I_{pix} = 600 nA and R_{pix} = 300 mΩ

Assuming pixel of 25 μm x 25 μm

A column of 10 cm would have 4000 pixels

Double sided powering

→ max drop length = 2000 pixels

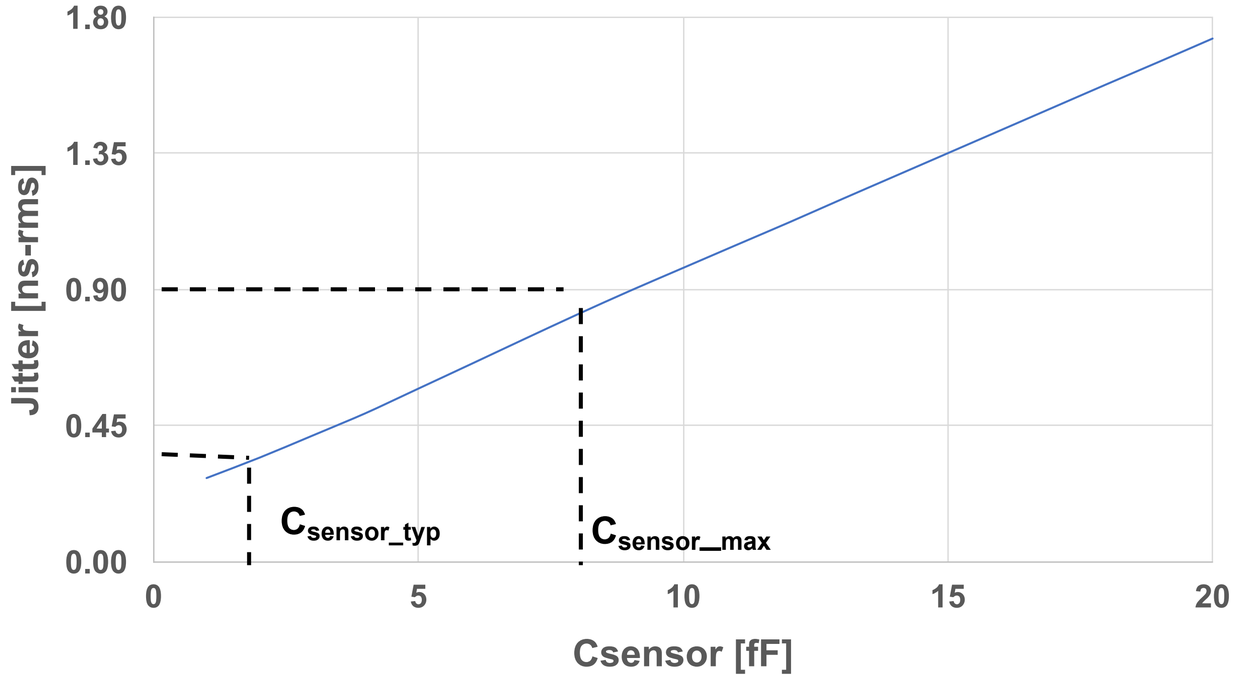


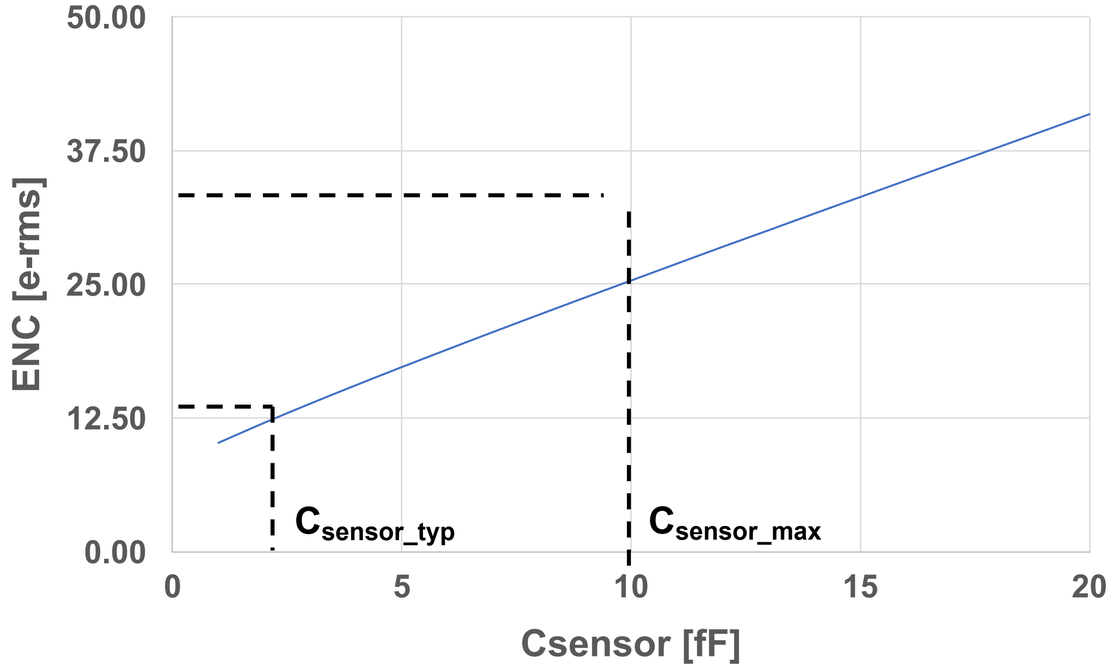
VDD-GND goes from 1.2 V near the power pads down to around 480 mV after 2000 pixels

The main limitation comes from large scale power distribution rather than cooling constraints

After 10^3 pixels (reticle, 2.5 cm), $V_{drop} \approx 0.1$ V
After 4 x 10^3 pixels (sensor, 10cm), V_{drop} = 1.5V !

Simulation of Jitter and ENC as a Function of C_{sensor}



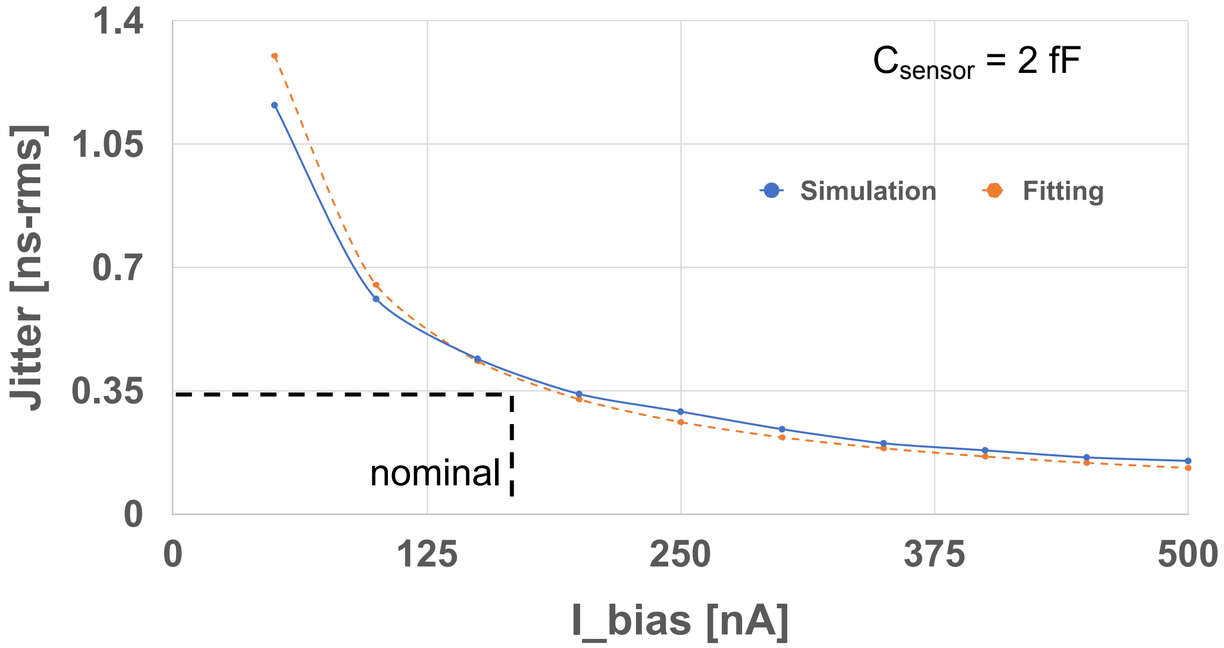


jitter = 400 ps for $C_{sensor\_typ} \approx 2$ fF → **Ok for Specs** ← **ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF**

These simulations are with a nominal pixel current of 600 nA → <Power density> = 115 mW/cm² x duty cycle
For e+e- machines such as ILC and C³, duty cycle is expected < 1%

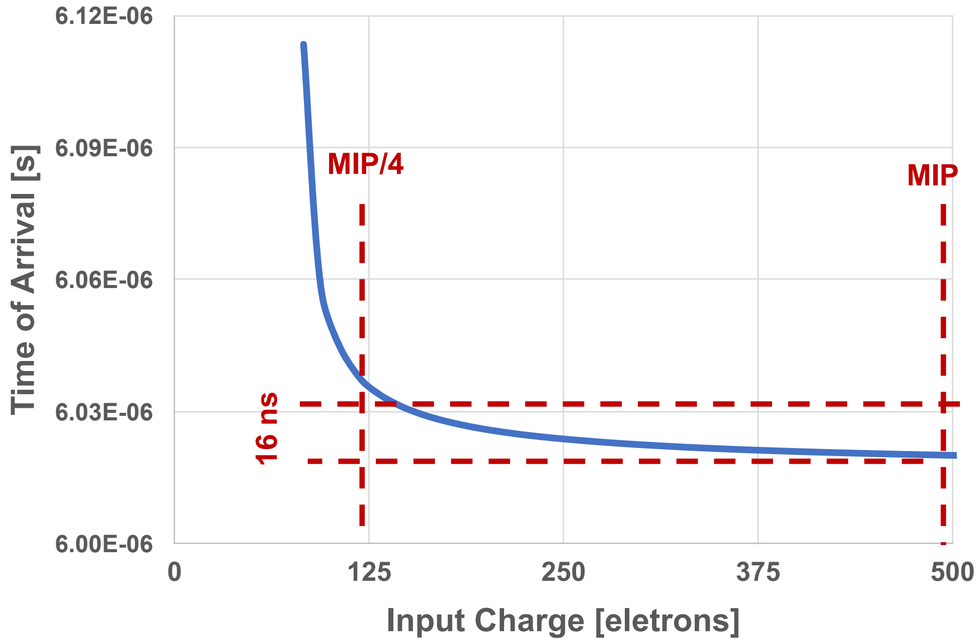
Simulation Results : Jitter and Time Walk

Jitter



I_bias = 200 nA ≡ pixel current = 600 nA
From theory we expect : $\sigma_{FE} \propto \frac{1}{(\mathrm{Power})^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

Time Walk



Time walk for MIP → MIP/4 = 16 ns
Not negligible and must be corrected
(in pixel? In balcony? Offline? TBD)