DuTiP :
Vertex Detector for Belle II Upgrade and Intermediate Silicon Tracker for ILC

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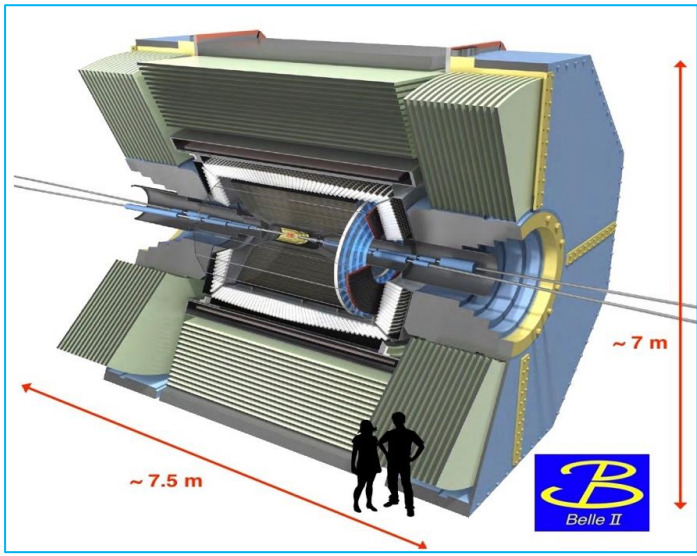
Belle II Vertex Detector Upgrade

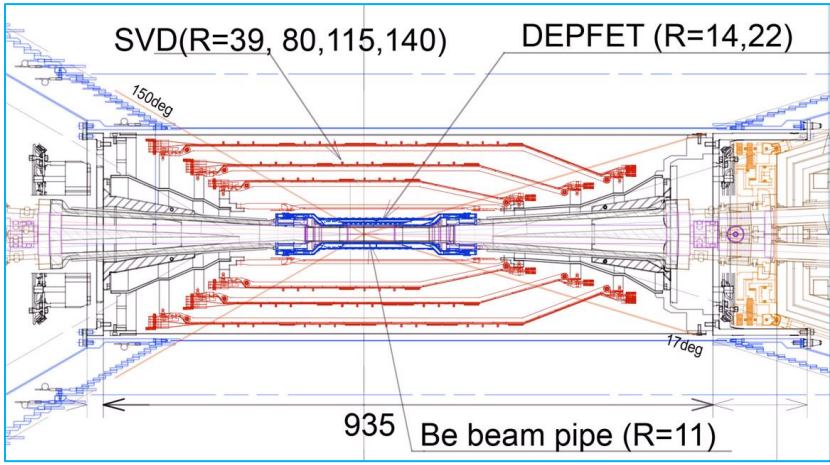
- Current Vertex Detector
  - 2-layer pixel (PXD:DEPFET)
    - Rolling shutter of 50kHz (20us) makes occupancy higher

system	layer	radius [mm]	hit rate [6] [MHz/cm^2]	occupancy [%]	TID [kGy/smy]	neutron [10^{10}n$_{eq}$/cm^2/smy]
PXD	1	14	22.6	1.3	19.9	40
	2	22	11.3	0.5	4.9	20

  - 4-layer strip (SVD:DSSD)
- Requirement for the upgrade

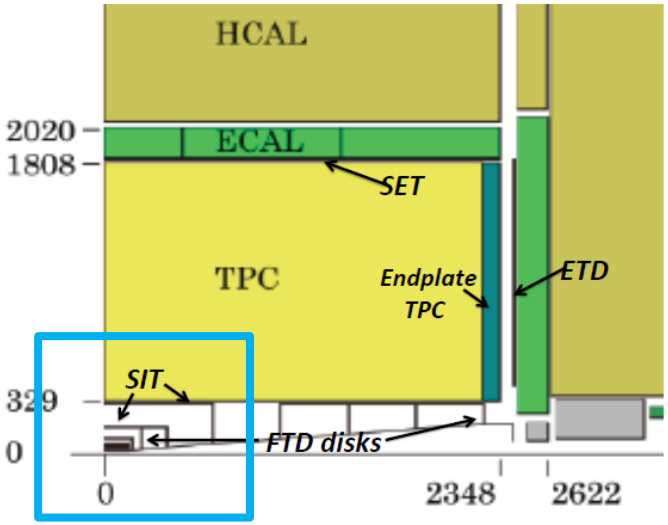


item	Requirement
# of layer	>=6
Position resolution	15um
Time resolution	~100ns
Readout rate	> 30kHz
Trigger latency	> 4.4us
Power consumption	< 100mW/cm^2



ILD Silicon Intermediate Tracker

- Location
  - Outside the VTX detector
- Purpose
  - Track extrapolation from/to TPC/VTX
    - position resolution 7um
  - Bunch identification
    - 1312 bunches with a spacing of 337ns
- Detector
  - Single-sided strip detector was baseline
    - Layer 7-10 (two doublets)
  - The first doublet (layer7,8) can be replaced to pixel detector
    - To minimize material
    - Better pattern recognition



SIT characteristics (current baseline = false double-sided Si microstrips)

Geometry			Characteristics		Material
R [mm]	Z [mm]	cos θ	Resolution R-ϕ [μm]	Time [ns]	RL [%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

DuTiP and SOI

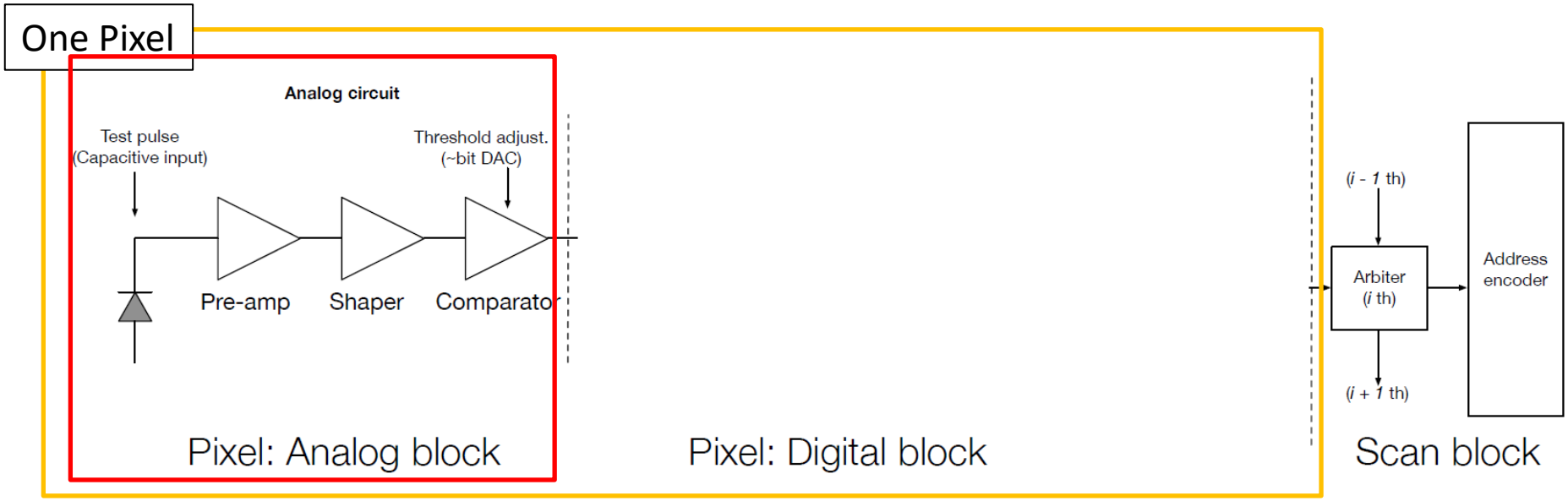
- We invented Dual Timer Pixel (DuTiP) concept for Belle II Vertex detector upgrade that can be also used for layer 7 and 8 of ILD SIT.

- Our requirements for Belle II Vertex detector
  - Binary detector to reduce data size and power consumption.
  - Relatively fast clock of > 10MHz to reduce the occupancy to O(10^{-4}) or less
  - Global shutter readout based on L1 Trigger to reduce data size.
  - Hold signals at least trigger latency of 4.4us
  - Low power consumption ~100W/cm^2
    - For normal temperature air cooling

- We adopted Silicon on Insulator (SOI) technology to realize the DuTiP

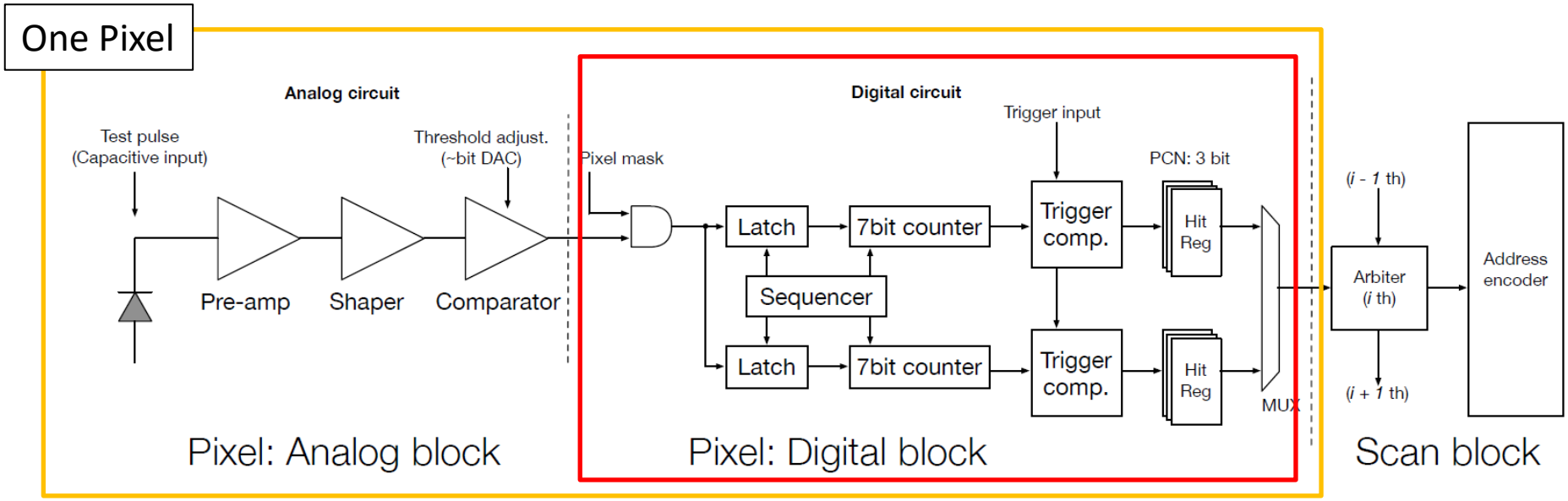
The Concept “DuTiP”

- Dual Timer Pixel
- Analog Circuit
  - In Pixel Amplifier/Shaper/Discriminator.
  - Binary signal sent to digital circuit in the pixel.



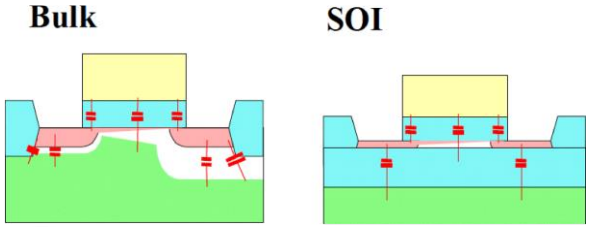
The Concept “DuTiP”

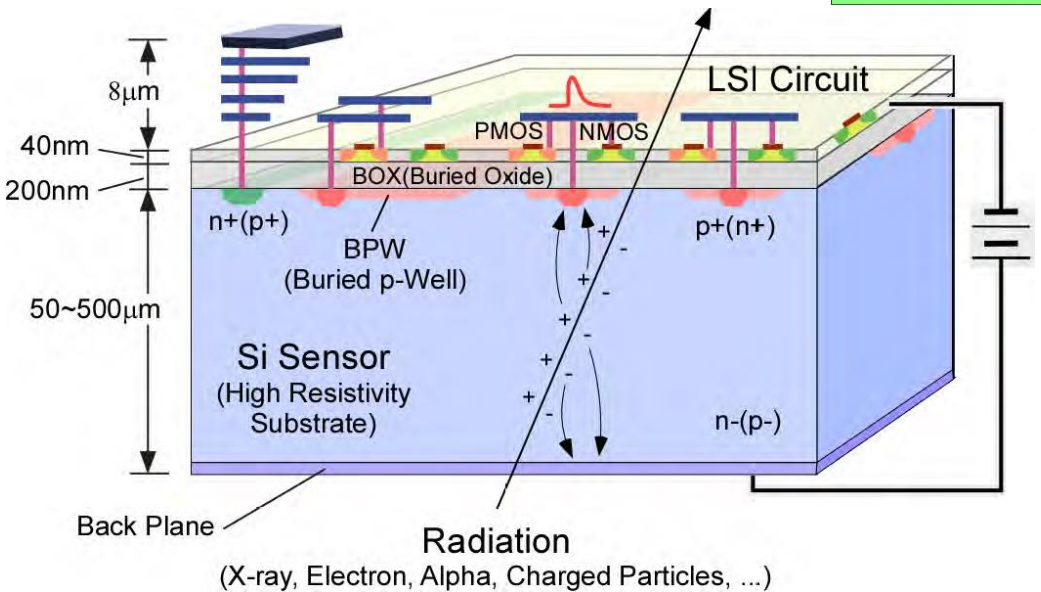
- Dual Timer Pixel
  - Dual Timer (down time counters) in a Pixel to store signal and wait for trigger signal
  - 7bit timer can wait trigger upto 127 x CLK.
  - Two timers allow the second hit during trigger latency
  - Hit registers for three time buckets, previous, current and next for timing scan



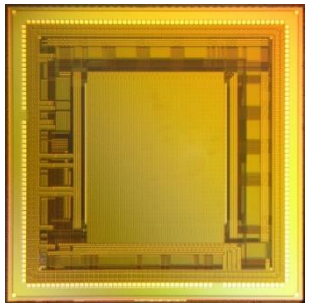
Silicon-on-Insulator (SOI)

- Insulator layer (BOX layer) sandwiched by circuit and sensor layer
  - Complicated circuit can be fabricated on circuit layer w/o bump bonding
- Fully depleted sensor : Fast signal, good S/N
- CMOS logics w/o well structure : High density, small parasitic capacitance
- Monolithic : Low material budget
- Good for high energy physics
- We adopt Lapis semiconductor 0.2um FD-SOI process





DuTiP1 with SOI technology



- Dimension
  - 6mm^2 chip
  - Pixel Size 45um x 45um
    - 45um/√12=13um
    - charge sharing improves the resolution
  - 64x64 pixel array
  - 300um^t (to be thinned to ~50um^t)
- Analog circuit
  - ALPIDE analog circuit fabricated on SOI by Strasbourg and modified by KEK.
  - Low power consumption amplifier
- Digital Circuit
  - 7bit timer x 2
  - 15.9MHz(62.9ns) CLK (SuperKEKB 509MHz/32(1.97ns*32))
    - Trigger latency of at most 8us (4.4us requirement)
  - Only current and previous time buckets (no next bucket)
  - No sophisticated readout circuit not fabricated

Estimation of Occupancy and Data Rate/Size

- Occupancy is enough small O(10^{-4}) or less

Layer	hit rate [Hz/pixel]	hit occupancy in PCN [10^{-4}]
1	458	0.86
2	229	0.43

system	layer	radius [mm]	hit rate [6] [MHz/cm^2]	occupancy [%]	TID [kGy/smy]	neutron [10^{10}n$_{eq}$/cm^2/smy]
PXD	1	14	22.6	1.3	19.9	40
	2	22	11.3	0.5	4.9	20

PCN : previous, current and next time buckets

- Data rate/size are enough small even for layer1.
  - Thanks to in pixel discriminator

Layer	data rate per SS chip [Mbps]	data rate per ladder [Mbps]	data rate per layer [Mbps]	data size [TB/smy]
1	11.3	34.0	272	340
2	5.65	22.6	271	339

Intrinsic and Impact parameter Resolutions with GEANT4

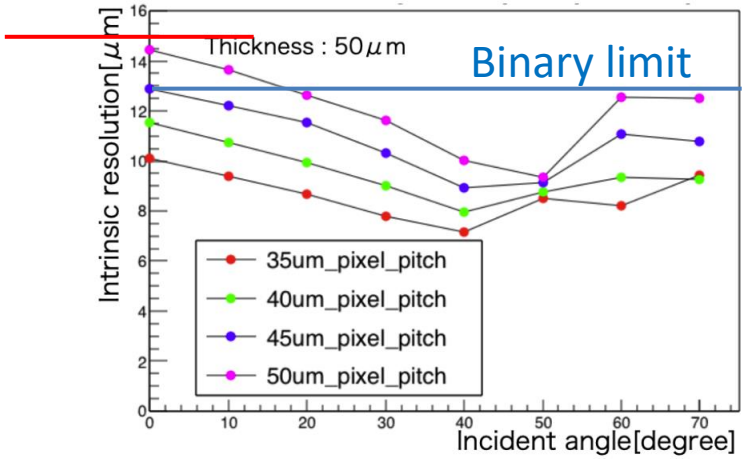
- Sensor intrinsic resolution and impact parameter resolution has been studied with simple geometry using GEANT4 MC.
  - Intrinsic resolution is better than binary limit thanks to charge sharing

Beam pipe + 2layer DuTiP + 4Layer SVD

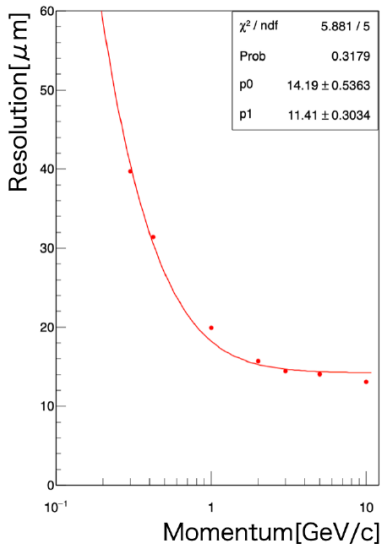
impact parameter resolution for theta=90deg

requirement

intrinsic resolution

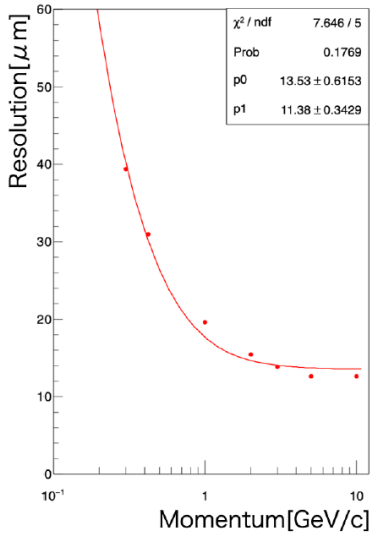


Z resolution



$$\sigma_Z(\mu m) = 14.2 \oplus \frac{11.4}{p \sin^{\frac{5}{2}}\theta}$$

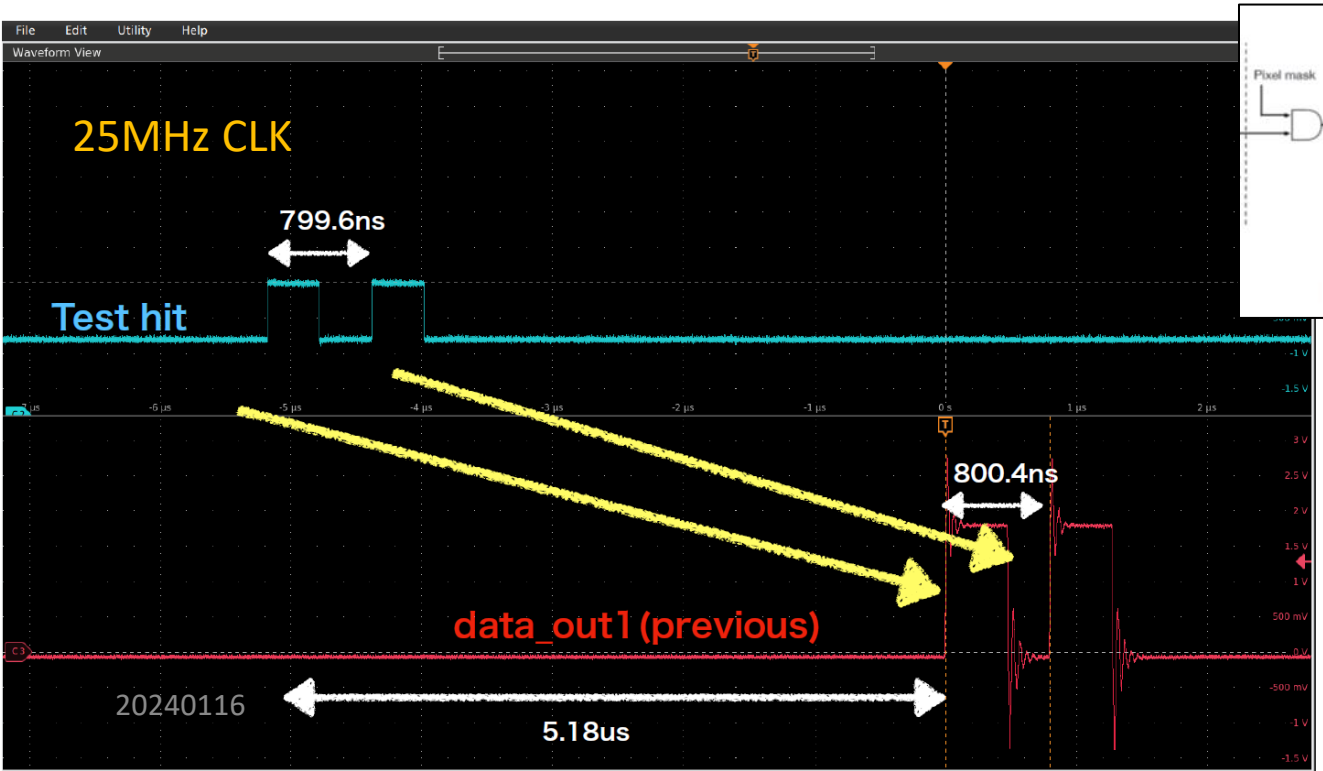
rϕ resolution

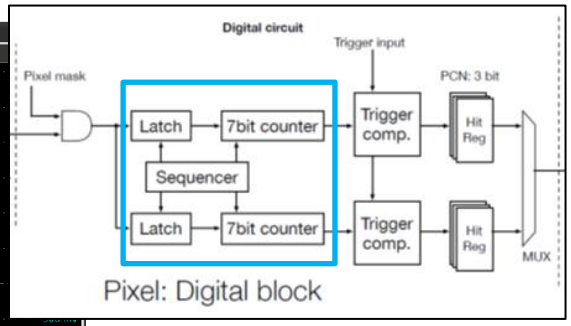


$$\sigma_{r\phi}(\mu m) = 13.5 \oplus \frac{11.4}{p \sin^{\frac{3}{2}}\theta}$$

Characterization Sequencer/Dual Timer

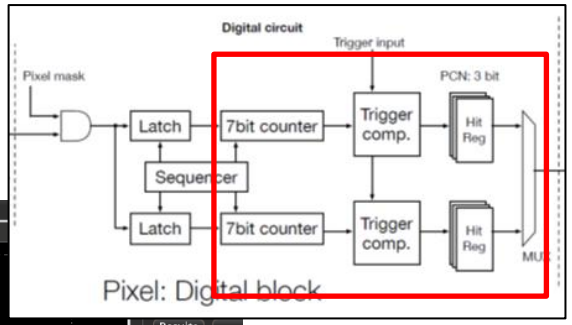
- Two test hit signals with 800ns interval which is less than trigger latency are injected.
- Triggers are also injected to previous timing
  - Two output signal can be correctly seen in previous buckets

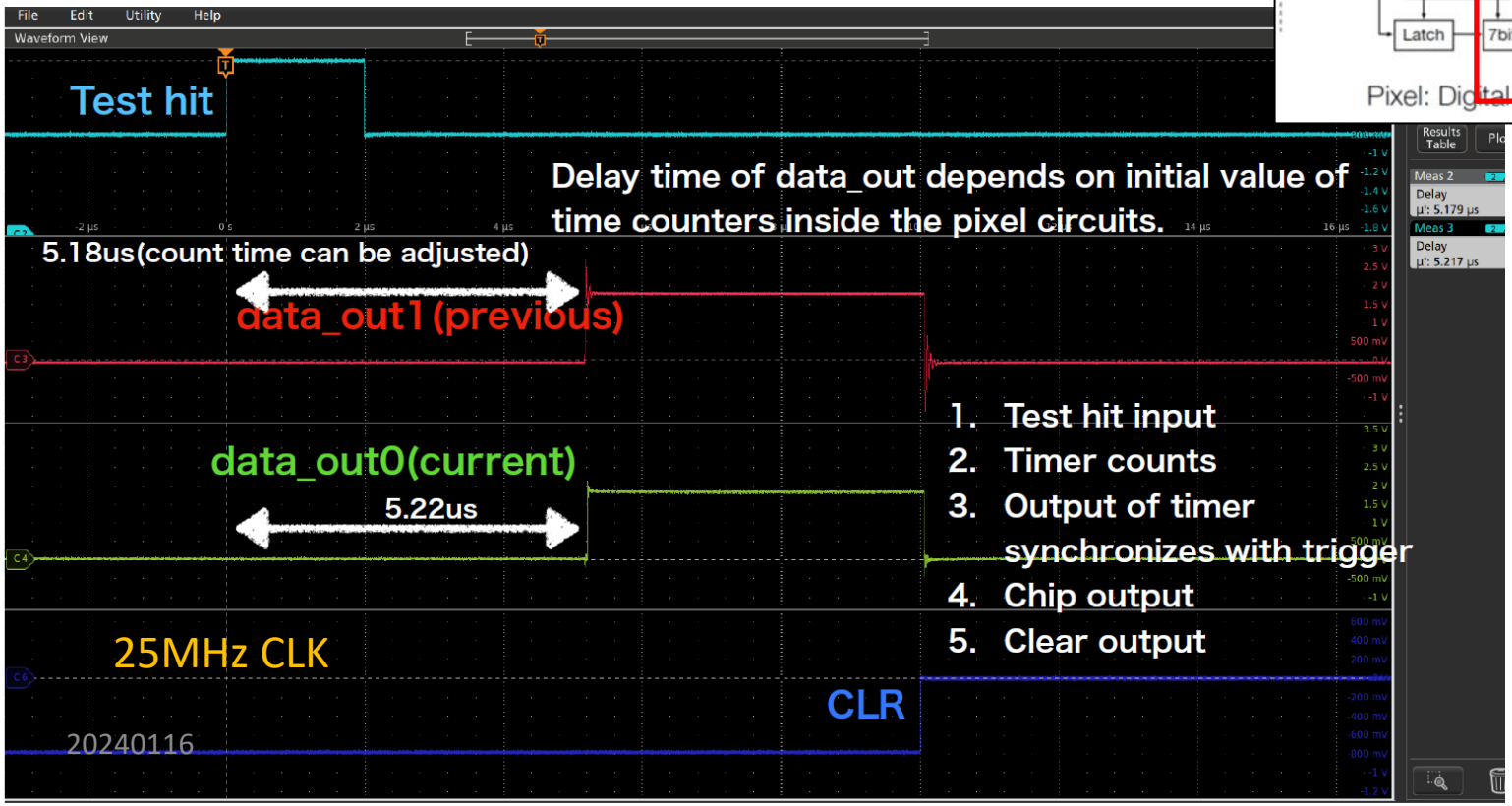




Characterization
Timers and Time Buckets

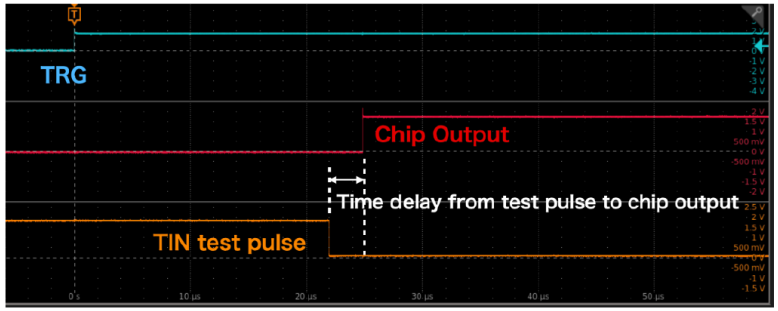
- test hit signal
  - 7bit counters (127*40ns=5080ns) are working fine
  - Correctly assigned to previous and current time bucket
- Digital Circuit is working perfectly.

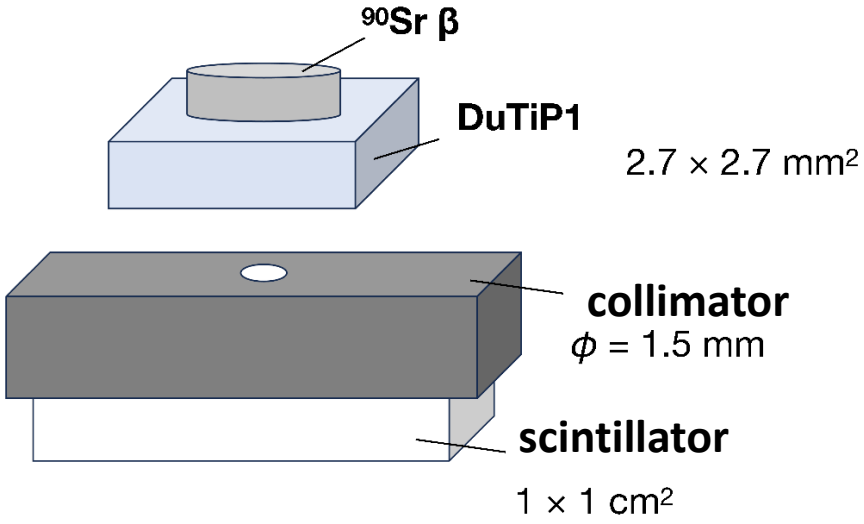




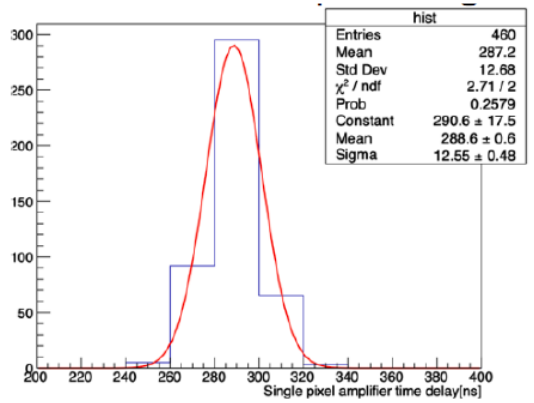
Timing Resolution for single pixel

- DuTiP + Scintillation counter
- Tested with ^{90}Sr and 50MHz CLK (20ns)
  - Timing resolution is 11.2ns
    - With test pulse ~10ns
  - Enough smaller than time bucket of 63ns





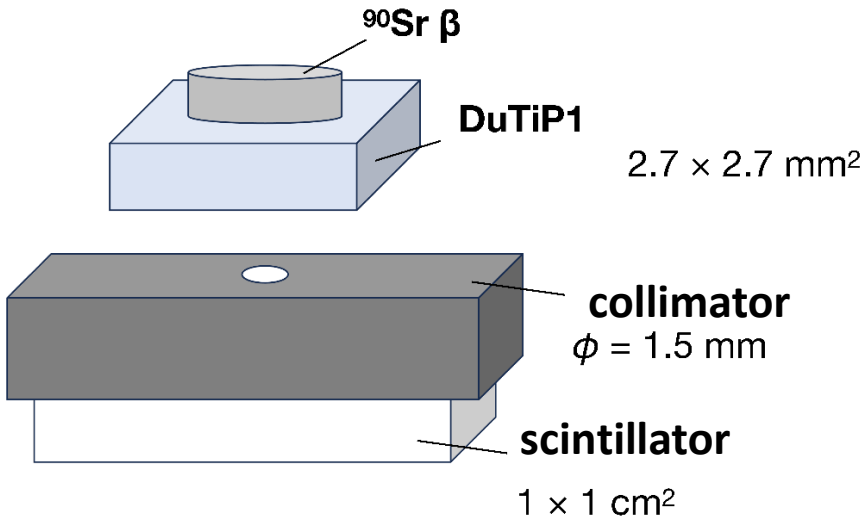
12.6ns including binning effect



Efficiency and Yield

- Efficiency
  - Using ^{90}Sr : ~98+-2%
  - Cosmic or accidental noise hit are subtracted with dry run data.
  - Large systematic uncertainty due to limited setup
  - To be tested with test beam

- Production yield is checked without collimator
  - More than 99% pixel is working



^{90}Sr irradiation

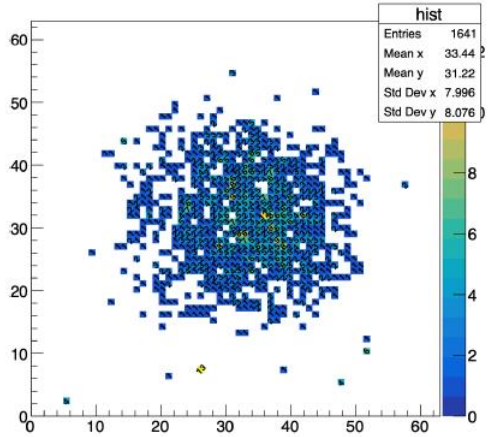


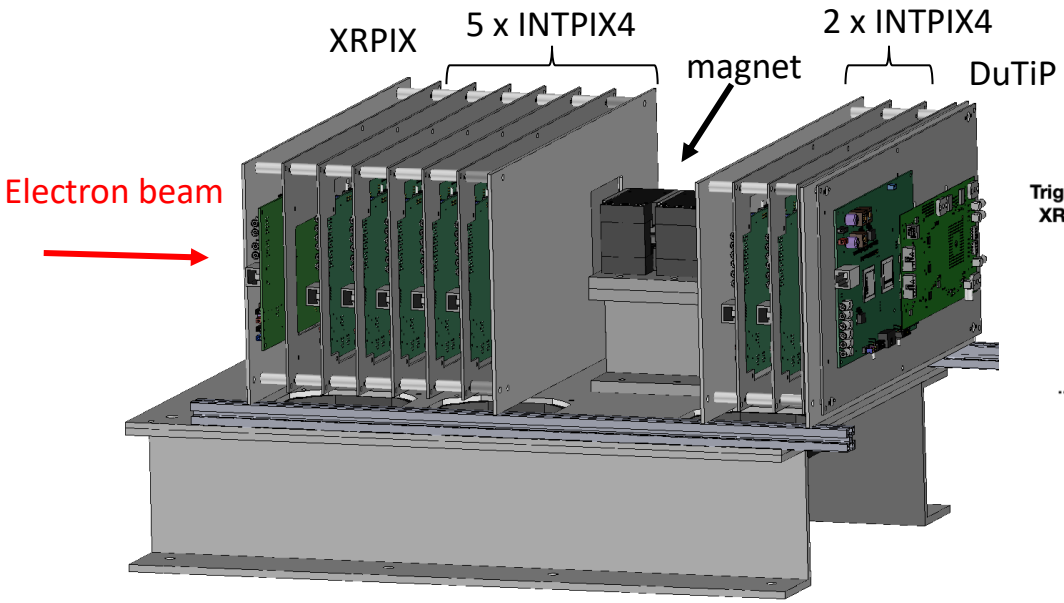
fig. The histogram image of the beta ray. Triggered by the electrons restricted by the collimator.

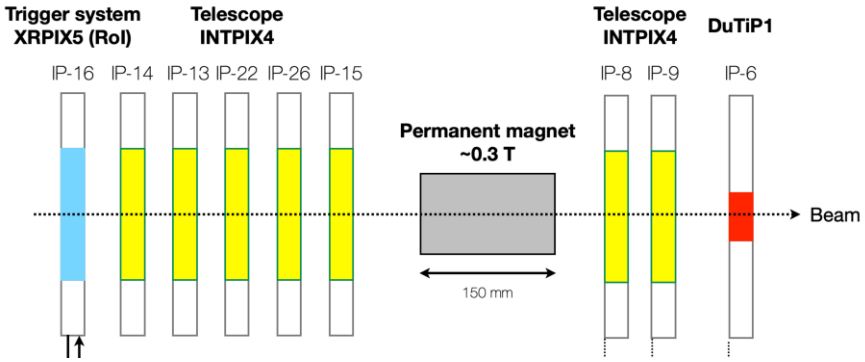
Electron Beam Test at ARTBL/KEK

- KEK have a new electron beam line ARTBL
  - upto 5GeV electron can be used.
- Upstream station
  - XRPIX Trigger System, 5 layers of INTPIX4
- Downstream station (about 19cm is displaced from upstream)
  - 2 layers INTPIX4
  - DuTiP

Since the DuTiP1 firmware for test beam was finalized just before the beam test, DuTiP1 should be placed most downstream.

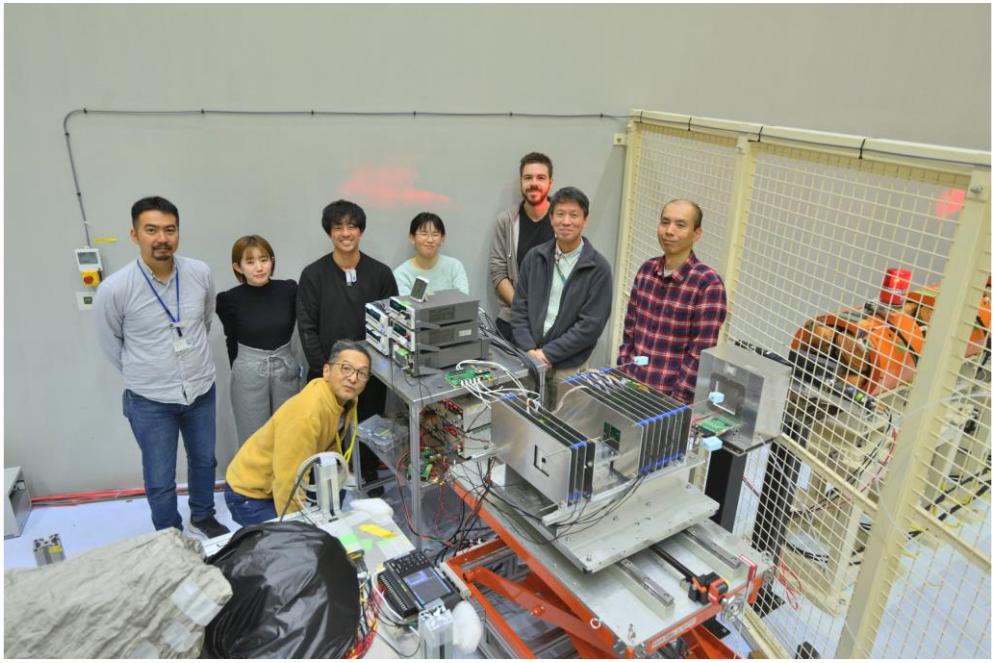
- Each layer has 32mm displacement in z direction

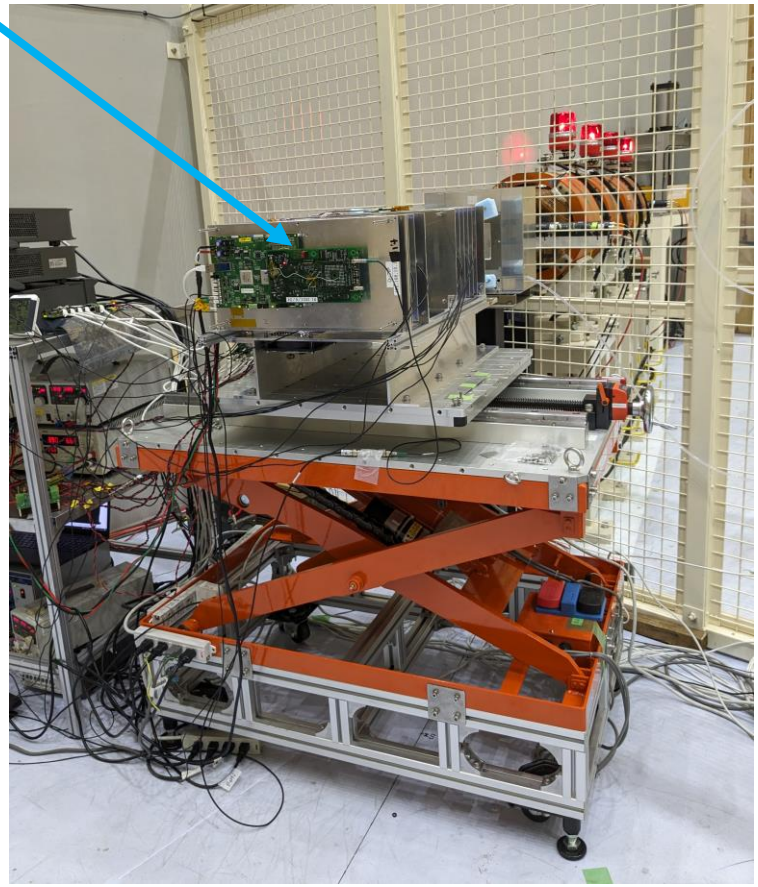




Picture of the Setup

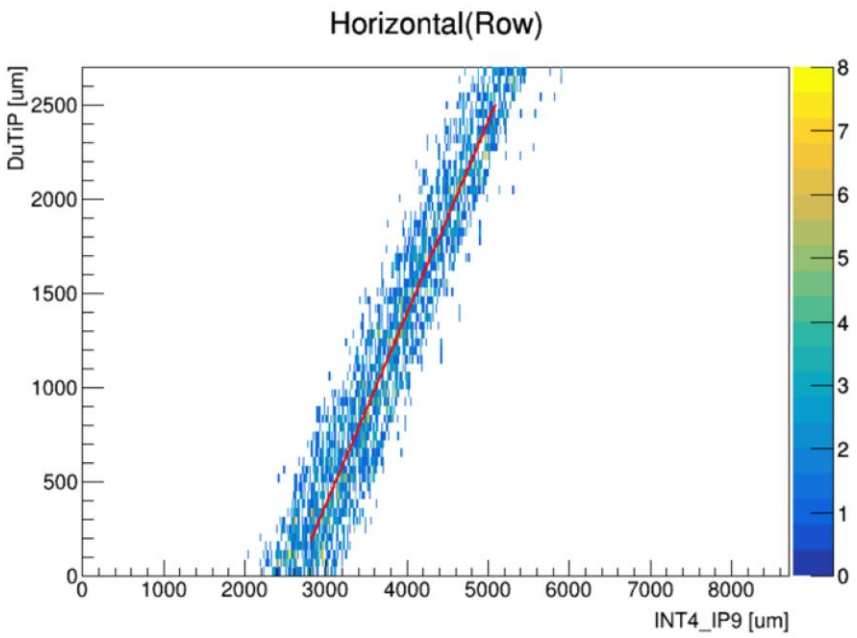
- DuTiP layer is located at most downstream

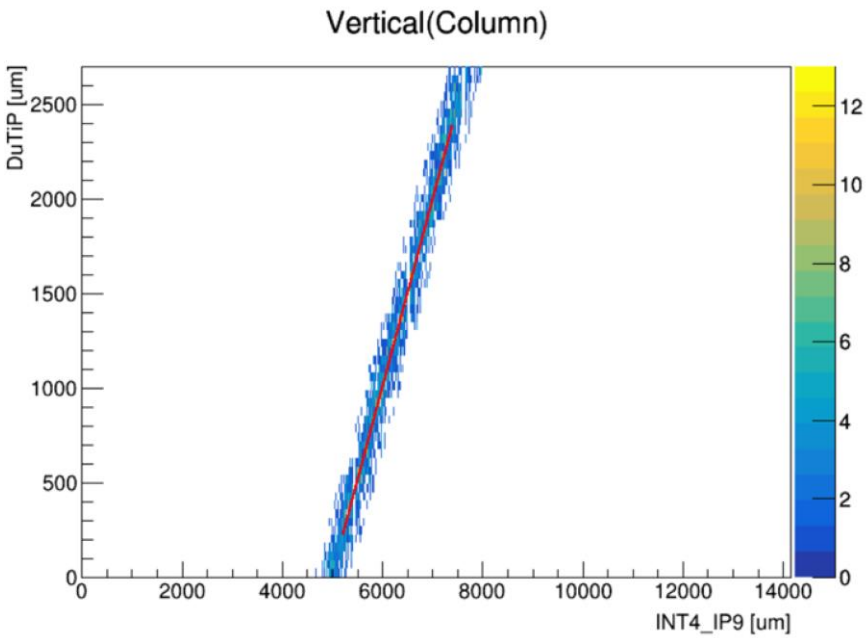




Correlation of hits

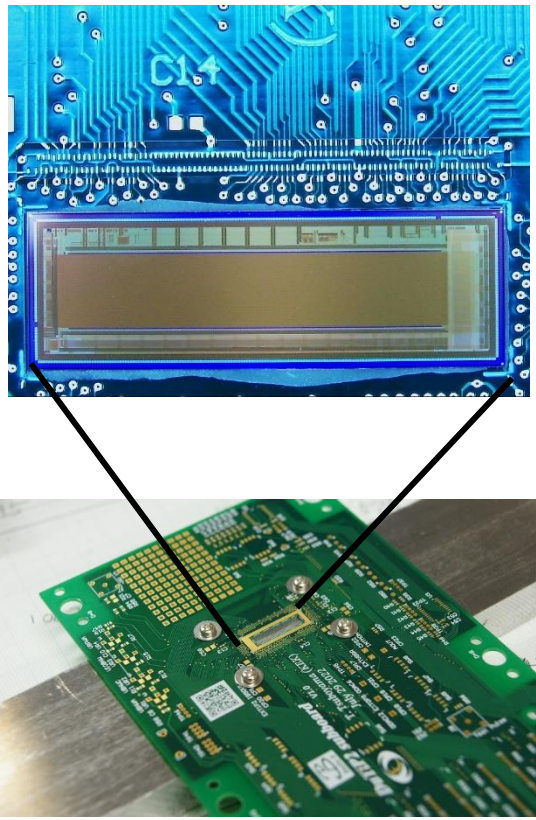
- Electron beam (MIP) was seen with DuTiP!
- We check the correlation of hits between DuTiP and INTPIX4 (closest to DuTiP) without alignment.
- We see clear correlation both in horizontal and vertical directions.





DuTiP2 and DuTiP3

14.4mm x 2.88mm



- DuTiP2
  - Almost Full functionality
    - Except for PLL and pixel array scan system
  - Full size chip just for row direction (r-phi)
    - Chip size : 17.2mm x 6.0mm
    - Pixel array : 14.4mm (row) x 2.88mm (column)
      - Full size chip 14.4mm (row) x 28.8mm (column)
    - Increasing the size to z (column) direction is trivial
  - Delivered in 2022 June.
  - Characterization on-going
- DuTiP3
  - Same chip as DuTiP1 except for analog circuit improvement
  - Delivered in 2024 March.
  - Preparing subboard and packaging

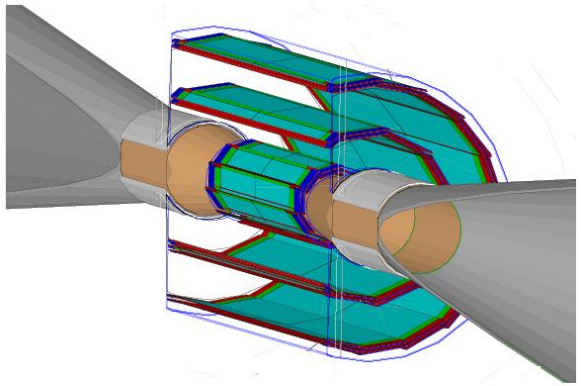
Summary

- We invented new pixel detector concept DuTiP for Belle II and ILC
- Three prototypes were fabricated using SOI technology.
- Performance of DuTiP1 with 300um^{t} was tested
  - Using ^{90}Sr
    - Good timing resolution, efficiency, and production yield
  - Using electron beam
    - MIP was seen
    - Correlation between other silicon detector was seen
- DuTiP2 and DuTiP3
  - Characterization on-going for DuTiP2
  - Characterization to be started for DuTiP3

backup

ILD Vertex Detector

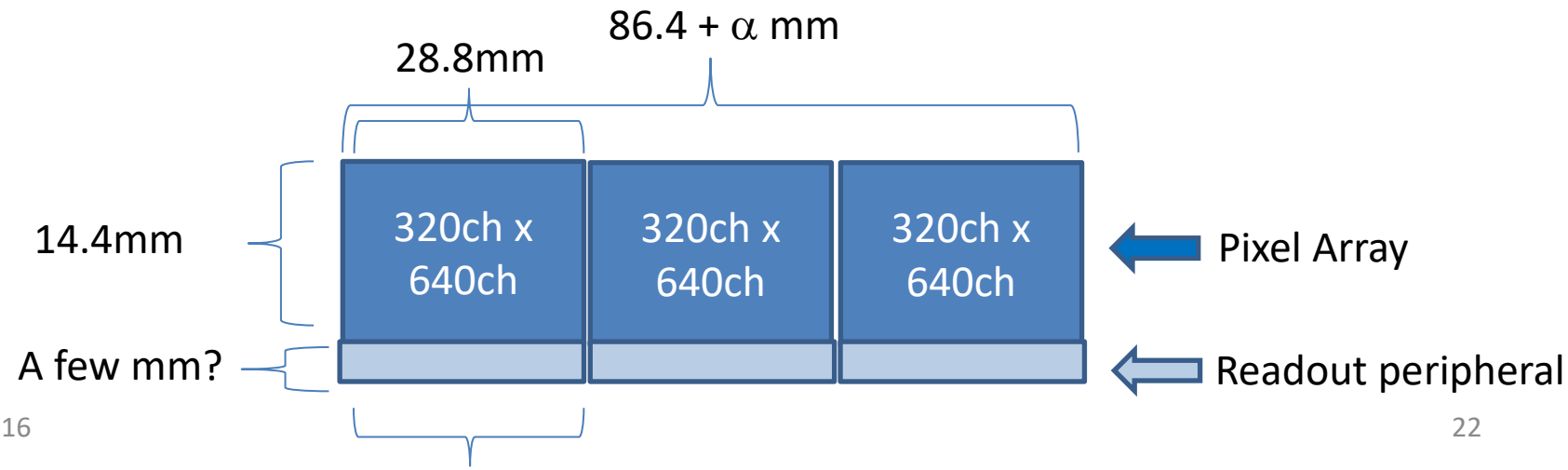
- 6-layer vertex detector
- Requirements
  - Impact Parameter resolution
    - $\sigma_b = 5 \oplus 10/p\sin^{3/2}\theta[\mu m]$
  - Position resolution
    - < 3μm
  - Radiation length
    - 0.15%/layer
  - Radius for inner most layer
    - R=1.6cm for B=3.5T
  - occupancy
    - < a few %
  - Power consumption
    - 100mW/cm^2



	R (mm)	$\lvert z\rvert$ (mm)	$\lvert\cos\theta\rvert$
Layer 1	16	62.5	0.97
Layer 2	18	62.5	0.96
Layer 3	37	125	0.96
Layer 4	39	125	0.95
Layer 5	58	125	0.91
Layer 6	60	125	0.9

Sensors for Layer1

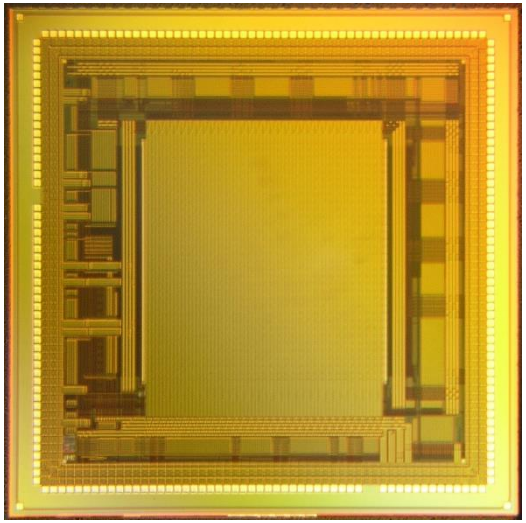
- Layer1 : R=1.4cm, Z=7cm
- maximum mask size for SOI is 2.46 x 3.08 cm^2
- We need three chip to cover the acceptance in Z.
  - Row : 45um x 320ch = 14.4mm
  - Column : 45um x 1920ch (640ch x 3) = 86.4mm (28.8mm x 3)
  - Thickness : $50um^t$
  - (Stitching buffer width: ~10um if we adopt stitching)
- 8 ladders to cover the acceptance in phi



Prototype1 : DuTiP1

- Designed for Belle II pixel detector
- Dimension
  - Size 6x6mm^2
  - Pixel size 45x45um^2
- Circuit fabricated
  - Modified ALPIDA-type analog circuit for FD-SOI
  - Basic in-pixel digital circuit of DuTiP concept
  - Many test circuits
- Circuit NOT fabricated
  - Sophisticated pixel scanning circuit
  - Fast data transfer circuit from the periphery to outside
    - LVDS/PLL are developed separately.
  - Issuing input signal to L1 track trigger system
- DuTiP1 Chip Delivered from Lapis
  - sub-board production just completed yesterday
  - Chip packaging on-going at REPIC
  - Firmware/software development started

DuTiP1



DuTiP1 sub-board

Characterization of DuTiP1

- Analog
  - Basics of modified ALPIDA-type analog circuit for FD-SOI
    - gain
    - Noise level
    - Threshold tuning
    - shaping time
- Digital
  - PIXOR digital circuit had worked perfectly with 50MHz so we think it should work
  - Test each elements
    - Sequencer for dual timer
    - Timer
    - Trigger time comparison
- If everything works fine, a beam test with thinned chip is performed at KEK PF electron beam line.
  - Efficiency
  - Position resolution

Prototype2 : DuTiP2

- Full functionality
  - Circuit NOT fabricated for DuTiP1 should be
    - Sophisticated pixel scanning circuit
    - Fast data transfer circuit from the periphery to outside
    - Issuing input signal to L1 track trigger system
      - Separate chip (outer layer)?
      - Single timer enough for outer layers
  - Full size chip just for row direction, ex. 17.2mm (row) x 9.0mm (column)
    - Full size chip 17.2mm (row) x 29.6mm (column)
    - Increasing the size to z direction is trivial

pitch [μm]	row $\times$ column [pixels]	array r-ϕ $\times$ z [mm^2]	array area [cm^2]	chip r-ϕ $\times$ z [mm^2]
45	320 $\times$ 640	14.4 $\times$ 28.8	4.15	17.2 $\times$ 29.6

- Submit the chip in the end of 2021
  - Dependent on MPW schedule

Summary

- Two SOI detectors are being developed.

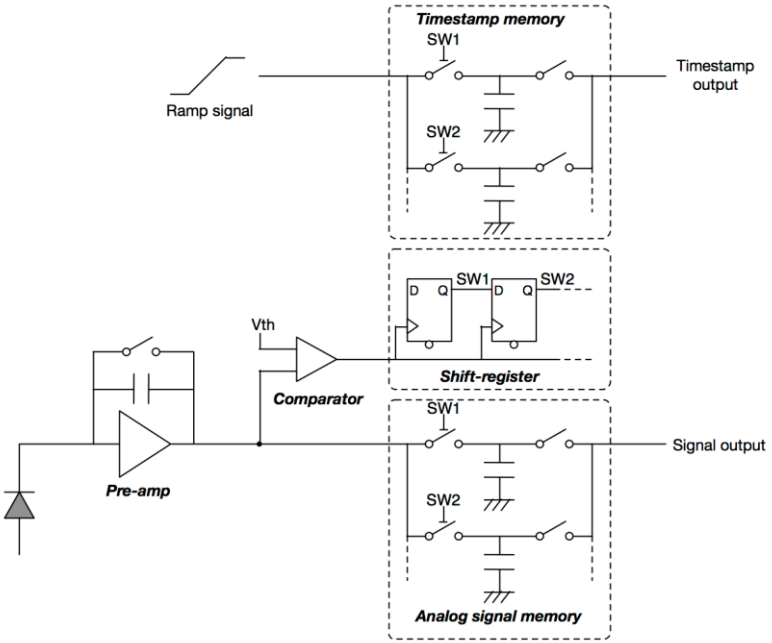
- SOFIST
  - FNAL beam test study
  - Budget problem…

- DuTiP
  - First prototype for Belle II
    - Characterization started.
  - Second prototype in this JFY
  - To be modified for the SIT

SOFIST

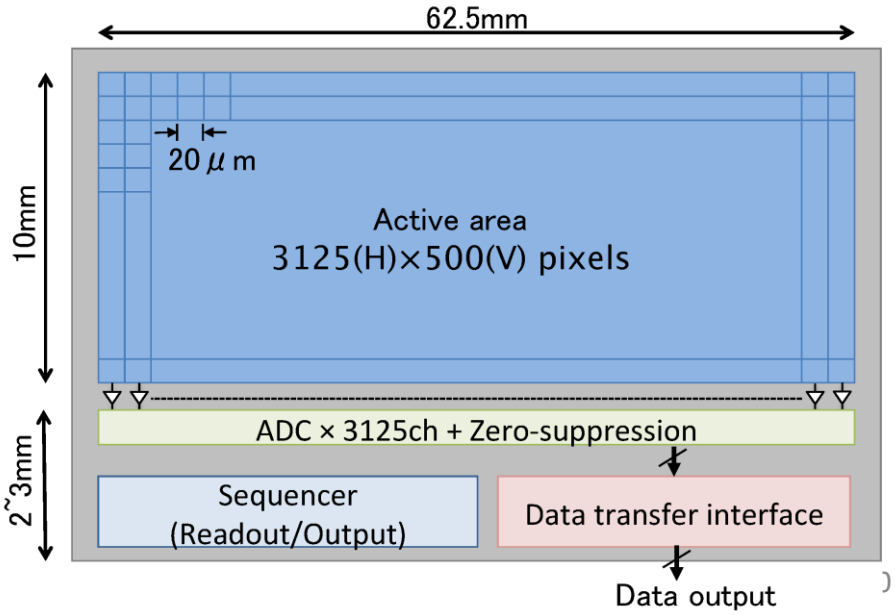
SOI For **Fi**ne Measurement of **S**pace and **T**ime

- Concept
  - Position is measured with 20um pixel pitch with analog readout
    - Resolution of <3um possible
  - Timing is measured with the analog time stamping memory
    - If a hit is found in a pixel, charge is injected to the analog memory till the end of a train.
  - Inter-train readout

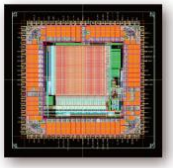
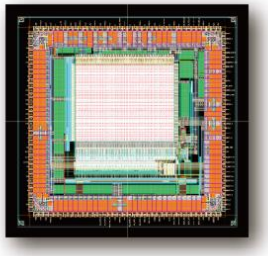
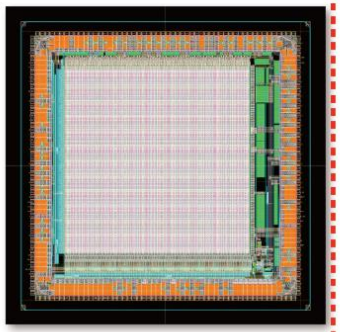
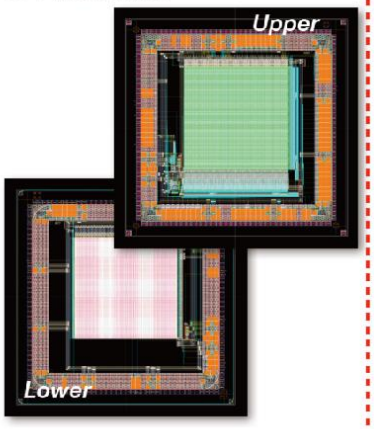


SOFIST

- Size
  - 62.5 x 10.0 mm
- In pixel
  - amp/comparator/shift register
  - Three memories are fabricated in a pixel for multiple hits in a train
- On chip
  - ADC
  - Zero suppression



SOFIST

SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
	Beam test at FNAL in Jan. 2017 Analog signal	Beam test at FNAL in Feb. 2018 Analog signal or Timestamp	Beam test at FNAL in Feb. 2019 Analog signal and Timestamp	Beam test at FNAL in Feb. 2020
				
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Time resolution ~1.92 μs	Delivered (Jan. 2019 ~) Under evaluation

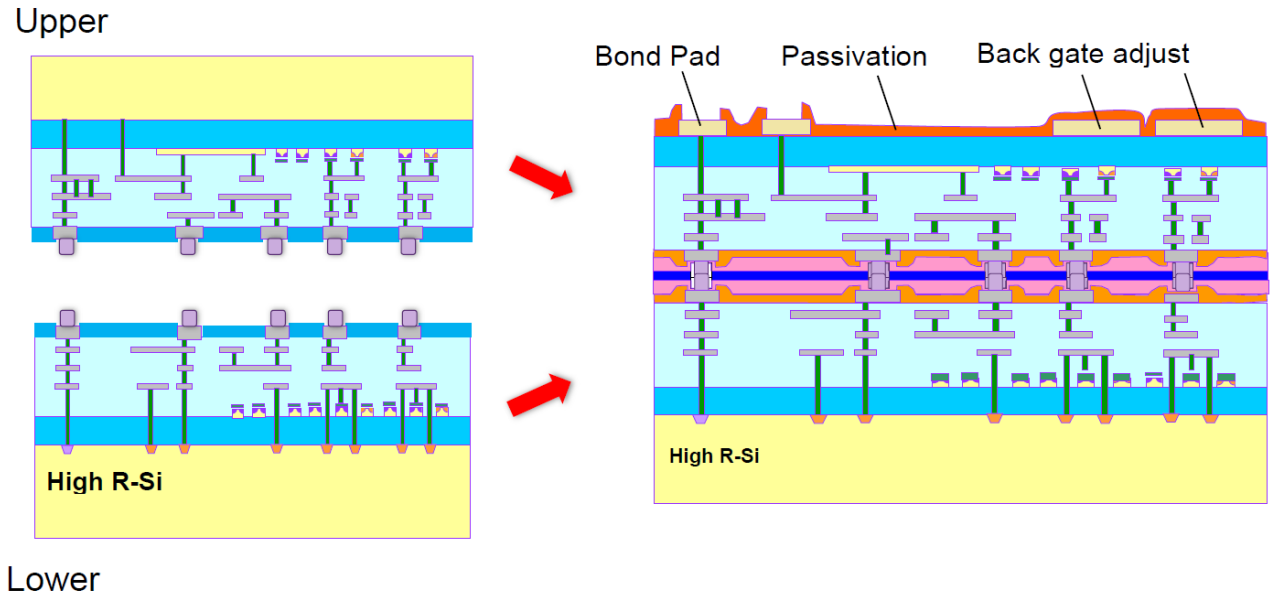
Performance

- With SOFIST3, we already achieved
  - 1.4um position resolution
  - 1.9us timing resolution
- But the pixel pitch is 30um with 3 memories
  - A bit large in terms of buffer overflow probability

- We need to reduce the pixel size

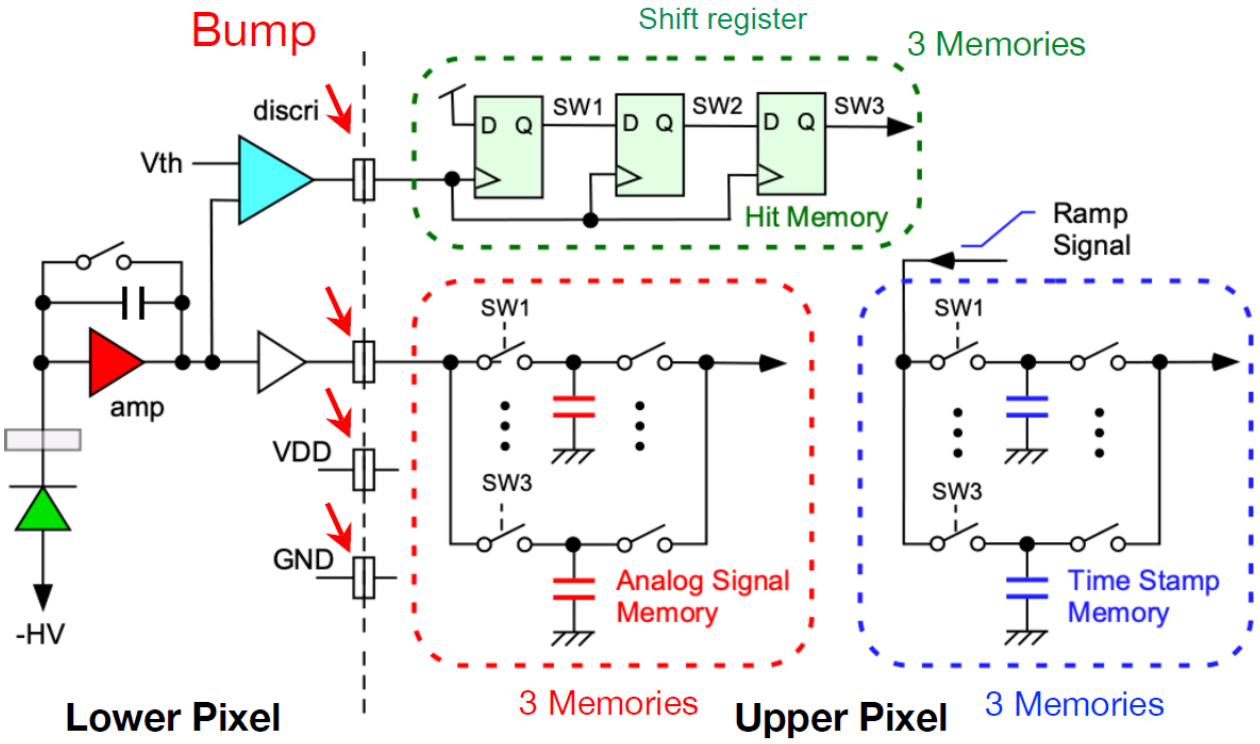
3D Stacking

- To achieve 20um pitch with complicated circuit, we need 3D stacking.
- Two SOI chip can be stacked to single one



SOFIST4 3D

- The bonding yield is more than 99.9%

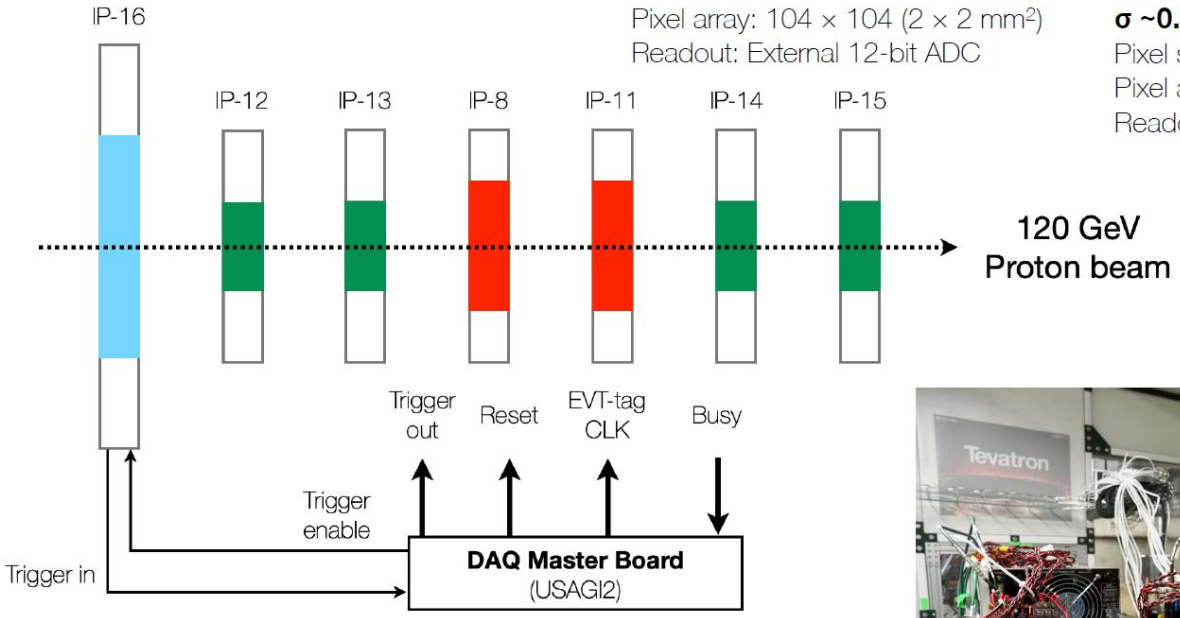


Beam Test

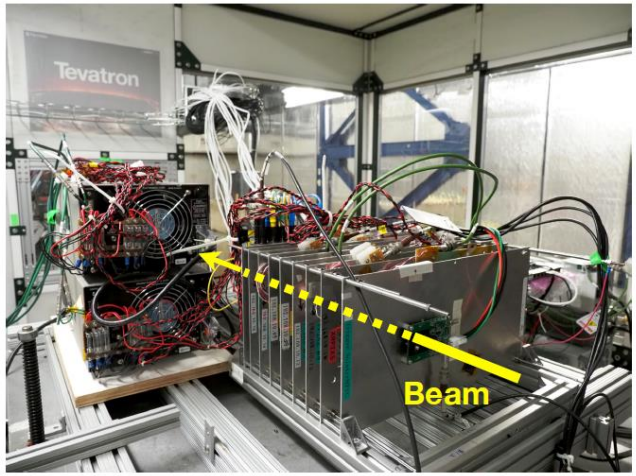
Beam: 120 GeV proton (Fermilab Beam Test Facility)
DAQ rate: ~120 events/s

SOFIST4
Pixel size: 20 × 20 μm²
Pixel array: 104 × 104 (2 × 2 mm²)
Readout: External 12-bit ADC

FPIX2 (SOIPIX)
Telescope for SOFIST
σ ~0.7 μm
Pixel size: 8 × 8 μm²
Pixel array: 128 × 128 (1 × 1 mm²)
Readout: External 12-bit ADC



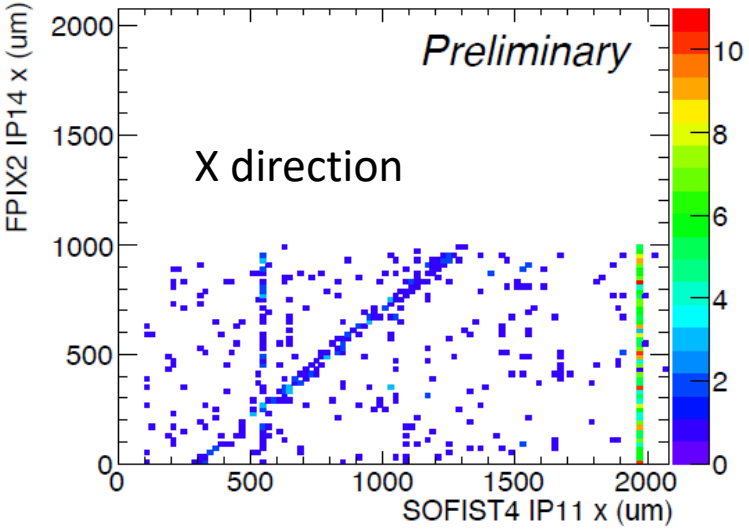
XRPIX5 (SOIPIX)
Trigger counter
Pixel size: 36 × 36 μm²
Pixel array: 608 × 384 (24.6 × 13.8 mm²)
Region of Interest function
Readout: External 12-bit ADC

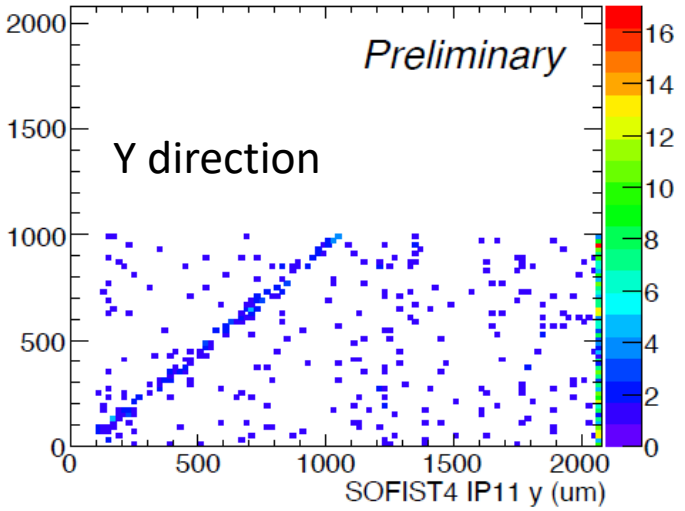


SOFIST4 : Preliminary Result

- Hit correlation is seen both x and y directions
  - Since the time resolution of reference is not good, many noise are seen.
- Analysis is on-going to obtain the time and position resolution

Reference





SOFIST

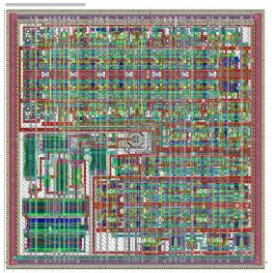
DuTiP

DuTiP for the Belle II

- Dual Timer Pixel concept (shown in next pages) based on FD-SOI CMOS technology by Lapis semiconductor
  - Binary detector
  - 45x45um^2 pixel size
  - 50um^t
  - Two 7bit timers to hold signals and wait for trigger
  - 15.9MHz clock (63ns) syncrnzed with SuperKEKB clock
- 7-layer Vertex detector replacing PXD+SVD

- This pixel detector can be used for layer7 and 8 of SIT at ILD, which requires <337ns time resolution for bunch ID, with minor modifications
  - Elongated pixel 30um x 180um?
  - 12bit timers?
  - Inter-train readout

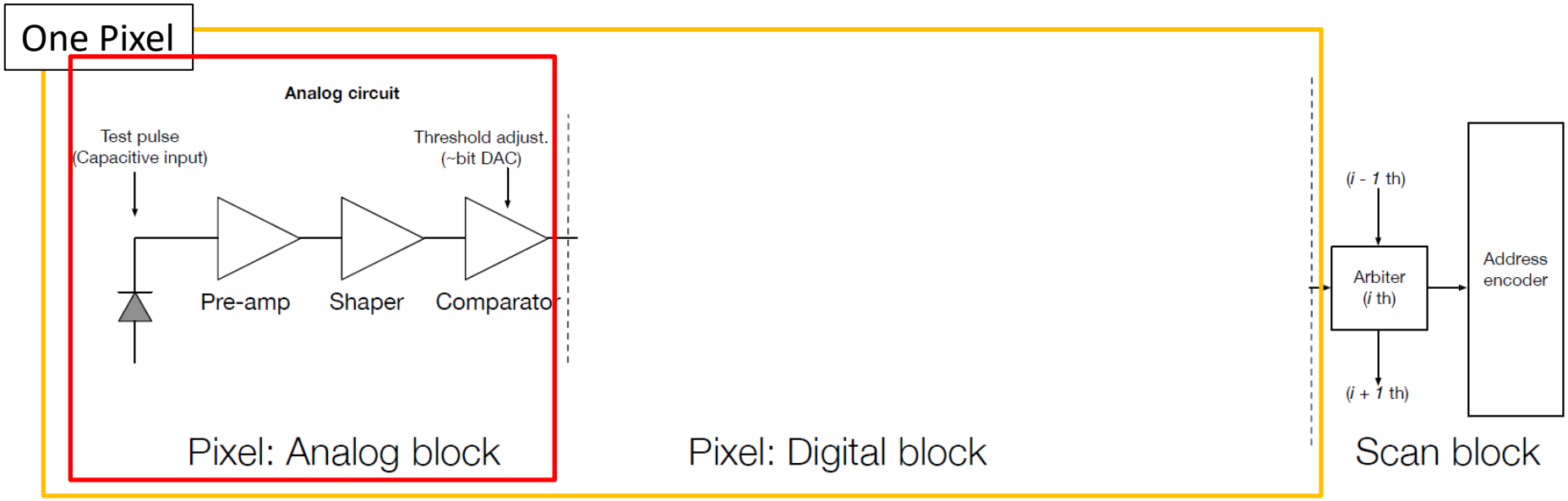
Pixel Layout



Layer	Radius [mm]	z Length [mm]
1	14	70
2	21	105
3	35	175
4	55	275
5	80	400
6	105	525
7	135	675

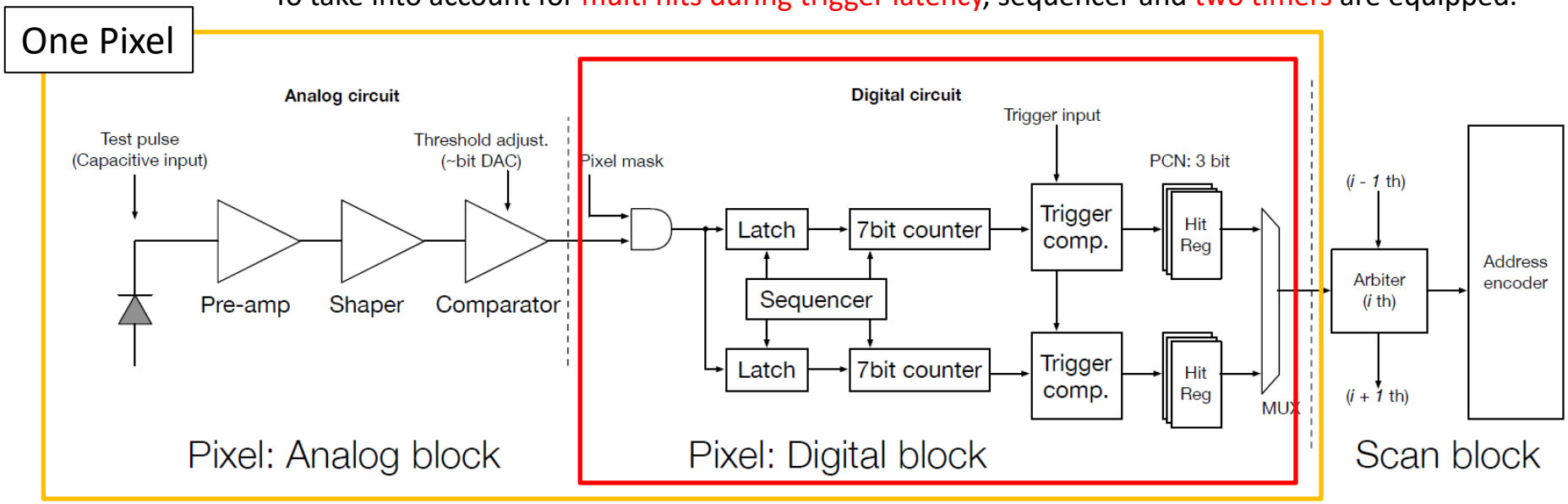
SOI for Belle II Upgrade DuTiP

- Analog Circuit
  - In Pixel Amplifier/Shaper/Discriminator.
  - Binary signal sent to digital circuit in the pixel.



The Concept “DuTiP”

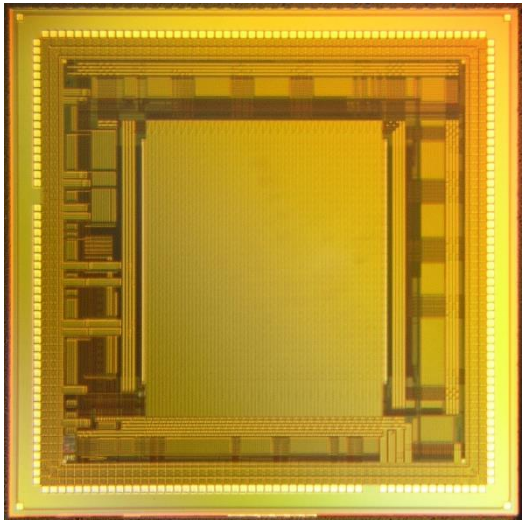
- Dual Timer Pixel
  - Dual Timer (down time counters) in a Pixel to store signal and wait for trigger signal
    - When hit signal is sent to digital circuit, one of the timers start counting down.
      - The starting time is set as trigger latency +1 CLOCK.
    - If the trigger signal is received when the timer is 1(2/0), the signal is readout as Current(Next/Previous) timing.
      - If trigger signal is not received → reset the timer.
    - Trigger latency is at most 2^n x clock period (n is a number of flipflops in timer).
    - To take into account for multi hits during trigger latency, sequencer and two timers are equipped.



Prototype1 : DuTiP1

- Designed for Belle II pixel detector
- Dimension
  - Size 6x6mm^2
  - Pixel size 45x45um^2
- Circuit fabricated
  - Modified ALPIDA-type analog circuit for FD-SOI
  - Basic in-pixel digital circuit of DuTiP concept
  - Many test circuits
- Circuit NOT fabricated
  - Sophisticated pixel scanning circuit
  - Fast data transfer circuit from the periphery to outside
    - LVDS/PLL are developed separately.
  - Issuing input signal to L1 track trigger system
- DuTiP1 Chip Delivered from Lapis
  - sub-board production just completed yesterday
  - Chip packaging on-going at REPIC
  - Firmware/software development started

DuTiP1



DuTiP1 sub-board

Characterization of DuTiP1

- Analog
  - Basics of modified ALPIDA-type analog circuit for FD-SOI
    - gain
    - Noise level
    - Threshold tuning
    - shaping time
- Digital
  - PIXOR digital circuit had worked perfectly with 50MHz so we think it should work
  - Test each elements
    - Sequencer for dual timer
    - Timer
    - Trigger time comparison
- If everything works fine, a beam test with thinned chip is performed at KEK PF electron beam line.
  - Efficiency
  - Position resolution

Prototype2 : DuTiP2

- Full functionality
  - Circuit NOT fabricated for DuTiP1 should be
    - Sophisticated pixel scanning circuit
    - Fast data transfer circuit from the periphery to outside
    - Issuing input signal to L1 track trigger system
      - Separate chip (outer layer)?
      - Single timer enough for outer layers
  - Full size chip just for row direction, ex. 17.2mm (row) x 9.0mm (column)
    - Full size chip 17.2mm (row) x 29.6mm (column)
    - Increasing the size to z direction is trivial

pitch [μm]	row $\times$ column [pixels]	array r-ϕ $\times$ z [mm^2]	array area [cm^2]	chip r-ϕ $\times$ z [mm^2]
45	320 $\times$ 640	14.4 $\times$ 28.8	4.15	17.2 $\times$ 29.6

- Submit the chip in the end of 2021
  - Dependent on MPW schedule

Summary

- Two SOI detectors are being developed.

- SOFIST
  - FNAL beam test study
  - Budget problem…

- DuTiP
  - First prototype for Belle II
    - Characterization started.
  - Second prototype in this JFY
  - To be modified for the SIT

backup

DuTiP

Expression of Interest for Belle II VXD Upgrade DuTiP Vertex Detector with an SOI Technology

Yasuo Arai,[4] Jérôme Baudot,[10] Andrzej Bozek,[9] Mingyi Dong,[5] Jing Dong,[5]
Yowichi Fujita,[4] Junji Haba,[4,1,11] Kazuhiko Hara,[14] Marek Idzik,[2] Akimasa Ishikawa,[4,1,7,*]
Maciej Kachel,[10] Piotr Kapusta,[9] Ikuo Kurachi,[4] Taohan Li,[11] Yunpeng Lu,[5]
Toshinobu Miyoshi,[4] Yoshiyuki Onuki,[12] Qun Ouyang,[5] Hwanbae Park,[8] Maria Rozanska,[9]
Junichi Suzuki,[4] Toru Tsuboyama,[4,1,†] Takehiro Takayanagi,[4] Gary Varner,[3]
Miho Yamada,[13] Masashi Yokoyama,[12,6] Hongyu Zhang,[5] and Yang Zhou[5]

List of Institutions in backup
Happy to add possible contributors

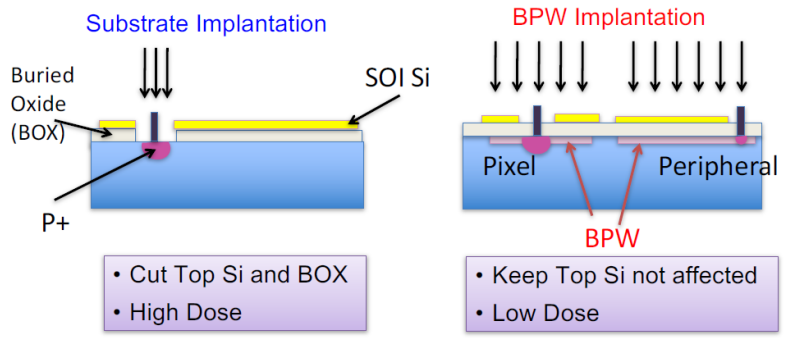
Lapis Semiconductor

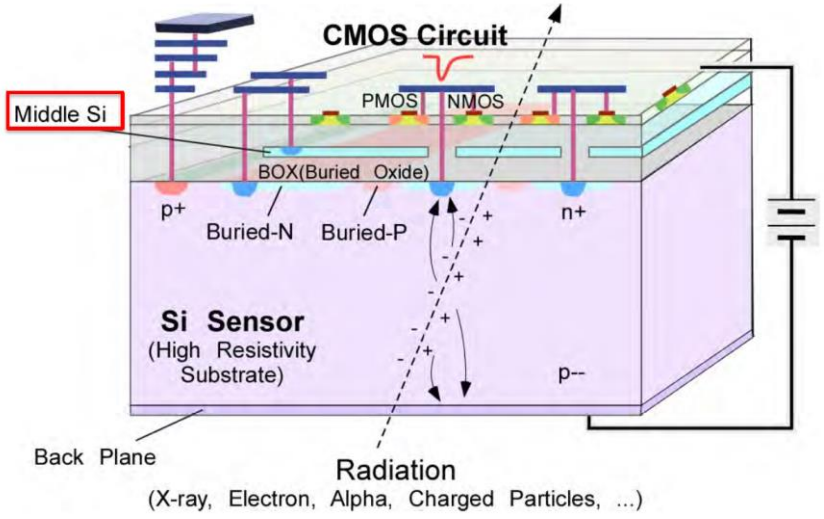
- 0.2um Low Leakage Fully Depleted SOI CMOS
- We have been collaborating with them since 2005.
  - 20km from Tohoku Univ to Miyagi factory
  - Many Pixel sensors are developed
    - SOPHIAS, XRPIX, PIXOR, CNTPIX, FPIX etc
    - SOPHIAS already used at RIKEN Sakura

Production line is fully controlled with Robots. Good for production of small quantity and also for HEP level mass production.

Two difficulties for SOI Solved

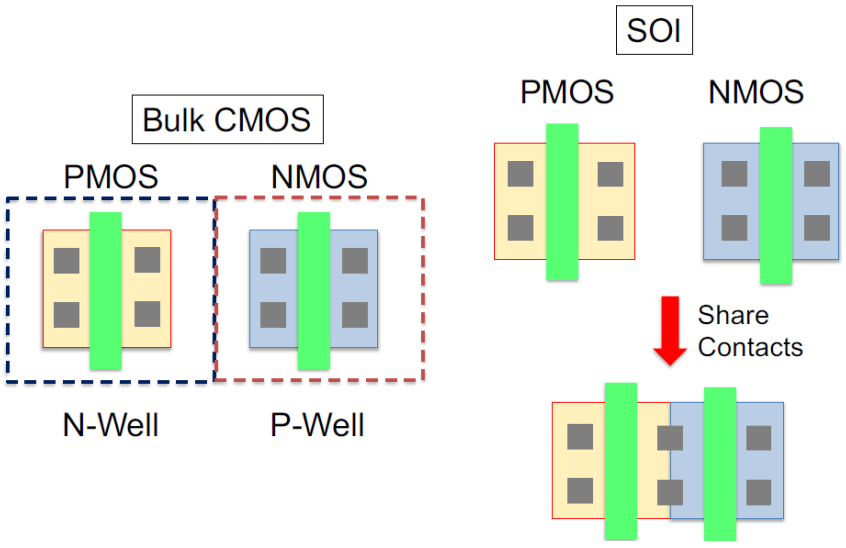
- Back-gate effect
  - Applied E-field affects the circuit
  - Suppressed by buried P well (BPW)
    - Additional well below the circuit.
- Radiation tolerance (hole trapped by BOX)
  - E-field by holes affects the circuit
  - compensated by Double SOI
    - Additional silicon layer in BOX layer applied LV.
  - Upto 20Mrad was tested with transistor TEG.

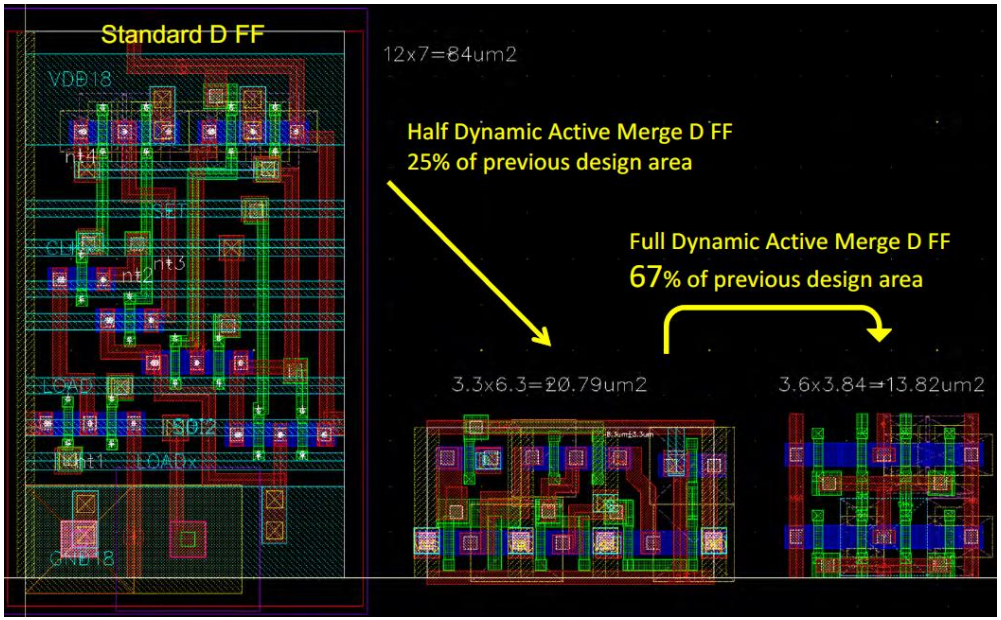




Active Merge Technique To Reduce Circuit Area

- PMOS and NMOS can be merged by sharing the active region
- Smaller layout than bulk CMOS is possible with the same process rule
  - Circuit area of D-type FF can be reduced to 17%





SOI for Belle II

- Originally considered to replace in 2028 (with previous plan) for upgraded SuperKEKB with L= $4x10^{36}$ but of course we can use it for upgrade in 2026 for $6x10^{35}$.

- Binary detector to reduce data size and power consumption.
- Fast clock to reduce the occupancy of $O(10^{-3})$ or less at upgraded SuperKEKB L=$4x10^{36}$
- Trigger based readout to reduce data size.
- Hold signals at least 4.4us trigger latency
- Small power consumption < $1W/cm^2$

- We invented the “DuTiP” concept for this purpose.

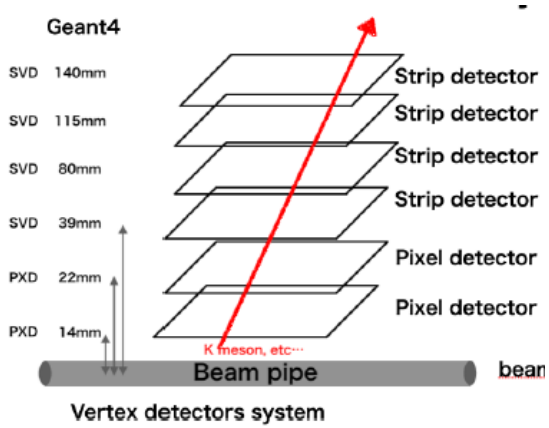
DuTiP with SOI technology

- 0.2um FDSOI process by Lapis semiconductor
- Pixel size
  - 45um → 45um/√12 ~ 13um resolution
  - But better than this → see next pages
- Thickness
  - 50um
- Amplifier/Shaper/Comparator
  - ALPIDE low power ASD (thanks to Strasbourg group!)
  - Noise ~ 86e^- (threshold is 1000e^- or so)
- Timer and digital circuit
  - 7bit x 2
  - 15.9MHz(63ns) CLK (SuperKEKB 509MHz /2^5(1.97ns*2^5))
    - DuTiP is synchronous to SuperKEKB
    - Trigger latency of at most 8us.
  - Digital Circuit is based on PIXOR which worked perfectly with 50MHz

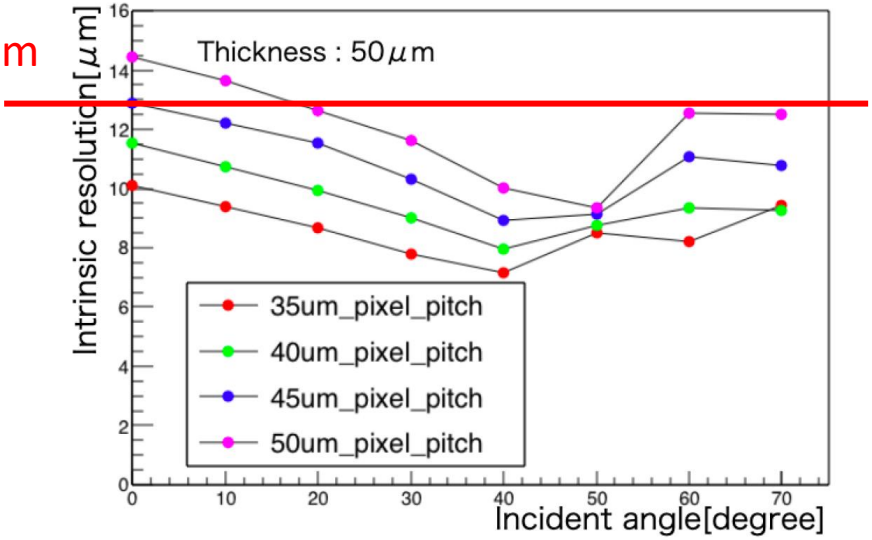
"Development of the Pixel OR SOI detector for high energy physics experiments",
Y. Ono, A. Ishikawa, H. Yamamoto, Y. Arai, T. Tsuboyama, Y. Onuki, A. Iwata, T. Imamura, T. Ohmoto,
NIM A 731, 266-269, 2013, doi:10.1016/j.nima.2013.06.044

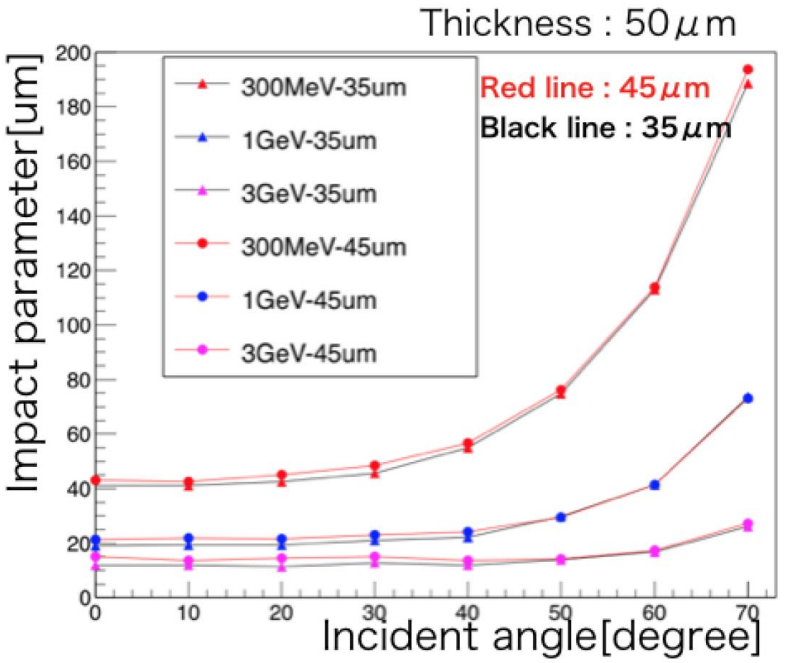
Position Resolution/IP resolution in Z

- We performed GEANT4 simulation to check the resolutions.
  - show position resolution results with 45um pixel pitch
- By taking CoG even with binary detector, the expected resolution in Z direction is better than pitch/√12=13um, In average, 11um or so.
- IP resolution in Z direction is dominated by multiple scattering with beam pipe for Belle II case.



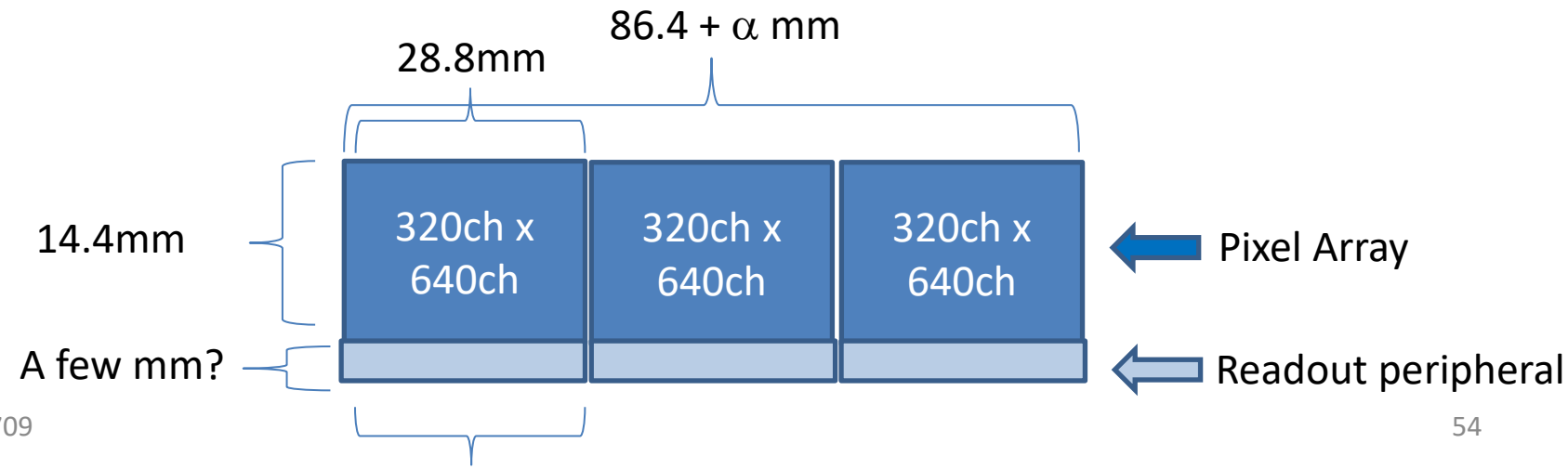
13um





Sensors for layer1

- Layer1 : R=1.4cm, Z=7cm
- maximum mask size for SOI is 2.46 x 3.08 cm^2
- We need three chip to cover the acceptance in Z.
  - Row : 45um x 320ch = 14.4mm
  - Column : 45um x 1920ch (640ch x 3) = 86.4mm (28.8mm x 3)
  - Thickness : $50um^t$
  - (Stitching buffer width: ~10um if we adopt stitching)
- 8 ladders to cover the acceptance in phi



Occupancy at Upgarded SuperKEKB L=4x10^{36}

- Assuming common initial requirements
  - 113MHz/cm^2 for layer1

https://indico.cern.ch/event/810687/attachments/1827433/3072784/BELLE2-NOTE-TE-2019-011.pdf

- Occupancies
  - Hit occupancy is for tracking
    - Hit in 3frames ; Previous, Current and Next
  - Dual Timer occupancy is computed when both timers are occupied.
    - Even 1 Timer is occupied, the detector can work.

	Time window	Occupancy
Hit	3*63ns	0.024%
Dual Timer	4.4us (trg latency)	0.010%
	8us (trg latency)	0.032%

Factor 3 for PCN timings

- Even under 5x larger luminosity, the occupancy is enough small.
  - We could use two times slower clock

Data Transfer Rate and Size

- Assuming 150kHz trigger rate at Upgraded Belle II L=4x10^{36}
- Row+column addresses (9bit+10bit) and PCN timing (2bit) are transferred from the chip
- Data transfer Rate

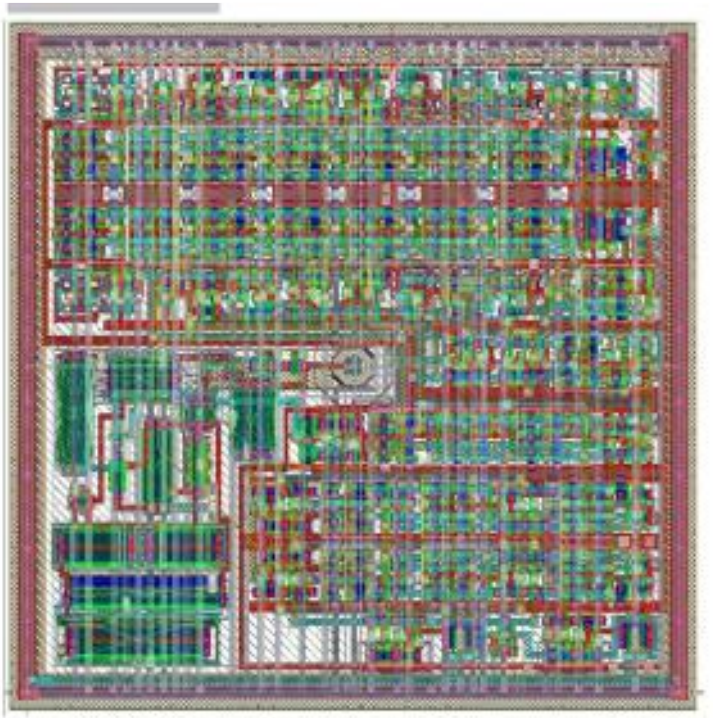
	Data transfer rate	Data size in 10^7s
Chip (360ch x 640ch)	277Mbps	
Ladder (3Chip)	833Mbps	
Layer1 (8Ladder)	6662Mbps	8.33PB

- Need fast data transfer technology fabricated on SOI
  - LVDS

DuTiP1 Submitted

- The chip
  - Chip size 6x6mm^2
  - Pixel size 45um
  - Pixel Array 64x64
  - Thickness 50um (to be thinned)
  - ALPIDE amplifier
  - Two counters in each pixel
- Miscellaneous functions
  - Test pulse input
  - Monitoring each analog circuit
- No sophisticated readout from pixel array to outside chip yet.
  - Next page for simulation
- We will receive the 1st prototype in Spring 2021.

Pixel Layout



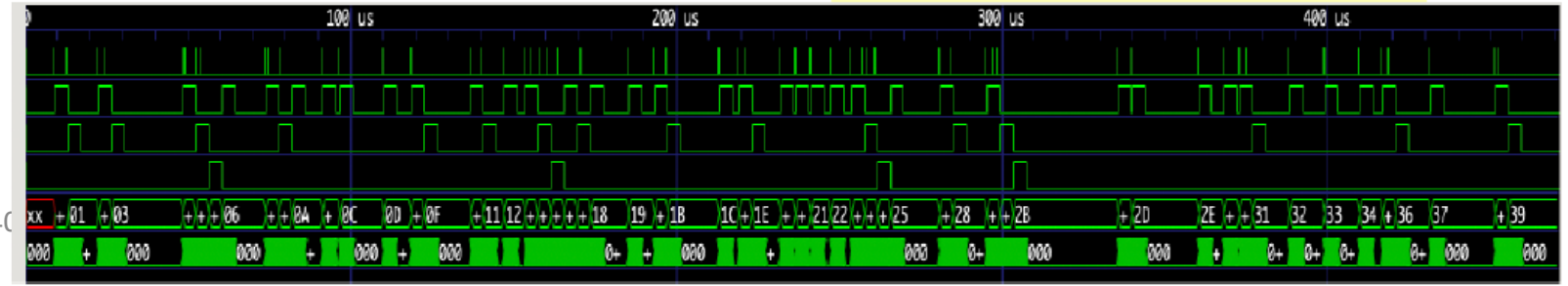
Data Transfer from Pixel Array to Periphery

- Study with Verilog simulation
  - Asynchronous readout
    - Assuming 64MHz clock
      - DuTiP clock is 15.9MHz (509MHz/32).
  - 3 hit memory on each pixel.
  - Assume many FIFO in periphery.
  - 400 pixels in a row (larger than current design 320 pixels)

Level-1 trigger rate (kHz)	Triggers generated	Triggers accepted	Efficiency (%)
30	292	292	100
100	1138	1130	99.3
200	2128	1987	93

- Assuming 113MHz/cm2 hit rate (L=4x10^{36}), busy rate at this stage is less than 1% with 100kHz L1 trigger input, and no busy is issued with 30kHz

Example with 100 KHz Trigger

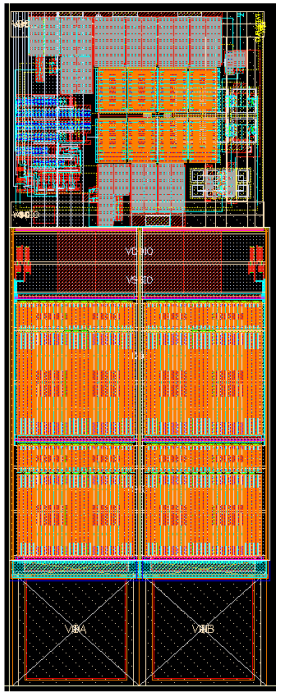


LVDS/PLL on SOI

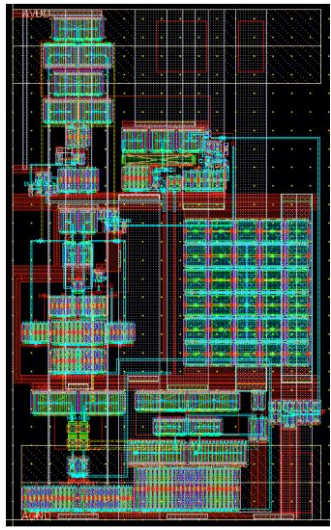
- Data transfer from the chip, LVDS should be used.
- We are developing 1.8V LVDS and PLL on SOI which should work with 600Mbps.
  - According to the designer, 800Mbps might be possible.
- We have submitted the LVDS driver and receiver together with DuTiP in this Dec.

- Only two LVDS lines (1.2Gbps) are needed to transfer data from single chip even for 4×10^{36} SuperKEKB.
  - Can reduce the number of cables.

LVDS driver



LVDS receiver



Power Consumption

- Power consumption for each item
  - Analog 0.36 uW/pixel → 0.018W/cm^2
  - Digital 0.60 uW/pixel → 0.030W/cm^2
  - LVDS 0.1W/channel
- Assuming 320x640 pixel array (14.4x28.8mm^2) and two LVDS channels
  - 0.4W/chip (in average ~0.1W/cm^2)

- Power density is large around LVDS
- Small in pixel array
  - 0.05W/cm^2