Next Generation LLRF Control Platform for Compact C-band Linear Accelerator

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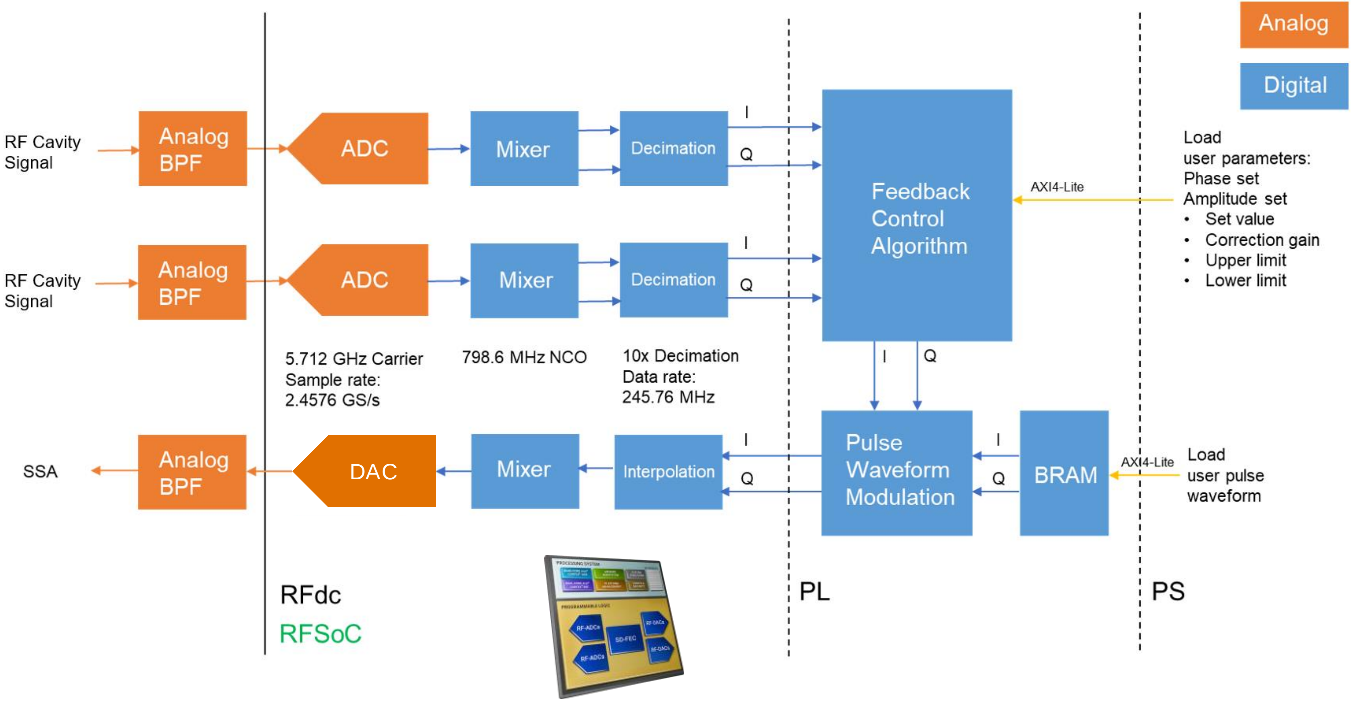
Agenda

- Introduction
    - System, hardware and software of NG-LLRF
    - Summary of previous work for RFSoC based LLRF
- High Power Test of NG-LLRF with C3 Accelerating Structure
    - Pulse-to-pulse fluctuation with SSA
    - Klystron output measurements
    - Accelerating structure rf measurements
- Conclusions and Future Works

Why new generation LLRF platform?

- LLRF systems for future particle accelerators become more critical because it could be a limiting factor with stringent **rf field stability specs** and the hardware **size, weight and power consumption (SWaP)** and **cost** requirements
- LLRF system design is challenging as multi-discipline knowledge required, such as RF/digital circuit, software, control algorithms, DSP and beam physics
- Rf system-on-chip (RFSoC) technology integrate all the essential components for a LLRF system - data converters, programmable logic, and processors
- RFSoC base LLRF significantly reduces hardware complexity and highly adaptable to different accelerators - simplifies the architecture of the system and enables more flexibility in operation

Next Generation LLRF (NG-LLRF) Control System



Analog

Digital

RF Cavity Signal → Analog BPF → ADC → Mixer → Decimation → I, Q → Feedback Control Algorithm

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5.712 GHz Carrier
Sample rate:
2.4576 GS/s

798.6 MHz NCO

10x Decimation
Data rate:
245.76 MHz

Feedback Control Algorithm → I, Q → Pulse Waveform Modulation

BRAM → I, Q → Pulse Waveform Modulation → I, Q → Interpolation → Mixer → DAC → Analog BPF → SSA

AXI4-Lite

Load
user parameters:
Phase set
Amplitude set
- Set value
- Correction gain
- Upper limit
- Lower limit

AXI4-Lite

Load
user pulse
waveform

RFdc

RFSoC

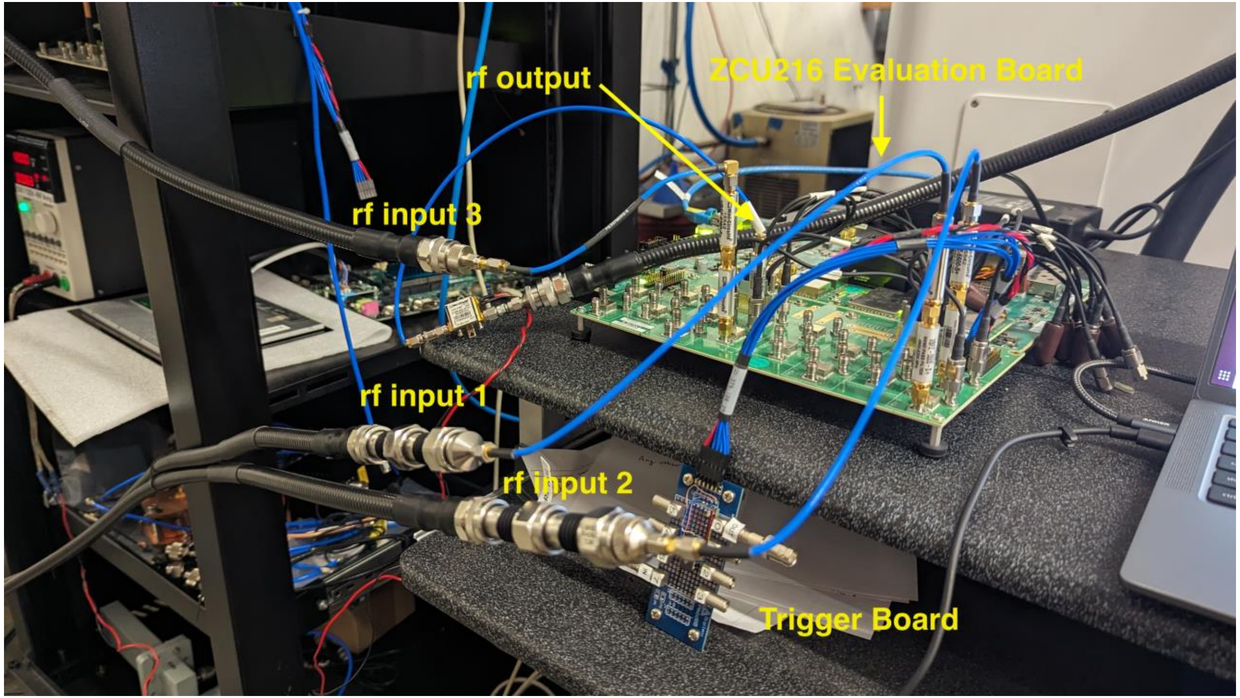
PL

PS

System Summary:

- Integrated data converters in RFSoC
- Direct RF sampling without analog mixing even in higher order Nyquist zone
- 16 ADCs and 16 DACs for a compact and cost-effective LLRF platform
- Maximum direct rf input frequency 6 GHz
- Designed based on the requirements of Cool Copper Collider (C3)

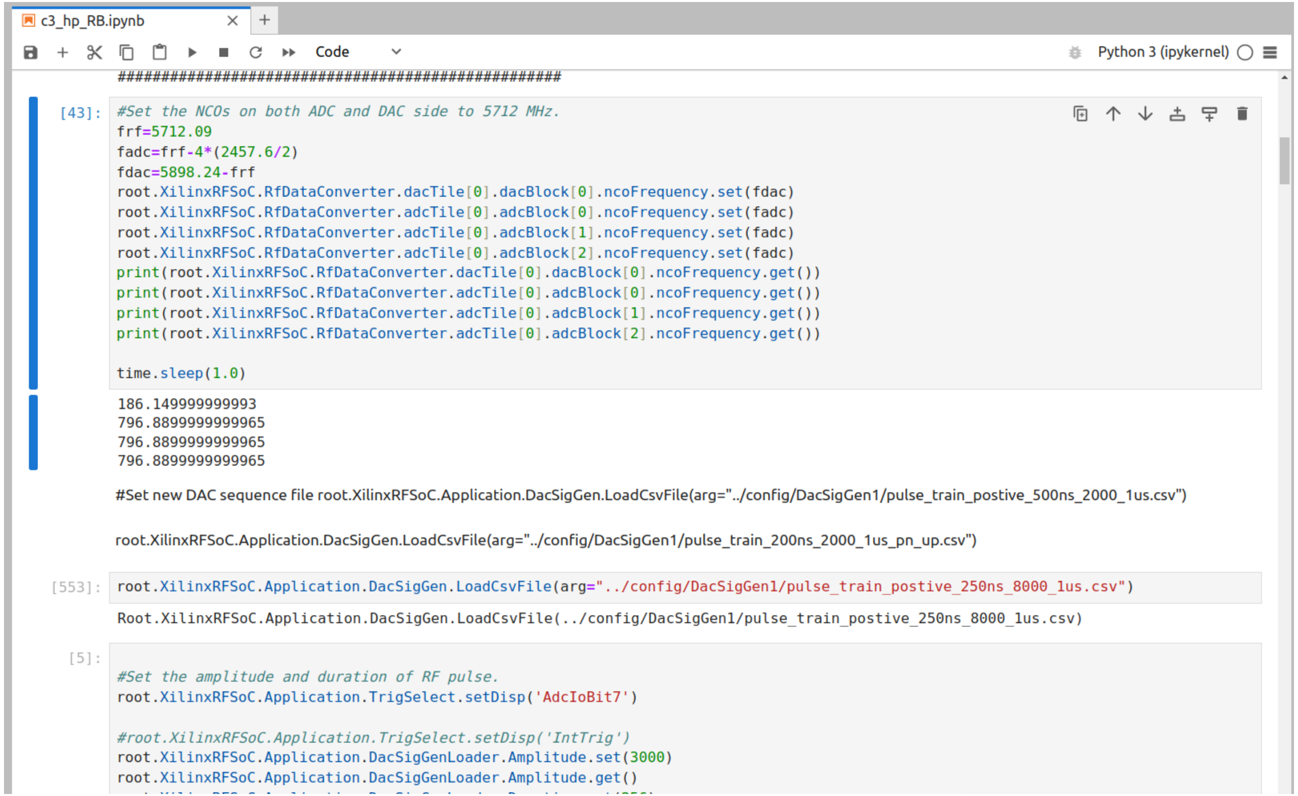
NG-LLRF Prototype Hardware



Technical Specs

- ZCU216 evaluation board
- 1 DAC (up to 16 channels) - generating rf pulse
- 3 ADCs (up to 16 channels) - digitize rf signals, perform down conversion, and capture baseband data
- 245.76 MHz of bandwidth centred around 5.712 GHz
- Tigger input or output

NG-LLRF Software



```
###################################################

[43]: #Set the NCOs on both ADC and DAC side to 5712 MHz.
frf=5712.09
fadc=frf-4*(2457.6/2)
fdac=5898.24-frf
root.XilinxRFSoC.RfDataConverter.dacTile[0].dacBlock[0].ncoFrequency.set(fdac)
root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[0].ncoFrequency.set(fadc)
root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[1].ncoFrequency.set(fadc)
root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[2].ncoFrequency.set(fadc)
print(root.XilinxRFSoC.RfDataConverter.dacTile[0].dacBlock[0].ncoFrequency.get())
print(root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[0].ncoFrequency.get())
print(root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[1].ncoFrequency.get())
print(root.XilinxRFSoC.RfDataConverter.adcTile[0].adcBlock[2].ncoFrequency.get())

time.sleep(1.0)

186.149999999993
796.8899999999965
796.8899999999965
796.8899999999965
```

#Set new DAC sequence file root.XilinxRFSoC.Application.DacSigGen.LoadCsvFile(arg="../config/DacSigGen1/pulse_train_postive_500ns_2000_1us.csv")

root.XilinxRFSoC.Application.DacSigGen.LoadCsvFile(arg="../config/DacSigGen1/pulse_train_200ns_2000_1us_pn_up.csv")

```
[553]: root.XilinxRFSoC.Application.DacSigGen.LoadCsvFile(arg="../config/DacSigGen1/pulse_train_postive_250ns_8000_1us.csv")

Root.XilinxRFSoC.Application.DacSigGen.LoadCsvFile(../config/DacSigGen1/pulse_train_postive_250ns_8000_1us.csv)

[5]:
#Set the amplitude and duration of RF pulse.
root.XilinxRFSoC.Application.TrigSelect.setDisp('AdcIoBit7')

#root.XilinxRFSoC.Application.TrigSelect.setDisp('IntTrig')
root.XilinxRFSoC.Application.DacSigGenLoader.Amplitude.set(3000)
root.XilinxRFSoC.Application.DacSigGenLoader.Amplitude.get()
```

Features

- Remote control and update
- Jupyter notebook for demonstration
- Data converter mixing frequency setup
- Baseband pulse setup
  - Duration
  - Amplitude
  - Delay
- Fast data capturing
- Real-time data visualization
- EPICS compatible

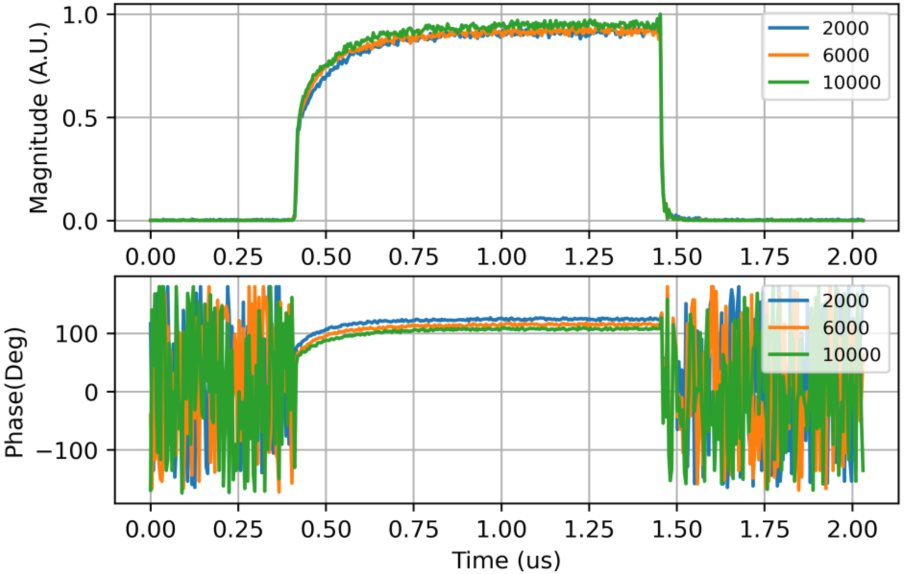
Rf Performance Evaluation and Measurement Overview

- Aim
  - LLRF system measures, regulates and stabilizes the rf field for beam acceleration
  - Prove the NG-LLRF platform can drive and measure with the desired precision
- Evaluation and measurement
  - LLRF and SSA loopback at lower power to characterize performance for the platform : magnitude and phase stability
  - High power test with C3 accelerating structure: resolve the features in rf signals at different stages – klystron forward, cavity forward and cavity reflection
- Outcomes
  - NG-LLRF system as customized characterization tool for accelerator parts
  - Based-on the rf signal measurements - control algorithm design proposal

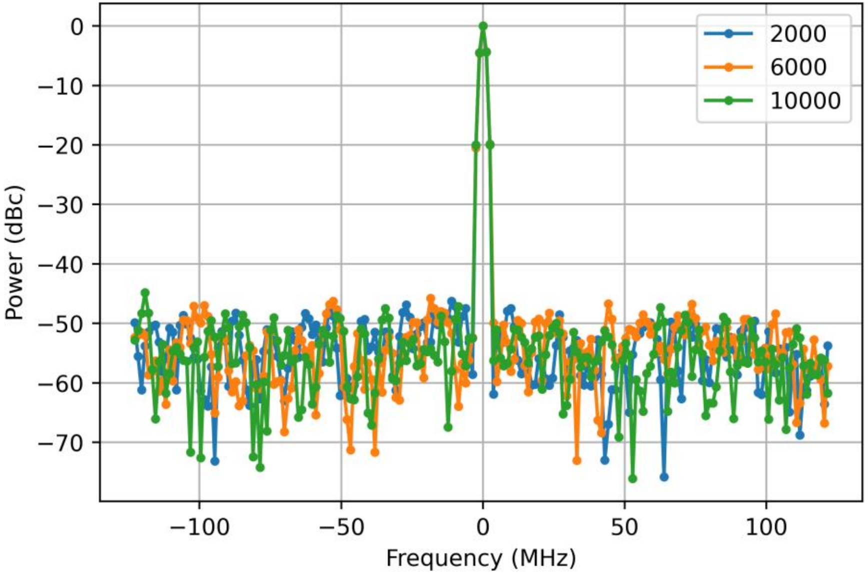
SSA-LLRF Loopack Output Signals

SSA integrated with klystron driven by an NG-LLRF DAC with rf pulse with 1 µs duration and amplitude from 2000 to 10000 (output: 3.2 to 60.8 W) and SSA output measured by NG-LLRF ADC. IQ samples converted to following:

Time domain: Rise time to flat top ~300ns and similar for all levels



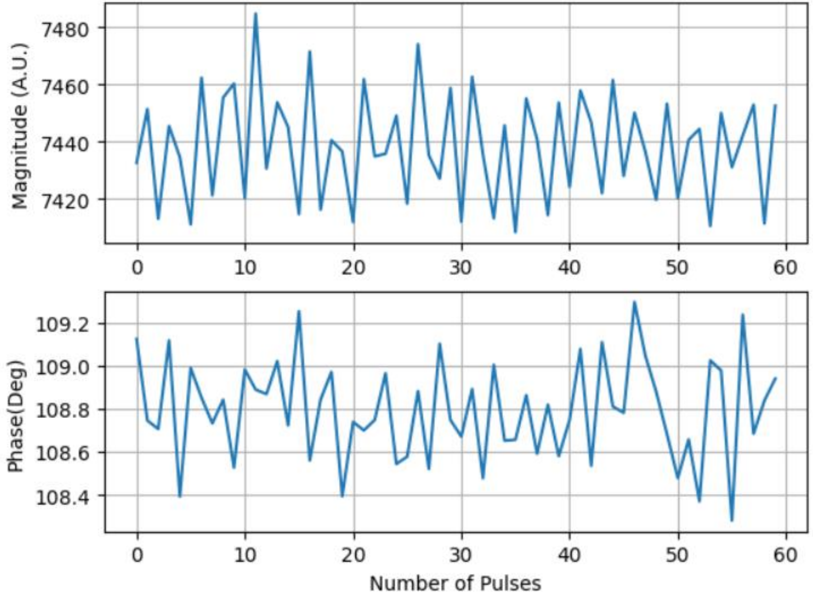
Frequency domain: Centre frequency at 5.71209 GHz and 245.76 MHz - **no spikes on both side bands**



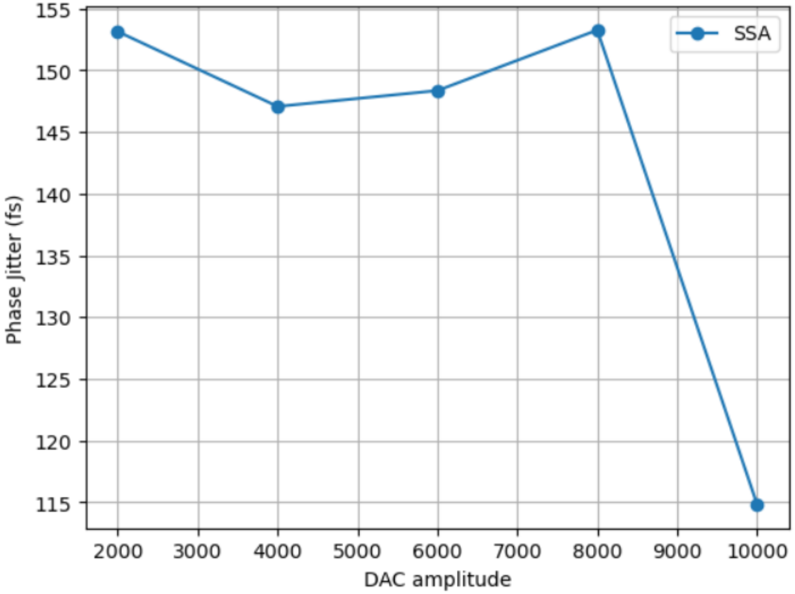
SSA Output Stability Analysis

SSA amplitude and phase stability measured with 60 consecutive rf pulses with duration of 1 μs at 60 Hz at power level from 3.2 to 60.8 W.

Average amplitude and phase on flat-top :
Pulse to pulse fluctuation **0.23% and 0.24°**

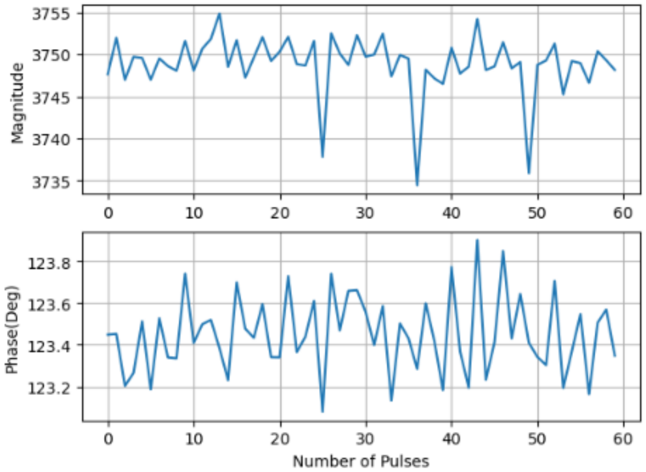


Phase jitter converted to time units at different power levels: lower jitter at higher power level



Pulse-to-pulse Fluctuation with SSA

Averaged phase and amplitude values for 60 pulses

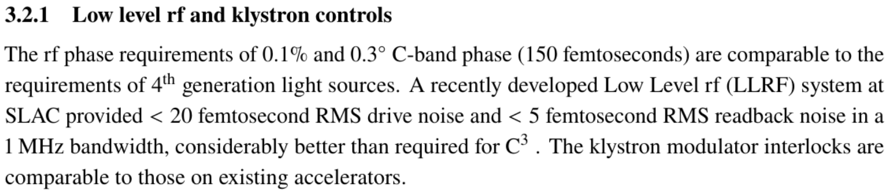


Pulse-to-pulse fluctuation for 60 pulses

- Magnitude
  - RMS (SD/Mean): 0.09%
- Phase
  - RMS (SD) : 0.18° (**87.54 femotoseconds**)

Test Summary

- 60 consecutive pulses captured in IQ format and the average phase and magnitude calculated for each pulses.
- RFSoC-based LLRF with the custom SSA delivers considerably lower phase jitter than required for Cool Cooper Collider (C^3).



3.2.1 Low level rf and klystron controls

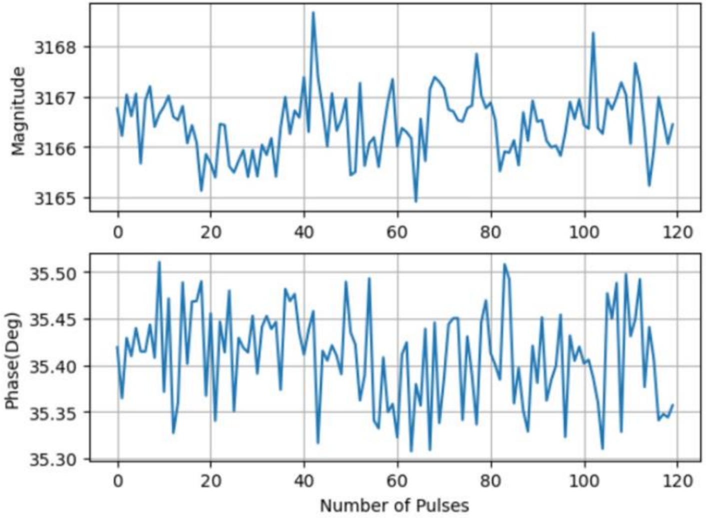
The rf phase requirements of 0.1% and 0.3° C-band phase (150 femtoseconds) are comparable to the requirements of 4th generation light sources. A recently developed Low Level rf (LLRF) system at SLAC provided < 20 femtosecond RMS drive noise and < 5 femtosecond RMS readback noise in a 1 MHz bandwidth, considerably better than required for C^3 . The klystron modulator interlocks are comparable to those on existing accelerators.

E. Nanni et al., "Status and future plans for C3 R&D", Journal of Instrumentation, vol. 18, no. 09, p. 09040, 2023. https://doi.org/10.1088/1748-0221/18/09/P09040

C. Liu et al., IPAC2024, https://arxiv.org/abs/2405.08219

RFSoC Performance Evaluation for S-band LINACs

Averaged phase and amplitude values for 120 pulses



Pulse-to-pulse fluctuation for 120 pulses

- Magnitude
  - RMS (SD/Mean): 0.02%
- Phase
  - RMS (SD) : 0.05° (**48.6 femotoseconds**)

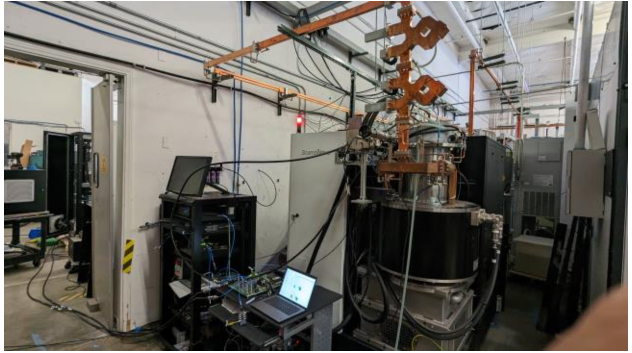
Test Setup and Summary

- RFSoC platform can also be applied to S-band LINACs at 2.856 GHz , such as LCLS
- ZCU208 with DAC and ADC sampling at 5.89824 GSPS and 4.9152 GSPS (more samples in each RF cycle)
- Loop-back with BPF centred at 2.856 GHz
- Pulse rate set to 120 Hz and pulse duration set to 3 µs
- Excellent pulse-to-pulse fluctuation performance
- The phase fluctuation can be improved by subtracting the digital common mode noise.
- RFSoC-based platform can used as new or upgrade paths for S-band LINACs' LLRF control system

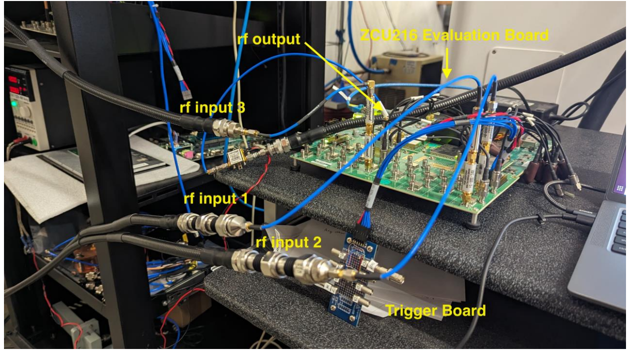
C. Liu et al., IPAC2024, https://arxiv.org/abs/2405.08219

High Power Test Setup with NG-LLRF and C3

RFSoC DAC drives the Klystron

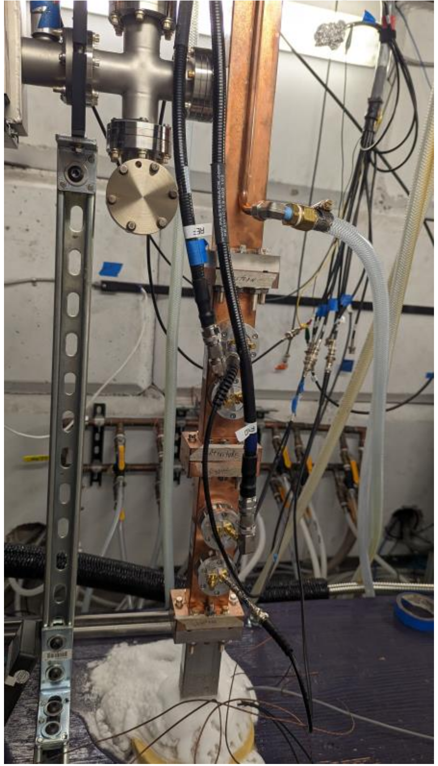


RF signals captured by RFSoC ADCs



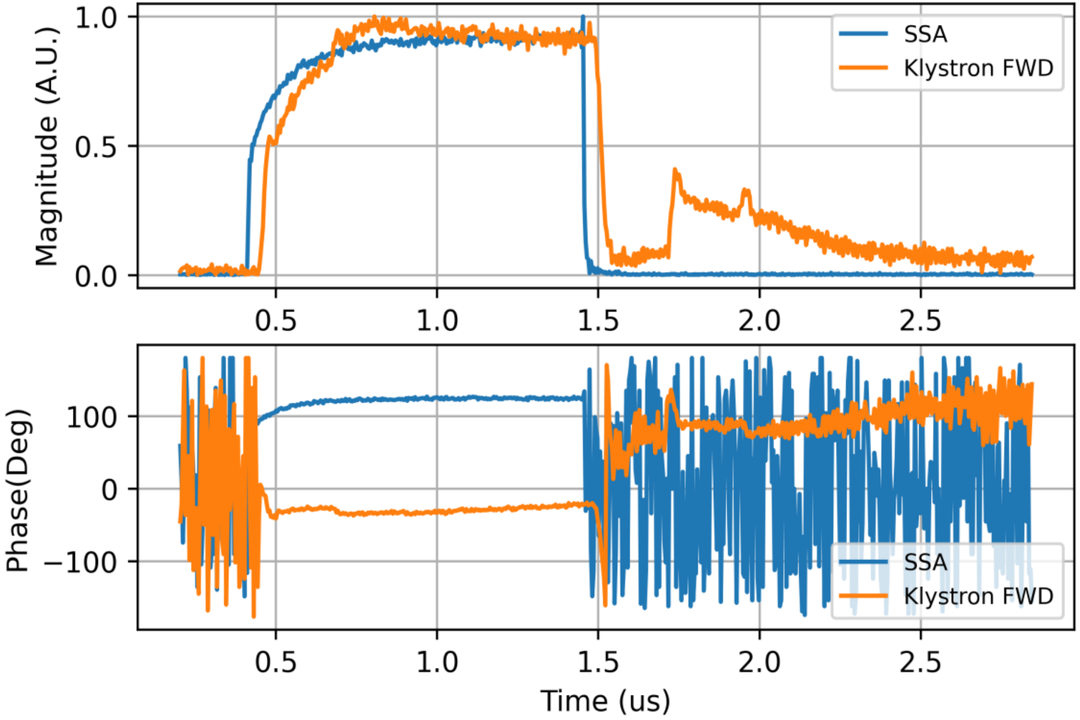
RF power injected to C3

FWD and REF via coupler



Klystron Forward Evaluation

SSA output and klystron forward measured with peak power of 4.6 MW

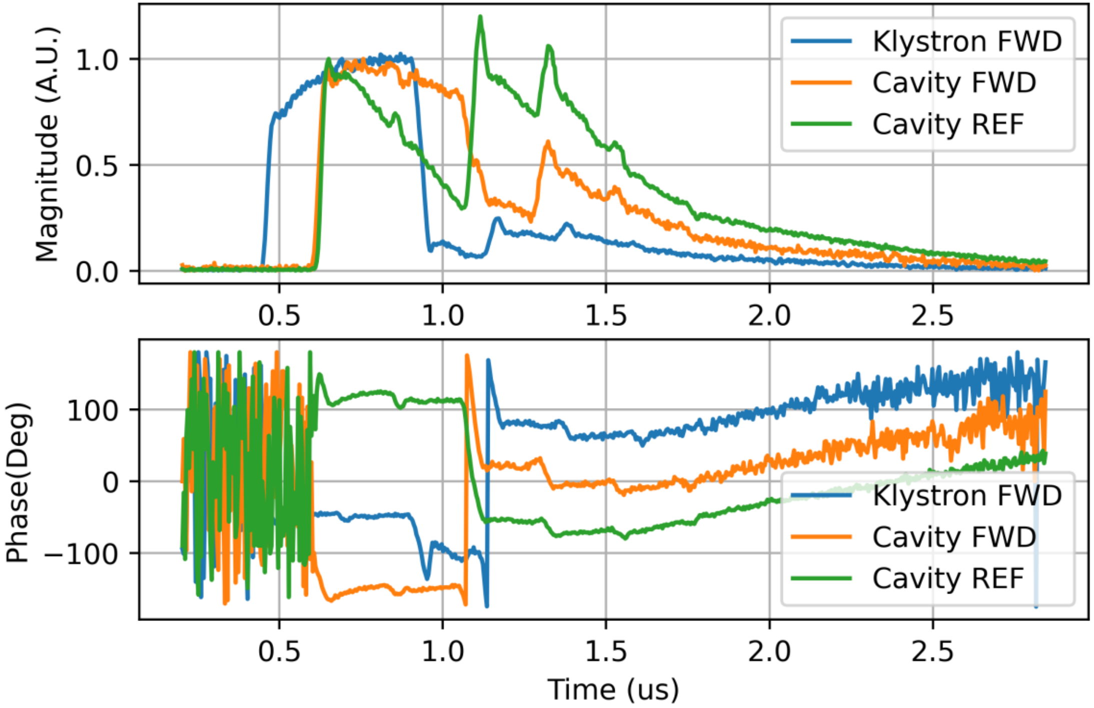


Summary and Analysis

- Measured with 1 μs rf pulse at 10 Hz and 4.6 MW peak power within the desire breakdown rate (100/hr)
- Klystron forward signal follows the SSA output with a minor delay
- Klystron supplies rf power to two lines and the power is divided by a power splitter and phase shifter (PSPS)
- PSPS reflect rf power back after rf is turned off and picked up by the klystron forward coupler – appeared as the second peak on the klystron forward

Accelerating Structure Measurement (16MW 450 ns)

Accelerating structure rf signals scaled to the first peak

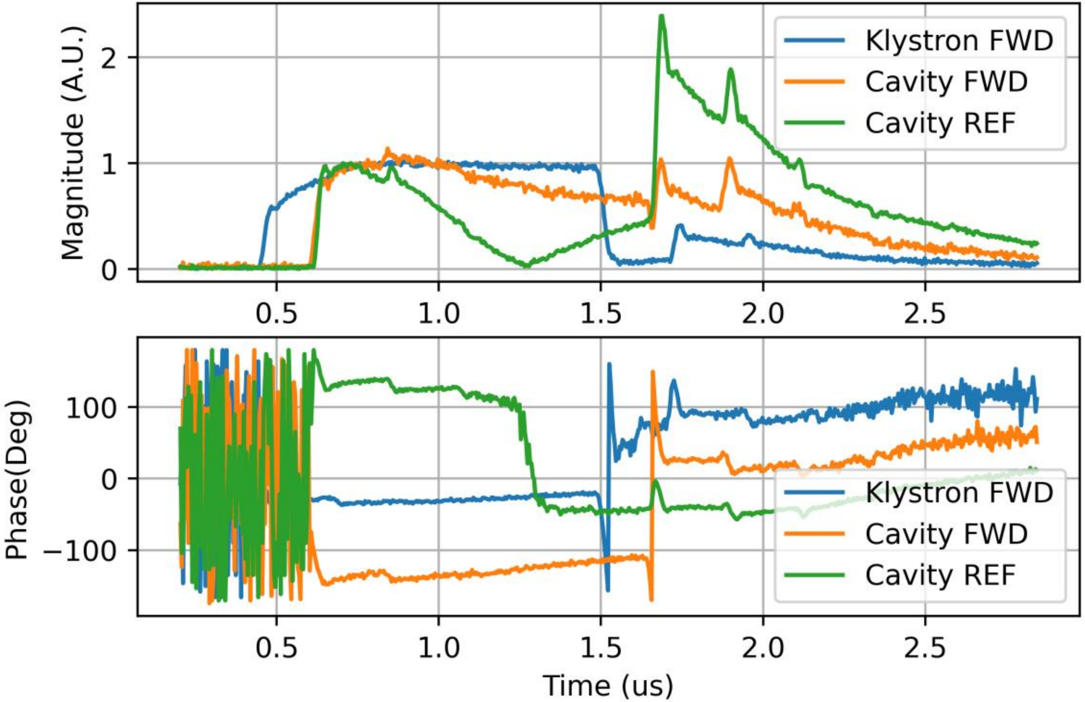


Summary and Analysis

- Measured with 450 ns rf pulse at 60 Hz at peak power of 16.45 MW within the desire breakdown rate
- Klystron forward signal turned off just after ramped up to flat top
- Cavity reflection ramp down linearly with steep slope as the field filling the structure - could not reach zero before rf is off (not fully filled)
- Rf power dissipation process picked up on cavity reflection as it ramps down
- PSPS reflected rf power picked up by both cavity forward and reflection

Accelerating Structure Measurements (5MW 1us)

Accelerating structure rf signals scaled to the first peak



Summary and Analysis

- Measured with 1 µs rf pulse at 10 Hz at peak power of 5.17 MW within the desire breakdown rate
- Cavity reflection ramped down to zero - field fully filled
- Excess power reflected with magnitude ramp up and phase flipped on REF
- The full rf field filling process can be monitored from the rf signals
- The NG-LLRF can resolve the features in the rf signals

Conclusion and Future Works

- NG-LLRF system with SSA delivered a phase jitter considerably better than the requirement of C^3.
- The rf performance of RFSoC based platforms is adequate for a range of S and C band LINACs.
- The high integration level of NG-LLRF offers a significantly more compactly and cost-effectively LLRF control platform solution for future accelerators.
- Comprehensive understandings on accelerating structure rf signals from high power tests - those are the real signals will be used for feedback control.
- Customized and adaptive RFSoC-based modular electronics under development.
- Full real-time feedback control firmware algorithm for C^3 under development.
- NG-LLRF not limited to control
  - Beam diagnostic: higher order mode (HOM) measurements for bunch displacement monitoring at first cyro module LCLS II injector, customized test or measurement facility
  - Beyond Linac applications, such as readout for CMB telescope, quantum sensors and axion dark matter search experiments
  - Open source and open to collaboration - contact me if you are interested in developing or using NG-LLRF.

Acknowledgements

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