



Contribution ID: 93

Type: **Oral presentation (in person)**

Next Generation LLRF Control Platform for Compact C band Linear Accelerator

Wednesday 10 July 2024 12:00 (20 minutes)

The Low-Level RF (LLRF) control circuits of linear accelerators (LINACs) are conventionally realized with heterodyne based architectures, which have analog RF mixers for up and down conversion with discrete data converters. We have developed a new LLRF platform for C band linear accelerator based on the Frequency System-on-Chip (RFSoc) device from AMD Xilinx. The integrated data converters in RFSoc can directly sample the RF signals in C band and perform the up and down mixing digitally. The programmable logic and processors required for signal processing for LLRF control system are also included in a single RFSoc chip. With all the essential components integrated in a device, the RFSoc-based LLRF control platform can be implemented more cost-effectively and compactly, which can be applied to a broad range of accelerator applications. In this paper, the structure and configuration of the newly developed LLRF platform will be described. We have performed a detailed performance evaluation based on the requirements of C band linear accelerators and part of the characterization results will be presented and discussed.

Apply for poster award

Primary author: LIU, Chao (SLAC National Accelerator Laboratory)

Co-authors: NANNI, Emilio (SLAC National Accelerator Laboratory); RUCKMAN, Larry (SLAC National Accelerator Laboratory); HERBST, Ryan (User)

Presenter: LIU, Chao (SLAC National Accelerator Laboratory)

Session Classification: Normal conducting RF

Track Classification: Accelerator: Normal Conducting RF