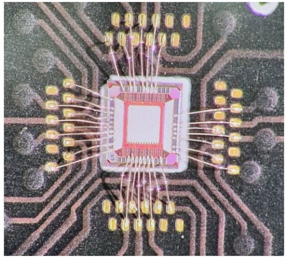
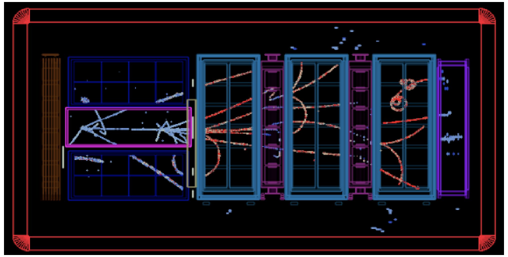
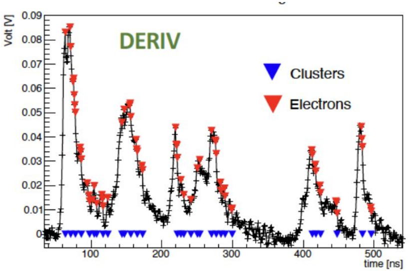
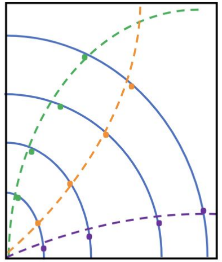








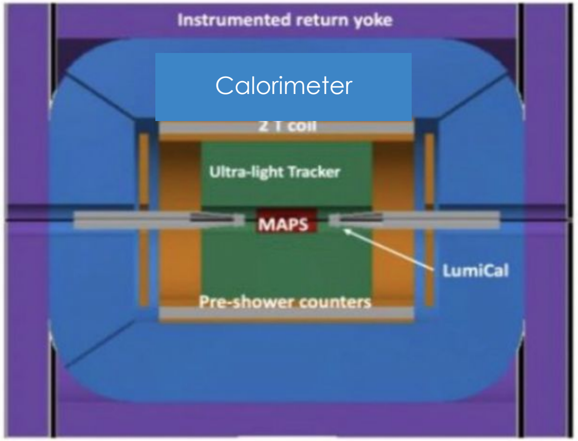
Tracking Vertexing and Timing Detectors Summary

Ziad El Bitar (CNRS)
Nicola De Filippis (Politecnico and INFN Bari)
Shinya Narita (Iwate University)
Ariel Schwartzman (SLAC)
Caterina Vernieri (SLAC)

LCWS2024 International Workshop on Future Linear Colliders

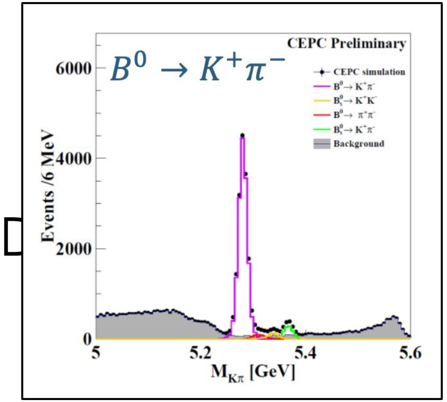
11-July-2024

Outline

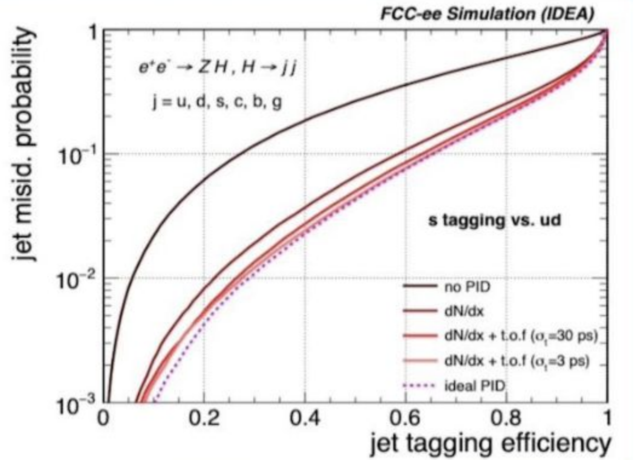


- **Vertex detector** (MAPS)
- **Tracker**
  - Dual Timer Pixel (Belle)
  - TPC
  - Drift Chamber
  - CLD silicon
- **Timing layers**
- **Particle ID**
  - dE/dX / dN/dx
  - impact of RICH in CLD silicon tracking performance

flavor physics



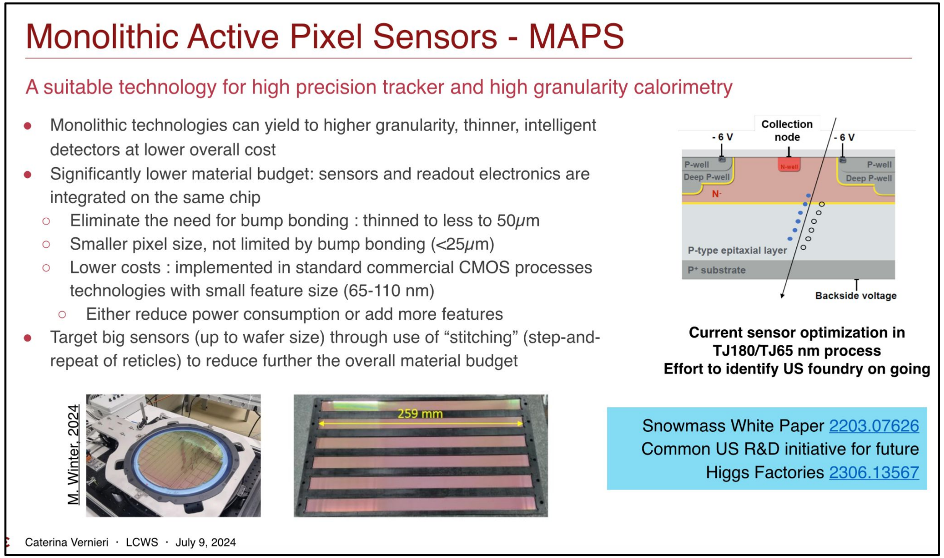
strange-tagging



https://agenda.linearcollider.org/event/10134/sessions/5593/#all

MAPS for tracking and calorimetry

Caterina Vernieri



Monolithic Active Pixel Sensors - MAPS

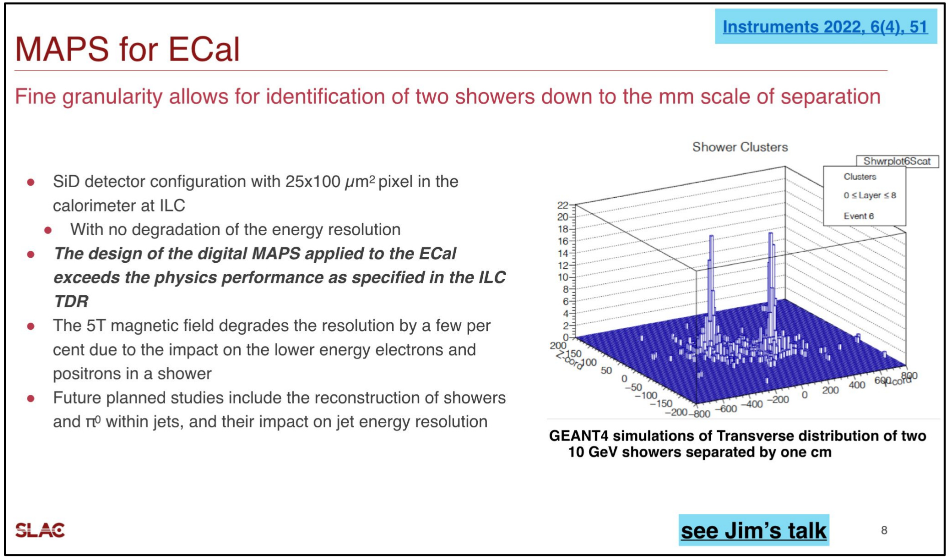
A suitable technology for high precision tracker and high granularity calorimetry

- Monolithic technologies can yield to higher granularity, thinner, intelligent detectors at lower overall cost
- Significantly lower material budget: sensors and readout electronics are integrated on the same chip
  - Eliminate the need for bump bonding : thinned to less to 50μm
  - Smaller pixel size, not limited by bump bonding (<25μm)
  - Lower costs : implemented in standard commercial CMOS processes technologies with small feature size (65-110 nm)
    - Either reduce power consumption or add more features
- Target big sensors (up to wafer size) through use of "stitching" (step-and-repeat of reticles) to reduce further the overall material budget

Current sensor optimization in TJ180/TJ65 nm process
Effort to identify US foundry on going

Snowmass White Paper 2203.07626
Common US R&D initiative for future Higgs Factories 2306.13567

Caterina Vernieri · LCWS · July 9, 2024



Instruments 2022, 6(4), 51

MAPS for ECal

Fine granularity allows for identification of two showers down to the mm scale of separation

- SiD detector configuration with 25x100 μm^2 pixel in the calorimeter at ILC
  - With no degradation of the energy resolution
- ***The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR***
- The 5T magnetic field degrades the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower
- Future planned studies include the reconstruction of showers and π^0 within jets, and their impact on jet energy resolution

GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

SLAC

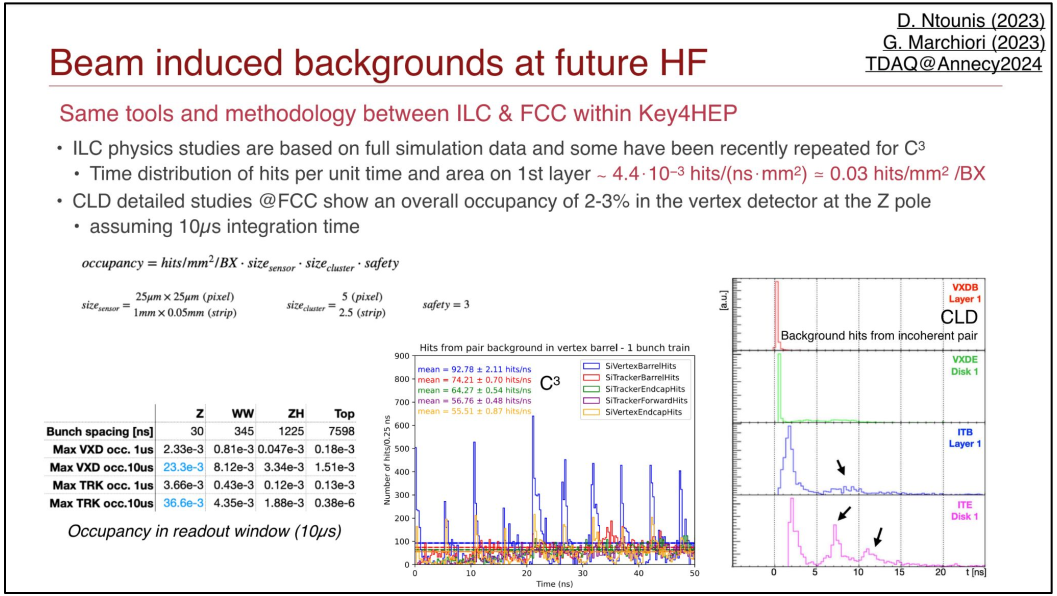
see Jim's talk

8

- 65nm CMOS imaging process
  - increased density for circuits: higher spatial resolution and improved timing at same power consumption
  - supports stitching → Wafer scale MAPS

MAPS for tracking and calorimetry

- **Focus on achieving nanosecond timing resolution at low power consumption**:
  - Suppression of beam backgrounds to keep occupancy low and/or trigger decision before reading out the detector



D. Ntounis (2023)
G. Marchiori (2023)
TDAQ@Annecy2024

Beam induced backgrounds at future HF

Same tools and methodology between ILC & FCC within Key4HEP

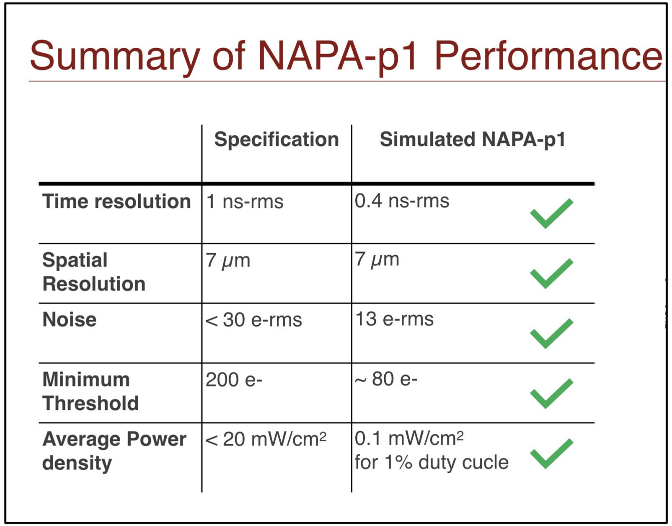
- ILC physics studies are based on full simulation data and some have been recently repeated for C^3
  - Time distribution of hits per unit time and area on 1st layer ~ $4.4 \cdot 10^{-3}$ hits/(ns·mm^2) ≃ 0.03 hits/mm^2 /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole
  - assuming 10μs integration time

$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m \ (pixel)}{1mm \times 0.05mm \ (strip)} \qquad size_{cluster} = \frac{5 \ (pixel)}{2.5 \ (strip)} \qquad safety = 3$$

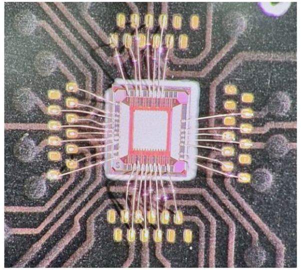
	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

Occupancy in readout window (10μs)



Summary of NAPA-p1 Performance

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 μm	7 μm ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓



Napa-p1

Belle II

SOIPIX
Silicon-On-Insulator Pixel Detector Project

LCWS2024 International Workshop on Future Linear Colliders

DuTiP : Vertex Detector for Belle II Upgrade and Intermediate Silicon Tracker for ILC

Yasuo Arai, Tristan Fillinger, Junji Haba, **Akimasa Ishikawa**,
Ikuo Kurachi[B], Kenkichi Miyabayashi[D], Miki Mitani[C], Emi Ozaki[D],
Takehiro Takayanagi, Ayaki Takeda[C], Hina Tagashira[D],
Toru Tsuboyama, Miho Yamada[E]

KEK, D&S[B], Miyazaki University[C], Nara Women's University[B], TMCIT[E]

KEK

Tokyo Metropolitan College of Industrial Technology

DuTiP and SOI

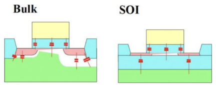
- We invented Dual Timer Pixel (DuTiP) concept for Belle II Vertex detector upgrade that can be also used for layer 7 and 8 of ILD SIT.

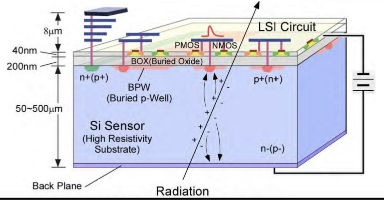
- Our requirements for Belle II Vertex detector
  - Binary detector to reduce data size and power consumption.
  - Relatively fast clock of > 10MHz to reduce the occupancy to O(10^{-4}) or less
  - Global shutter readout based on L1 Trigger to reduce data size.
  - Hold signals at least trigger latency of 4.4us
  - Low power consumption ~100W/cm^2
    - For normal temperature air cooling

- We adopted Silicon on Insulator (SOI) technology to realize the DuTiP

Silicon-on-Insulator (SOI)

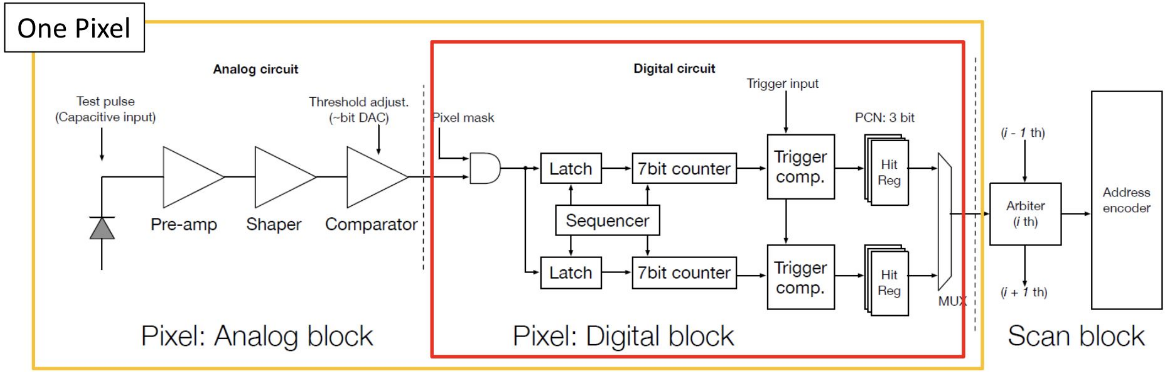
- Insulator layer (BOX layer) sandwiched by circuit and sensor layer
  - Complicated circuit can be fabricated on circuit layer w/o bump bonding
- Fully depleted sensor : Fast signal, good S/N
- CMOS logics w/o well structure : High density, small parasitic capacitance
- Monolithic : Low material budget
- Good for high energy physics
- We adopt Lapis semiconductor 0.2um FD-SOI process



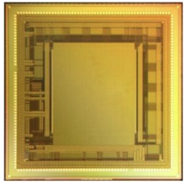


The Concept "DuTiP"

- Dual Timer Pixel
  - Dual Timer (down time counters) in a Pixel to store signal and wait for trigger signal
  - 7bit timer can wait trigger upto 127 x CLK.
  - Two timers allow the second hit during trigger latency
  - Hit registers for three time buckets, previous, current and next for timing scan

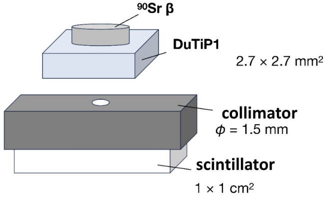


DuTiP1 with SOI technology



- Dimension
  - 6mm^2 chip
  - Pixel Size 45um x 45um
    - 45um/√12=13um
    - charge sharing improves the resolution
  - 64x64 pixel array
  - 300um^t (to be thinned to ~50um^t)
- Analog circuit
  - ALPIDE analog circuit fabricated on SOI by Strasbourg and modified by KEK.
  - Low power consumption amplifier
- Digital Circuit
  - 7bit timer x 2
  - 15.9MHz(62.9ns) CLK (SuperKEKB 509MHz/32(1.97ns*32))
    - Trigger latency of at most 8us (4.4us requirement)
  - Only current and previous time buckets (no next bucket)
  - No sophisticated readout circuit not fabricated

Efficiency and Yield



- Efficiency
  - Using ^{90}Sr : ~98+-2%
  - Cosmic or accidental noise hit are subtracted with dry run data.
  - Large systematic uncertainty due to limited setup
  - To be tested with test beam
- Production yield is checked without collimator
  - More than 99% pixel is working

^{90}Sr irradiation

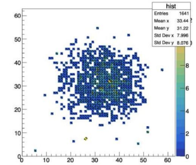
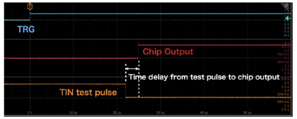
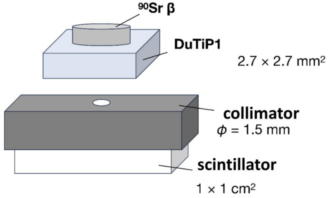


fig. The histogram image of the beta ray. Triggered by the electrons restricted by the collimator.

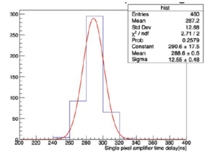
Timing Resolution for single pixel

- DuTiP + Scintillation counter
- Tested with ^{90}Sr and 50MHz CLK (20ns)
  - Timing resolution is 11.2ns
    - With test pulse ~10ns
  - Enough smaller than time bucket of 63ns





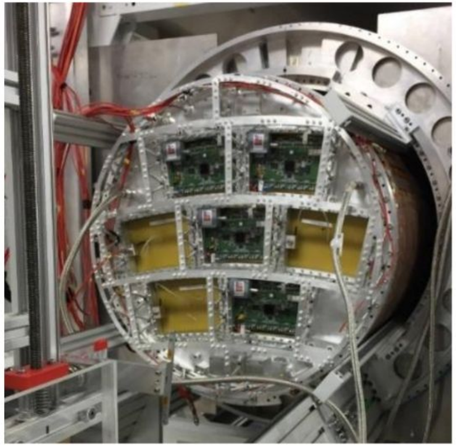
12.6ns including binning effect



New TPCs with charge spreading resistive Micromegas for T2K near detector

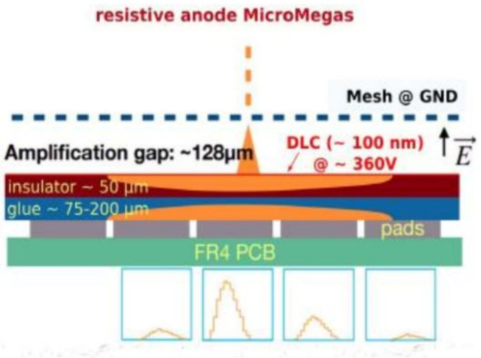
JENNIFER2
EU grant n.822070

Paul Colas, U. Paris Saclay



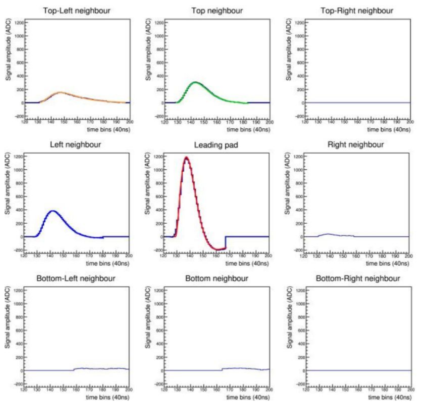
From ILC TPC R&D to a real neutrino experiment in Japan

Charge spreading



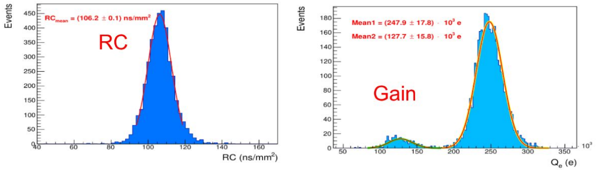
By adding a resistive layer and a dielectric layer on top of the anode, we obtain a **resistive-capacitive** continuous network that spreads evenly the charge between the hit pad and its neighbours.

This allows a barycentre to be determined, which greatly improves the resolution : resolutions as good as 1/50 times the pad size are obtained.



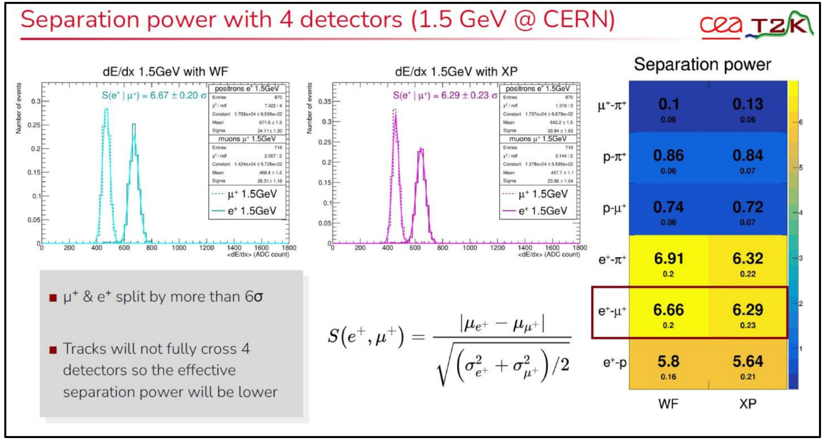
For a given pad, for each deposit fit simultaneously the Waveforms of the leading pads

Extract RC, Gain and deposit position/time



Nucl.Instrum.Meth.A 1056 (2023) 168534

S. Joshi
J.-F. Laporte, S. Hassani



Separation power with 4 detectors (1.5 GeV @ CERN)

- μ$^+$ & e$^+$ split by more than 6σ
- Tracks will not fully cross 4 detectors so the effective separation power will be lower

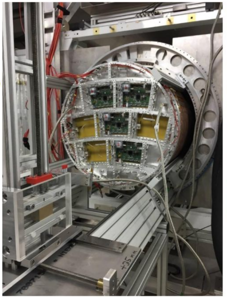
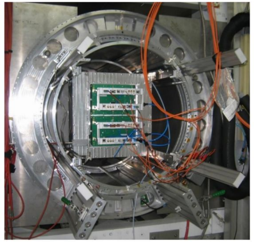
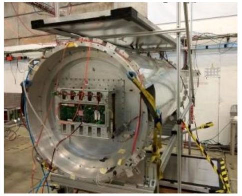
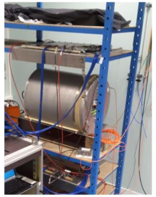
$$S(e^+,\mu^+) = \frac{|\mu_{e^+} - \mu_{\mu^+}|}{\sqrt{\left(\sigma^2_{e^+} + \sigma^2_{\mu^+}\right)/2}}$$

Separation power

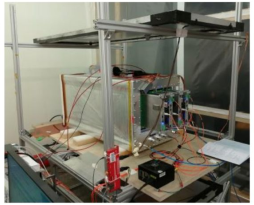
	WF	XP
μ$^+$-π$^+$	0.1 0.06	0.13 0.06
p-π$^+$	0.86 0.06	0.84 0.07
p-μ$^+$	0.74 0.06	0.72 0.07
e$^+$-π$^+$	6.91 0.2	6.32 0.22
e$^+$-μ$^+$	6.66 0.2	6.29 0.23
e$^+$-p	5.8 0.16	5.64 0.21

Many tests in recent years

Beam test at DESY in 2015 (LCTPC, 2 DLC modules)
Cosmic-ray test at Saclay in 2017 (T2K)
Beam test at CERN in August 2018 (T2K)
Beam test at DESY in November 2018 (LCTPC)
Cosmic-ray test in Saclay since January 2019 (LCTPC/FCC)
Beam test at DESY in June 2019 and 2021 (T2K)
Cosmic test at CERN since December 2019 (T2K)
Cosmic tests in Saclay during the covid year (T2K) (4-6 modules)

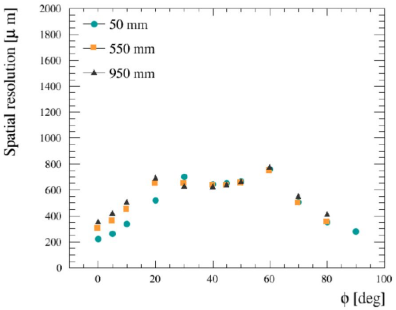





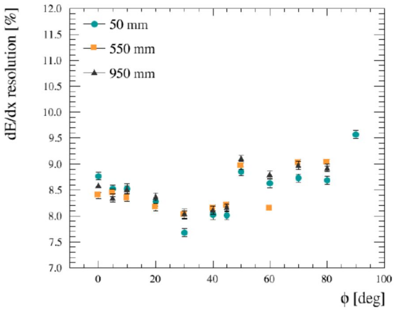
5 TPC of 15, 58, 60, 100 and 150 cm length with 1000 to 2000 channels
All with DLC charge spreading



Overal conclusion : extremely reliable and stable operation

Performance (beam test at DESY in 2021)

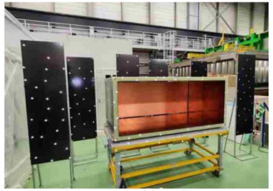
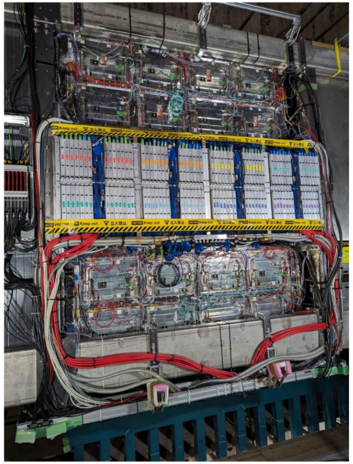




Installation at JPARC

32 (+spares) ERAM modules built at CERN (Rui de Oliveira) and characterized/tested at CERN
Field cages built in industry in Spain under supervision by T. Lux, G. Collazuol et al.).

TPCs assembled at CERN (gluing stripped kapton and soldering resistor chains) and transported by plane to JPARC.
Then re-tested on surface and lowered in the T2K pit (T. Lux).
100% operationnal. Excellent gas (system by R. Guida built at CERN and commissioned by E. Radionici) : 2 ppm O_2 and 5 ppm H_2O

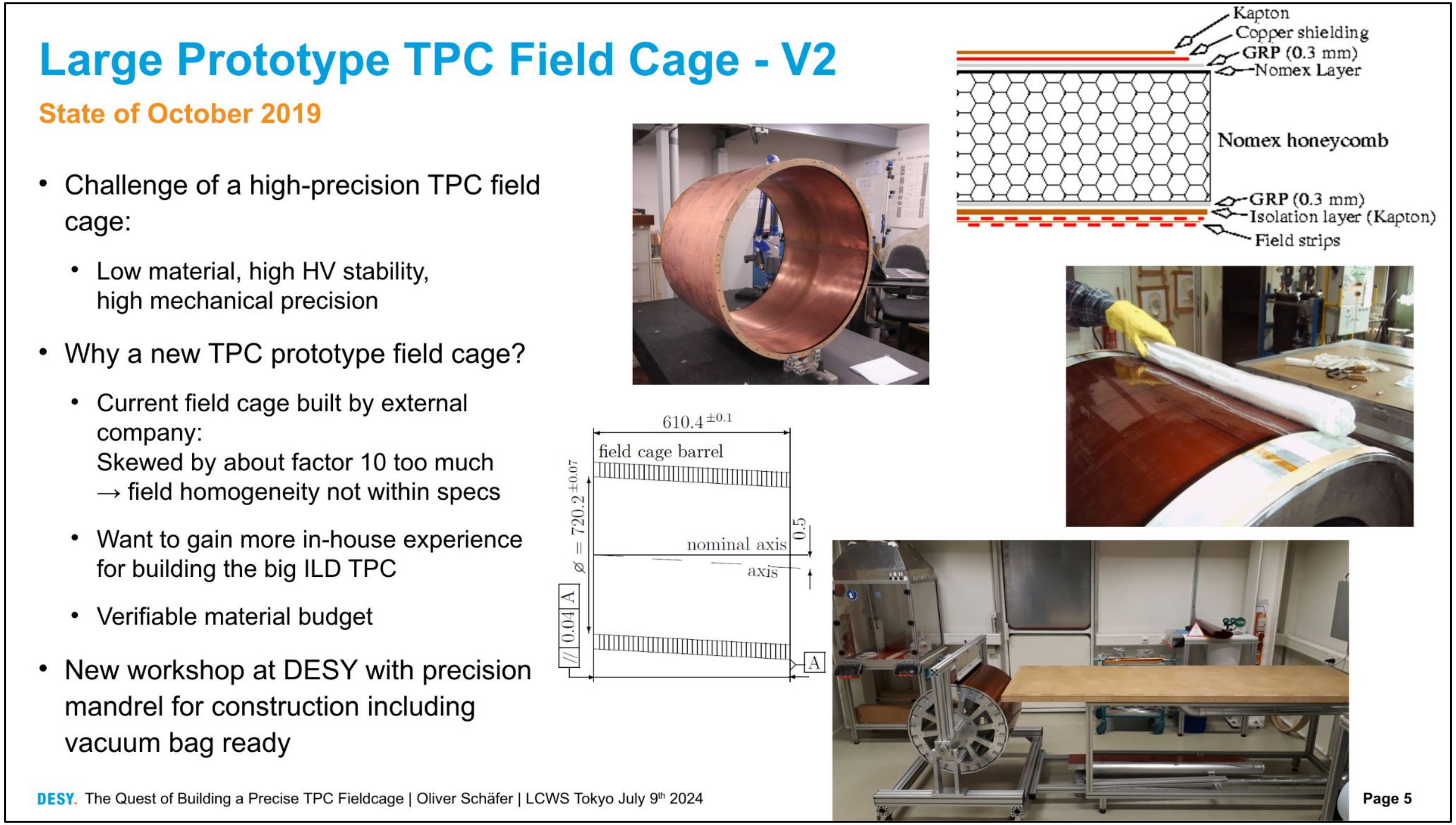



Summary

- In the last 8 years, a new type of TPCs has been designed, constructed and commissioned. It uses the ERAM technology (Encapsulated Resistive Anode Micromegas) to spread the charge and protect the electronics.
- A lot of progress has been obtained within T2K to understand the charge spreading, the homogeneity of the gain and RC maps.
- Two new such TPCs have been installed and commissionned at JPARC in the T2K Near Detector, contributing to a very significant upgrade of this experiment.
- All this will prove very useful as a preparation for an ILC TPC.

Building a Precise TPC Field Cage

Oliver Schafer



Large Prototype TPC Field Cage - V2

State of October 2019

- Challenge of a high-precision TPC field cage:
  - Low material, high HV stability, high mechanical precision
- Why a new TPC prototype field cage?
  - Current field cage built by external company: Skewed by about factor 10 too much → field homogeneity not within specs
  - Want to gain more in-house experience for building the big ILD TPC
  - Verifiable material budget
- New workshop at DESY with precision mandrel for construction including vacuum bag ready

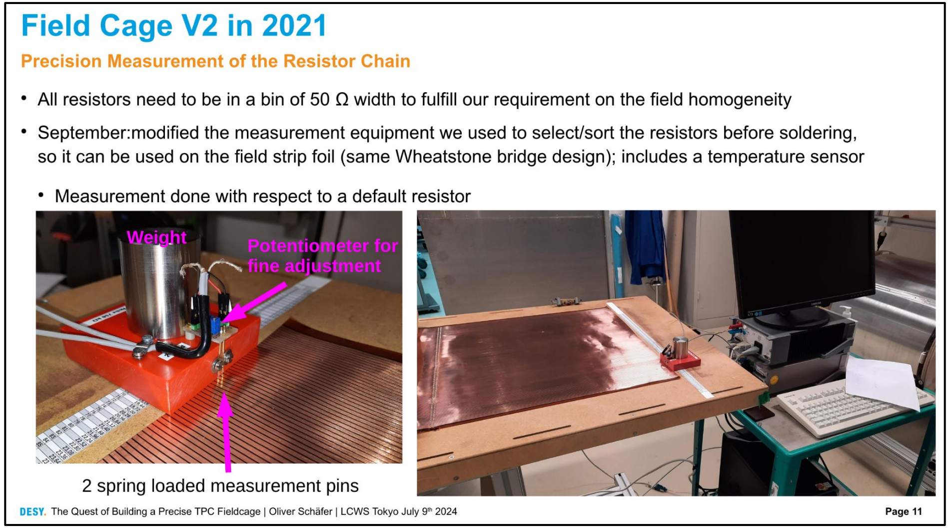
DESY. The Quest of Building a Precise TPC Fieldcage | Oliver Schäfer | LCWS Tokyo July 9th 2024

Page 5

Field Cage V2 in 2020

Field Strip Foil

- December: Investigating and fixing resistance mismatch
  - Signal runtime measurements (reflectometry) lead to find a tiny hole to the mirror strip side
  - Recorded the growth of that hole by interplay of electrical discharges and thermal decomposition (see separate video)
  - Carefully “cleaned” hole borders and removed copper
  - Closed by gluing in a polyimide patch
  - Re-painted conducting pattern on top
  - Resistance after repair roughly as expected
- December 16th: "We stay at home" rule
  - HV test of the repaired place planned
  - Final gluing delayed, no activity in workshop since



Field Cage V2 in 2021

Precision Measurement of the Resistor Chain

- All resistors need to be in a bin of 50 Ω width to fulfill our requirement on the field homogeneity
- September:modified the measurement equipment we used to select/sort the resistors before soldering, so it can be used on the field strip foil (same Wheatstone bridge design); includes a temperature sensor
  - Measurement done with respect to a default resistor

2 spring loaded measurement pins

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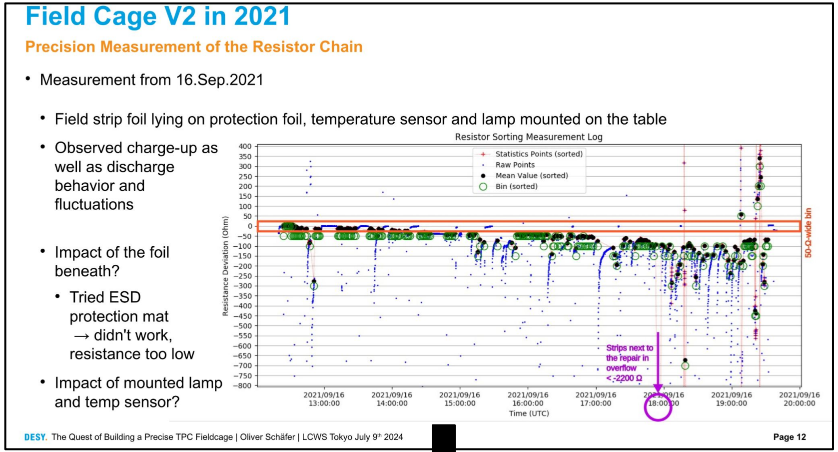
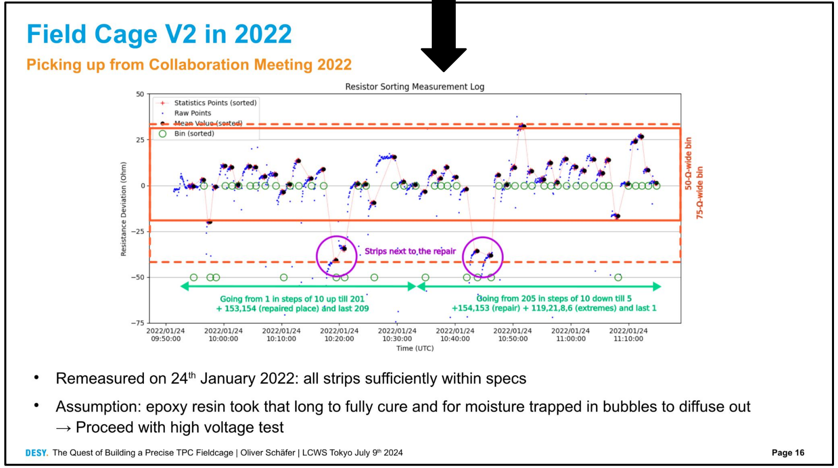


Field Cage V2 in 2021

Precision Measurement of the Resistor Chain

- Measurement from 16.Sep.2021
  - Field strip foil lying on protection foil, temperature sensor and lamp mounted on the table
  - Observed charge-up as well as discharge behavior and fluctuations
  - Impact of the foil beneath?
    - Tried ESD protection mat → didn't work, resistance too low
  - Impact of mounted lamp and temp sensor?

DESY. The Quest of Building a Precise TPC Fieldcage | Oliver Schäfer | LCWS Tokyo July 9th 2024 **Page 12**



Field Cage V2 in 2022

Picking up from Collaboration Meeting 2022

- Remeasured on 24th January 2022: all strips sufficiently within specs
- Assumption: epoxy resin took that long to fully cure and for moisture trapped in bubbles to diffuse out → Proceed with high voltage test

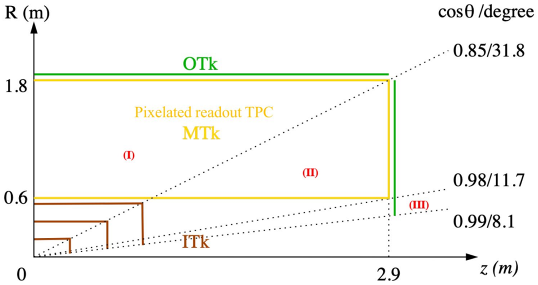
DESY. The Quest of Building a Precise TPC Fieldcage | Oliver Schäfer | LCWS Tokyo July 9th 2024 **Page 16**

High Granularity TPC for Tera-Z at CEPC

Huirong Qi

Track detector system in CEPC Phy.&Det. TDR

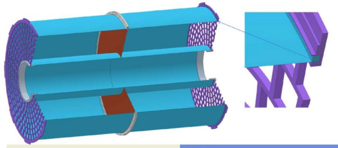
- The track detector system's geometry finalized.
  - All of physics simulation used the updated geometries for CEPC TDR document
  - Pixelated readout TPC as the **main track (MTK)** from radius of 0.6m to 1.8m



Geometry of the track detector system in CEPC TDR

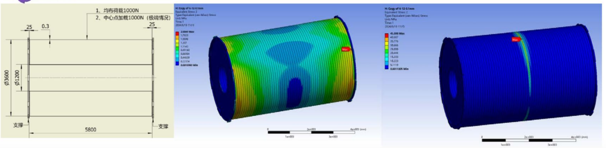
#1. Material budget at endcape/barrel Carbon Fibber √

- Consideration of new Carbon Fiber barrel instead of the honeycomb barrel
- **Ultra-light material** of the TPC barrel : **0.63% X_0 in total, including**
  - FEA preliminary calculation: 0.2mm carbon fibber barrel can tolerant of LGAD OTK (**100Kg**)
- Optimization of the connection back frame of the endcap (on going)



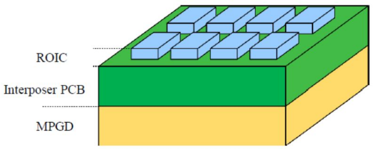
Material budget of TPC barrel

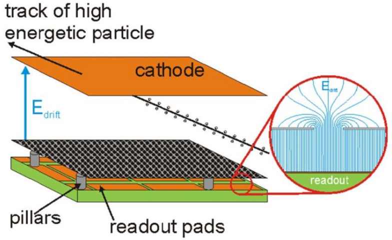
Layer of the barrels	D[cm]	X_0[cm]	d/X_0[%]
Copper shielding	0.001	1.45	0.07
CF outer barrel	0.020	25.28	0.08
Mirror strips	0.003	1.35	0.19
Polyimide substrate	0.005	32.65	0.02
Field strips	0.003	1.35	0.19
CF inner barrel	0.020	25.28	0.08
Sum of the material budget			**0.63**



Pixelated readout TPC technology for CEPC TDR

- A pixelated readout TPC is **a good option to provide realistic physics requirements** of Higgs Physical and Tera-Z Physics also (2E36) at CEPC.
  - Pixelated readout→ better resolution → low gain → less distortion
- **Highlights** of Pixelated readout TPC technology for CEPC TDR
  - Can deal with high rates (MHz/cm^2)
  - High spatial resolution → better momentum resolution
  - PID: dE/dx + dN/dx (**In space**)
  - Excellent two tracks separation





- **Low voxel occupancy** : 1E-5 to 1E-6 (cite#2)
- At 2 E36 with Physics event only, even bunch distribution(cite#3).
  - Pixelated readout much **LOWER** inner most occupancy (**0.6m inner radius**)
  - Pixelated readout can easily handle a high hits rate at Z pole. (cite#4)
  - The data at the inner radius @40M BX Z pole@1 Module ~0.05Gbps(Maximum).

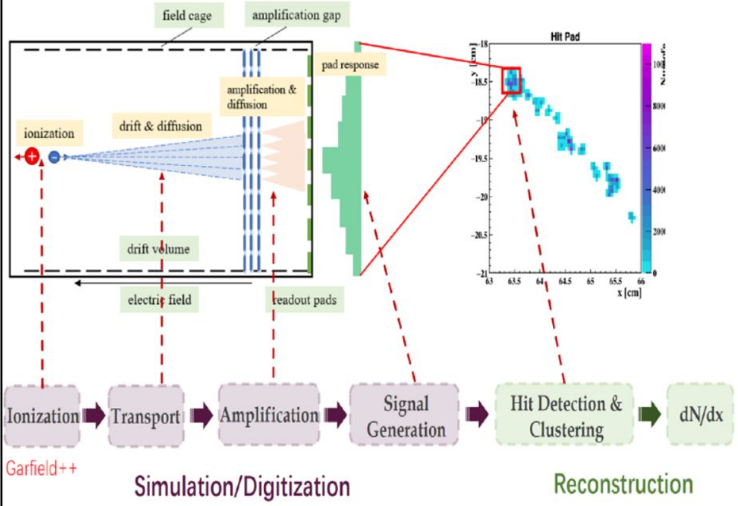
Prototype setup to verify power, spatial resolution, and distortion tolerances

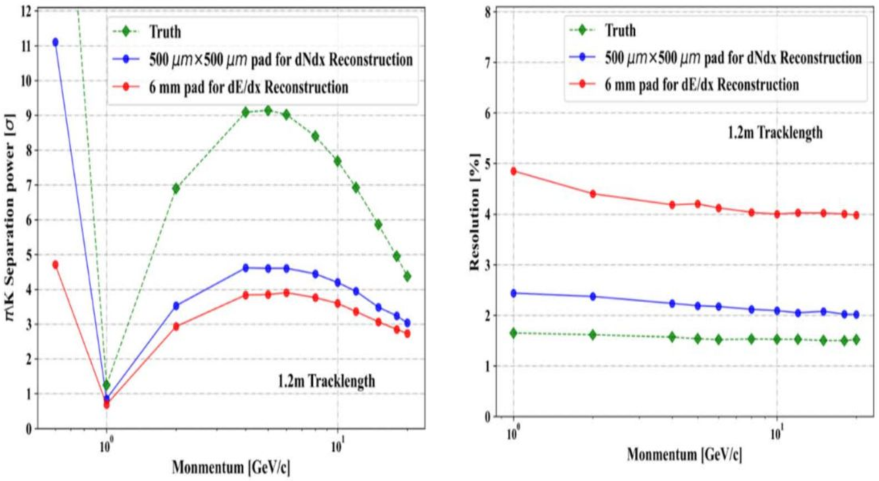
High Granularity TPC for Tera-Z at CEPC

#3. Improved dE/dx+dN/dx √

- Full simulation framework of pixelated TPC developed using Garfied++ and Geant4 at IHEP
- Investigating the π/κ separation power using reconstructed clusters, **a 3σ separation at 20GeV** with 50cm drift length can be achieved
- dN/dx has significant potential for **improving PID resolution**

$$\mathrm{Sp} = \frac{|\mu_A - \mu_B|}{\frac{\sigma_A + \sigma_B}{2}}$$





Cite#5 DOI: 10.22323/1.449.0553
Cite#6 EPS-HEP 2023 talk by Yue Chang

Simulation of TPC detector under 3T/2T and T2K mixture gas

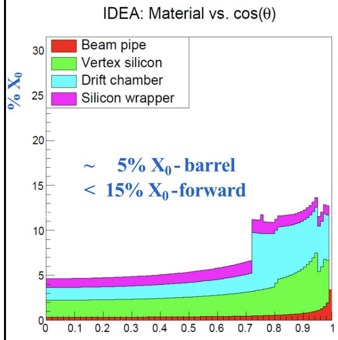
Drift Chamber for IDEA at FCC-ee

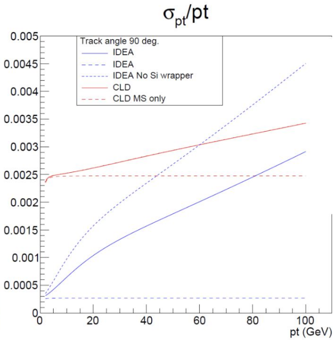
Nicola De Filippis

Design features of the IDEA Drift Chamber

For the purpose of tracking and ID at low and medium momenta mostly for heavy flavour and Higgs decays, the IDEA drift chamber is designed to cope with:

- ➢ transparency against multiple scattering, more relevant than asymptotic resolution
- ➢ a high precision momentum measurement
- ➢ an excellent particle identification and separation





Particle momentum range far from the asymptotic limit where MS is negligible

$$\frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\,p_T}{0.3\,B_0 L_0^2}\sqrt{\frac{5}{N+5}}$$

$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{0.3\beta\,B_0 L_0}\sqrt{\frac{d_{tot}}{X_0\,\sin\theta}}$$

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

Challenges for large-volume drift chambers

- **Electrostatic stability** condition: $\frac{\lambda^2}{4\pi\varepsilon}\frac{L^2}{w^2} < wire\ tension\ < YTS \cdot \pi r_w^2$

λ = linear charge density (gas gain)
L = wire length, r_w wire radius, w = drift cell width
YTS = wire material yield strength

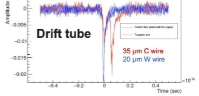
The proposed drift chambers for FCC-ee and CEPC have lengths **L = 4 m** and plan to exploit the cluster counting technique, which requires gas gains **~5×10⁵**.
This poses serious constraints on the drift cell width (**w**) and on the wire material (**YTS**).

⇒ new wire material studies

- **Non-flammable gas / recirculating gas systems**

Safety requirements (**ATEX**) demands stringent limitations on flammable gases;
Continuous increase of **noble gases cost**

⇒ gas studies

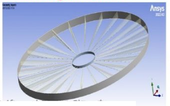


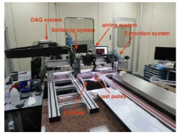
- **Data throughput**

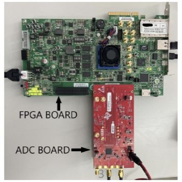
Large number of channels, high signal sampling rate, long drift times (slow drift velocity), required for cluster counting, and high physics trigger rate (Z_0-pole at FCC-ee) imply data transfer rates in excess of **~1 TB/s**

⇒ on-line real time data reduction algorithms

- **New wiring systems for high granularities / / new end-plates / new materials**



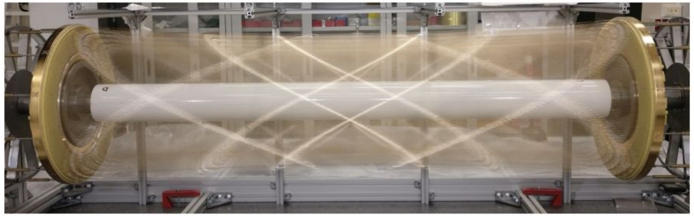




- ➢ inner radius R_{in} = 0.35m, outer radius R_{out} = 2m
- ➢ length L = 4m
- ➢ drift length ~1 cm
- ➢ drift time ~150ns

➢ 343968 wires in total:

sense vires: 20 μm diameter W(Au) => 56448 wires
field wires: 40 μm diameter Al(Ag) => 229056 wires
f. and g. wires: 50 μm diameter Al(Ag) => 58464 wires



Drift Chamber for IDEA at FCC-ee

2025 full-length prototype: Goals

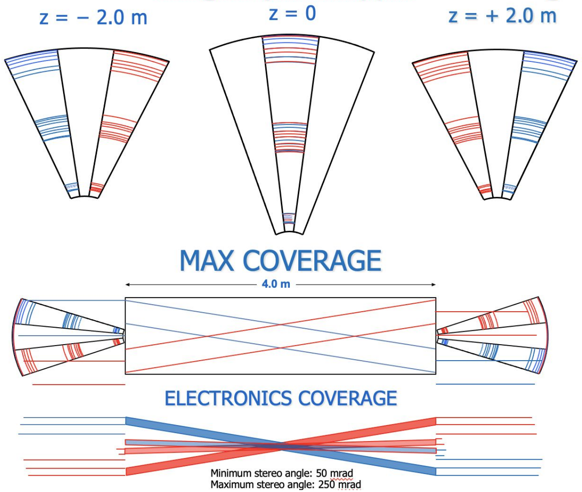
- ▶ Check the limits of the wires' electrostatic stability at full length and at nominal stereo angles
- ▶ Test different wires: uncoated Al, C monofilaments, Mo sense wires, …, of different diameters
  - o Test different wire anchoring procedures (soldering, welding, gluing, crimping, …) to the wire PCBs
  - o Test different materials and production procedures for spokes, stays, support structures and spacers
  - o Test compatibility of proposed materials with drift chamber operation (outgassing, aging, creeping, …)
- ▶ Validate the concept of the wire tension recovery scheme with respect to the tolerances on the wire positions
  - o Optimize the layout of the wires' PCBs (sense, field and guard), according to the wire anchoring procedures, with aim at minimizing the end-plate total material budget
- ▶ Starting from the new concepts implemented in the MEG2 CDCH robot, optimize the wiring strategy, by taking into account the 4m long wires arranged in multi-wire layers
- ▶ Define and validate the assembly scheme (with respect to mechanical tolerances) of the multi-wire layers on the end plates
  - o Define the front-end cards channel multiplicity and their location (cooling system necessary?)
- ▶ Optimize the High Voltage and signal distribution (cables and connectors)
- ▶ Test performance of different versions of front-end, digitization and acquisition chain

2025 full-length prototype: Coverage

TOTAL LAYERS: 8
Sense wires: 168
Field wires: 965
Guard wires: 264

PCBoards wire layers: 42
Sense wire boards: 8
Field wire boards: 22
Guard wire boards: 12
HV values: 14

Readout channels: 8+8 + 16+16+16+16 + 16+16 = 112



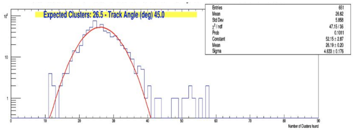
Minimum stereo angle: 50 mrad
Maximum stereo angle: 250 mrad

2021/2022 beam test results: performance plots

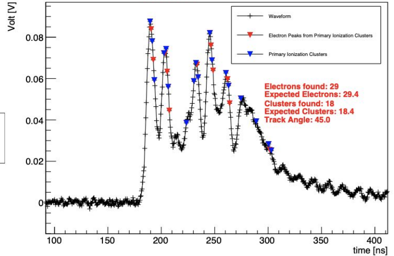
- Several algorithms developed for electron peak finding:

✓ Derivative Algorithm (DERIV)
✓ and Running Template Algorithm (RTA)
✓ NN-based approach (developed by IHEP)

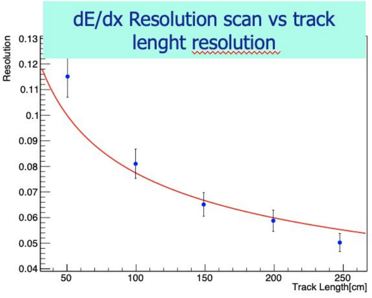
Poissonian distribution for the number of clusters

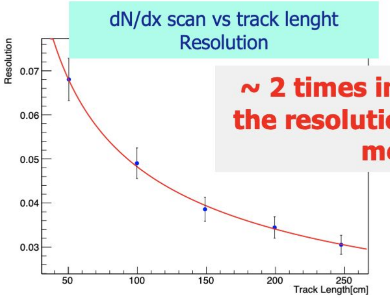


Sense Wire Diameter 15 μm; Cell Size 1.0 cm
Track Angle 45; Sampling rate 2 GSa/s
Gas Mixture He:IsoB 80/20



2021/2022 beam test results: resolutions

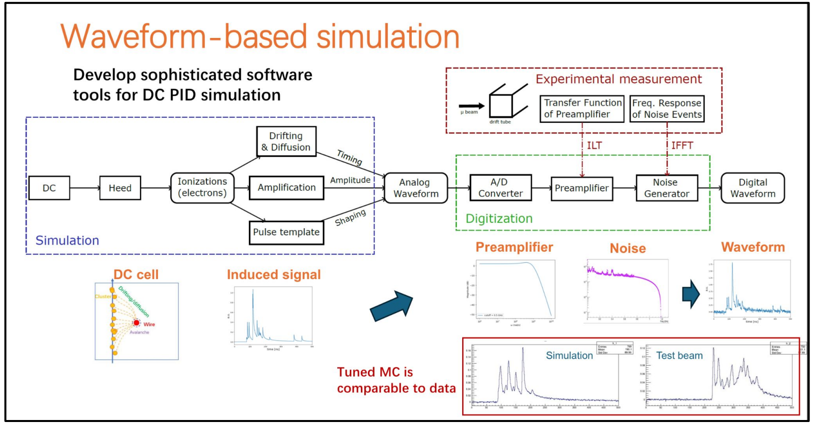




~ 2 times improvement in the resolution using dN/dx method

Drift Chamber Cluster Counting for CEPC

Guang Zhao



Waveform-based simulation

Develop sophisticated software tools for DC PID simulation

Experimental measurement

Transfer Function of Preamplifier

Freq. Response of Noise Events

DC cell

Induced signal

Preamplifier

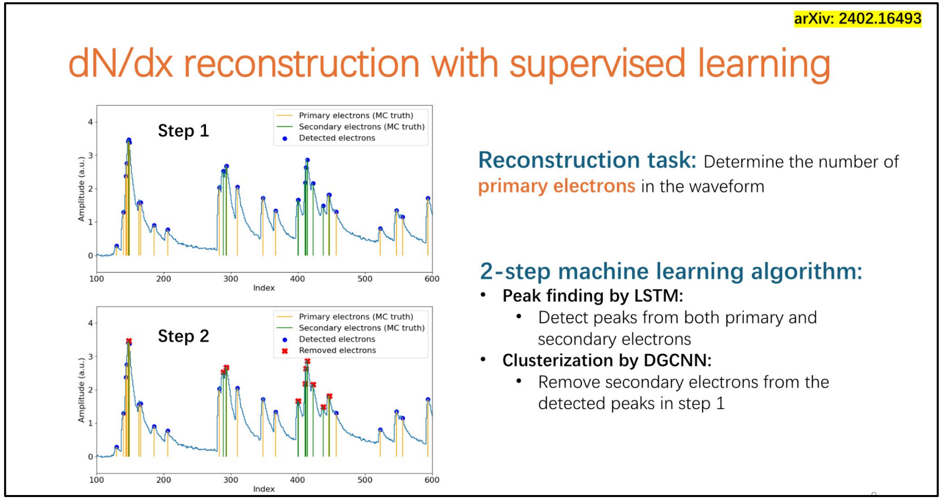
Noise

Waveform

Simulation

Test beam

Tuned MC is comparable to data



arXiv: 2402.16493

dN/dx reconstruction with supervised learning

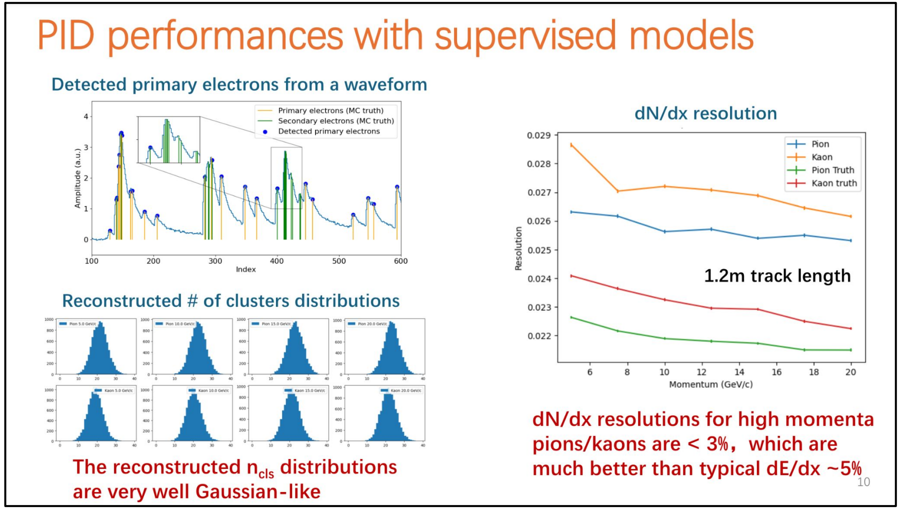
Step 1

Step 2

Reconstruction task: Determine the number of **primary electrons** in the waveform

2-step machine learning algorithm:

- **Peak finding by LSTM:**
  - Detect peaks from both primary and secondary electrons
- **Clusterization by DGCNN:**
  - Remove secondary electrons from the detected peaks in step 1



PID performances with supervised models

Detected primary electrons from a waveform

Reconstructed # of clusters distributions

The reconstructed n_{cls} distributions are very well Gaussian-like

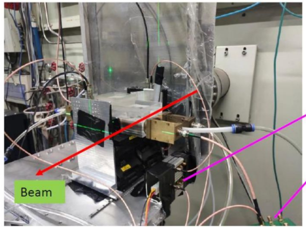
dN/dx resolution

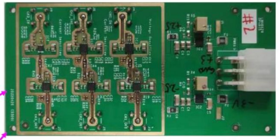
1.2m track length

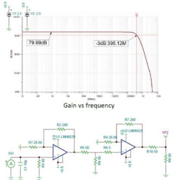
dN/dx resolutions for high momenta pions/kaons are < 3%，which are much better than typical dE/dx ~5%

Drift Chamber Cluster Counting for CEPC

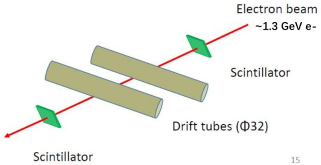
Test beam with detector prototype (IHEP)







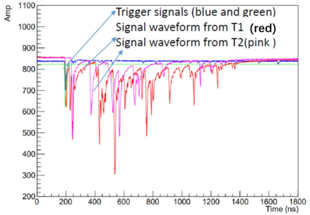
High bandwidth current sensitive preamplifiers based on LMH6629 have been designed and developed

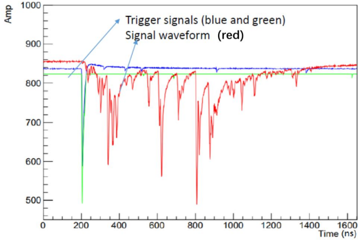


- Two drift tubes + preamps + ADC (1GHz)
- The system was tested with electron beam at IHEP

Typical collected waveforms

- He: iC_4H_{10} = 90 : 10
- Digitizer: DT5751
  - Sampling rate: 1GHz
  - Four channels, two for scintillators, two for drift tubes





- Clear electron peaks: ~ns risetime

dN/dx reconstruction with domain adaptation

Computer Physics Communications 300, 109208 (2024)

Loss for labeled samples in source domain

$$\min_{f,g}\left[\sum_{i=1}^{m} L_s\left(y_i^s, f(g(x_i^s))\right) + \boxed{\frac{1}{m_l}\sum_{i=1}^{m_l} L_t\left(y_i^{t,l}, f\left(g(x_i^{t,l})\right)\right)} + \min_{\gamma\in\Delta}\sum_{i,j}^{m}\gamma_{ij}\left(\alpha\|g(x_i^s)-g(x_j^t)\|^2 + \lambda_t L_t\left(y_i^s, f\left(g(x_j^t)\right)\right)\right)\right]$$

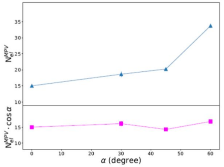
Loss for labeled samples in target domain (THIS WORK)

Cost of feature differences between source and target

Cost of 'label' differences between source and target

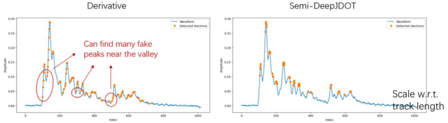
Cost of joint feature-label distribution for OT

Semi-supervised domain adaptation



ML algorithm is stable w.r.t. track length

Single-waveform results between derivative alg. and DL alg.



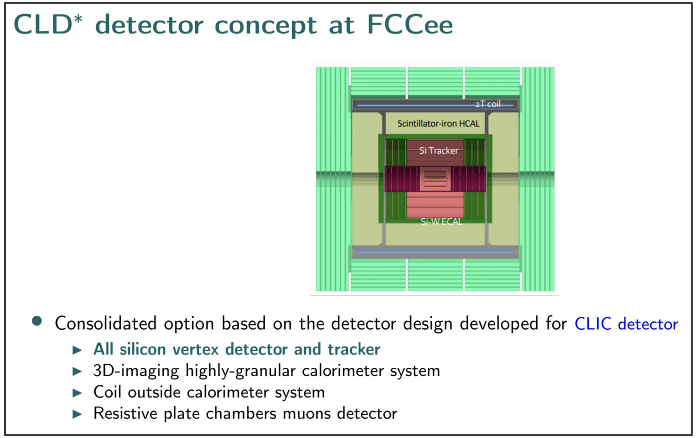
ML algorithm is more powerful to discriminate signals and noises

Summary

- **R & D progress of the CEPC drift chamber**
  - PID performance: >3σ K/π separation at 20 GeV/c for 1.2 m track length
  - dN/dx reconstruction with deep learning shows promising performance for simulation and testbeam data
  - Fast electronics is under development. Preliminary analysis with the testbeam validates the electronics and the feasibility of dN/dx measurement
  - Preliminary mechanical design and FEA show a stable structure
  - Global electronics scheme is reasonable
- **Plans**
  - Fine detector optimization
  - Optimize deep learning algorithm and FPGA implementation
  - Prototyping and testing with full-length cells (mechanics, manufacturing, testing)

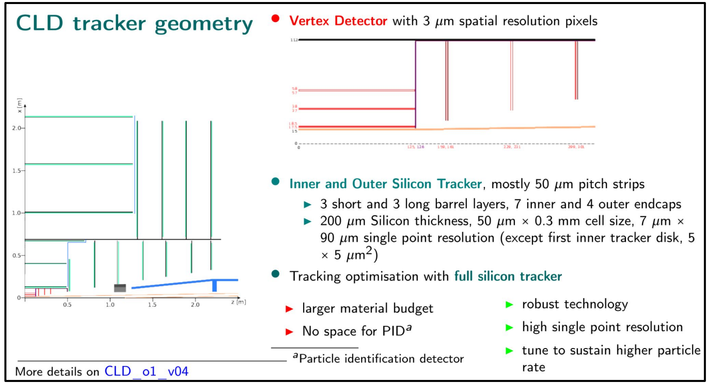
CLD Tracking Performance

Gaelle Sadowski



CLD* detector concept at FCCee

- Consolidated option based on the detector design developed for CLIC detector
  - **All silicon vertex detector and tracker**
  - 3D-imaging highly-granular calorimeter system
  - Coil outside calorimeter system
  - Resistive plate chambers muons detector



CLD tracker geometry

- **Vertex Detector** with 3 μm spatial resolution pixels

- **Inner and Outer Silicon Tracker**, mostly 50 μm pitch strips
  - 3 short and 3 long barrel layers, 7 inner and 4 outer endcaps
  - 200 μm Silicon thickness, 50 μm × 0.3 mm cell size, 7 μm × 90 μm single point resolution (except first inner tracker disk, 5 × 5 μm^2)
- Tracking optimisation with **full silicon tracker**
  - larger material budget
  - No space for PID[a]
  - robust technology
  - high single point resolution
  - tune to sustain higher particle rate

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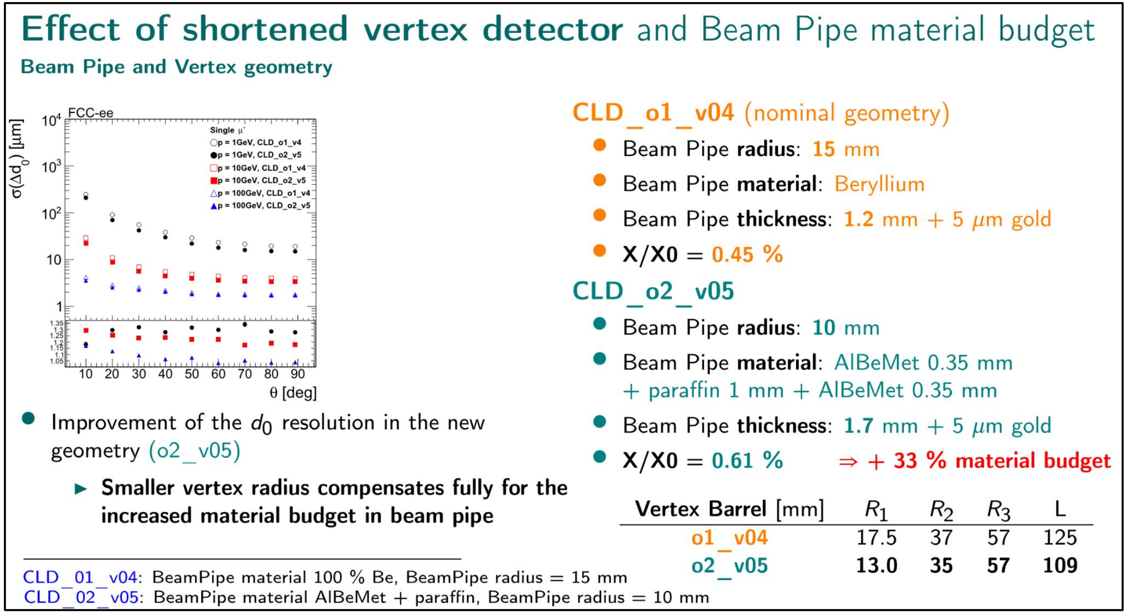
[a] Particle identification detector

More details on CLD_o1_v04



Effect of shortened vertex detector and Beam Pipe material budget

Beam Pipe and Vertex geometry

- Improvement of the d_0 resolution in the new geometry (o2_v05)
  - **Smaller vertex radius compensates fully for the increased material budget in beam pipe**

CLD_o1_v04 (nominal geometry)

- Beam Pipe **radius**: **15** mm
- Beam Pipe **material**: Beryllium
- Beam Pipe **thickness**: **1.2** mm + 5 μm gold
- **X/X0** = **0.45 %**

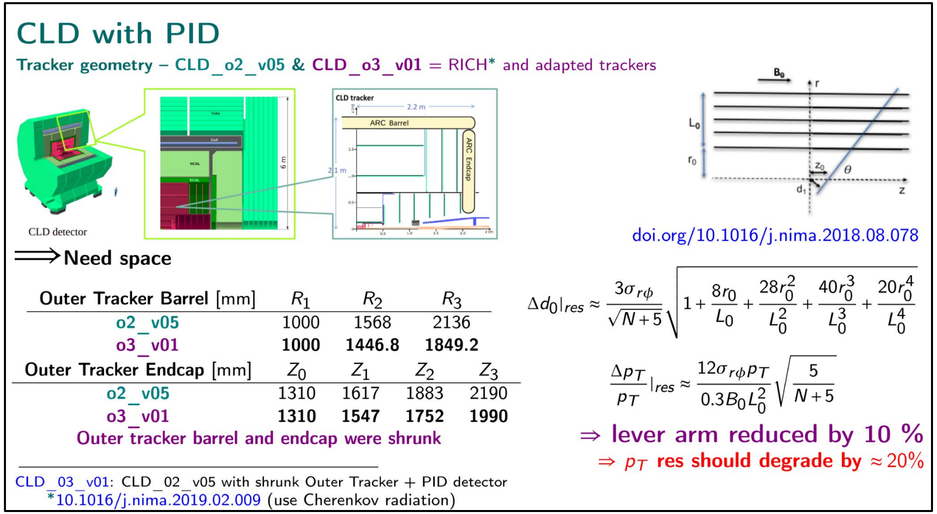
CLD_o2_v05

- Beam Pipe **radius**: **10** mm
- Beam Pipe **material**: AlBeMet 0.35 mm + paraffin 1 mm + AlBeMet 0.35 mm
- Beam Pipe **thickness**: **1.7** mm + 5 μm gold
- **X/X0** = **0.61 %** ⇒ **+ 33 % material budget**

Vertex Barrel [mm]	R_1	R_2	R_3	L
o1_v04	17.5	37	57	125
o2_v05	**13.0**	**35**	**57**	**109**

CLD_01_v04: BeamPipe material 100 % Be, BeamPipe radius = 15 mm
CLD_02_v05: BeamPipe material AlBeMet + paraffin, BeamPipe radius = 10 mm

CLD Tracking Performance



CLD with PID

Tracker geometry – CLD_o2_v05 & CLD_o3_v01 = RICH* and adapted trackers

doi.org/10.1016/j.nima.2018.08.078

$\Longrightarrow$ **Need space**

Outer Tracker Barrel [mm]	R_1	R_2	R_3
o2_v05	1000	1568	2136
o3_v01	**1000**	**1446.8**	**1849.2**

Outer Tracker Endcap [mm]	Z_0	Z_1	Z_2	Z_3
o2_v05	1310	1617	1883	2190
o3_v01	**1310**	**1547**	**1752**	**1990**

Outer tracker barrel and endcap were shrunk

$$\Delta d_0|_{res} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

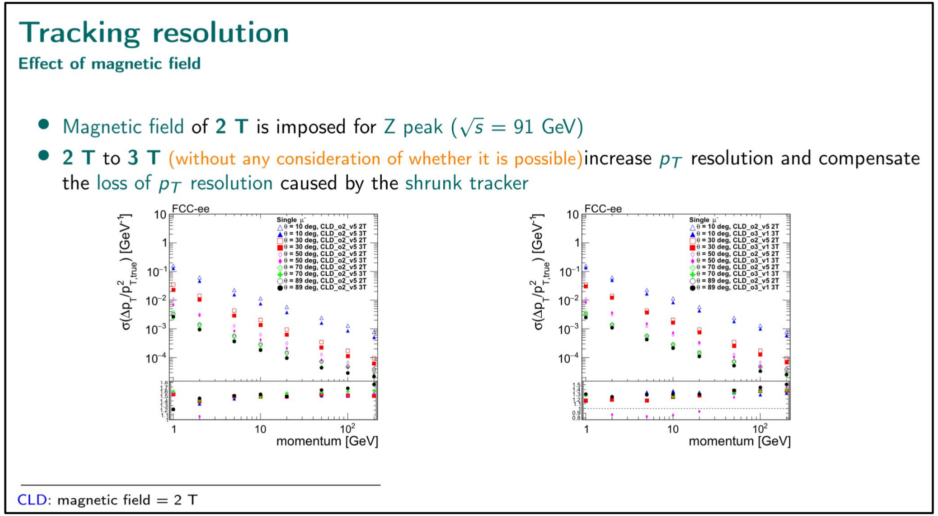
$$\frac{\Delta p_T}{p_T}|_{res} \approx \frac{12\sigma_{r\phi}p_T}{0.3B_0L_0^2}\sqrt{\frac{5}{N+5}}$$

$\Rightarrow$ **lever arm reduced by 10 %**

$\Rightarrow$ **p_T res should degrade by** $\approx 20\%$

CLD_03_v01: CLD_02_v05 with shrunk Outer Tracker + PID detector

*10.1016/j.nima.2019.02.009 (use Cherenkov radiation)



Tracking resolution

Effect of magnetic field

- Magnetic field of **2 T** is imposed for Z peak ($\sqrt{s} = 91$ GeV)
- **2 T** to **3 T** (without any consideration of whether it is possible)increase p_T resolution and compensate the loss of p_T resolution caused by the shrunk tracker

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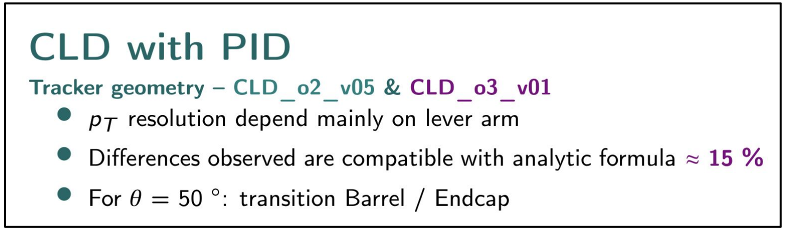
CLD: magnetic field = 2 T



CLD with PID

Tracker geometry – CLD_o2_v05 & CLD_o3_v01

- p_T resolution depend mainly on lever arm
- Differences observed are compatible with analytic formula $\approx$ **15 %**
- For $\theta = 50$ °: transition Barrel / Endcap

Summary

- Impressive progress in simulation, detector R&D, and building and testing prototypes to verify the functionality of various vertex and tracking technologies, as well as readout systems and ASICs
- Tracking, Vertex, and Timing Detector requirements continue to evolve as physics studies advance
    - particle ID both at low and high momentum: Timing layers, cluster counting and dE/dx, impact of RICH on tracker design
    - Long lived particles, kinks, …