Electronics for future detectors

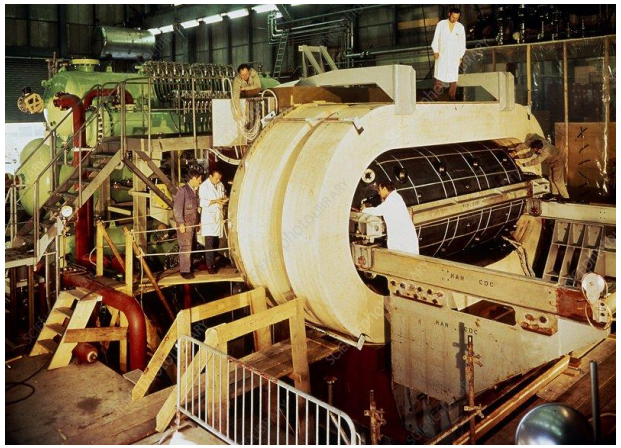
ILD workshop

Christophe de LA TAILLE

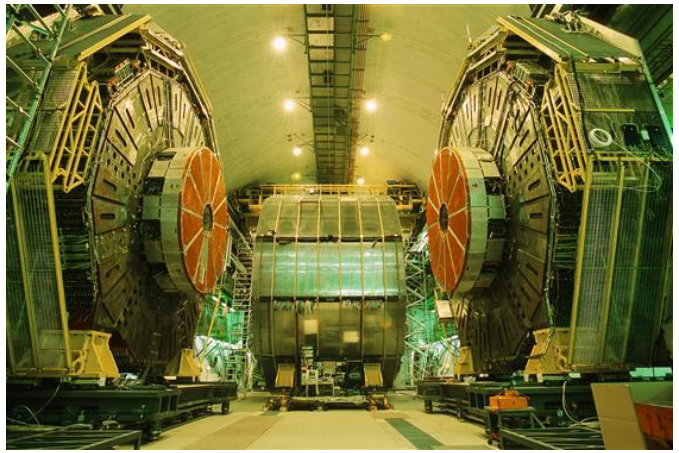
16 jan 2024

Organization for Micro-Electronics desiGn and Applications

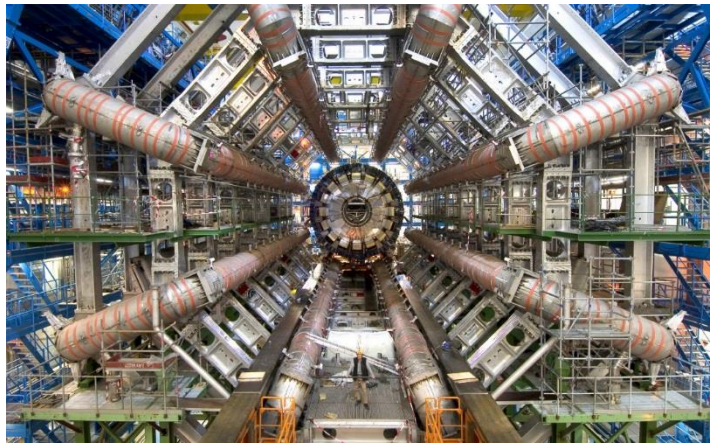
Evolution of experiments and technology



Gargamelle 1970

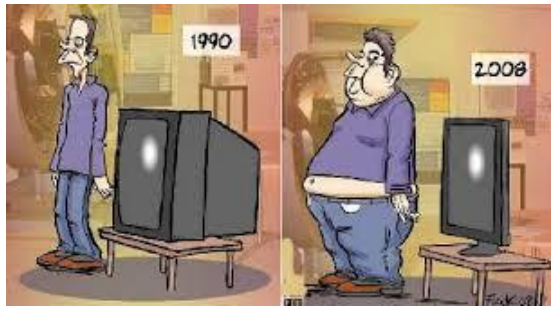


ALEPH 1990

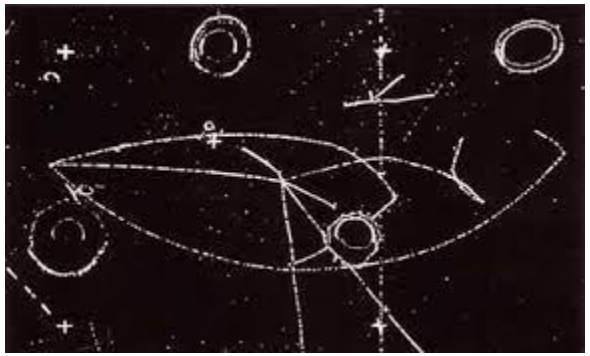


ATLAS 2010

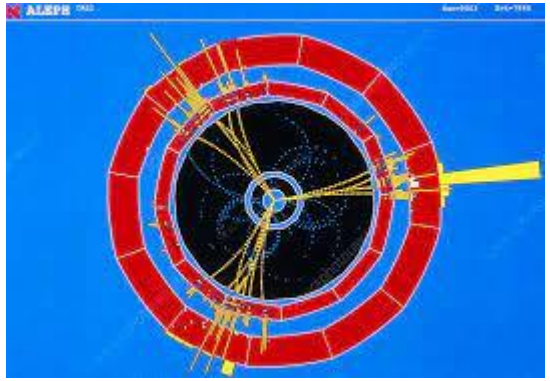
CMS upgrade 2030



Evolution of detectors and readout electronics



Gargamelle 1970



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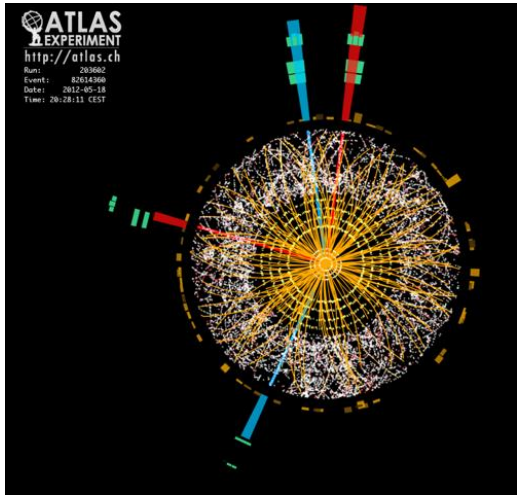
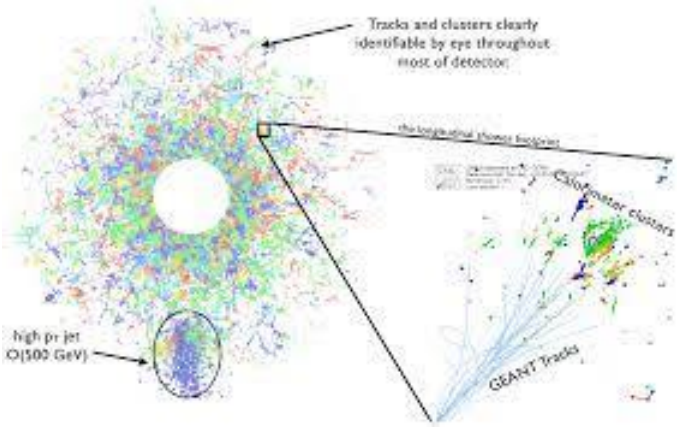
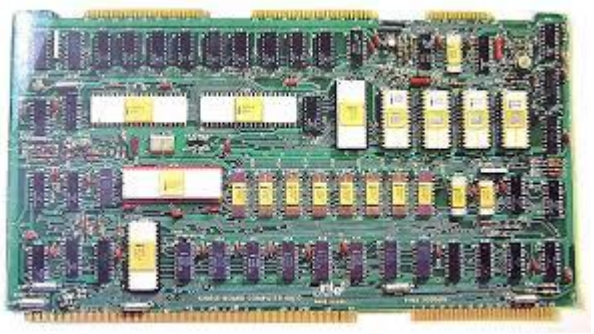
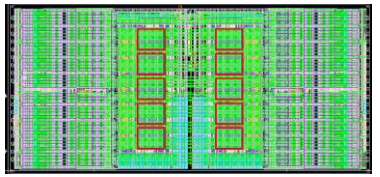


ATLAS 2010



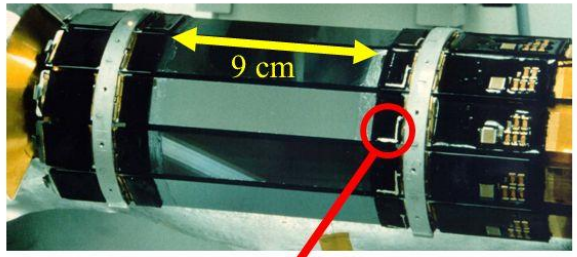
CMS 2030



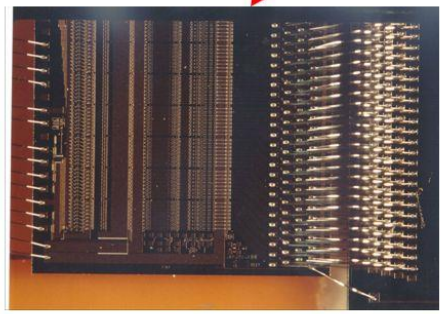


35 years of microelectronics in HEP [CERN]

MICROPLEX (1985)

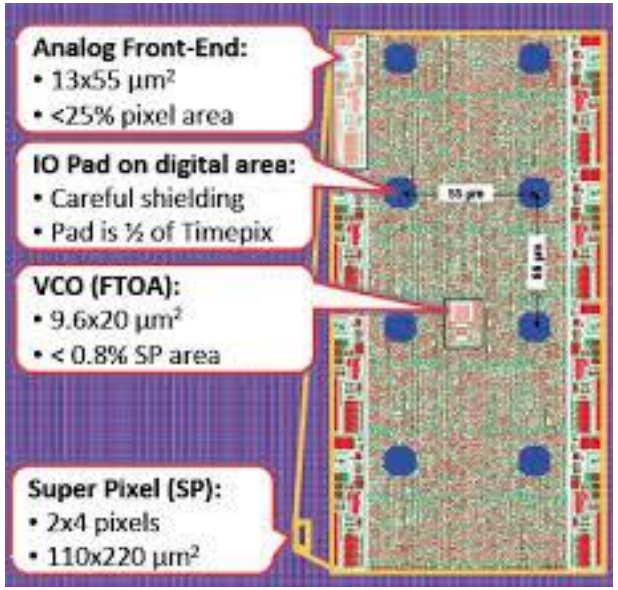


Silicon Strip
Vertex Detector:
MARK II experiment
at SLAC Linear Collider
(512 channels/module;
18K channels total)

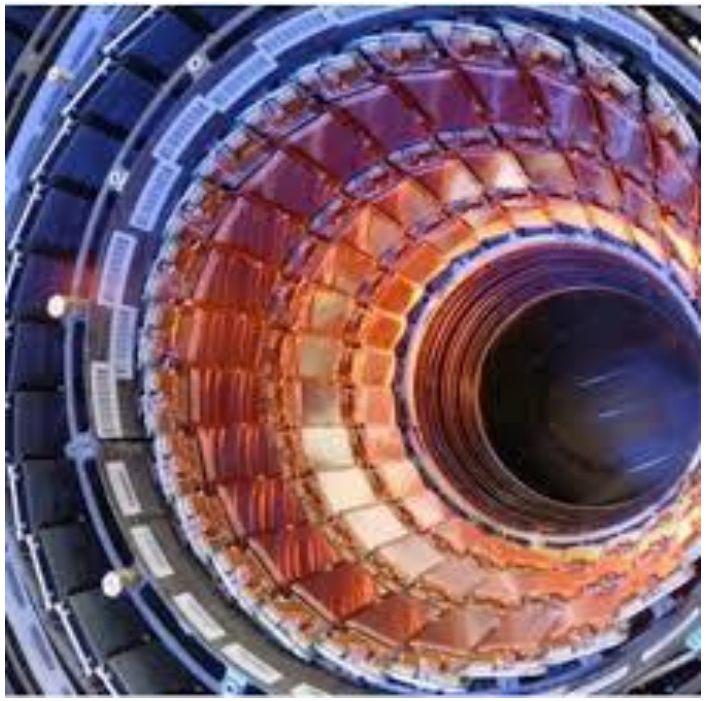


Microplex readout chip
128 channels, 47.5 µm pitch
(Walker, Parker, Hyams)

Parallel efforts in ALEPH, DELPHI, OPAL at LEP and CDF at the Tevatron Collider

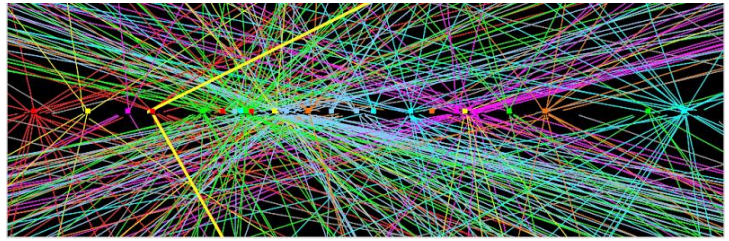


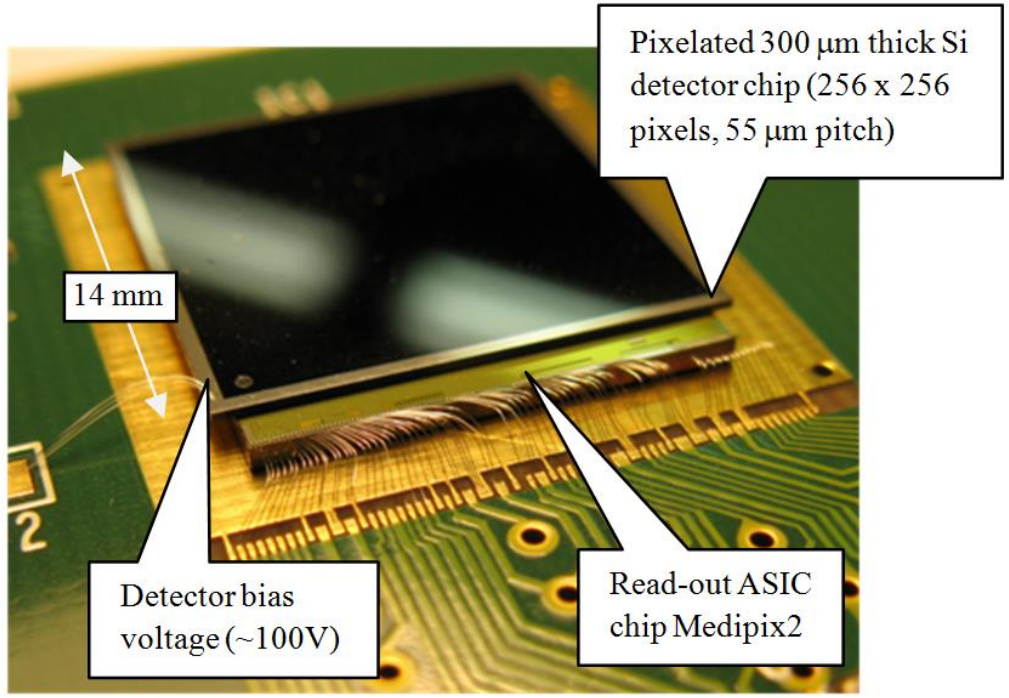
TIMEPIX4 (2020)

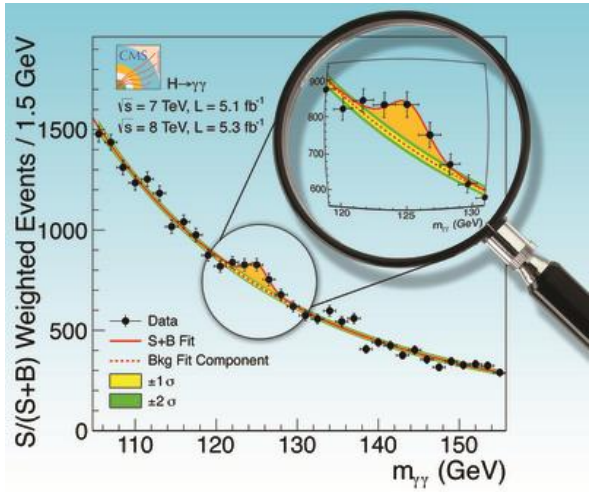


Why we do our chips instead of buying them ?

- ASIC = Application Specific Integrated Circuit
- Innovation in technology yields new/better detectors
- Specific requirements in HEP : physicists/designers interplay
- « No chip => no detector » => no experiment…

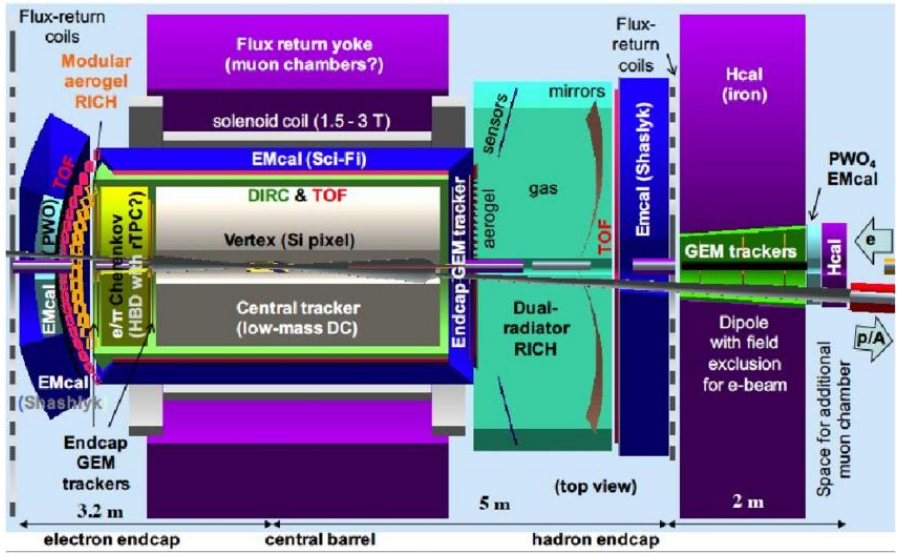


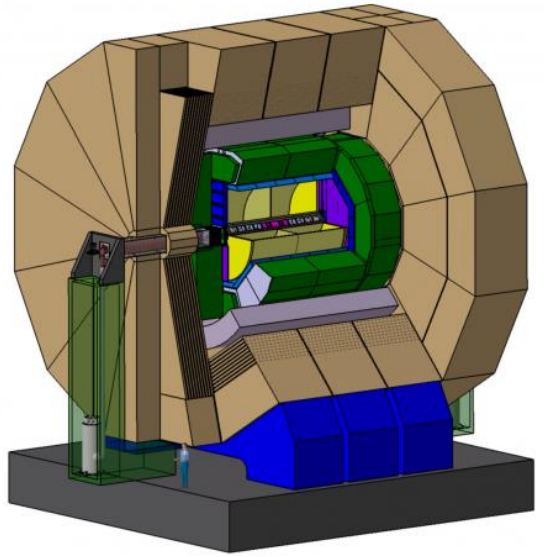




Future detectors

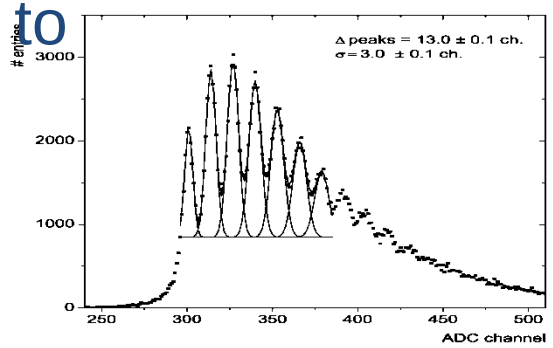
- New sensors regularly pop up…
  - SiPMs
  - MAPs
  - LGADs, ACLGADs
  - …
- Electronics also regularly improves…
  - Technology evolution (CMOS scaling)
  - More functionnalities (timing)
  - Lower power
  - Allows electronics on detector, better granularity, timing…
- Progress from either or both !

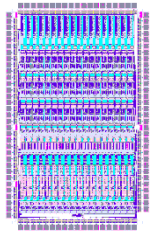




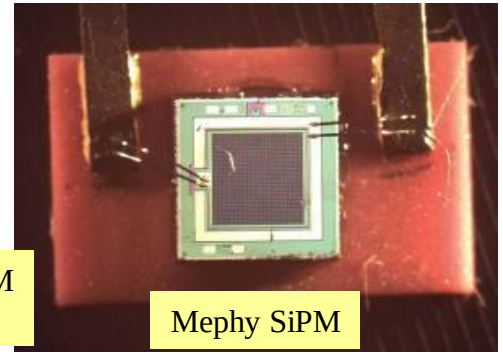
New detectors : SiPMs

- From first MEPHY SiPMs (CALICE 2005) to HGCAL, TOFHIR, MU2E….

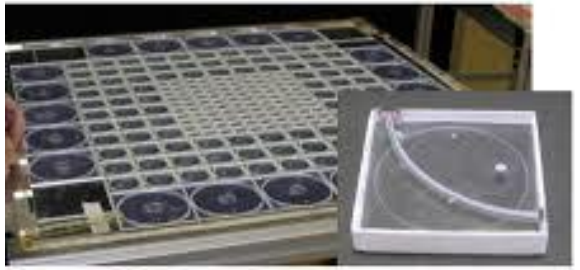


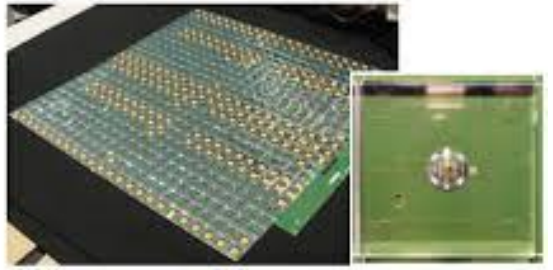


FLC_SiPM ASIC



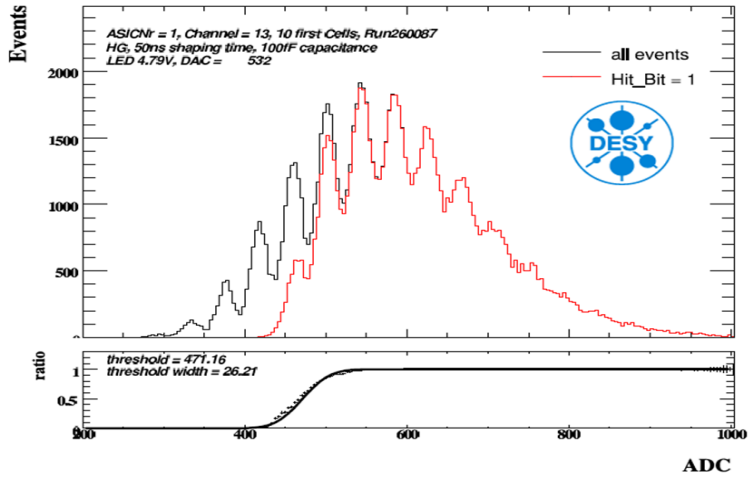
- Large progress in sensors (FBK, HPK…)
  - Lower dark noise
  - Better crosstalk
  - Larger area





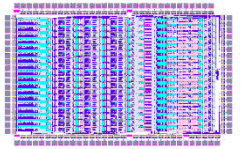
- Future
  - Larger area
  - optimized SiPM/ROC (granularity for best timing)
  - « Picosecond challenge »

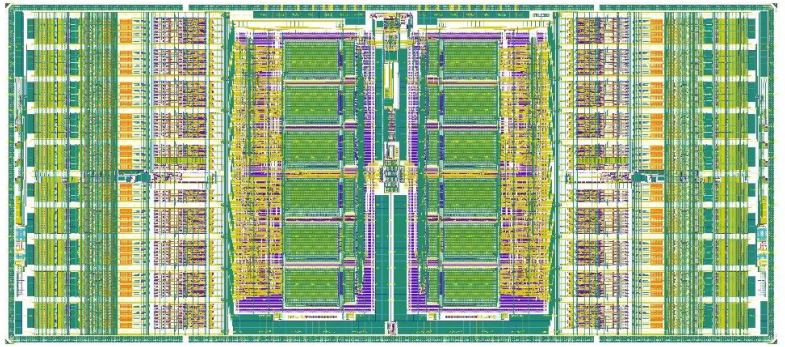
SiPM SPECTRUM with Autotrigger

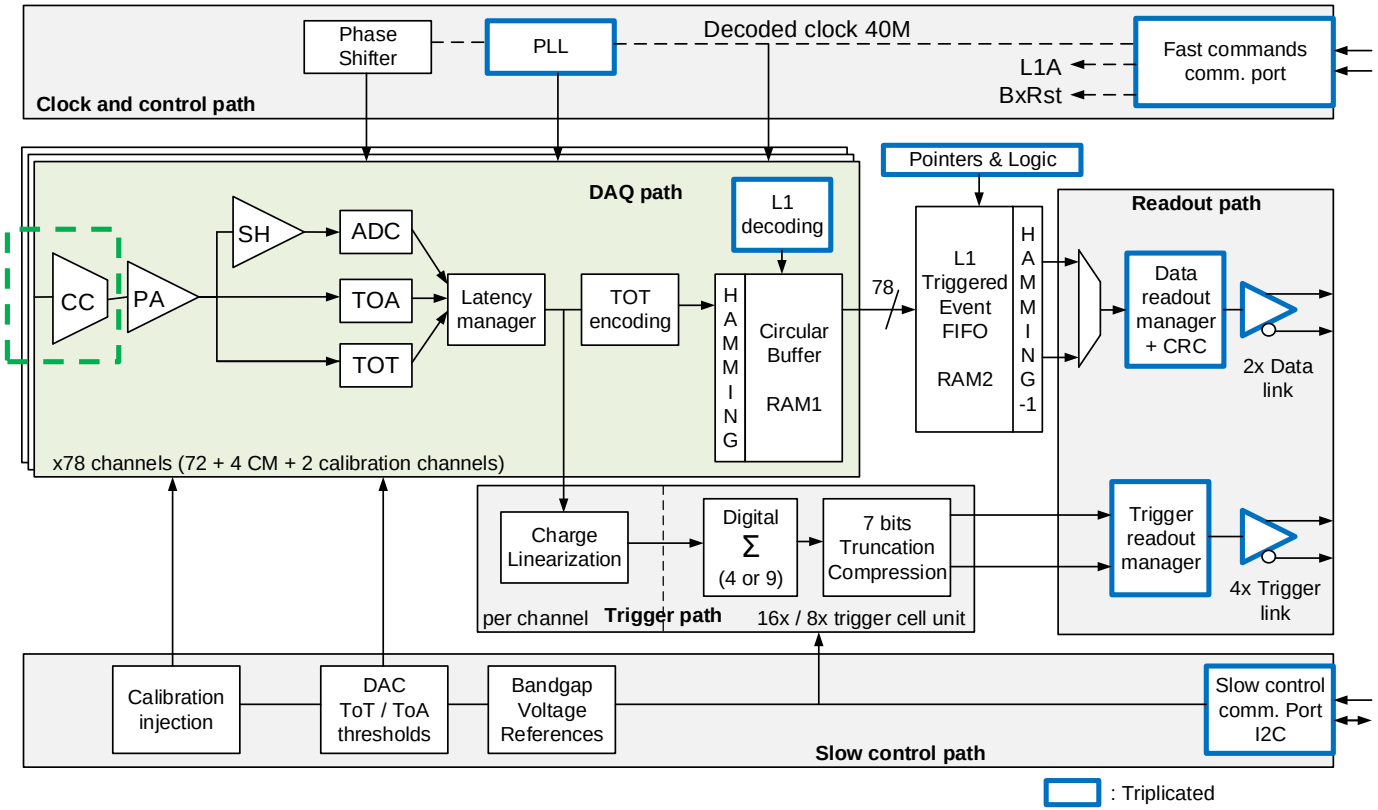


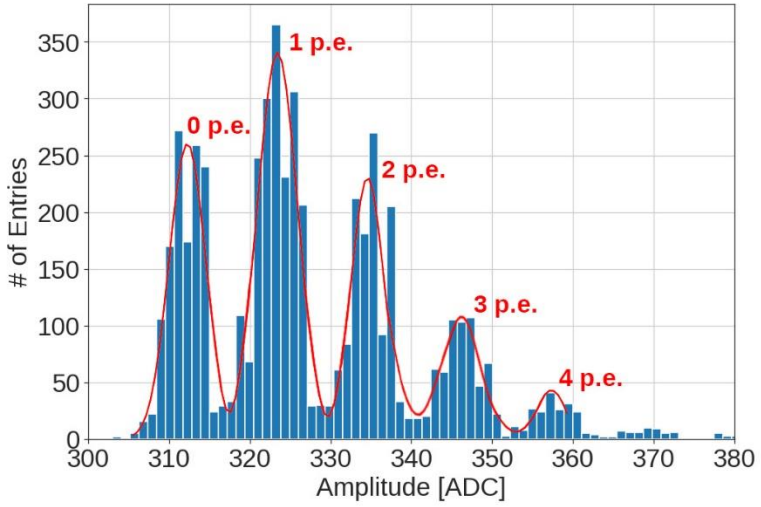
SiPM electronics

- From FLC-SiPM to H2GCROC, TOFHIR, FastIC…
- Preamps, ADCs, TDCs inside : SoC
  - Large dynamic range and few tens of ps timing





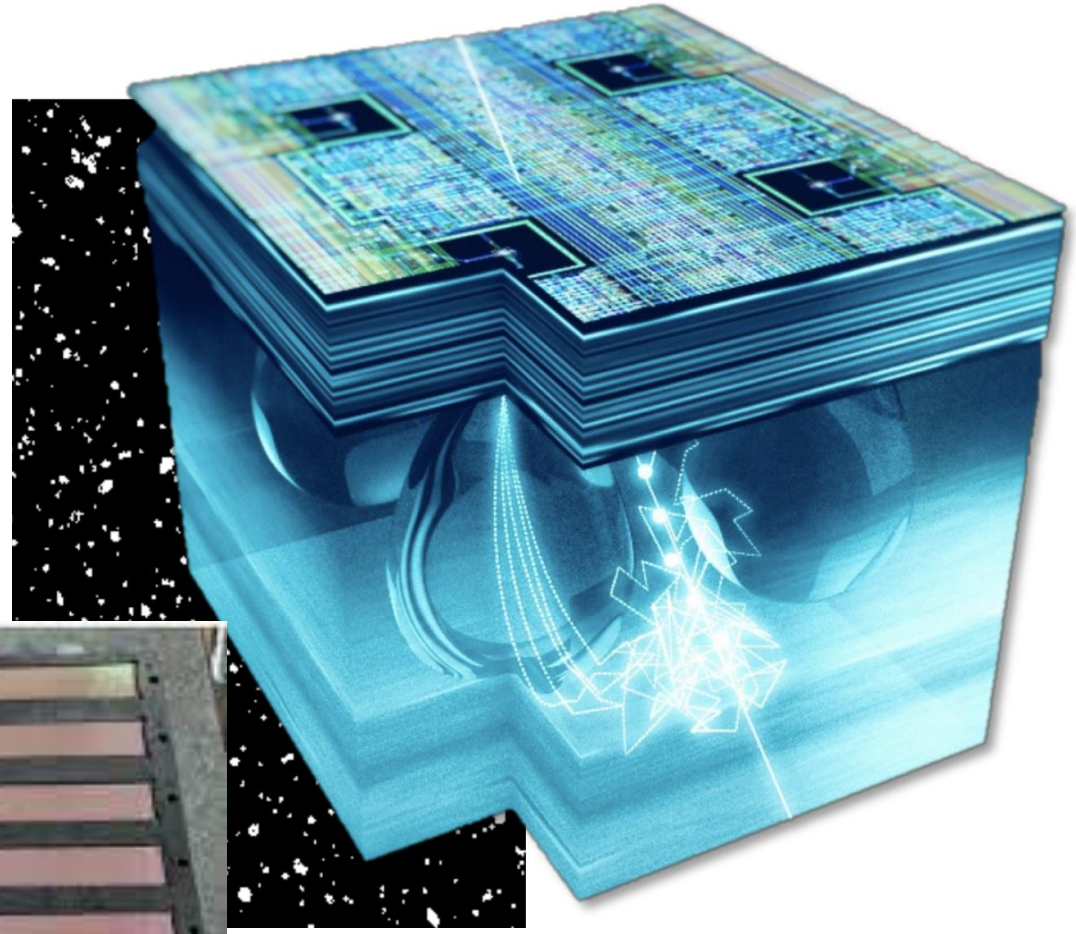




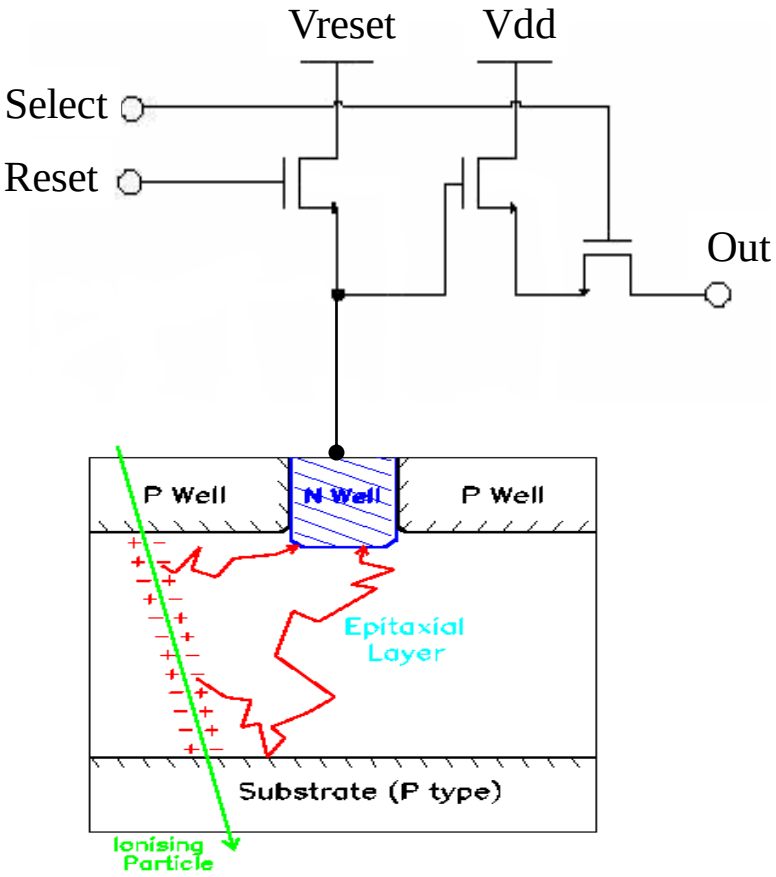
New detectors : MAPS [see talk by M. Winter]

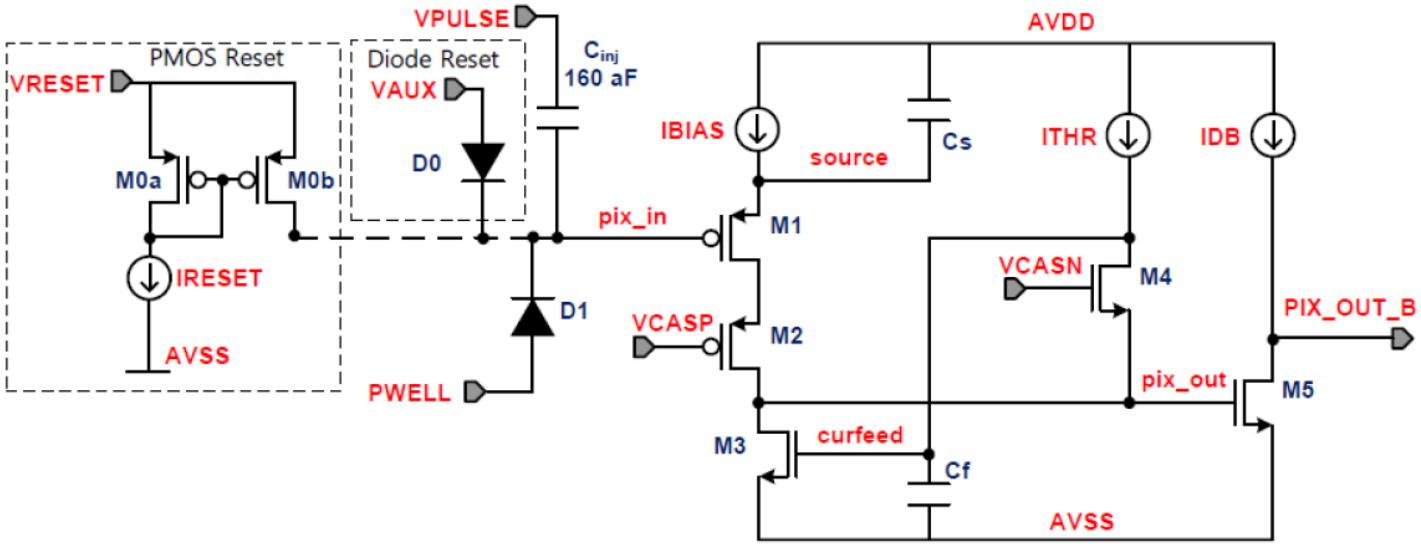
- Monolithic Active Pixels Sensors
- From MIMOSA to ALPIDE and MOSS
- Combined detector and readout electronics

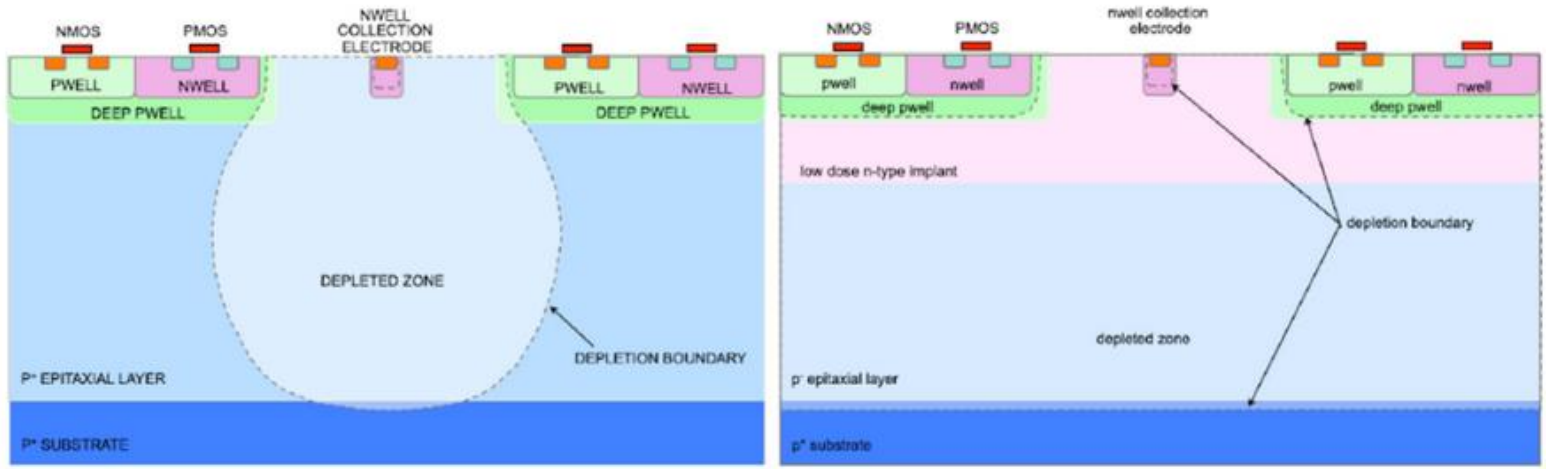
- Future
  - Large area (stitching)
  - MAPS with timing



- From 3T to ALPIDE (thanks to dpw and CMOS…)
  - Both sensor and R/O improved



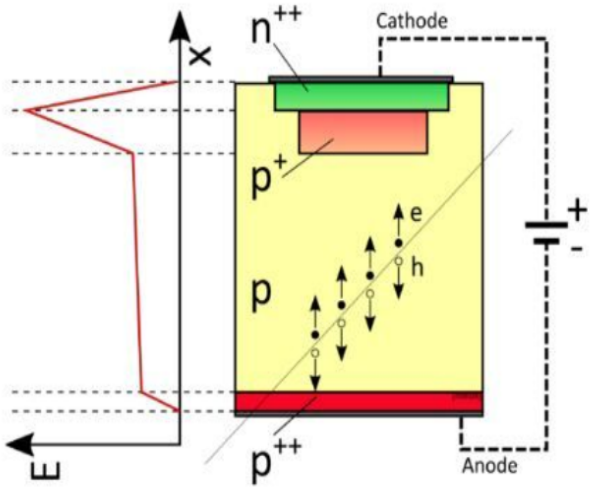


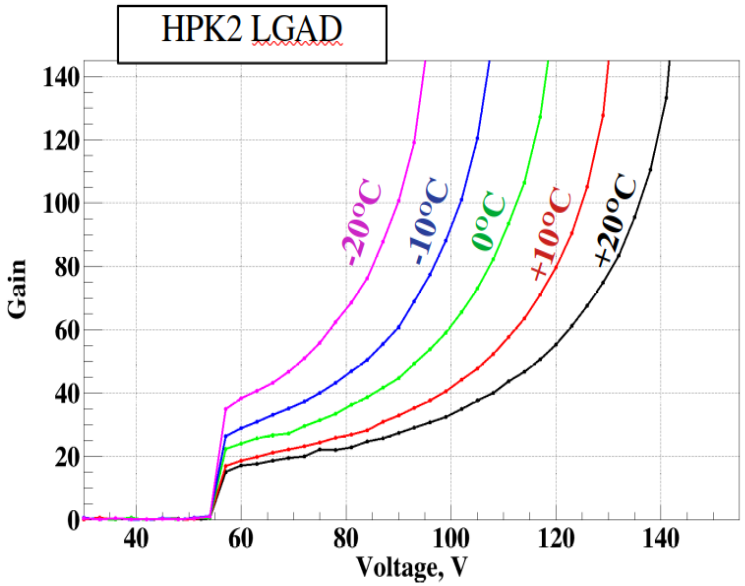


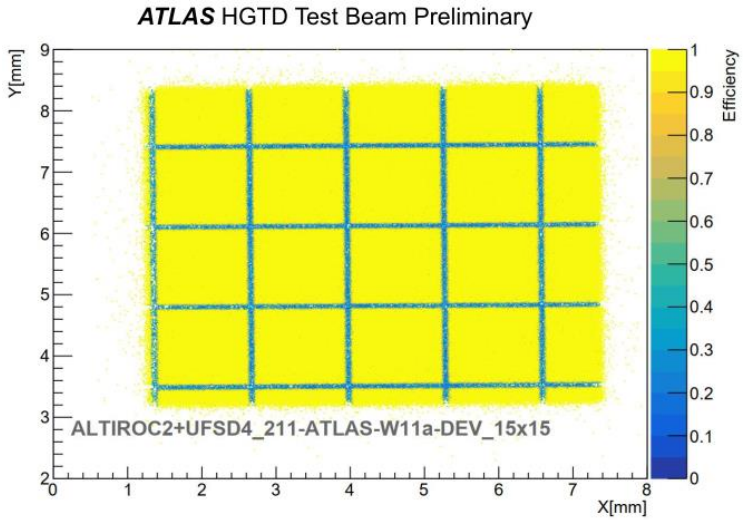
New detectors : LGADs

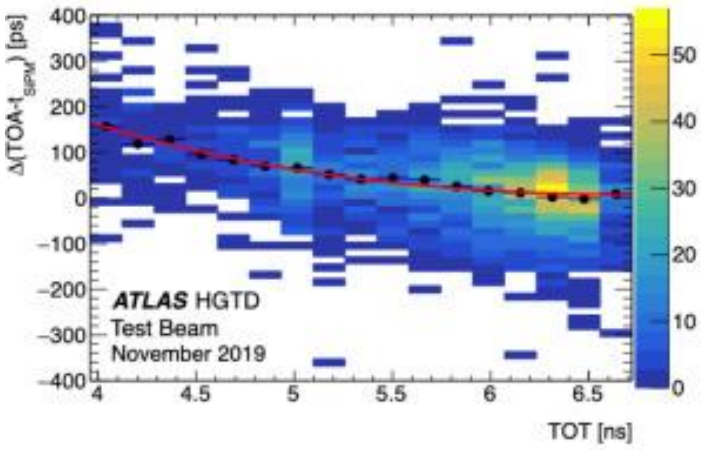
- Low-gain avalanche diodes
- Allow ~30 ps MIP timing detectors

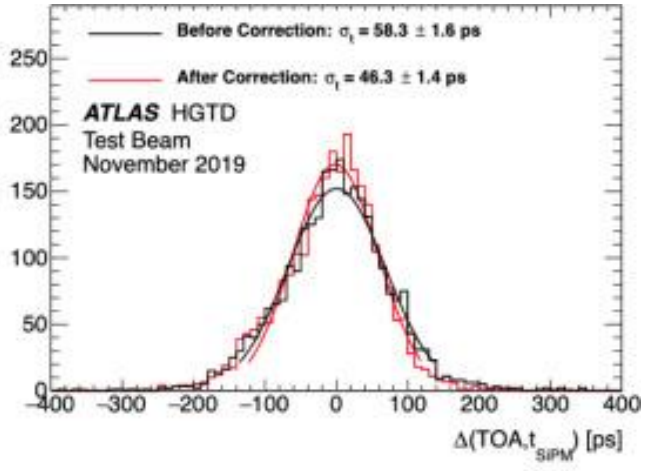
- Future
  - improved radiation hardness
  - AC LGADs







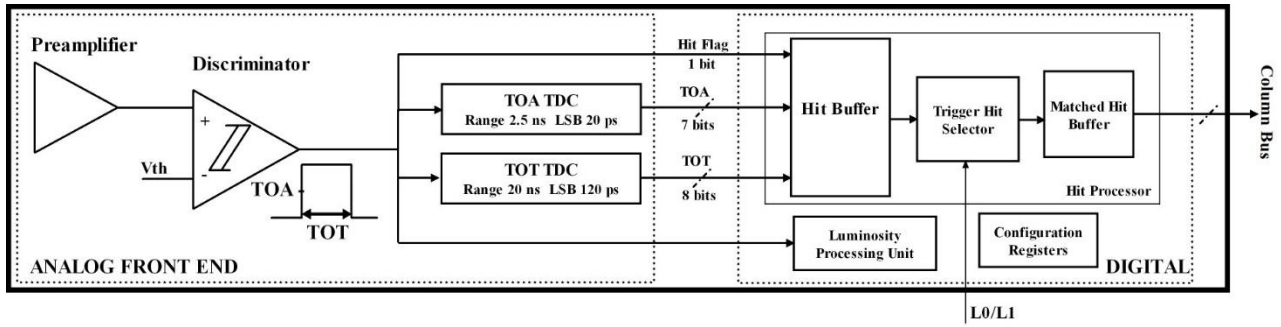




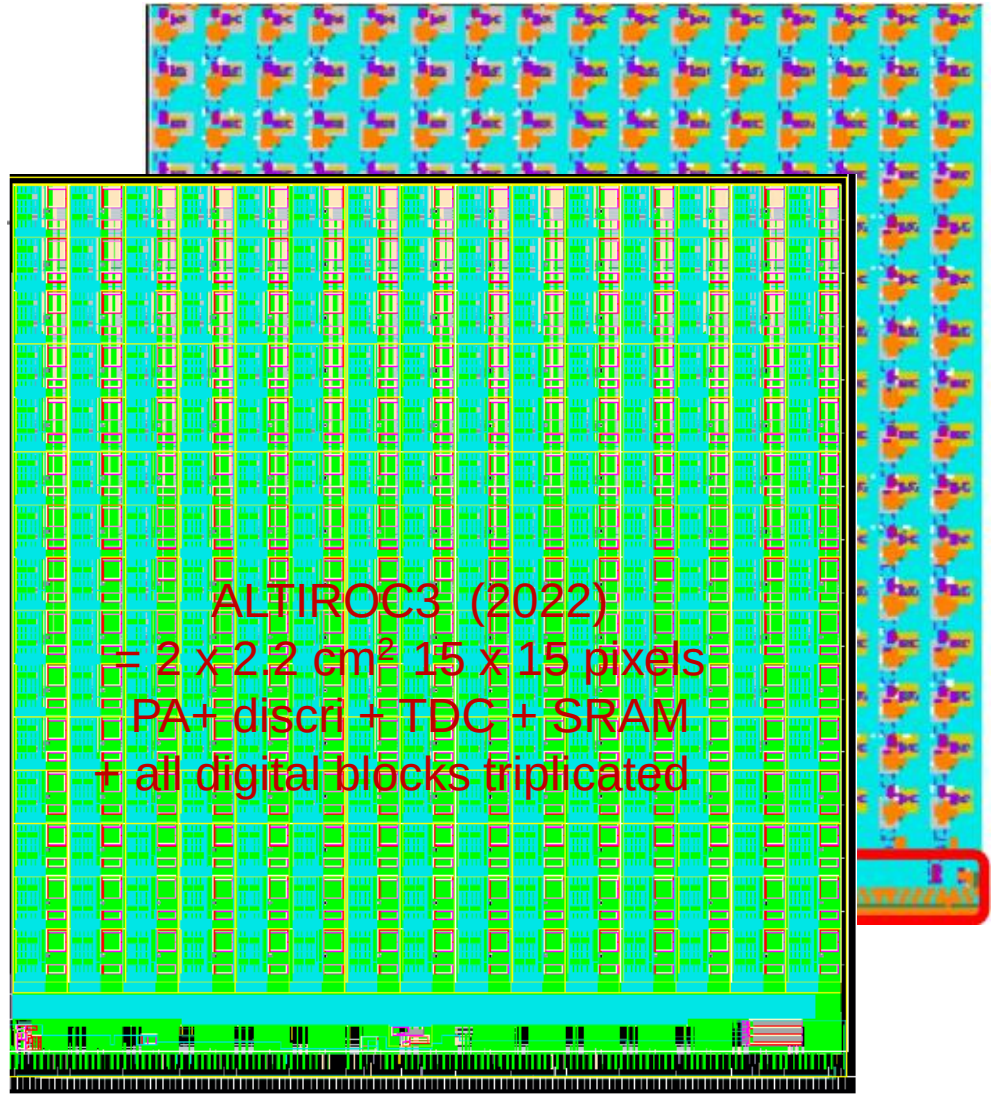
https://www.sciencedirect.com/science/article/pii/S0168900222002005

LGAD electronics

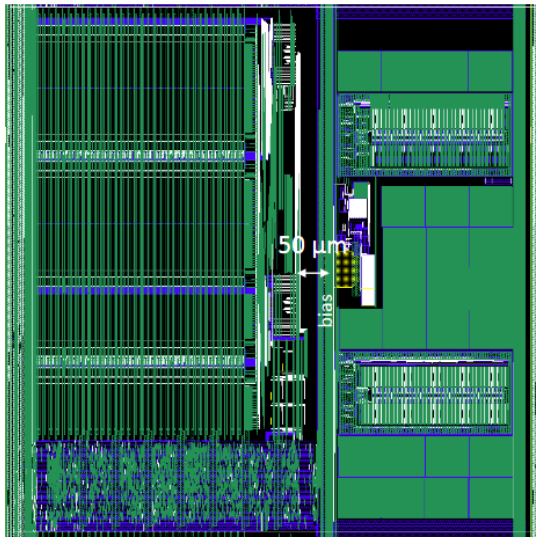
- ALTIROC (ATLAS) /ETROC (CMS) : (1.3mm)² pixels



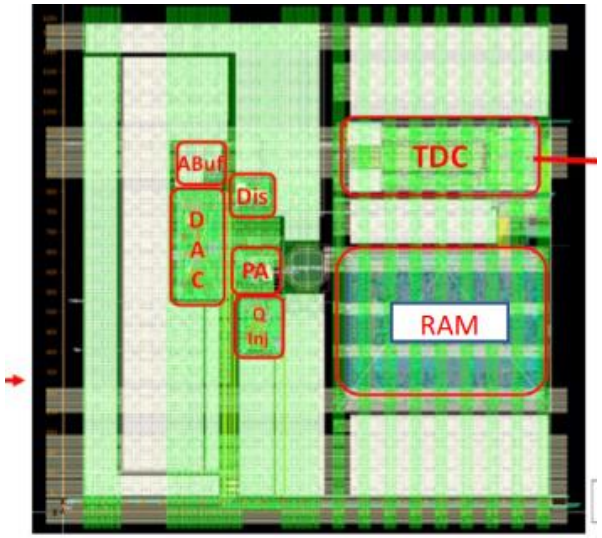
ETROC2 (2022)



ALTIROC2 pixel (130n)



ETROC2 pixel (65n)

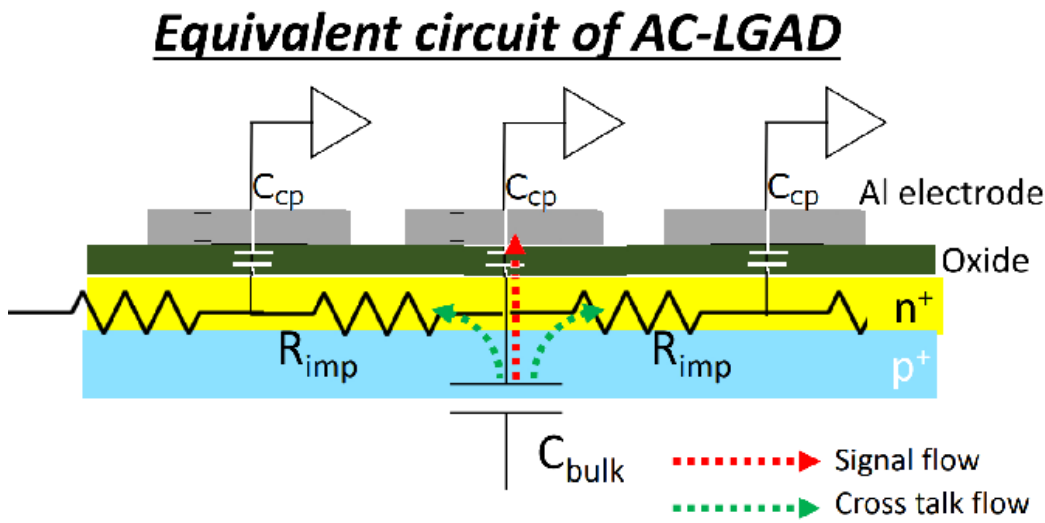


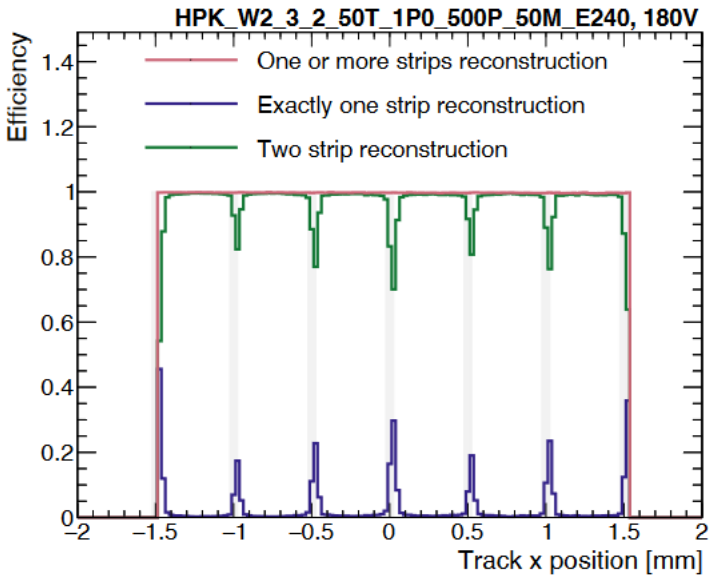
M. Casado et al. https://www.sciencedirect.com/science/article/pii/S0168900222002005

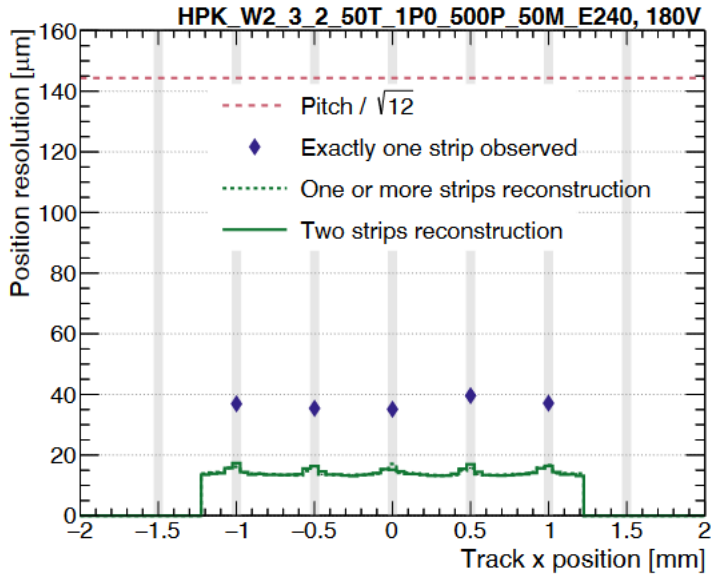
T Liu et al. (FNAL) https://indico.fnal.gov/event/22041/contributions/65917/attachments/41462/50166/ETROC-plan.pdf

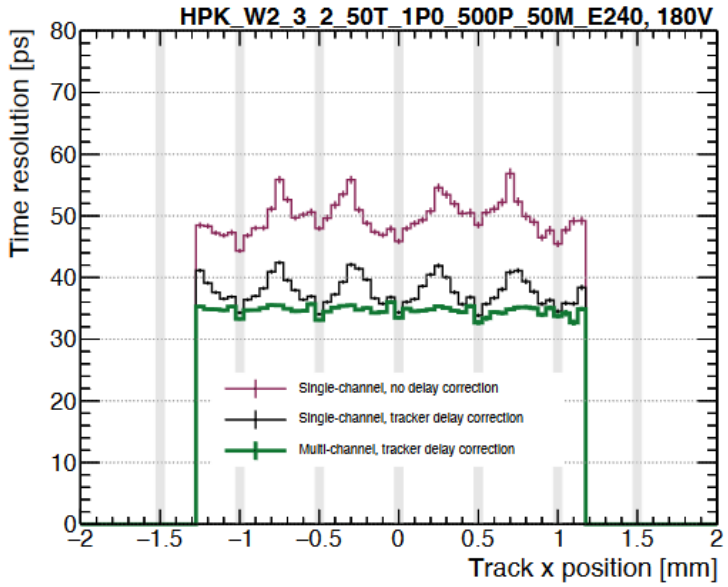
New detectors : AC-LGADs

- Introduced by N. Cartiglia et al. (~2015)
- Combines timing and spatial resolutions
- Already adopted by EIC for PID !









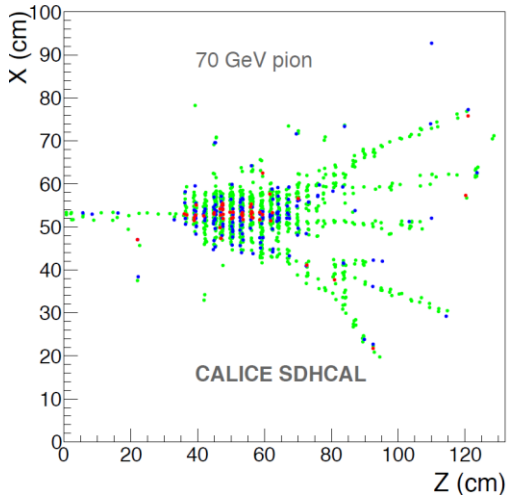
[S. Nanda et al. https://indico.bnl.gov/event/20473/contributions/85062/attachments/51842/88660/AC-LGAD_ePIC_vFinal.pdf]

Trends for calorimeter readout (DRD6)

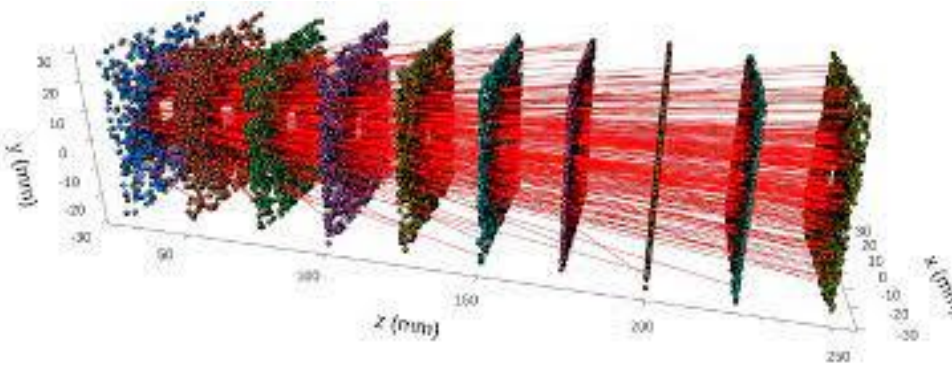
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : lower power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added



- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

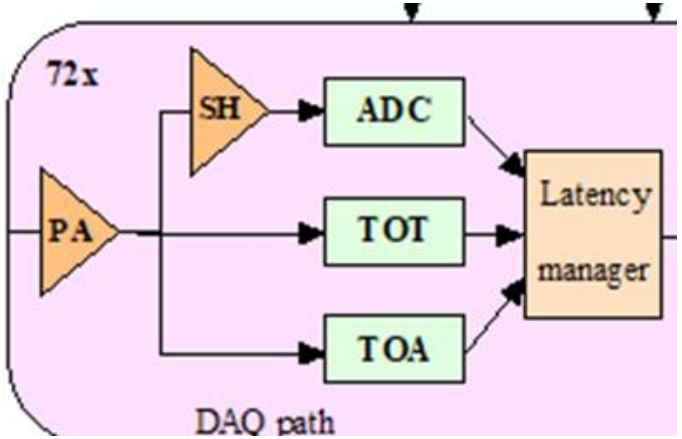


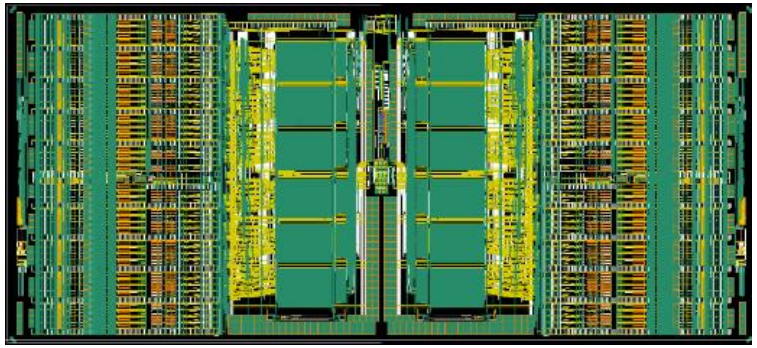
Embedded ASICs

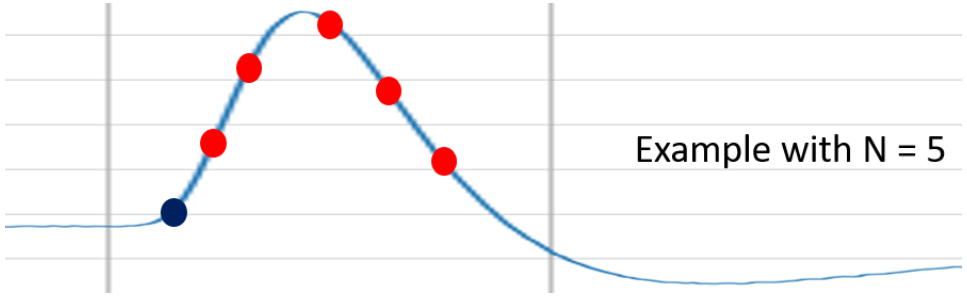
- Pioneered with CALICE R&D (SKIROC, SPIROC..)

- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)

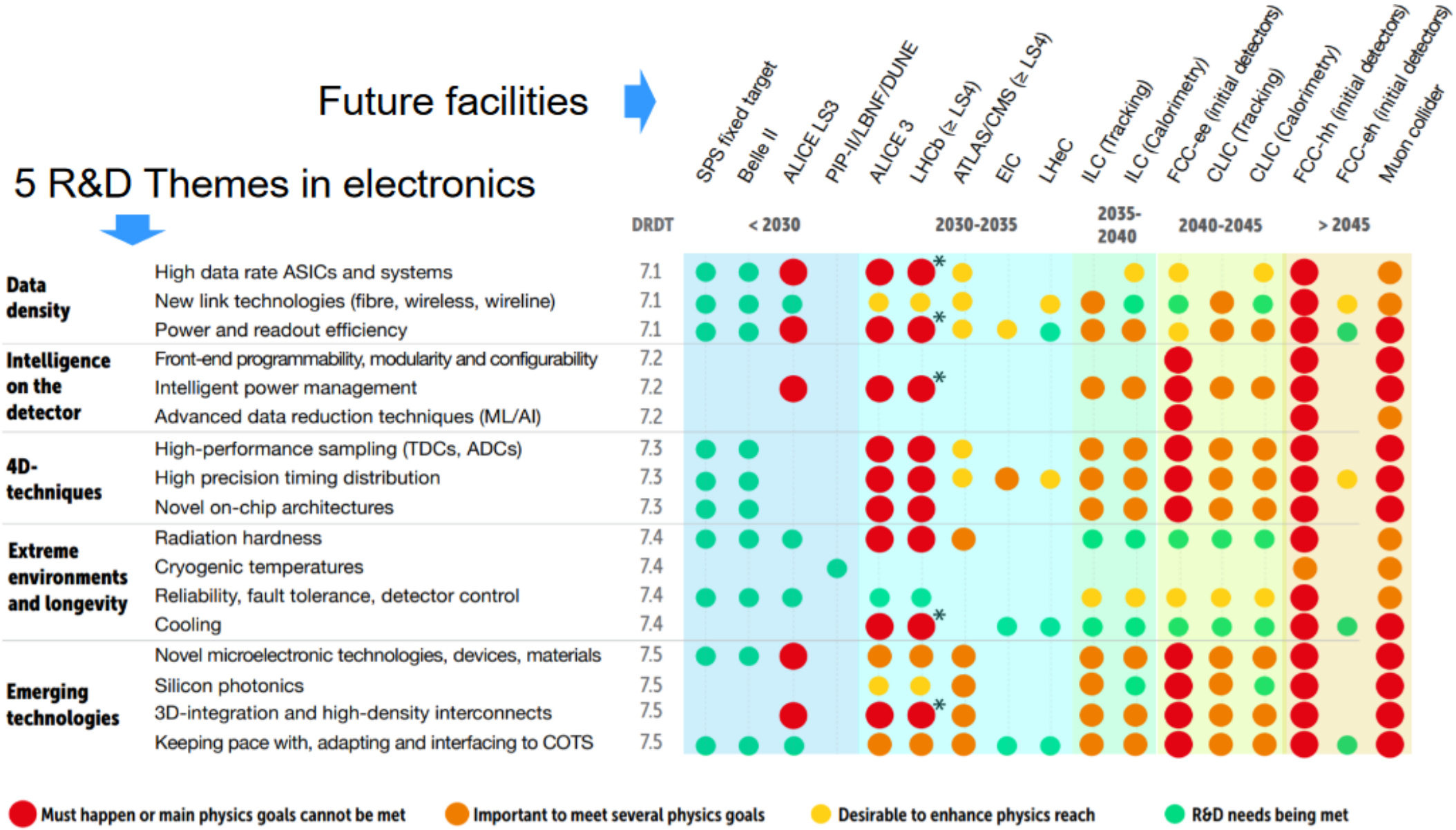
- Difficulties
  - Analog/digital couplings





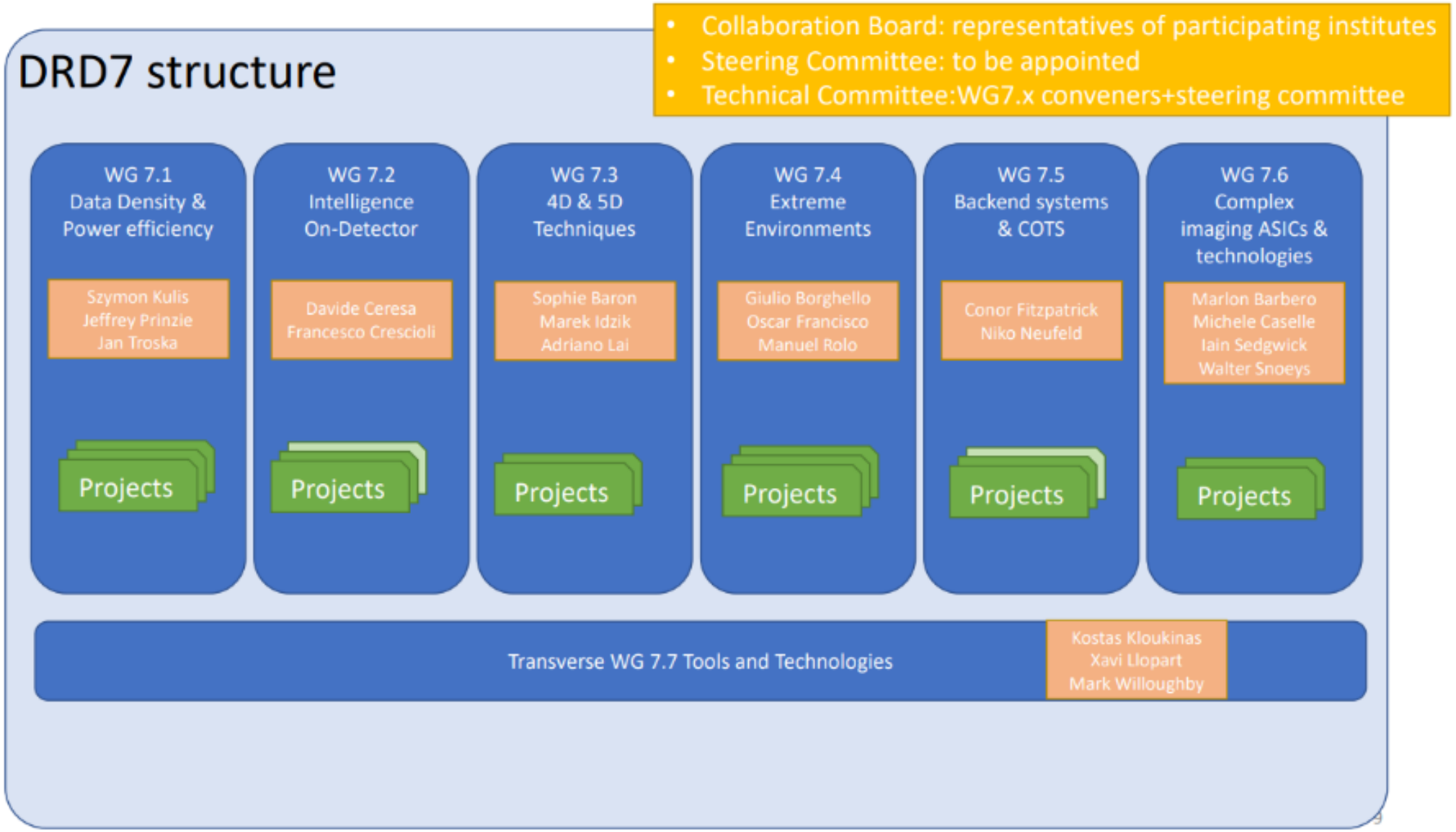


ICFA DRD7 : electronics



[F. Vasey et al. https://indico.slac.stanford.edu/event/8288/contributions/7684/attachments/3651/10115/DRD7_CPAD_9Nov23_Vasey.pdf]

DRD7 electronics



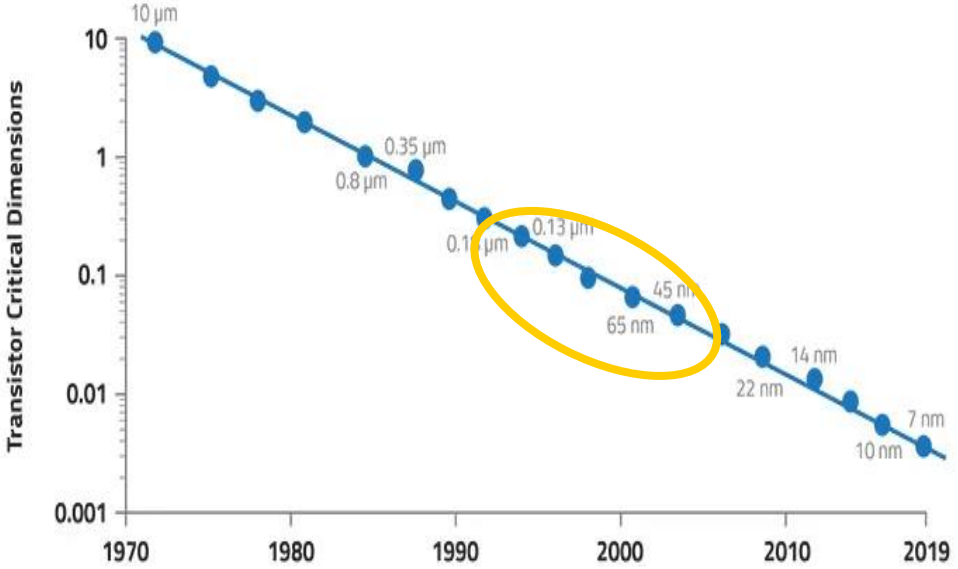
c4. Interface with other DRDs

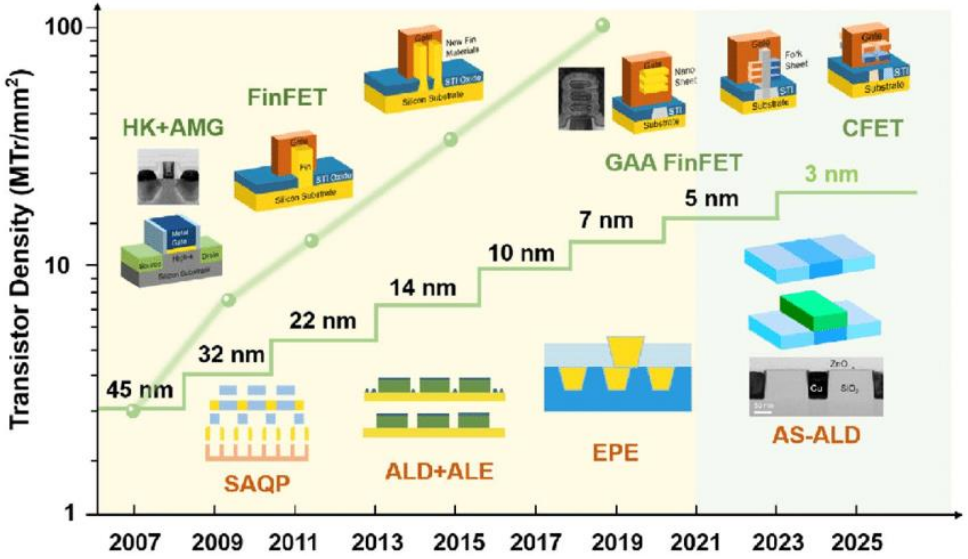
DRAFT, under discussion

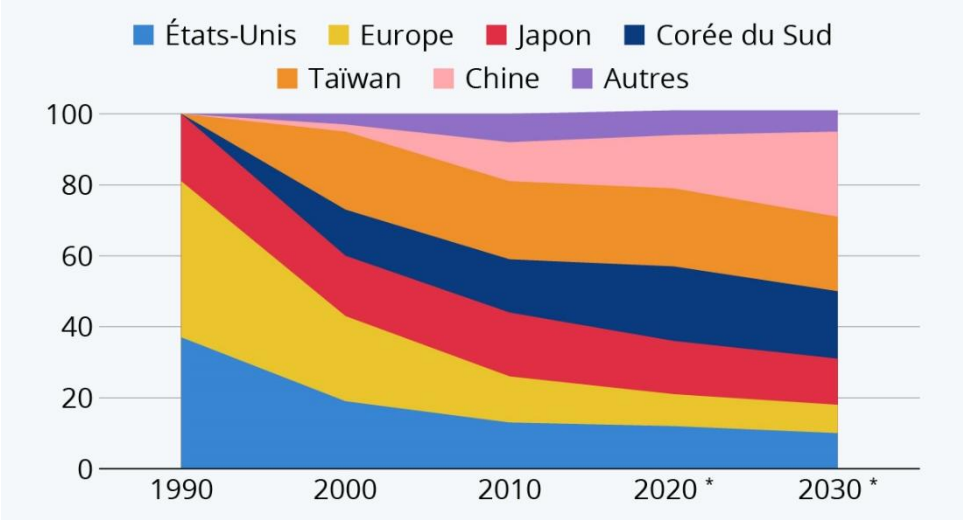
- R&D in electronics is not carried out in isolation
  - Many engineers will be active in both DRD-specific projects and DRD7 generic R&D
  - DRD-specific projects will take care of
    - Determination of system parameters and specifications
    - Planning and costing of prototype development and production
    - Production, verification, and integration of ASICs and other project-specific components
    - Testing and operation of large-scale prototypes
  - DRD7 projects will
    - Review system specifications and design as requested, possibly also on a rolling basis during the course of the project, and including analysis of engineering effort and specialised skills requirements
    - Provision access to tools and vendors
    - Develop and provision common IP, components, and subsystems, encompassing hardware, firmware and software
    - Develop common, generic, complete components or systems, when too big or too complex to be designed in one single DRD
    - Provision specialised or large-scale facilities for electronic development and testing

Evolution of technologies

- Evolution of CMOS technologies : more and more complex and expensive
  - Applies essentially to digital (consumer) electronics





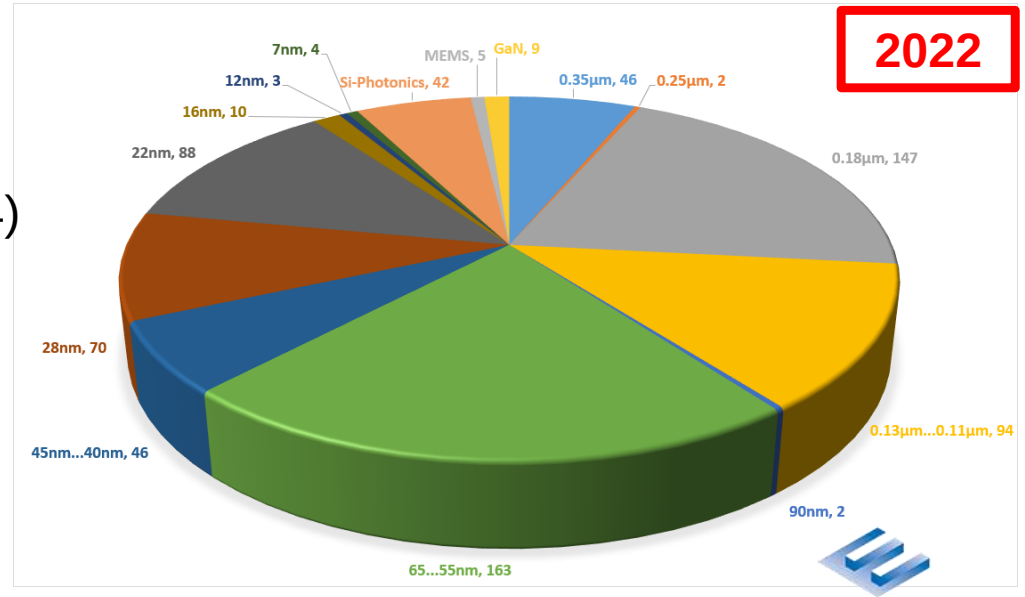


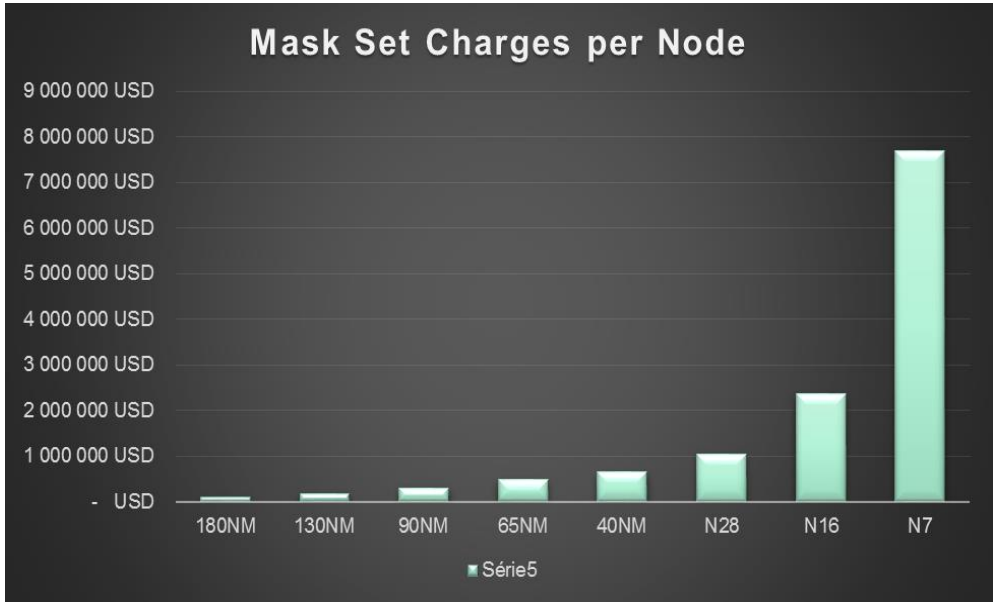
Technology choice for mixed-signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

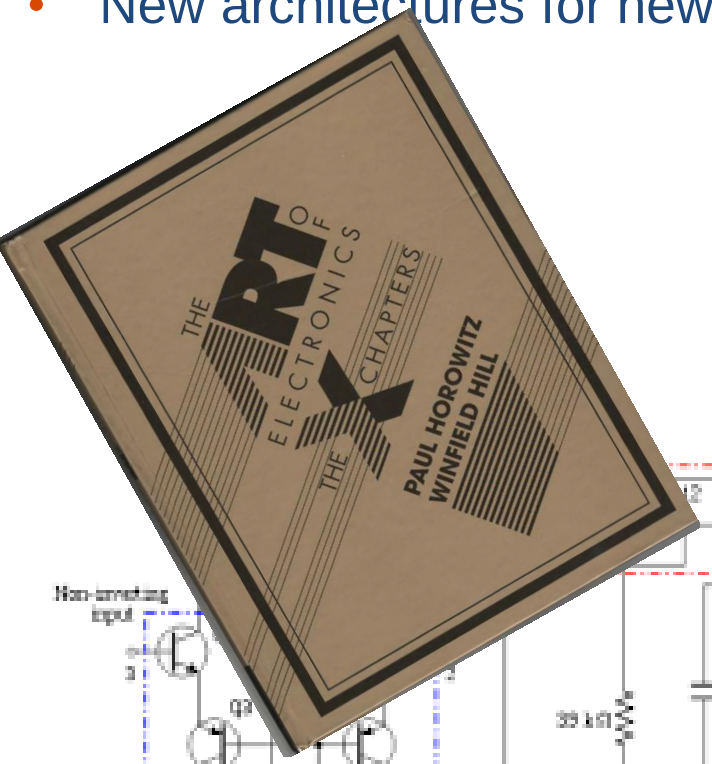
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run

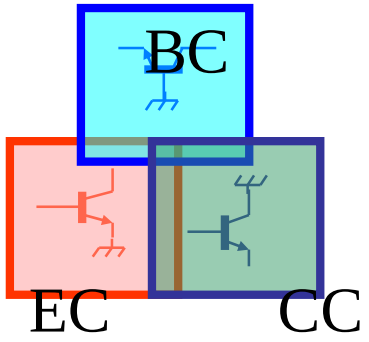


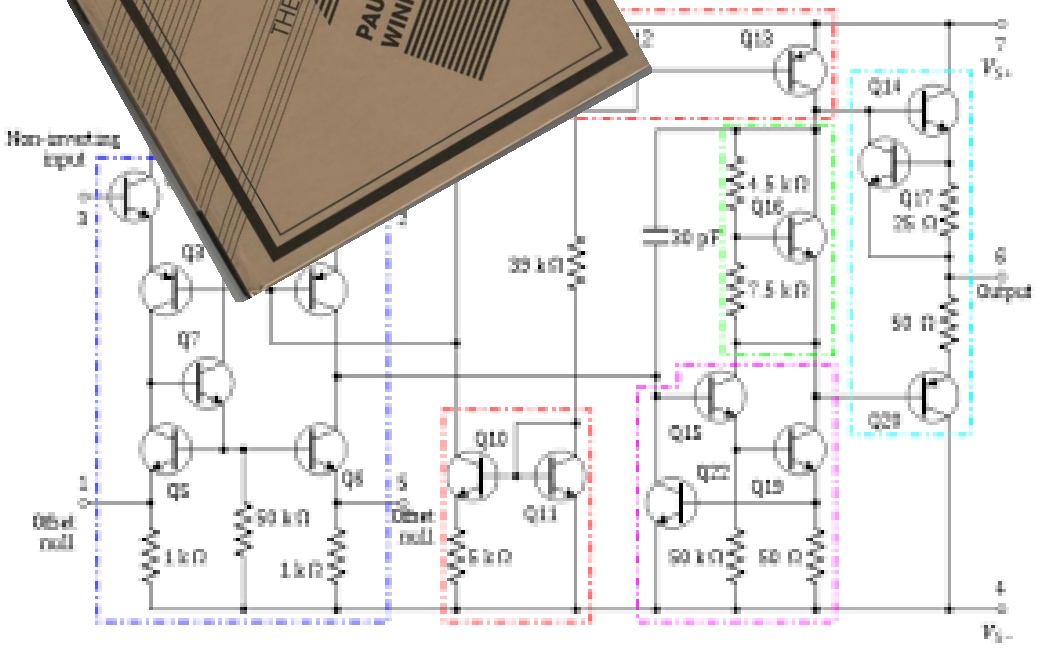


Why it is a research area?

- Research area : publications/thesis/conferences, similar to detectors/accelerators/computing
- « The Art of electronics » : creativity and innovation
- New architectures for new detectors





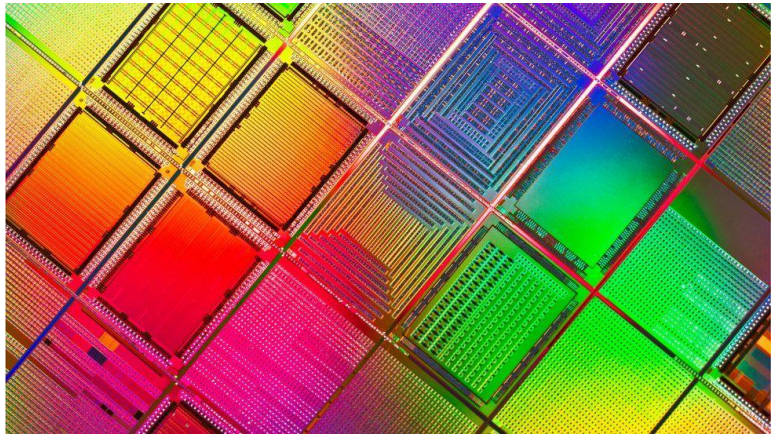


« The Art of Electronics »

- Will AI replace the designers ?

Conclusion

- New sensors regularly appear (SiPMs, LGADs….)
  - Unforseenable
  - Electronics quickly follows…
  - Detectors quickly adopt them
- Sensors and electronics are a joint development
  - Overall optimization (segmentation, pulse shape…)



- Electronics benefits from technology evolution (CMOS scaling) but not that much !
  - Lower dissipation for digital electronics
  - Smaller impact on analog blocks
  - Big jump for HL-LHC with SoC and timing
- Future detectors will have lower rates (until FCC hh…)
  - Emphasis now probably more on low power to improve granularity, data-driven, reduced material…
  - Probably also more on timing
  - Smaller step compared to HL-LHC
- R&D in DRDs and DRD7 for technological support