





# Electronics for future detectors

ILD workshop

Christophe de LA TAILLE 16 jan 2024

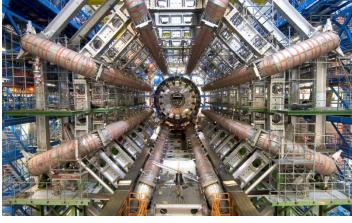
Organization for Micro-Electronics desiGn and Applications

#### **Evolution of experiments and technology**











Gargamelle 1970





CMS upgrade 2030





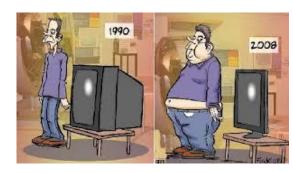




CdLT ILD workshop 16 jan 24



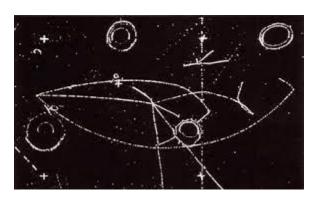


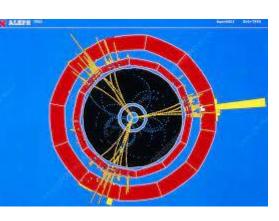


#### **Evolution of detectors and readout electronics**



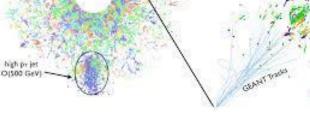
racks and clusters clearly stifable by eye throughout most of detector





ATLAS EXPERIMENT http://atlas.ch Run: 20362 Event: 82614360 Date: 2012-05-18 Tume: 20:265-18 Tume: 20:26511 (EST





CMS 2030

Gargamelle 1970

ALEPH 1990







		Contraction of the second second		
			and the second s	
1000000	State of the State of State	No. of Concession, Name	The Property lies	A REAL PROPERTY AND A REAL PROPERTY.
and a state of the	NET TO LOCAL STR	NUMBER OF STREET	LE REAL STREET	WELL COLUMN TRANSMENT
	STATISTICS OF			WITH MARKED AND ADDRESS
1 (111)				
COLUMN TWO IS	and the second second		STR STREET	A DECEMBER OF THE OWNER.
A Contractor		a second second	COLUMN TWO IS NOT	
		CONTRACTOR OF THE OWNER.	Salina Kinaki	NUMBER OF STREET, STRE
		1. R. R. R. M. M. M.	A REAL PROPERTY OF	A CONTRACTOR OF A CONTRACTOR O
	State State	Constant States	COLUMN TWO IS NOT	
			Contraction of the second s	A CONTRACTOR OF CONTRACTOR

.1

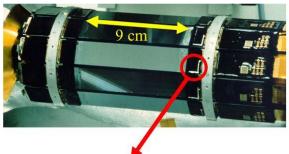


IMEP

-6102-42

B

#### MICROPLEX (1985)

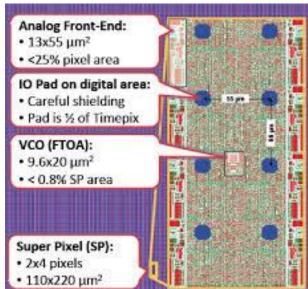


Silicon Strip Vertex Detector: MARK II experiment at SLAC Linear Collider (512 channels/module; 18K channels total)



Microplex readout chip 128 channels, 47.5 μm pitch (Walker, Parker, Hyams)

Parallel efforts in ALEPH, DELPHI, OPAL at LEP and CDF at the Tevatron Collider



#### TIMEPIX4 (2020)



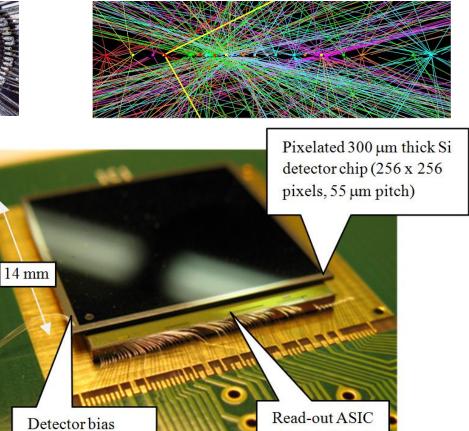


# Why we do our chips instead of buying them ?

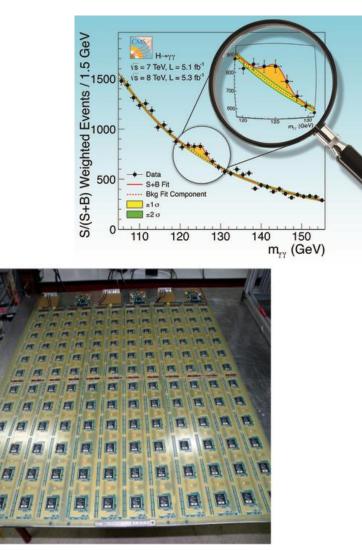
- ASIC = Application **Specific** Integrated Circuit
- Innovation in technology yields new/better detectors
- Specific requirements in HEP : physicists/designers interplay
- « No chip => no detector » => no experiment...

voltage (~100V)





chip Medipix2



mega

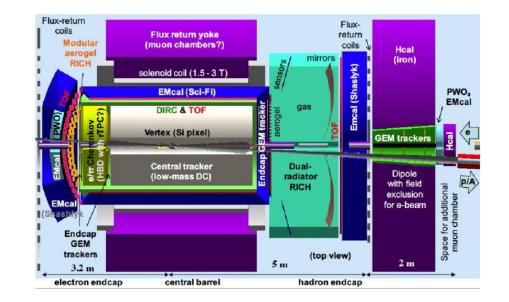
#### **Future detectors**

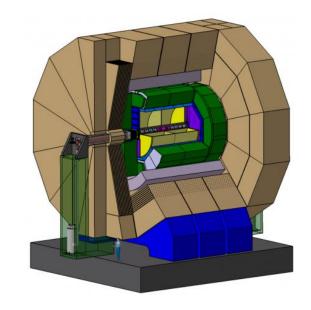
**O**mega

- New sensors regularly pop up...
  - SiPMs
  - MAPs

– LGADs, ACLGADs

- Electronics also regularly improves...
  - Technology evolution (CMOS scaling)
  - More functionnalities (timing)
  - Lower power
  - Allows electronics on detector, better granularity, timing...
- Progress from either or both !



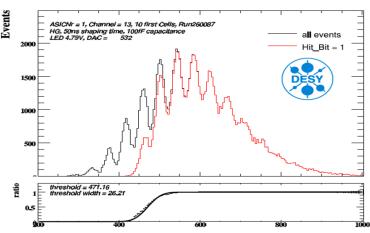


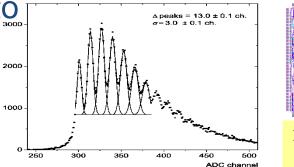
#### **New detectors : SiPMs**

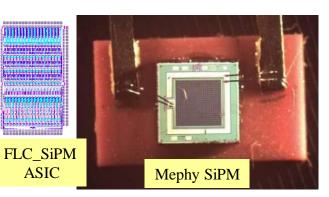
- From first MEPHY SiPMs (CALICE 2005) to HGCAL, TOFHIR, MU2E....
- Large progress in sensors (FBK, HPK...)
  - Lower dark noise
  - Better crosstalk
  - Larger area
- Future
  - Larger area
  - optimized SiPM/ROC (granularity for best timing)
  - « Picosecond challenge »



SiPM SPECTRUM with Autotrigger

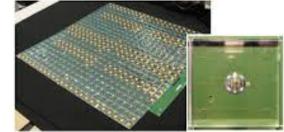






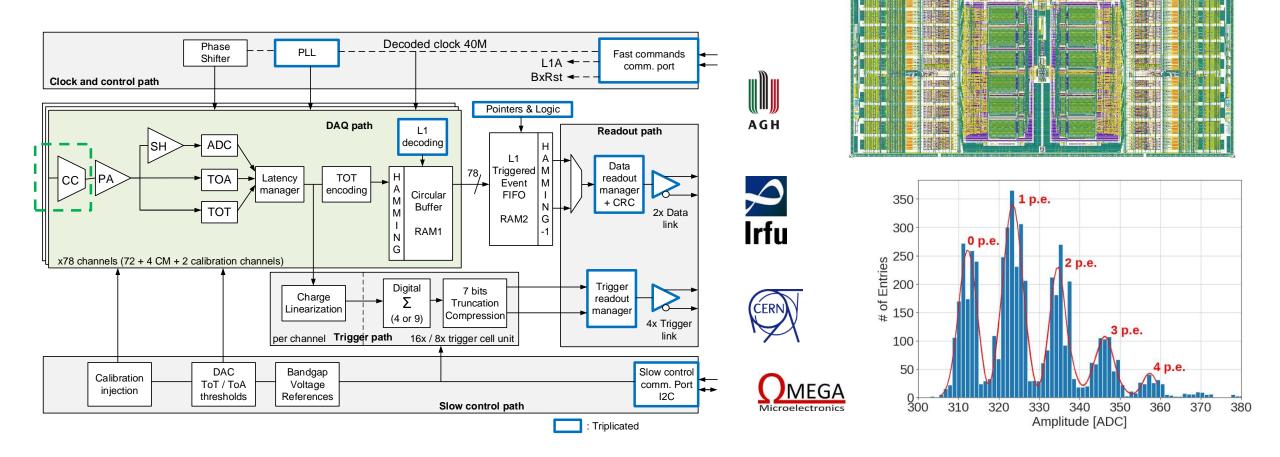


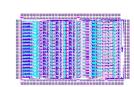




#### **SiPM electronics**

- From FLC-SiPM to H2GCROC, TOFHIR, FastIC...
- Preamps, ADCs, TDCs inside : SoC
  - Large dynamic range and few tens of ps timing





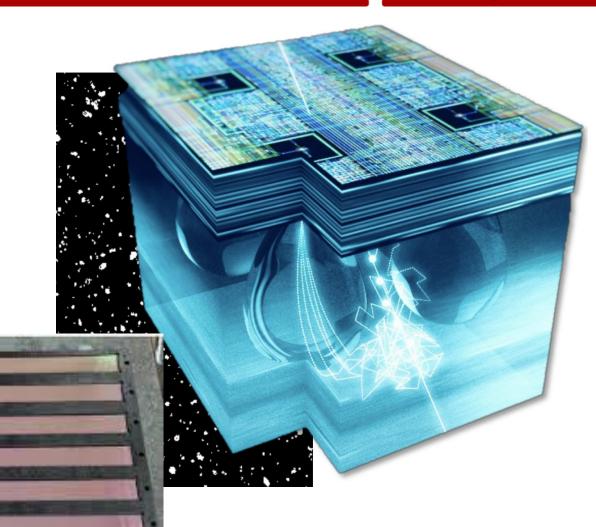


## **New detectors : MAPS** [see talk by M. Winter]

- Monolithic Active Pixels Sensors
- From MIMOSA to ALPIDE and MOSS
- Combined detector and readout electronics

MOSS

- Future
  - Large area (stitching)
  - MAPS with timing



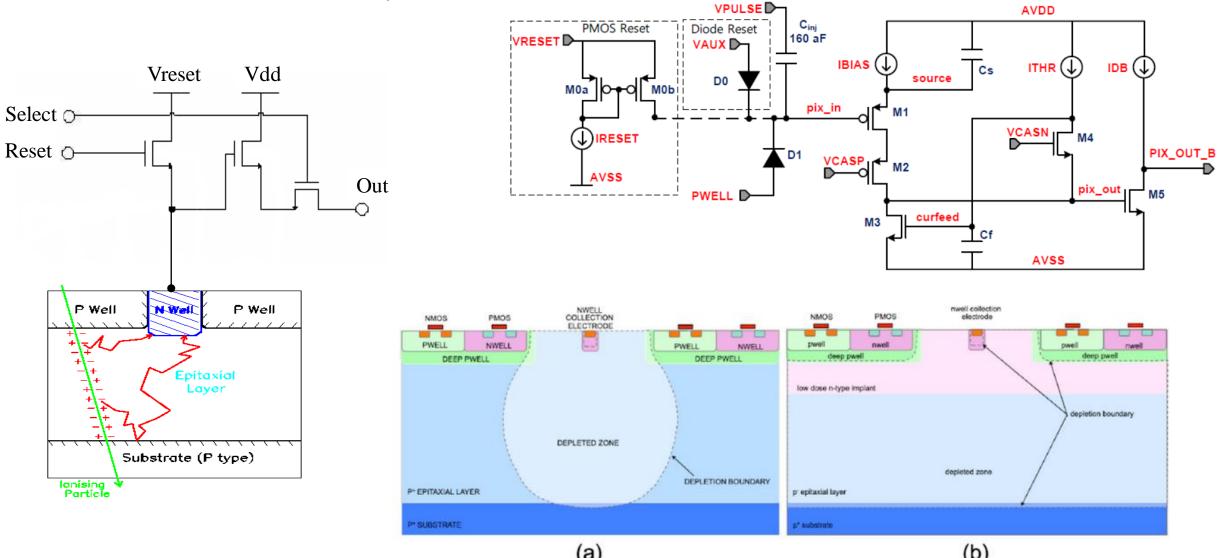
mega



#### **MAPs electronics**



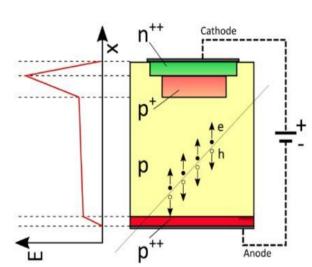
- From 3T to ALPIDE (thanks to dpw and CMOS...)
  - Both sensor and R/O improved

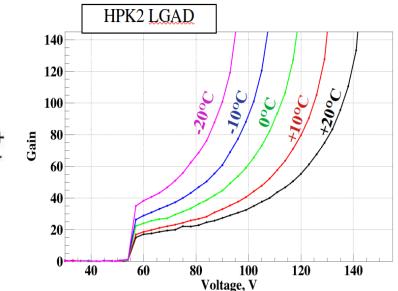


## **New detectors : LGADs**

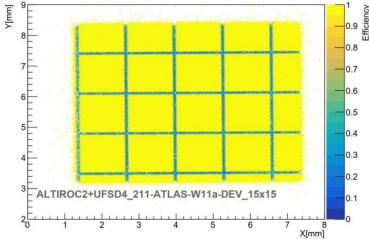


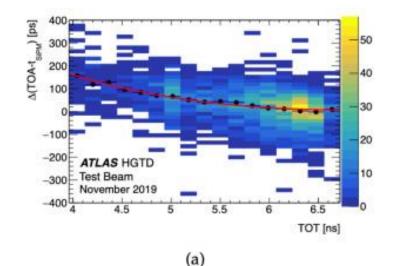
- Low-gain avalanche diodes
- Allow ~30 ps MIP timing detectors
- Future
  - improved radiation hardness
  - AC LGADs

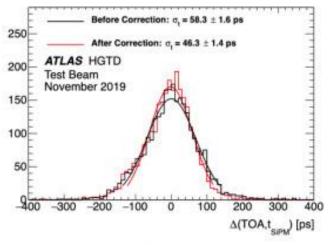




#### ATLAS HGTD Test Beam Preliminary







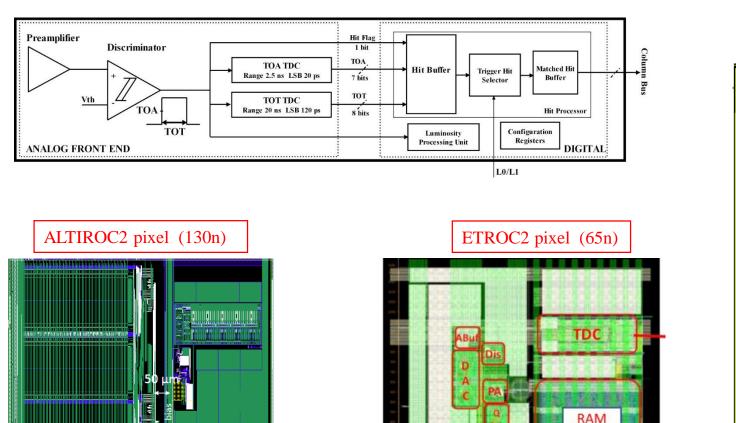
(b)

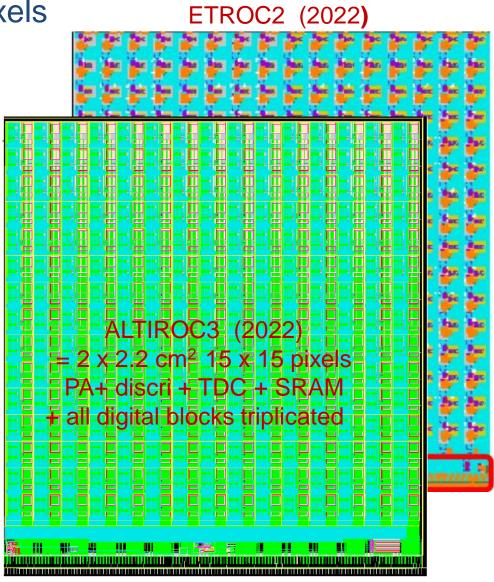
https://www.sciencedirect.com/science/article/pii/S0168900222002005

#### **LGAD electronics**



• ALTIROC (ATLAS) /ETROC (CMS) : (1.3mm)<sup>2</sup> pixels





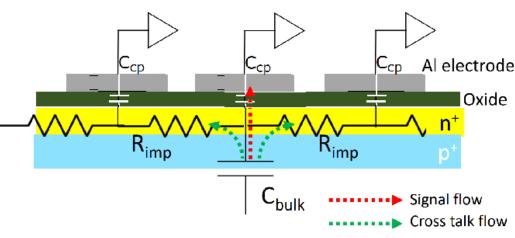
M. Casado et al. https://www.sciencedirect.com/science/article/pii/S0168900222002005 T Liu et al. (FNAL) https://indico.fnal.gov/event/22041/contributions/65917/attachments/41462/50166/ETROC-plan.pdf

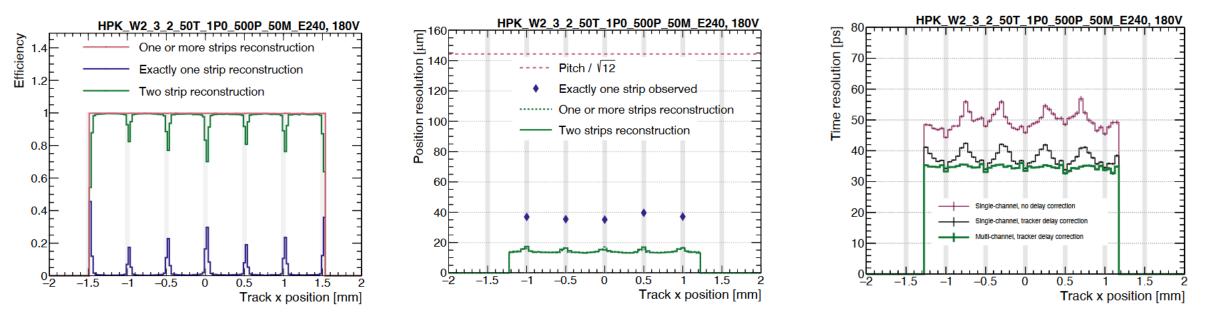
## **New detectors : AC-LGADs**



- Introduced by N. Cartiglia et al. (~2015)
- Combines timing and spatial resolutions
- Already adopted by EIC for PID !

**Equivalent circuit of AC-LGAD** 



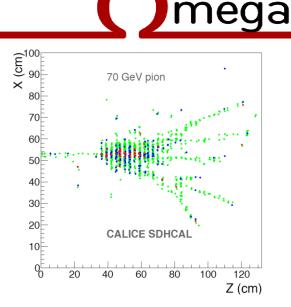


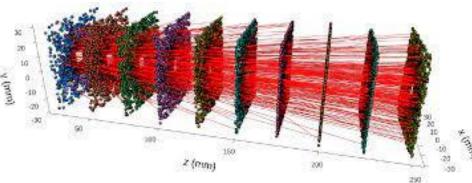
[S. Nanda et al. https://indico.bnl.gov/event/20473/contributions/85062/attachments/51842/88660/AC-LGAD\_ePIC\_vFinal.pdf]

- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC Lar, FATIC...
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider...
  - Challenges : lower power, data reduction
- Digital calorimetry : MAPs, RPCs...
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL...
  - Challenges : #channels, low power, data reduction

# **Digital calorimetry**

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm<sup>2</sup> pixels, low occupancy, ~1 mW/cm<sup>2</sup> (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added
- Electromagnetic : e.g. DECAL, ALICE FOCAL...
  - Based on ALPIDE :  $(30\mu m)^2$  pixels, high occupancy, ~ few 100 mW/cm<sup>2</sup>, slow
  - To be compared with embedded electronics ~10 mW/cm<sup>2</sup>
  - Most power in digital processing => would benefit a lot from < 28 nm node</li>
  - Semi-digital and/or larger pixels could be an interesting study

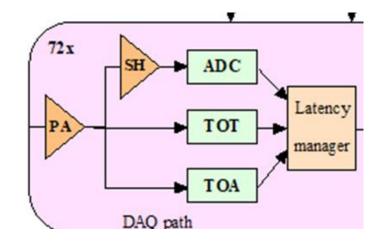


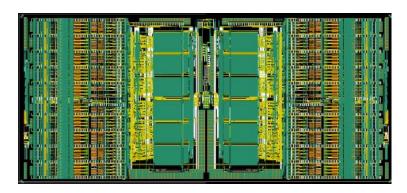


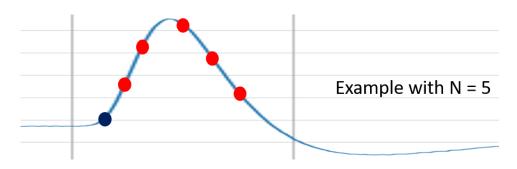
## **Embedded ASICs**

**O**mega

- Pioneered with CALICE R&D (SKIROC, SPIROC..)
- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)
- Difficulties
  - Analog/digital couplings









#### **Future facilities**

#### 5 DOD Thomas in clastronics

5 R&D	Future facilities	•	Sp.	Belle II age	AL	LHCE OUNE LHCDA OUNE ATASCASS	UC Maching	CCalorimenty) CC Celorimenty) CLIC (Tracus Celery) C. Tracus Celery	FCC hind and a second
-		DRDT		< 2030		2030-2035	2035- 2040	2040-2045	> 2045
Data density	High data rate ASICs and systems	7.1				•			
	New link technologies (fibre, wireless, wireline)	7.1				•	•	• • •	
	Power and readout efficiency	7.1				) 🌑 😐 😐 🔵	• •	• • •	
Intelligence on the detector	Front-end programmability, modularity and configurability	7.2				X			
	Intelligent power management	7.2					• •		
	Advanced data reduction techniques (ML/AI)	7.2							
4D- techniques	High-performance sampling (TDCs, ADCs)	7.3					• •		
	High precision timing distribution	7.3				) 🔴 🎈 🔴 🤞	• •		
	Novel on-chip architectures	7.3					• •		
Extreme environments and longevity	Radiation hardness	7.4					• •	• • •	
	Cryogenic temperatures	7.4				T			
	Reliability, fault tolerance, detector control	7.4							
	Cooling	7.4				) 🛑 🎽 🔹 🔹	• •	• • •	
Emerging technologies	Novel microelectronic technologies, devices, materials	7.5					• •		
	Silicon photonics	7.5		T			•		
	3D-integration and high-density interconnects	7.5					• •		
	Keeping pace with, adapting and interfacing to COTS	7.5		• • •	Ō		• •		

Must happen or main physics goals cannot be met

Important to meet several physics goals

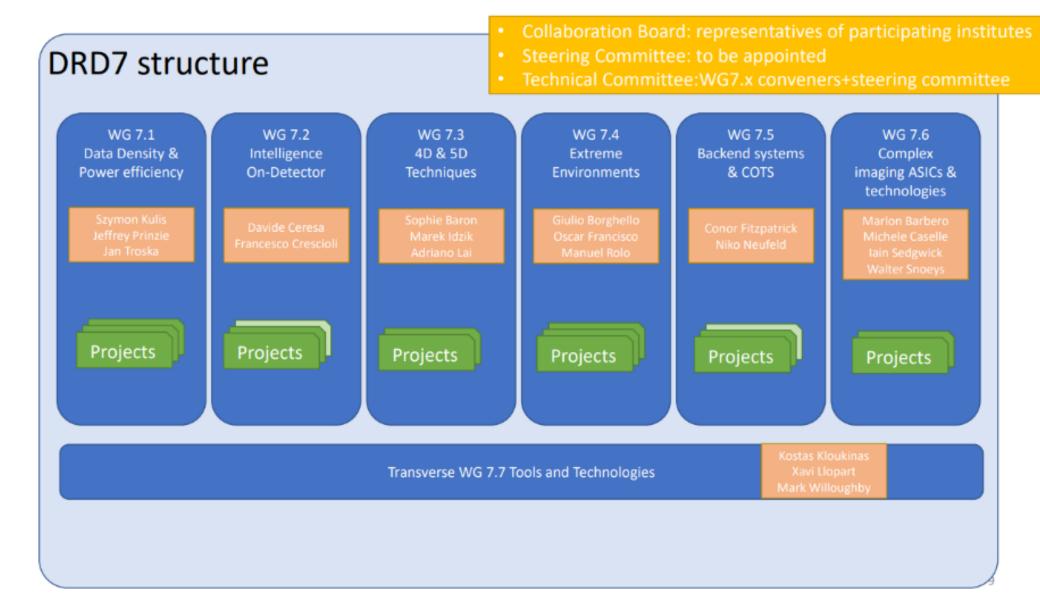
Desirable to enhance physics reach

🔵 R&D needs being met

[F. Vasey et al. https://indico.slac.stanford.edu/event/8288/contributions/7684/attachments/3651/10115/DRD7\_CPAD\_9Nov23\_Vasey.pdf]

CdLT ILD workshop 16 jan 24





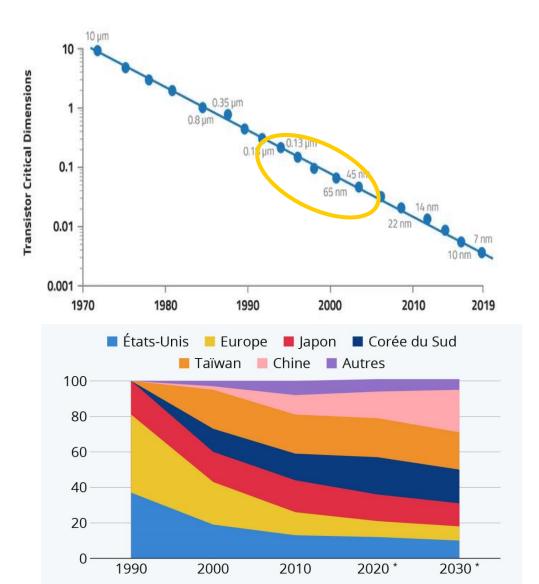


# c4. Interface with other DRDs

- R&D in electronics is not carried out in isolation
- DRAFT, under discussion Many engineers will be active in both DRD-specific projects and DRD7 generic R&D
  - DRD-specific projects will take care of
    - Determination of system parameters and specifications
    - Planning and costing of prototype development and production
    - Production, verification, and integration of ASICs and other project-specific components
    - Testing and operation of large-scale prototypes
  - DRD7 projects will
    - Review system specifications and design as requested, possibly also on a rolling basis during the course of the project, and including analysis of engineering effort and specialised skills requirements
    - Provision access to tools and vendors
    - Develop and provision common IP, components, and subsystems, encompassing hardware, firmware and software
    - Develop common, generic, complete components or systems, when too big or too complex to be designed in one single DRD
    - Provision specialised or large-scale facilities for electronic development and testing

# **Evolution of technologies**

- **O**mega
- Evolution of CMOS technologies : more and more complex and expensive
  - Applies essentially to digital (consumer) electronics

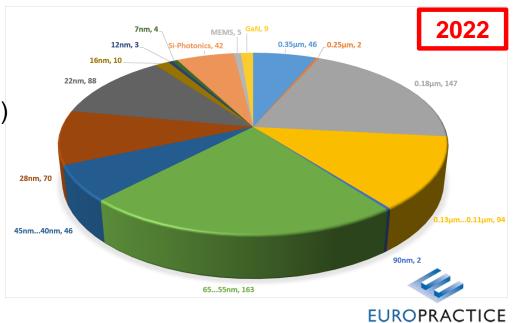


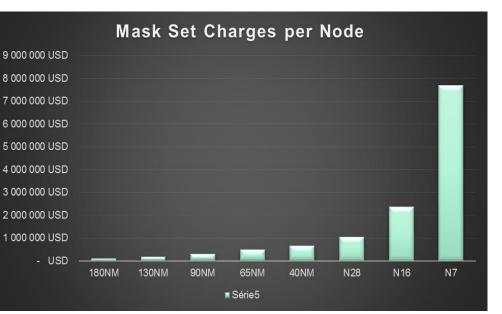




## **Technology choice for mixed-signal ASICs**

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm<sup>2</sup> MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?
- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm<sup>2</sup>, 700-800 k€/ engineering run
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm<sup>2</sup>, 1-1.5 M€/ eng run

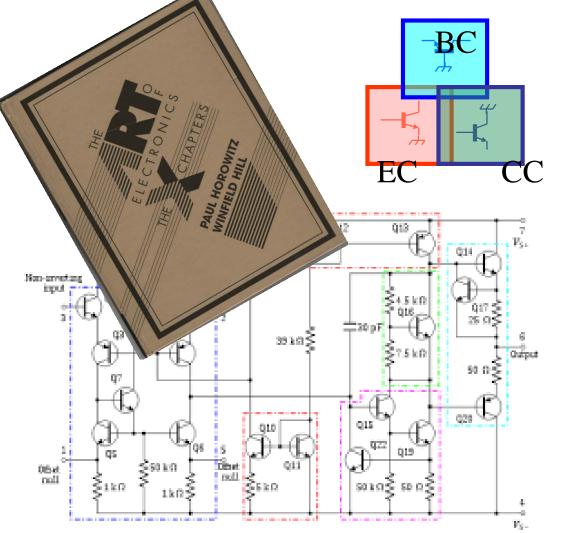






# Why it is a research area?

- Research area : publications/thesis/conferences, similar to detectors/accelerators/computing
- « The Art of electronics » : creativity and innovation
- New architectures for new detectors







mega







• Will AI replace the designers ?

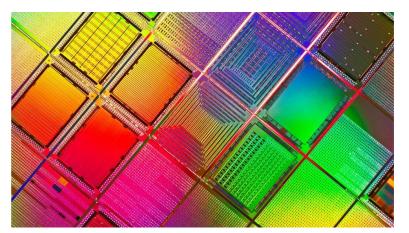






# Conclusion

- New sensors regularly appear (SiPMs, LGADs....)
  - Unforseenable
  - Electronics quickly follows...
  - Detectors quickly adopt them
- Sensors and electronics are a joint development
  - Overall optimization (segmentation, pulse shape...)



ega

- Electronics benefits from technology evolution (CMOS scaling) but not that much !
  - Lower dissipation for digital electronics
  - Smaller impact on analog blocks
  - Big jump for HL-LHC with SoC and timing
- Future detectors will have lower rates (until FCC hh...)
  - Emphasis now probably more on low power to improve granularity, data-driven, reduced material...
  - Probably also more on timing
  - Smaller step compared to HL-LHC
- R&D in DRDs and DRD7 for technological support