CMOS PIXEL SENSORS for TRACKING DEVICES at FUTURE HIGGS-TOP-EW FACTORIES : WHERE DO WE STAND ? WHAT CAN WE ANTICIPATE ? WHICH RELEVANCE for ILD ?

Marc Winter, IJCLab-Orsay, ILD meeting, CERN (15-17 January 2024)

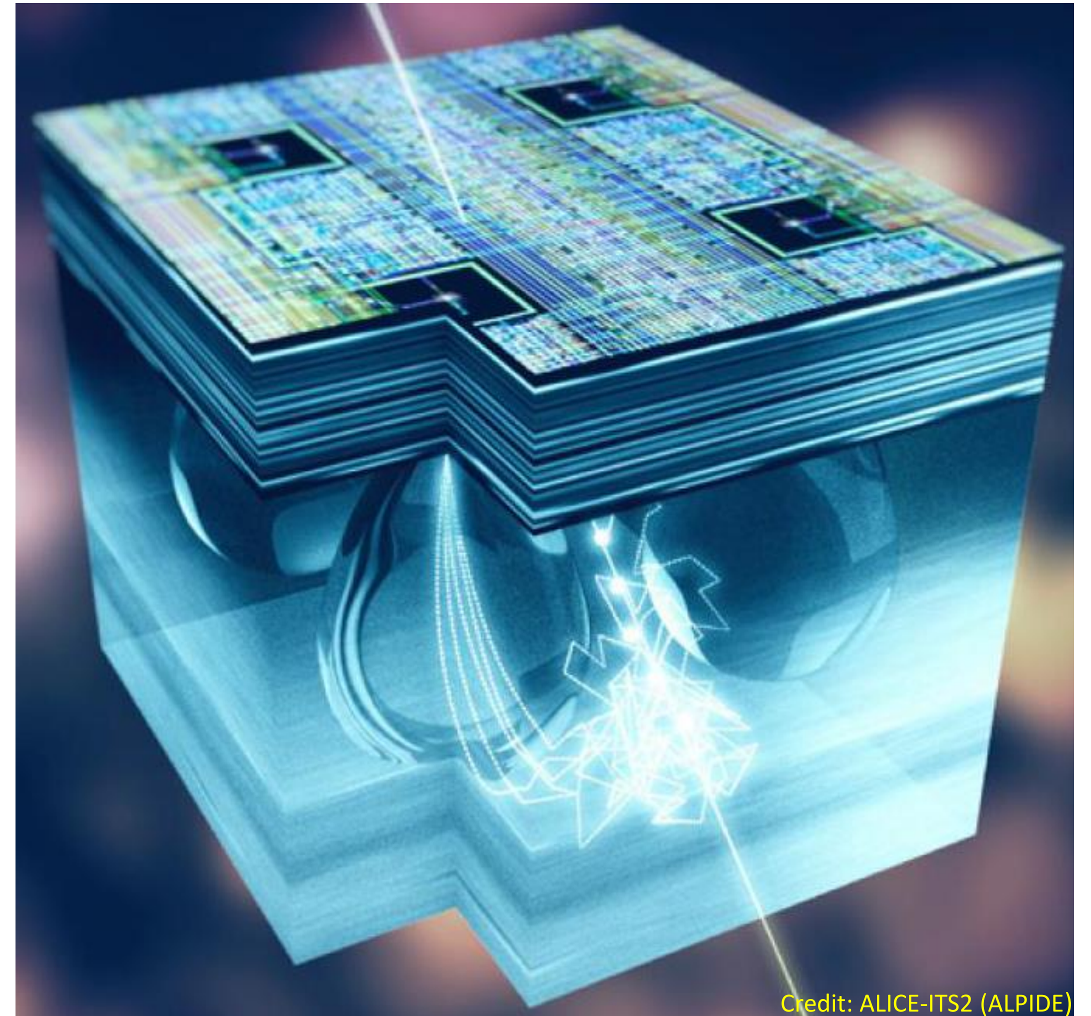
Reminder:
- some characteristic features of CMOS Pixel Sensors (CPS)
- illustrative set-ups/concepts based on CPS

Most advanced CMOS process: TPSCo 65 nm imaging technology

Generic development of the 65 nm sensors:
- R&D for fast and radiation tolerant sensors
  (main drivers: HL-LHC → FCChh)
- R&D privileging suppressed material budget and spatial resolution
  (main drivers: H.I. e.g. ALICE-ITS3, CBM-MVD, Belle-II -> Higgs-Fact)

ALICE-ITS3 project:
- Sensor developed for the ITS3 vertex detector
- **Salient features coming out from R&D on:**
  CMOS-65, stitching, system integration

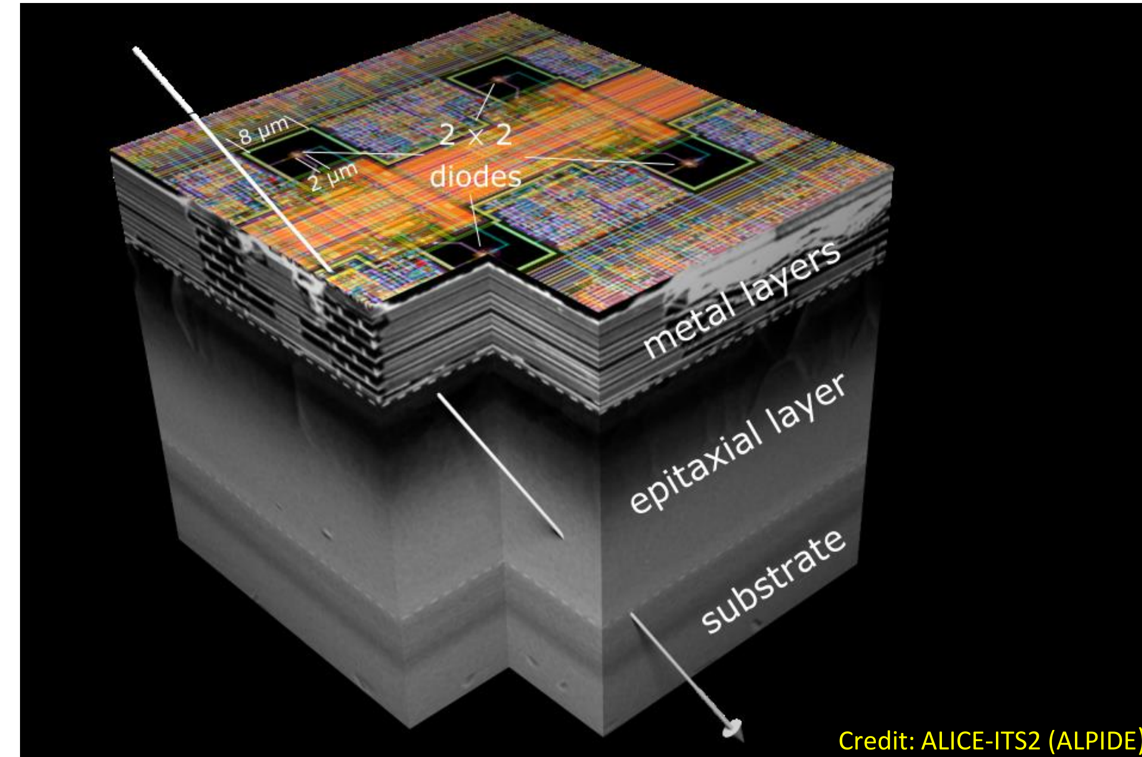
Other collaborative frameworks of R&D:
- DRD-TF*X* = 3, 7.6, 8 ; CERN-EP WP 1.2, 4 , …
- CBM, Belle-II, Mu3e, eIC, …



Numerous CMOS sensors in use or development: some general features

- Main asset: μ-circuits (steering, r.o., slow control) integrated on thin sensing substrate ➔ Monolithic & Thin (& T_{room})
- Numerous developments of custom design CMOS Pixel Sensors (CPS) on-going for vertexing and tracking devices foreseen to equip experiments at existing infrastructures (LHC, KEK, PSI, …) and future colliders (eIC, FAIR, FCCee, CEPC, C3, …)
- Some R&D for ECAL
- Optimisation imposes hierarchising conflicting requirements:

  Spatial resol. / Timing / Mat. budget (power) / Rad. Tol. / Hit rate
- Dependence on CMOS process (foundry) characteristics
- Frameworks: CERN-EP, DRD, ITS3 (main driver for Higgs factories: 65 nm techno with stitched curved sensors)
- 3 predominent foundries: TJsc, TPSCo, L Foundry
- System Integration is crucial for realistic detector optimisation:
  - Air cooling at which price ?
  - Services ➔ impact on FW region ?
  - Impact on choice of sensor technology and design ?



Numerous CMOS Sensors in Use or Development (illustrative sub-sample)

Name	Expt	Sub-syst	Area	Δ Pos., Time	Power (fid.)	Technology	Comment
ALPIDE	ALICE-ITS2	Vx & In. Trkr	10 m²	5 µm, ≤ 10 µs	≤ 50 mW/cm²	TJsc 180 nm EPI	In operation
MOSAIX	ALICE-ITS3	Vx only	0.12m²	5 µm, 2-10 µs	≤ 40 mW/cm² ?	TPSco 65 nm EPI	Wafer scale CPS
FASTPIX	→ HL-LHC	Demonstr.		≥ 1 µm, ≤ 100 ps	+++	TJsc 180 nm EPI	Timing & Rad. Tol.
MonoPix	→ ATLAS	ITk	few m²	< 10 µm, ≤ 20 ns	> 0.5 W/cm²	TJsc 180 nm EPI	Not retained
CACTUS	FCC, eIC, …	Timing det.		< 100 ps	300 mW/cm²	LF 150 nm	R&D proto.
MALTA	HL-LHC, …	Fast det.	few m²	36x40 µm², 25 ns	> 100 mW/cm²	TJsc 180 nm EPI	512x512 pixels
MIMOSIS	CBM/FAIR	Vx & In. Trkr	0.16 m²	5 µm, 5 µs	< 100 mW/cm²	TJsc 180 nm EPI	Fixed target HI expt
TaichuPix	CEPC	Vx & In. Trkr		≤ 5 µm	90-160 mW/cm²	TJsc 180 nm EPI	8x8 µm² n-well
NAPA	SiD/C3	Trkr, (calo.)		7µm pitch, O(ns)	20 mW/cm²	TPSCo 65 nm EPI	Target values
ARCADIA	IDEA/FCCee	Vx & In. Trkr		10-50 µm		LF 110 nm	Working horse
CLICpix	CLICdp	Vx & In. Trkr		25 µm pitch, 10 ns		TPSCo 65 nm EPI	Follows TimePix
OBELIX	Belle-II	Vx (7 layers)	O(1) m²	≤ 10 µm, ≤ 100 ns	≈ 200 mW/cm²	TJsc 180 nm EPI	Follows MonoPix
MuPix	Mu3e expt	Vx & Trkr		≤ 30 µm, ≤ 20 ns	≤ 350 mW/cm²	HV TJsc 180 nm	Fixed target expt

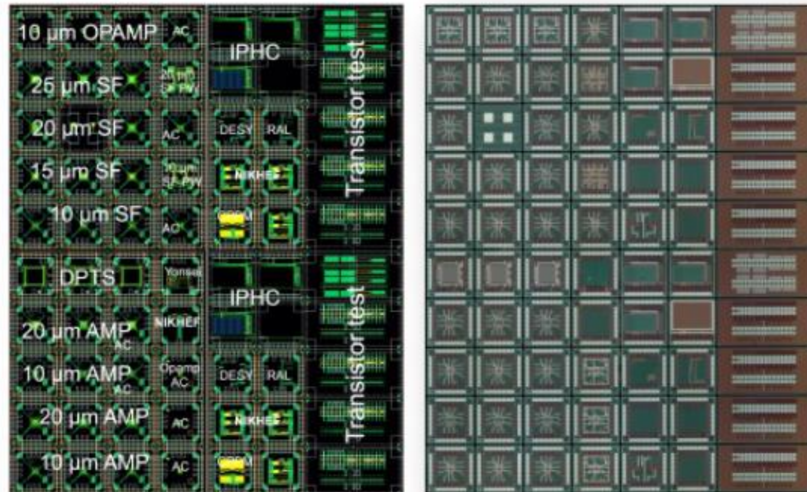
TPSCo 65 nm Technology

ECFA
European Committee for Future Accelerators

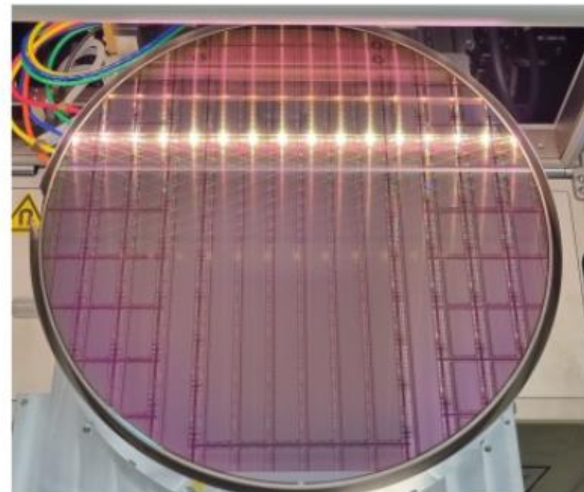
DRD7.6

TPSCo 65nm

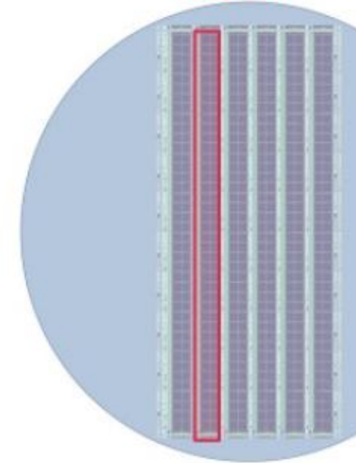
- Currently in use for ALICE ITS3 and EP R&D WP1.2
- Joint runs already carried out – MLR1, ER1
- CERN, IPHC, INFN, NIKHEF, STFC, SLAC, DESY, SLAC, Yonsei…



MLR1 (December 2020): 1.5 x 1.5 mm² test chips



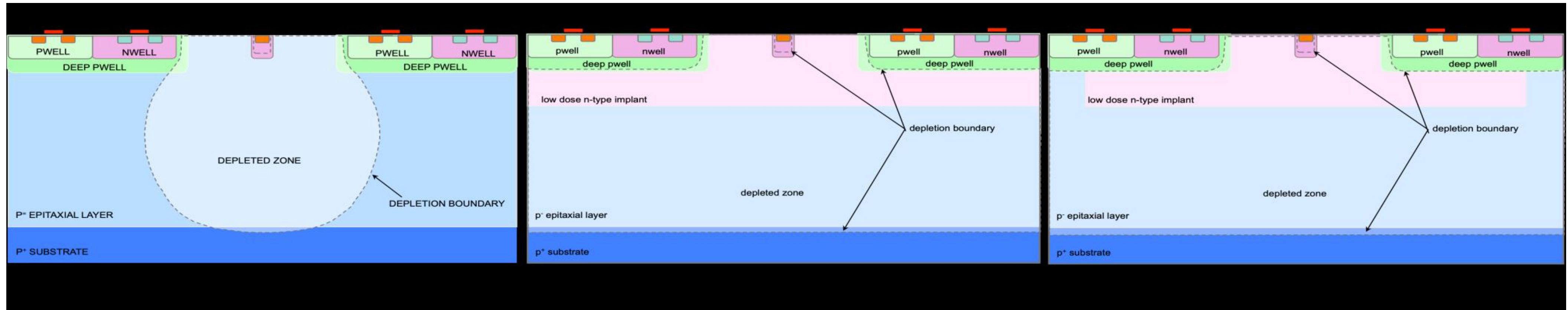
26cm long single silicon object



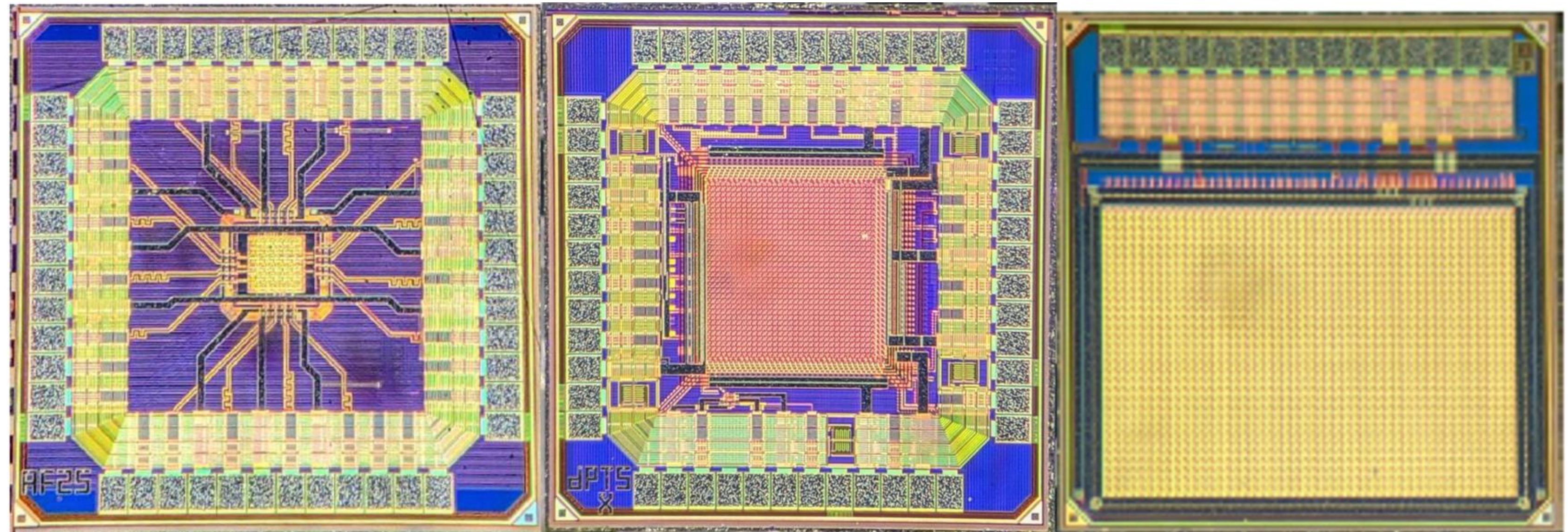
ER1 (December 2022): stitching

TPSCo 65 nm Prototyping for the ALICE ITS-3 Vertex Detector

MLR-1 run (2021): Analog & Digital output prototypes with 10-25 µm pitch & 3 epitaxial layer doping profiles



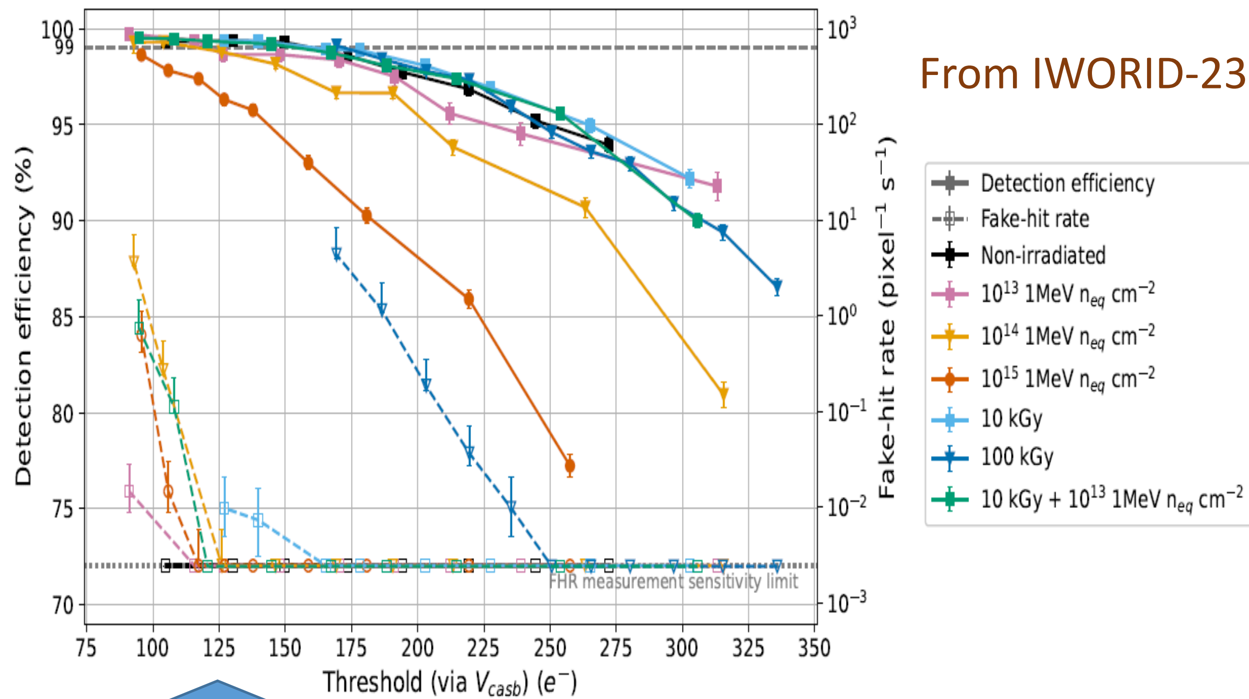
Technology validation & Detection Performance assessment based on 3 different Mini-sensors & various Test structures



APTS: analog output DPTS: digital output CE-65: analog output

MLR1 TEST RESULTS

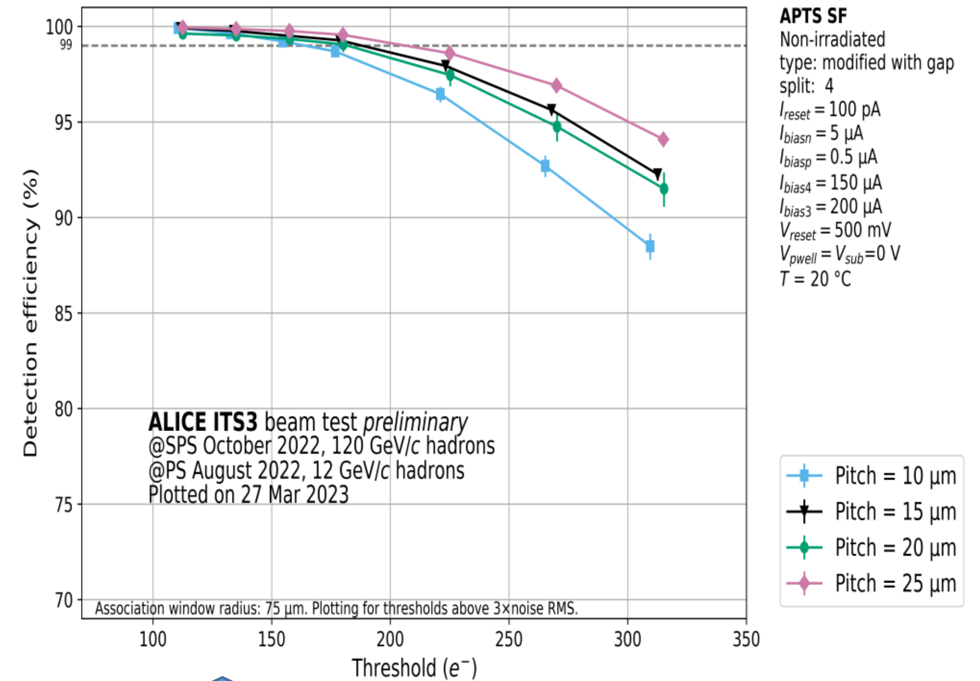
DPTS (15 µm pitch) Detection Efficiency versus NIEL and TID



From IWORID-23

Operation regime

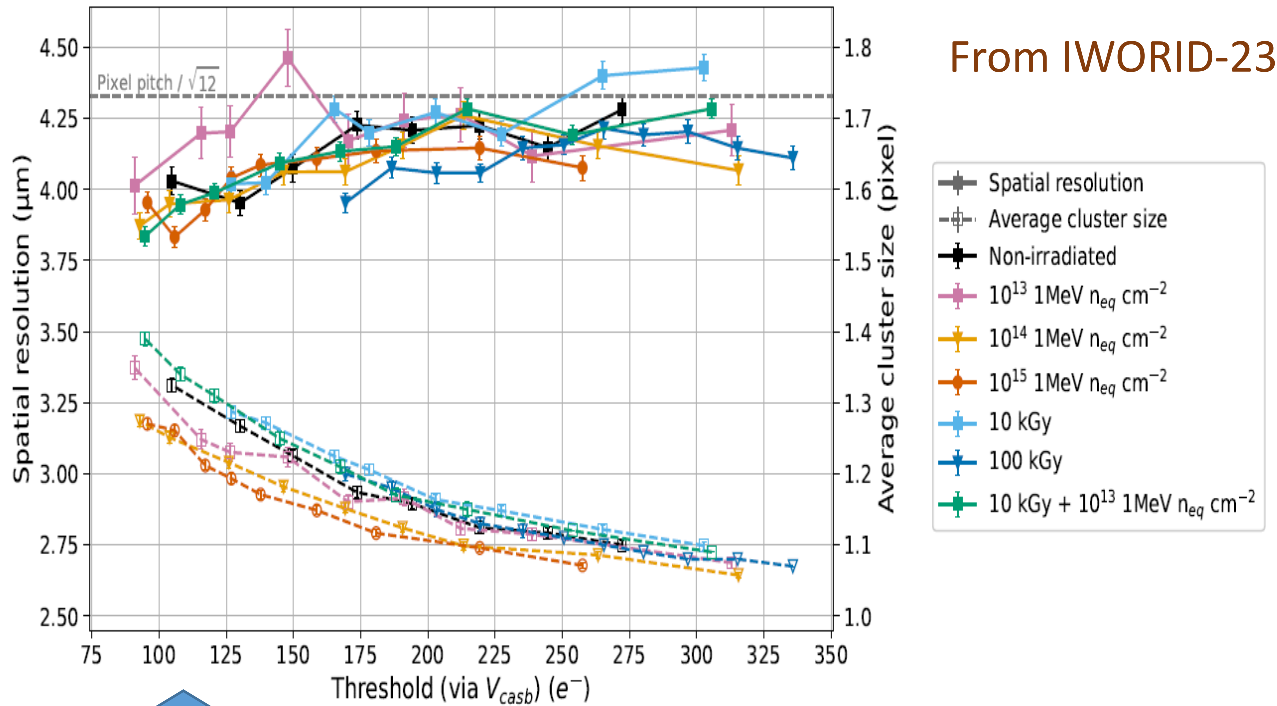
APTS Detection Efficiency for a pitch of 10, 15, 20, 25 µm



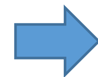
Operation regime

MLR1 TEST RESULTS: Spatial Resolution & Cluster Size

DPTS (15 µm pitch) vs NIEL and TID

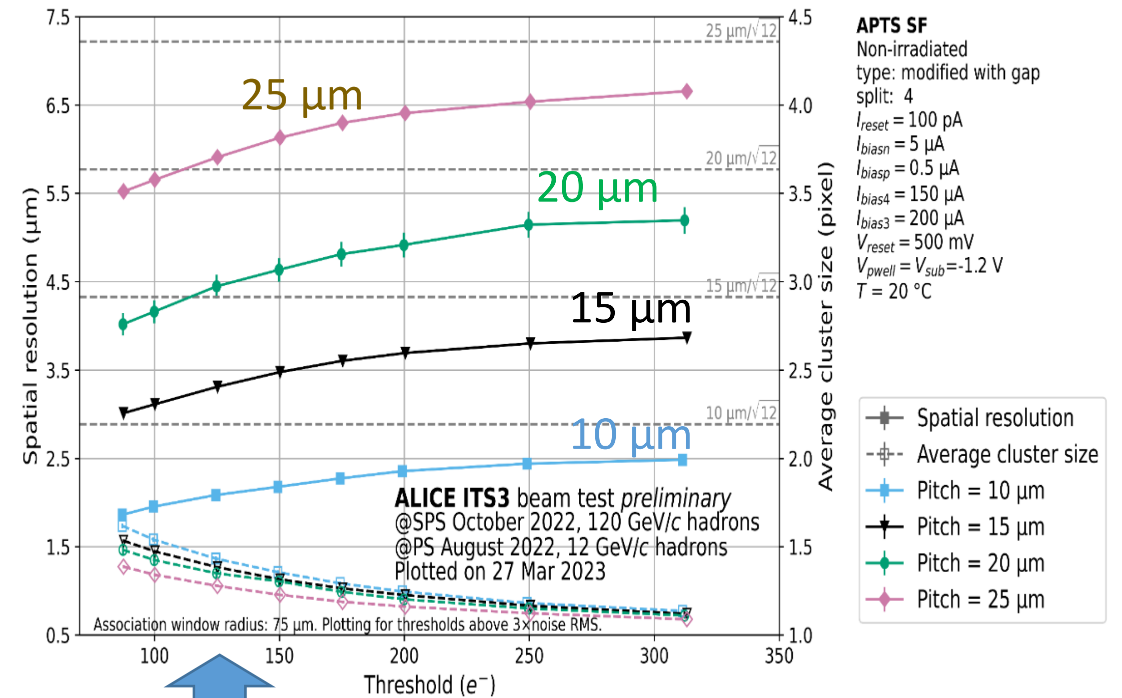


From IWORID-23



Operation regime

APTS (10, 15, 20, 25 µm pitch)

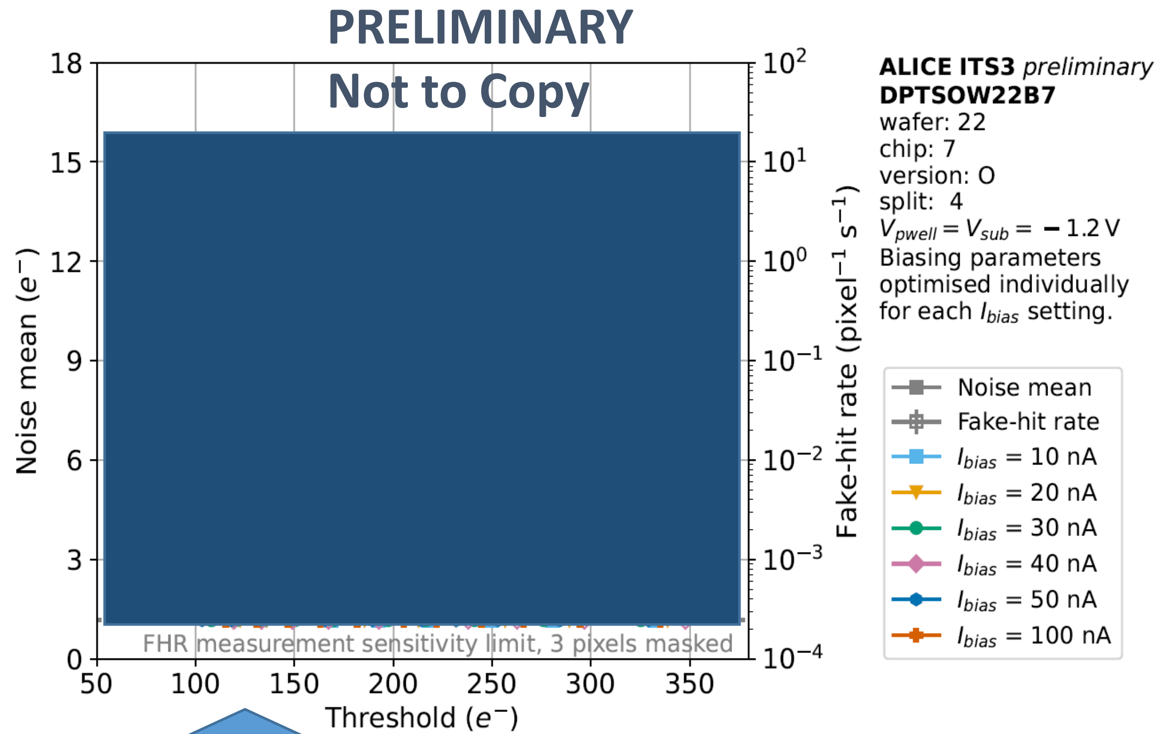


Operation regime

Binary resolution slightly better than pitch / √12 (impact of thin EPI ?)

MLR1 TEST RESULTS (soon to appear in ITS-3 TDR): Pixel Noise, Threshold Dispersion, Fake Hit Rate

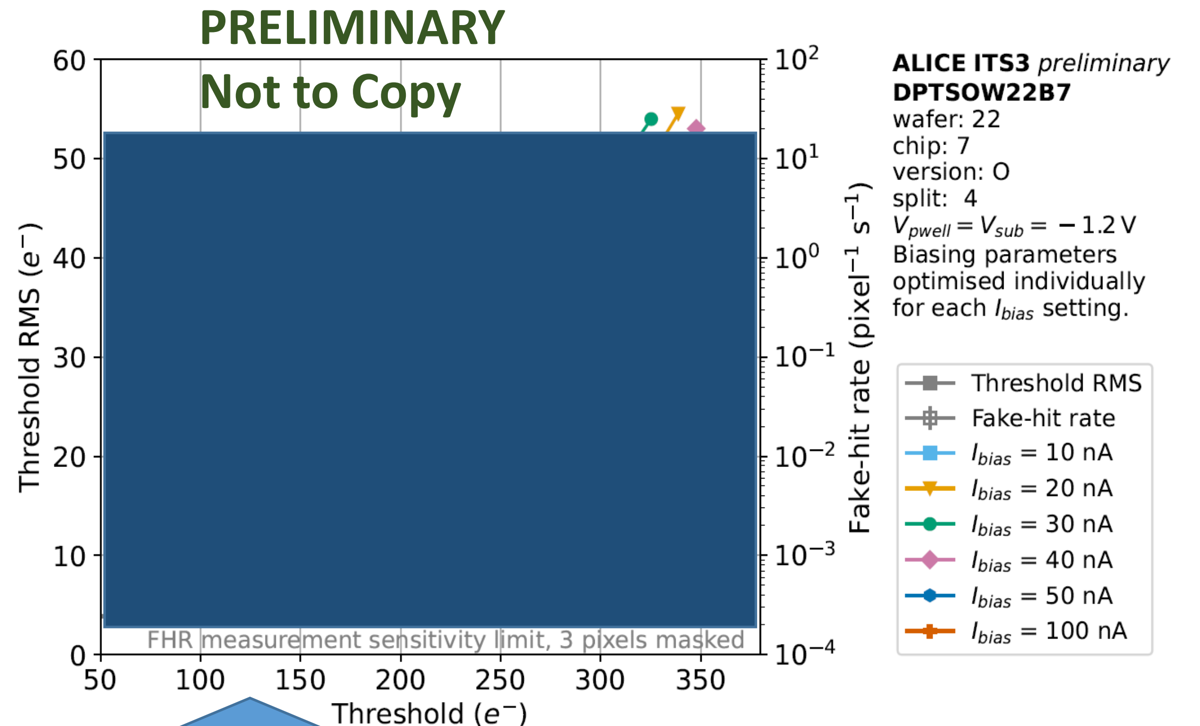
DPTS (15 µm pitch): Pixel Noise



Operation regime

ITS3 TDR (draft): private communication

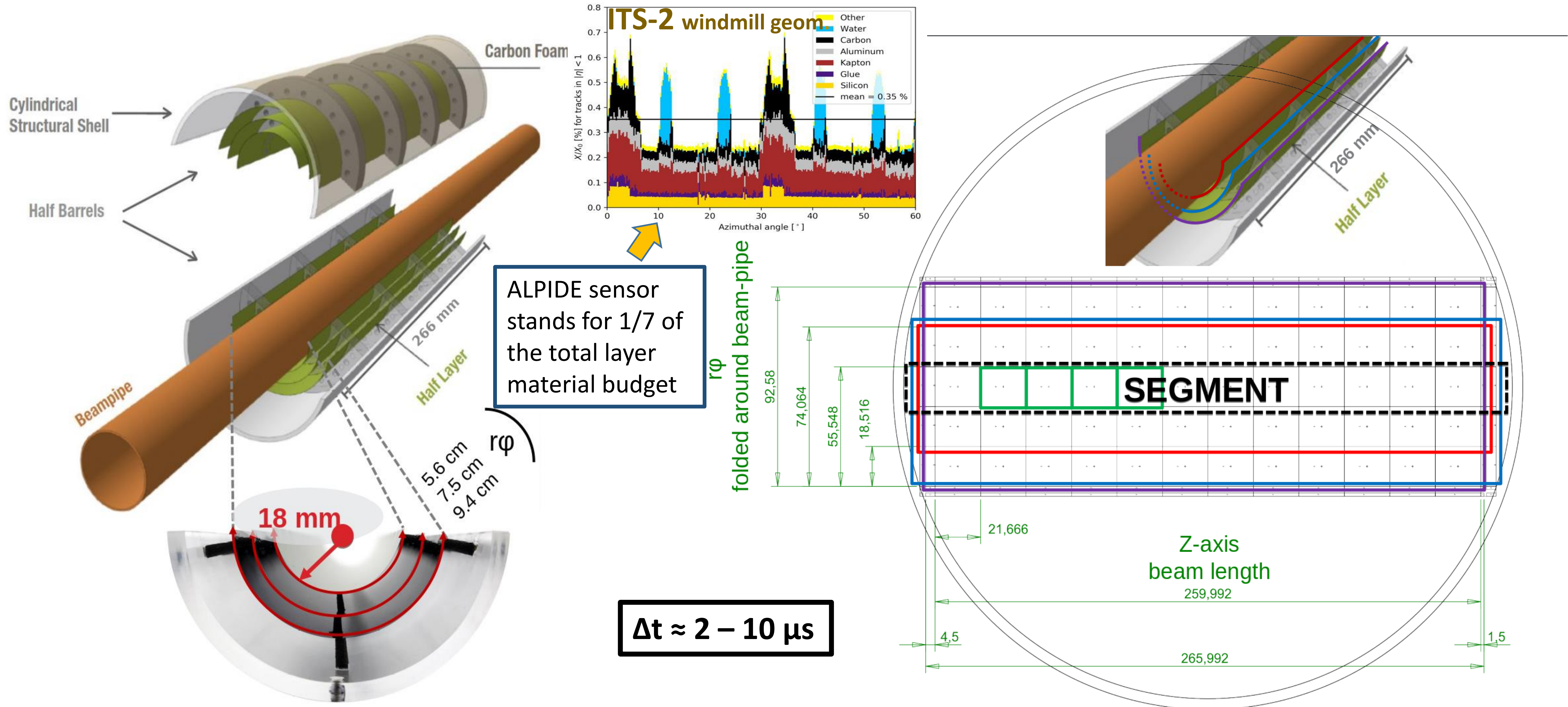
DPTS: Discri. Threshold Dispersion



Operation regime

LARGE STITCHED CMOS SENSORS DEVELOPED FOR THE ITS3

ITS3: multi-reticle (stepping), thin (≤ 50 µm), curved sensors to reach ≤ 0.1 % X0/ layer ⟹ stitching design rules



P
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2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
MLR 1		ER1	ER2	ER3	Commissioning			Run 4			

ER1 Submission

Aim at learning and proving **stitching**, submitted in December 2022

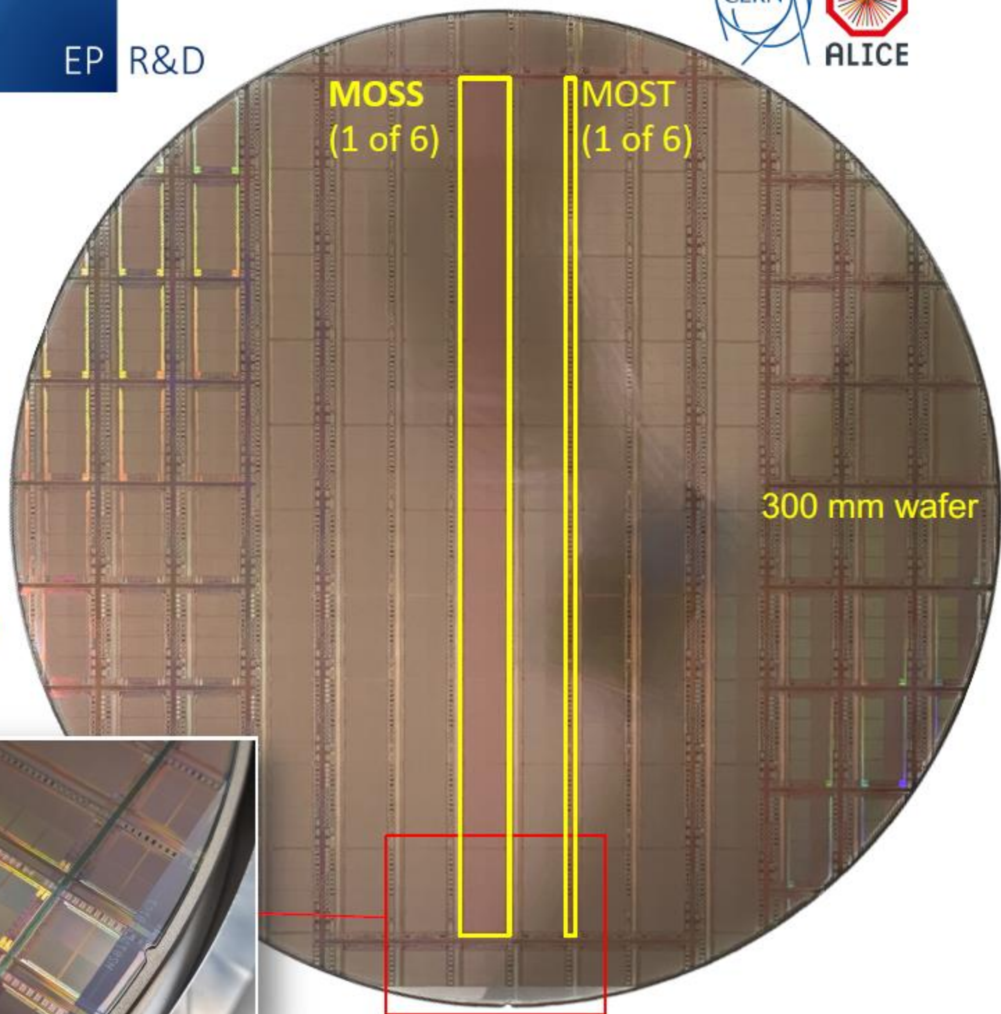
65 nm CMOS Imaging Technology

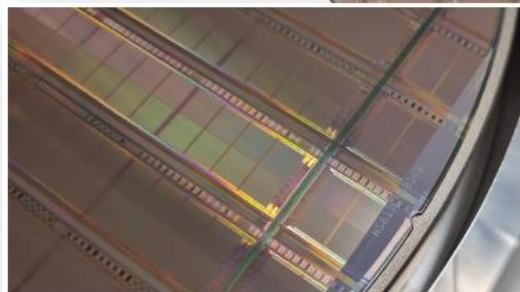
Design activities framed within **CERN EP R&D WP1.2**

Large effort of several teams and institutes

Two wafer scale stitched sensor chips (MOSS, MOST)

Different design approaches for resilience to manufacturing faults

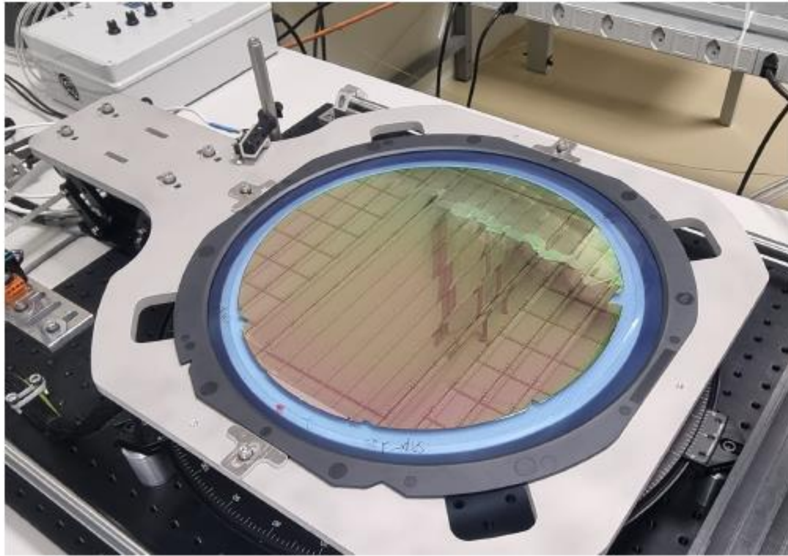


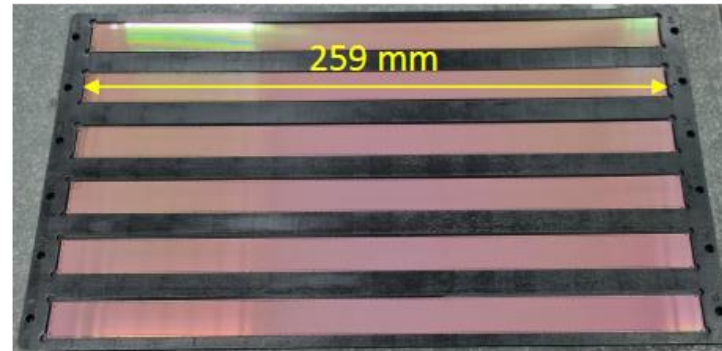


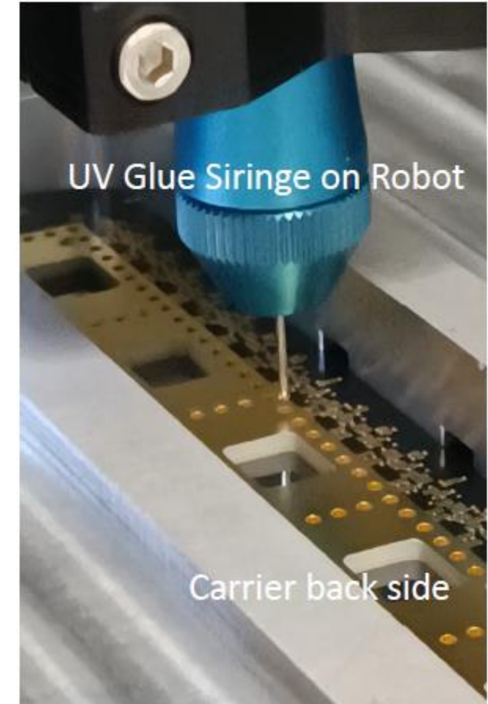
MOSS and MOST Tests on-going

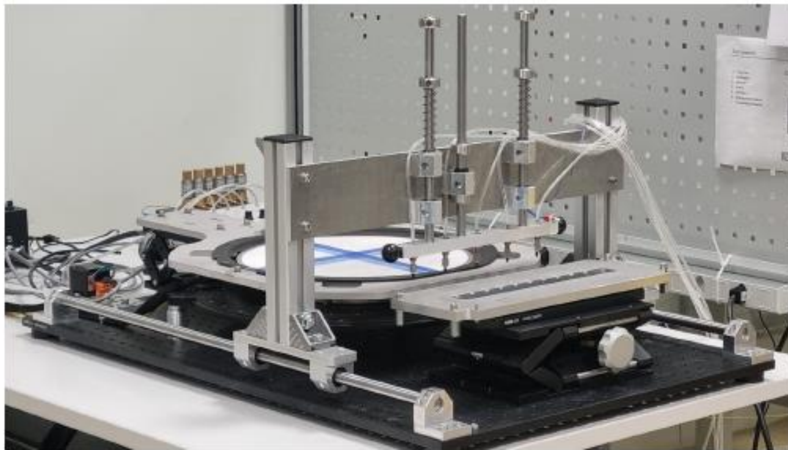
MOSS PROTOTYPE HANDLING

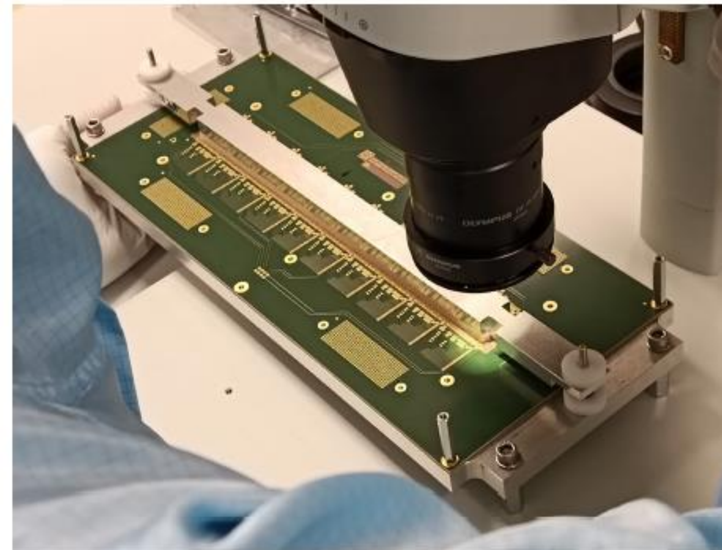
Pick, Align, Glue MOSS on Carrier

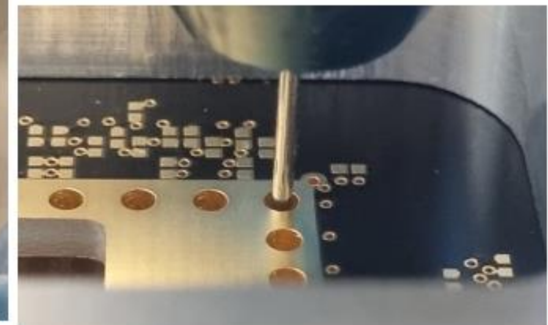




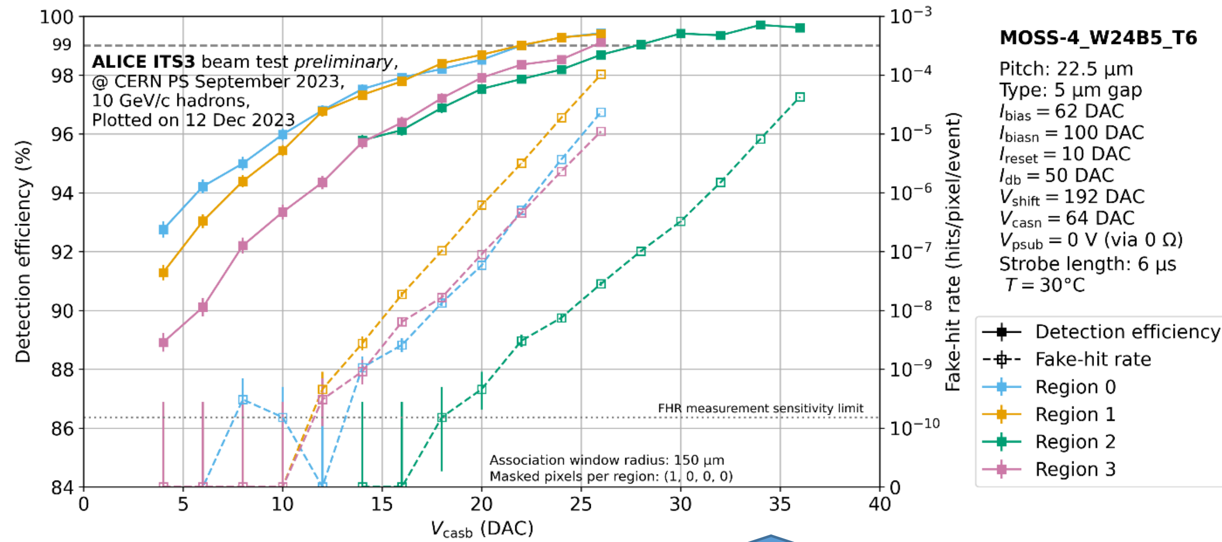




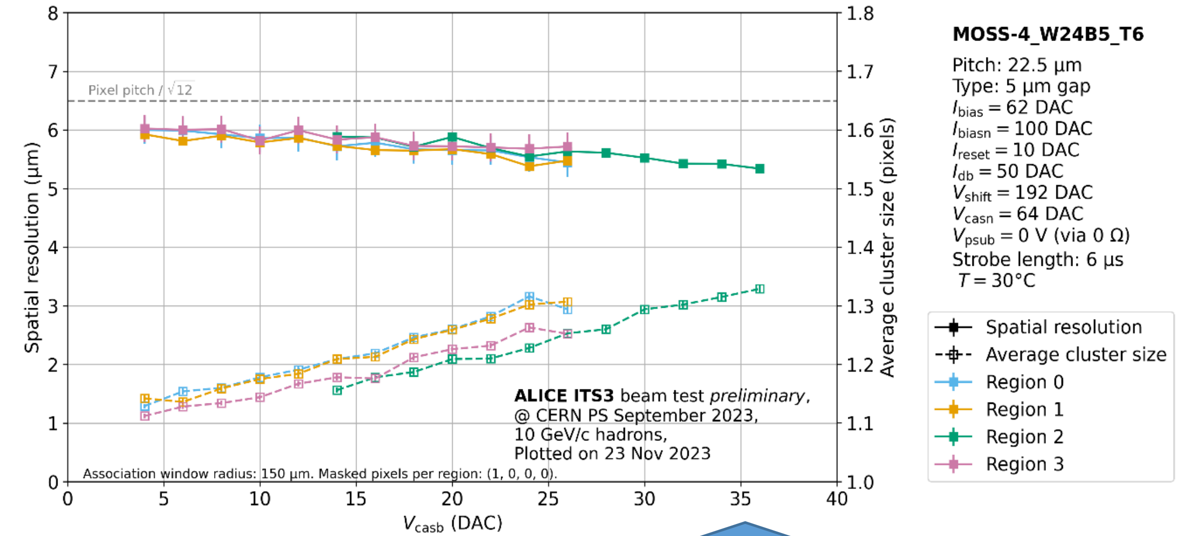




ER1: MOSS SENSOR TEST RESULTS



Operation regime



Operation regime

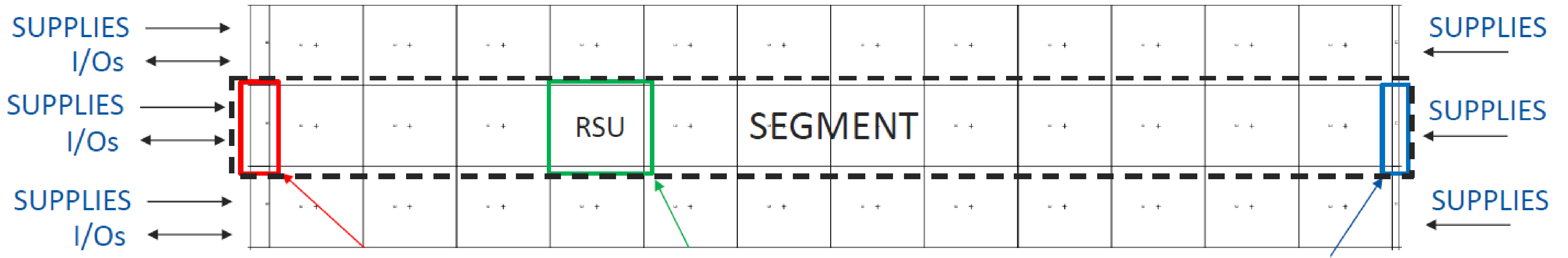
MOSS beam tests: 1st analyses indicate a spatial resolution ≈ 5 – 6 µm (binary charge encoding), close to pitch/√12

→ follows from pixel dimensions (22.5 µm x 20.8 µm) constrained by stitching rule induced system architecture design

→ shorter sensors (e.g. 12 cm long) may allow for (somewhat) smaller pixels, i.e. better spatial resolution (tbc)

Emblematic illustration of the necessity of a global approach when designing a sensor (experienced designers needed)

ER2: MOSAIX PIXEL SENSOR OVERVIEW



Control effects of yield, ageing, etc.

segmented pixel array

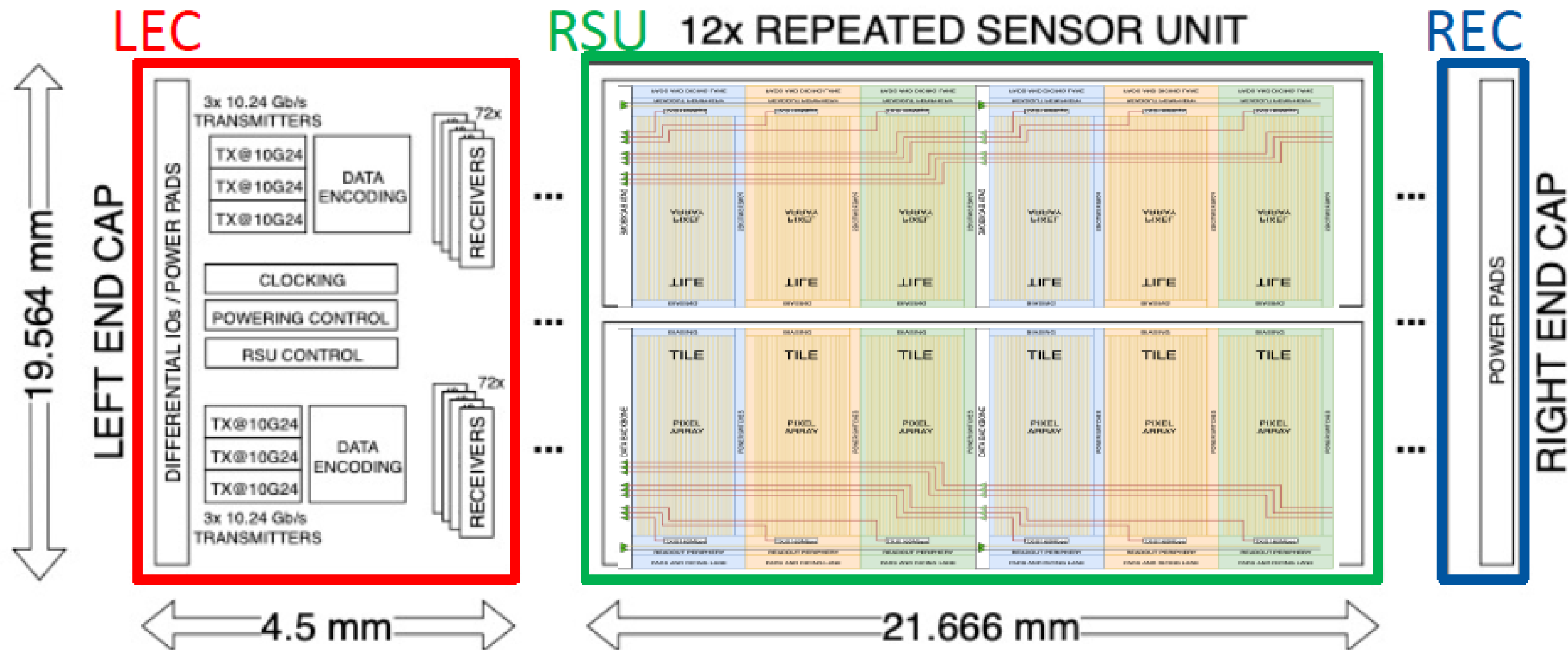
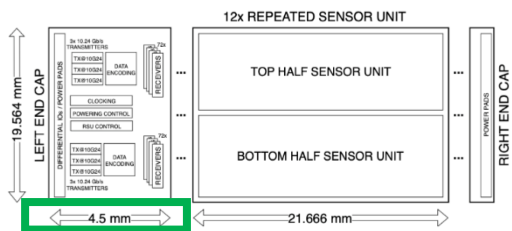


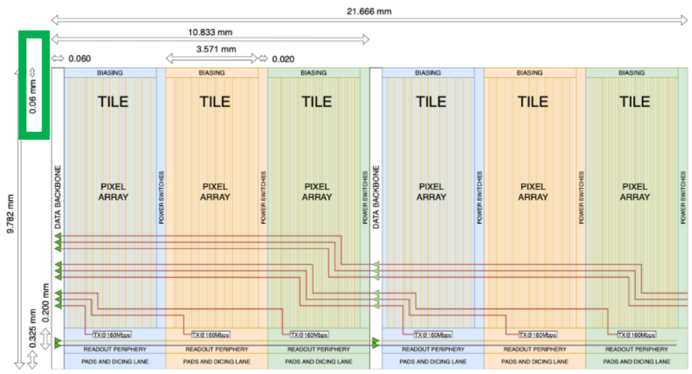
Figure 3.34: Block diagram of the sensor segment.

Courtesy of Gianluca Aglieri

Thermal analysis: Simulations with updated layout and heat map



Block diagram of the sensor segment (G.Aglieri)



Architecture of the bottom half sensor unit (not to scale)

	Power density [mW cm^{-2}]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

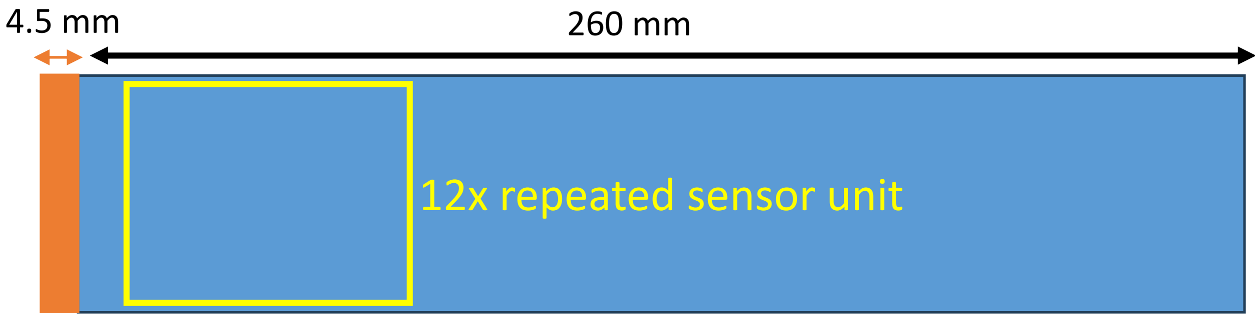
Estimates of power consumption

Total power dissipated by the 3 layers inside ITS-3 fiducial volume (1200 cm²):

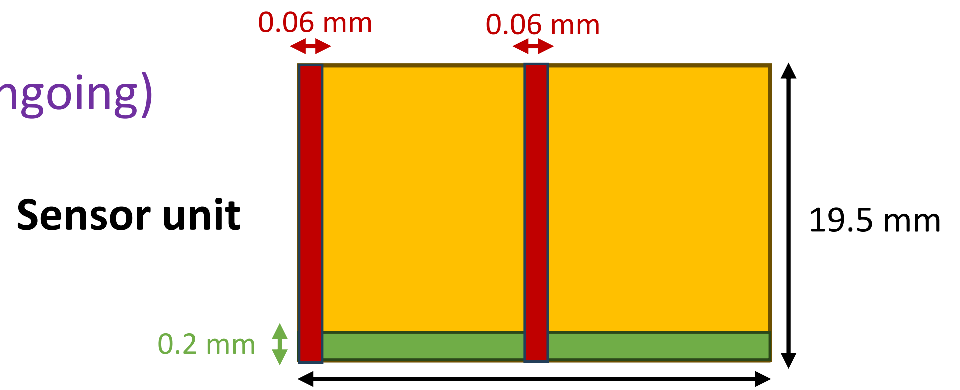
Ptot (fid. vol.) ≈ 50 W

- Update of the thermal simulation model with latest modifications
  1. Layout of L0 = 19 mm, L1 = 25.2 mm, L2 = 31.5 mm
  2. Heat map with all relevant components and power dissipations
- Pixel matrix power dissipation value not fixed → Simulations will be performed with 15 and 30 mW/cm²

Computational model (ongoing)



End Cap, 800 mW/cm²



21.6 mm

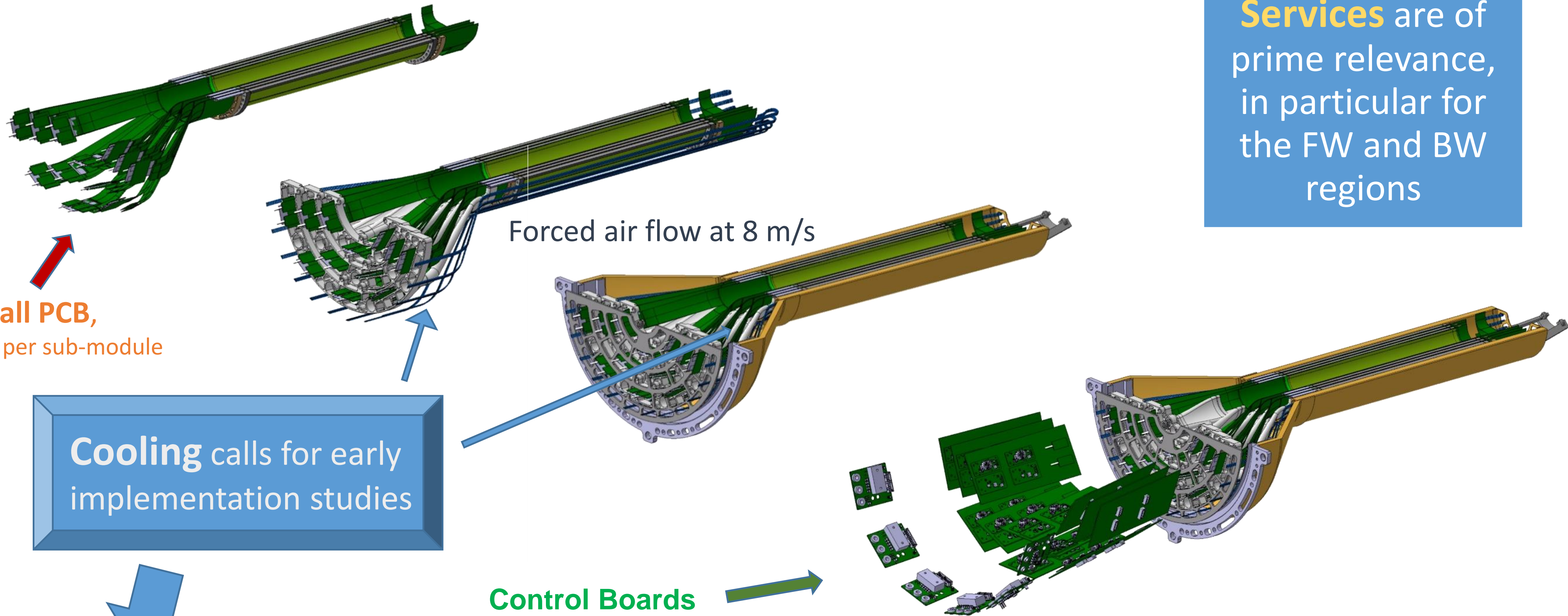
Matrix, 15 - 40 mW/cm²

Periphery, 450 mW/cm²

Data backbone, 700 mW/cm²

From C. Gargiulo

ITS-3 SYSTEM INTEGRATION PROCEDURE

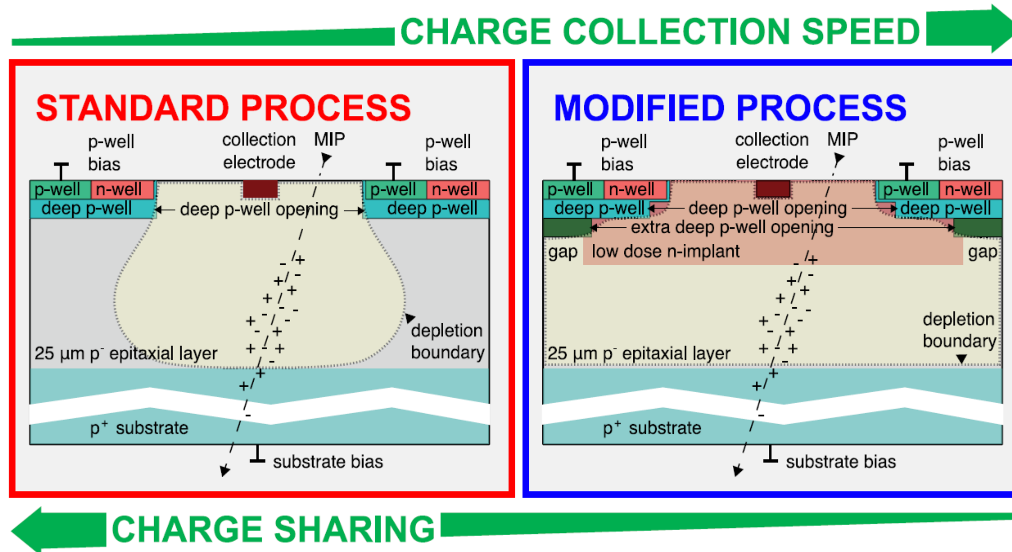


Control Boards

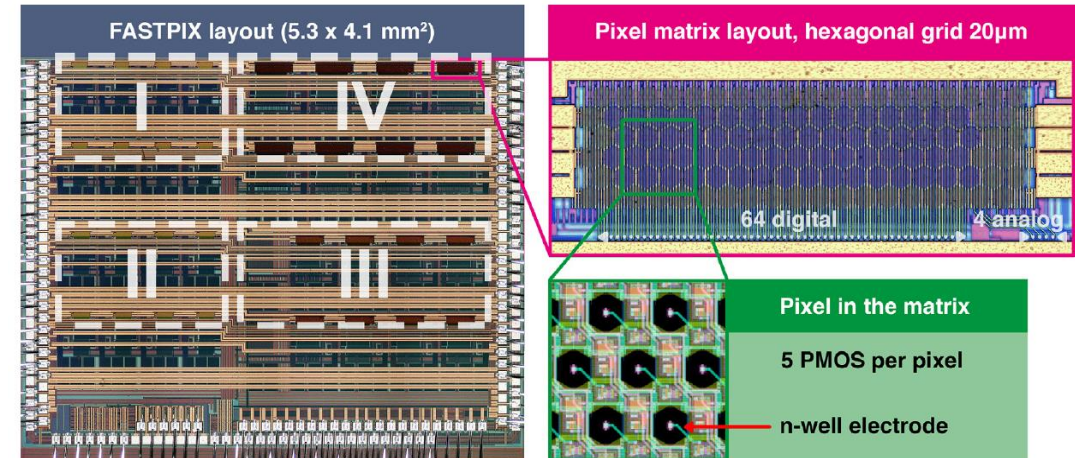
Contains all the remaining electronics
It is divided in several segments avoiding acceptance cone
Different layouts under study

Impact on choice of sensor technology and design

FAST CMOS SENSOR R&D



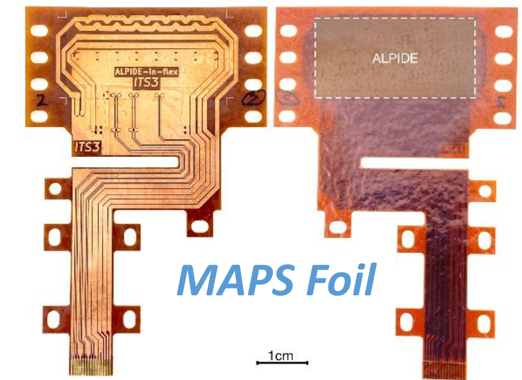
FASTPIX NIM A 1256 (2023) 168641



- FASTPIX: exploratory chip in TJsc 180 nm achieved O(100) ps time resolution with modified EPI
- Several prototypes fabricated in MLR-1 (TPSCo 65 nm) addressing HL-LHC and FCChh
- NAPA : CPS in TPSCo 65 nm for the C3 Higgs-Factory (goal ≈ 1 ns resolution with 25 µm pitch)

SUMMARY -- OUTLOOK

- **Significant progress in last few years in the development & use of CPS:**
  - TPSCo 65 nm process seems validated for tracking devices, with limitations:
    - small signal amplitude (thin EPI)
    - spatial (& time ?) resolution, fill factor, yield with stitched sensors (for extra-low mat. budget)
  - TJsc 180 nm process:
    - gets more (full custom) applications beyond ALICE-ITS2 (ALPIDE): CBM/FAIR, Mu3e, Belle-II, … : MIMOSIS-II for CBM may be a good seed for ILD
    - also considered for sub-nanosecond sensor design (FastPix)
    - used to investigate curved dices sensor mosaics (SuperAlpide) & embedded sensor blades



- **Most of the progress was achieved within the ITS-3 project:**
  - Validation of new CMOS technology (TPSCo-65) and assessment of its limits/consequences
  - Pioneering design methology of wafer scale sensors using stitching rules of foundry (25 cm long CPS),
  - Validation of curved, wafer-scale, thin sensor concept (material budget < 0.1 % X_0 / layer),
  - Realisation of complete, very light, vertex detector design (mechanics, cooling) → impact on FW/BW regions
- **Ccl:** $\sigma \approx 3$ µm, < 0.1 % X_0 / layer, < 50 mW/cm², $\Delta t \approx O(100)$ ns not yet achieved with a single sensor (next slide)
- **Sub-ns CMOS sensors:** still in early stage of R&D (no large sensor), but promising perspectives identified
- **CPS for calorimetry:** R&D with TPSCo-65 pursued by several groups

COMMENT on SENSOR OPTIMISATION for the EW RUN

Achieving simultaneously $\sigma \approx 3$ µm, < 0.1 % X_0 / layer, < 50 mW/cm^2, $\Delta t \approx$ O(100) ns within a single sensor seems unlikely with currently available CMOS technologies

➡ which parametres could be relaxed to preserve the others ?

Spatial resol. vs mat. budget: shorter sensors suspected to allow $\sigma \approx$ 4.x µm (?) while preserving the asset of large stitched sensors to achieve < 0.1 % X_0 / layer (tbc)

➡ should trigger R&D interest in the ILD community

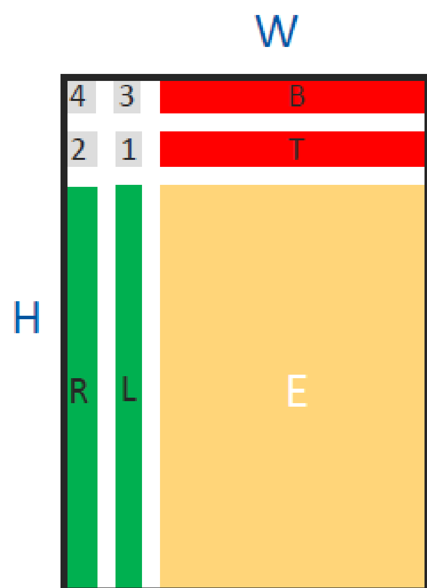
Power vs Δt for the sake of air cooling at $\sqrt{S}$ < HZ threshold:

- Higgs-top-EW factory ➡ Higgs, top, Z & T/QGC studies (HF comes in addition)
- EW running conditions at FCCee and Giga-Z (polar) are quite different because of the different beam time structures ➡ low machine duty cycle (e.g. Giga-Z) allows to circumvent the conflict

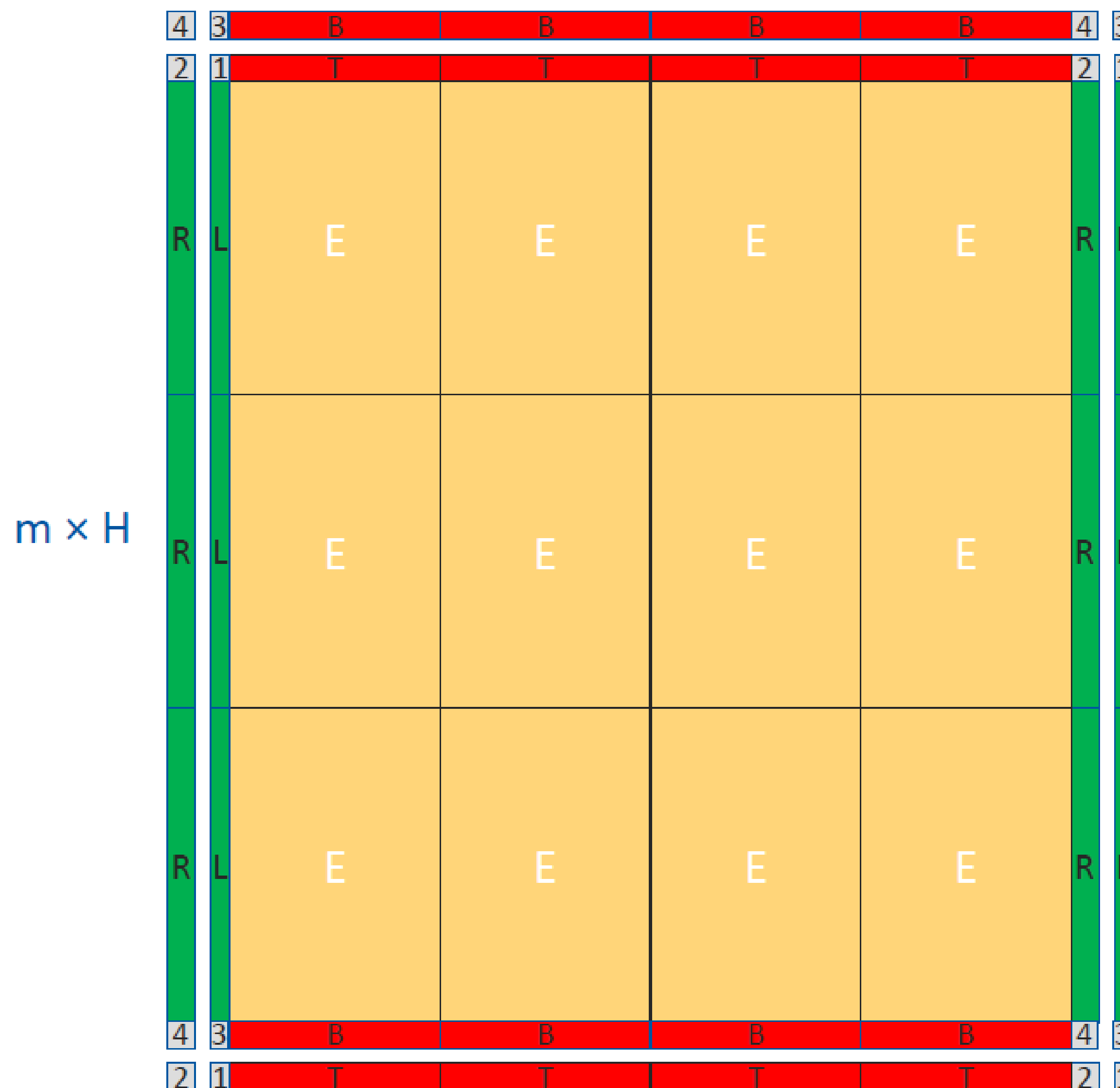
➡ how does ILD perform at Giga-Z vs at FCCee for EW physics final states relying on flavour tagging ?

Stitching

Design Reticle (typ. 2×3 cm)



Circuits on wafer



Courtesy of G. Aglieri