# → DRD6

# Calorimeters for ILD′

*Vincent Boudry*

**Institut Polytechnique de Paris**

**Work from ScECAL, SiW-ECAL, T-SDHCAL and AHCAL groups**
Special thanks to Imad, Katja, Wataru, Weihoa, Jiaxuan, ...

***ILD′ for FCC-ee***
***16/01/24 @ CERN***

# How to adapt calorimeters to FCC-ee conditions

**CALICE calorimeters:**

- Embbeded readout:
  compact design & DAQ
  - Minimal consumption by power pulsing
    - 1–2ms readout , 198–199 ms off.
    - Passive cooling ➞ no dead materials

**1) Rates and cross-sections**

- Z-peak out-of-scale wrt all the other configurations
  - One detector fits all ? “optimal” granularity ?
- DAQ Scheme ? Continuous readout ?

**2) Continuous running**

- Electronics base comsumption × 100–200 wrt ILC

**3) New opportunities: timing in calorimeters**

- Adds comsumption
- Large potential but at what cost ? What precision ?

# Linear → Circular Collider's Conditions

## Linear (ILC, HL-ILC… )

- 250 GeV (ZH), 365 GeV (tt), 500 GeV (ZHH) + [1000 GeV], $\mathscr{L}$ ~ cst.
- Power pulsing : 5 [10–15]Hz × 1 [2] ms    Power ~ $\mathscr{L}$ .

## More diverse et stringent conditions:

- 90GeV × $10^7$ fb × $5{\cdot}10^{36}$ $cm^{-2}$ $s^{-1}$ (qq × 20,000 ILC @ 250)
- 150 GeV (WW) + 250 GeV (ZH)+ 365 GeV (tt)
  ~$10^4$ fb × $5{\cdot}10^{35}$ $cm^{-2}$ $s^{-1}$ (qq × 5–10 ILC @ 250)

## From Pulsed to Continuous operation

- Power = **cst** + convertion+RO × local rates ($P_{Conv}$+$P_{RO}$ ~ 40% $P_{ACQ}$ )
- ASIC, Power/Cooling, DAQ, *Granularity, Precisions (E, t)*, New ideas…

**HL-ILC:**

- $\mathscr{L}$ × 4 (6)
- $N_{bunches}$ × 2 : $\tau_{Train:}$ 1 → 2 ms
- $f_{rep}$ ×2 (3): 5 → 15 Hz

Dominated by ACQ time: P(~25µW/ch) × 6

**HL-CLIC:**

- $\mathscr{L}$ × 2
- $N_{bunches}$ → : $\tau_{Train:}$ 176 ns
- $f_{rep}$ ×2 : 50 → 100 Hz

Dominated by Set-up & Conversion time: P (~82µW/ch) ×2

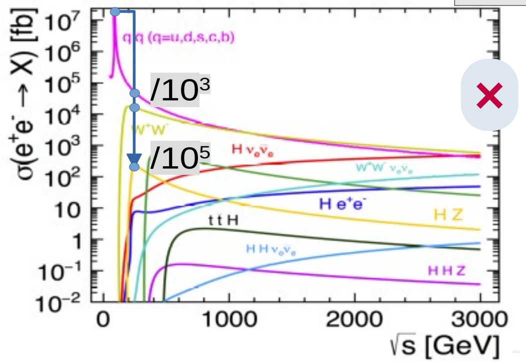
| FCC-ee parameters | | Z | W⁺W⁻ | ZH | ttbar |
|---|---|---|---|---|---|
| √s | GeV | 91.2 | 160 | 240 | 350-365 |
| Luminosity / IP | $10^{34}$ $cm^{-2}s^{-1}$ | 230 | 28 | 8.5 | 1.7 |
| Bunch spacing | ns | 19.6 | 163 | 994 | 3000 |
| "Physics" cross section | pb | 35,000 | 10 | 0.2 | 0.5 |
| Total cross section (Z) | pb | 40,000 | 30 | 10 | 8 |
| Event rate | Hz | 92,000 | 8.4 | 1 | 0.1 |
| "Pile up" parameter [μ] | $10^{-6}$ | 1,800 | 1 | 1 | 1 |

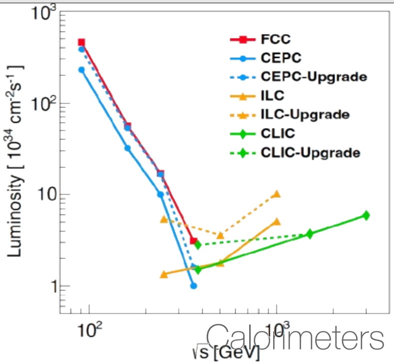
**Experimentally, Z pole most challenging**

- Extremely large statistics
- Physics event rates up to 100 kHz
- Bunch spacing at 20 ns
  - "Continuous" beams, no bunch trains, no power pulsing
- No pileup, no underlying event …
  - …well, pileup of 2 x $10^{-3}$ at Z pole

https://indico.cern.ch/event/1064327/contributions/4893208/
Mogens Dam @ FCC Week, 10/06/2022

Status of the CEPC, October 2022 J. Guimarães da Costa



# Rates in the Calorimeters

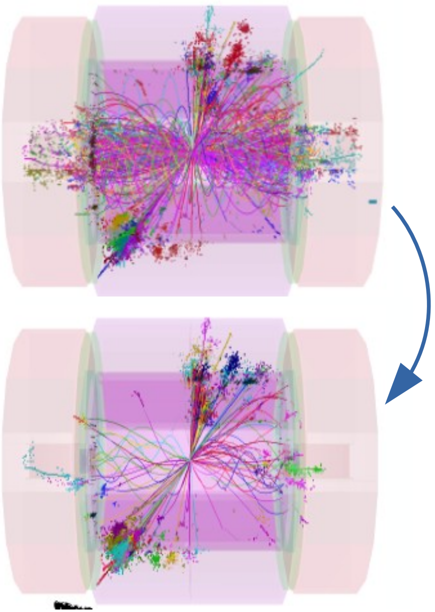
## See presentation from K. Hassouna

- $\Delta T$ = 25 ns (40 MHz) in FCC-Z4 config but with ILD_l5_v02 version (except for machine bgd)
  - Preliminary running ➞ will need to be redone with “final” ILD model.
- Highly non-uniform rates in depth
  - $1^{st}$ two third of ECAL mostly demanded (low E photons ?), much less in $3^{rd}$ part and HCAL
    - Background (number of hits) at 240 GeV ~ 4× 90 GeV [TBC]
  - Machine background : hadronic contribution near the beam-pipe
- Dymanic ranges up to 1000 MIPs [except in RPCs] ~ uniformly and identical at 90 and 240 GeV
- Late neutron contribution to be evaluated

# Timing in Calorimeters: 0.1–1 ns range

**1 cm/c = 30 ps**

## Cleaning of Events

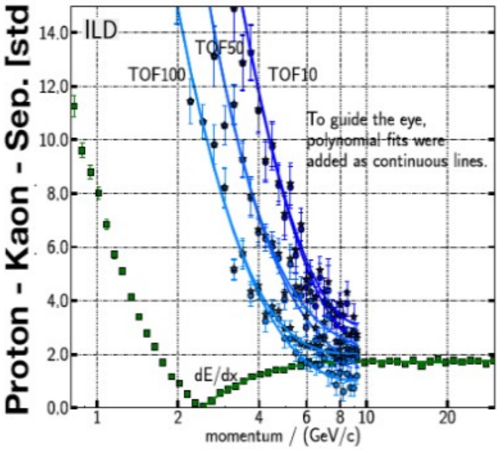


time cut

[CLIC CDR: 1202.5940]
adapted from L. Emberger

## Particle ID by Time-of-Flight

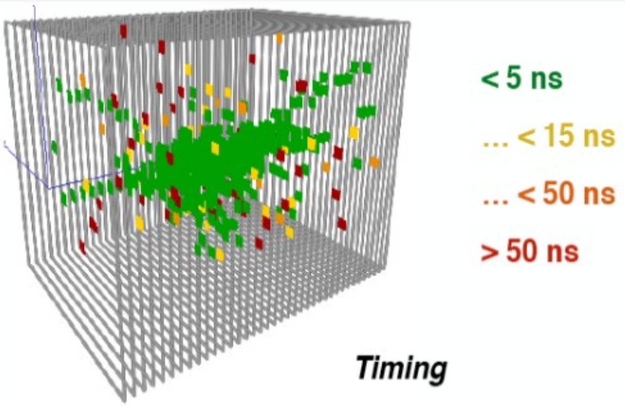
– Complementary to dE/dx
  - here with 100 ps on 10 ECAL hits




S. Dharani, U. Einhaus, J. List

## Ease Particle Flow:

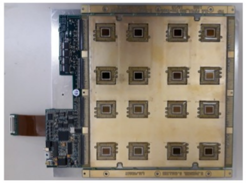
– Identify primers in showers
– Help against confusion
  *better separation of showers*
– Cleaning of late neutrons & back scattering.
– Requires 4D clustering

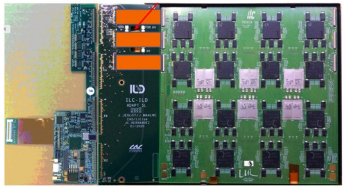



Ch. Graf

# SiW-ECAL

# Technological Prototype beam test at DESY & CERN





**FEV10, 11, 12**

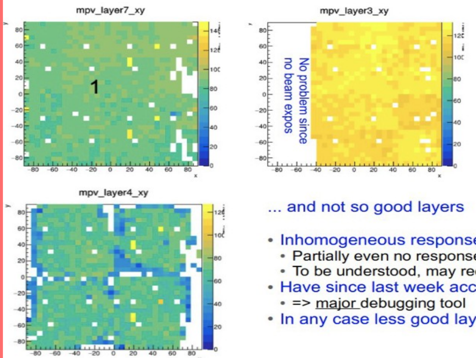
- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014

**FEV-COB**

- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

**FEV13**

- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

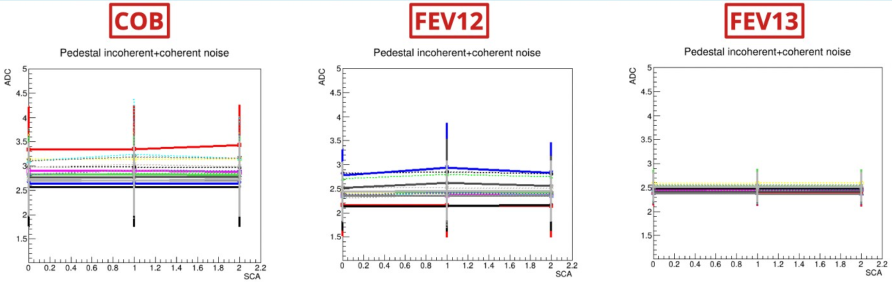



- We have good layers ...
  - Homogeneous response to MIPs over layer surface
  - Here white cells are masked cells due to PCB routing
    - Understood and will be corrected

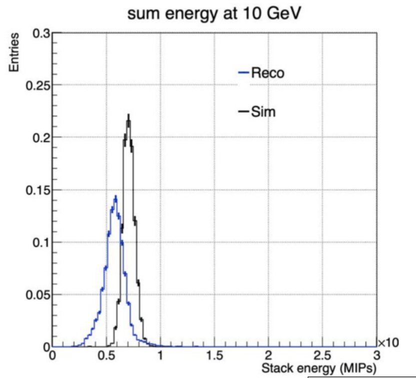
... and not so good layers

- Inhomogeneous response to MIPs
  - Partially even no response at all, in particular at the wafer boundaries
  - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
  - => major debugging tool
- In any case less good layers will be replaced in coming months

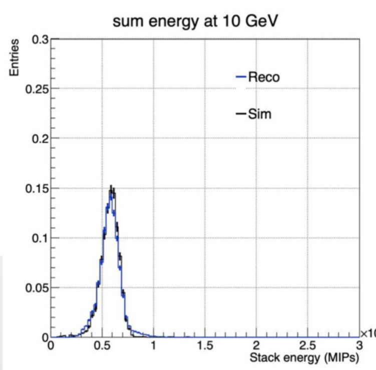
## Pedestal widths, 1st memory cells, per asic




- (Average ± Standard Deviation) of Sigmas for all 64 channels in the same chip
- Latest PCBs, with optimized routing of power distribution shows better behavior
- Slightly larger spread on COB due to a near lack of decoupling capacitors




Masking Beam profiling




Yuichi Okugawa (PhD in Feb.

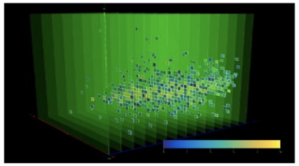


Fig. Simulation e- 100 GeV

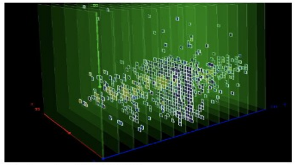


Fig. Reconstructed e- 100 GeV

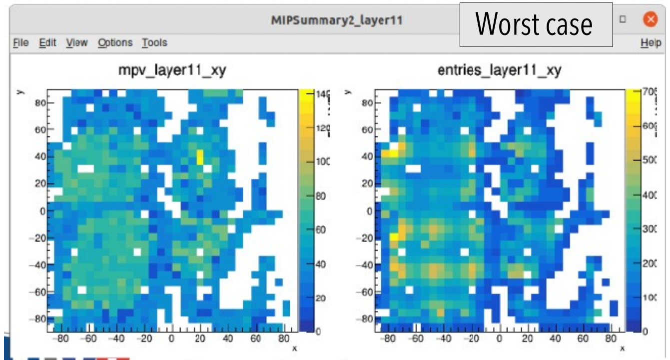
# → Homogenous prototype

**Goal:**

- 15 layers of FEV2.1 with 500µm wafers
  - Uniform and more performant electronics
  - Could be used for LUXE and Dark Photons exp’s.
- All material available

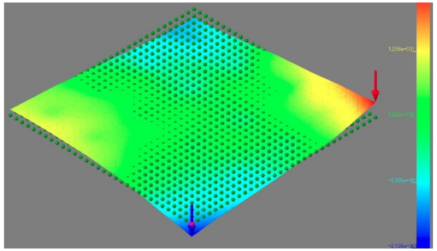
**Main issue: contact PCB–Sensor**

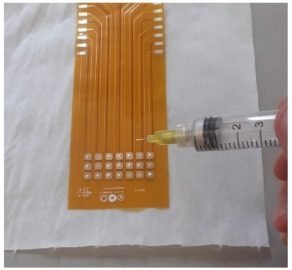
- Conductive glue dots of ∅2–3mm
- Aging, mechanical stress, manipulations, …

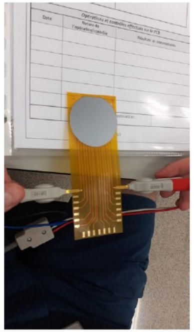


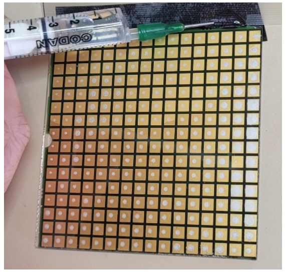

**Revisiting gluing (IFIC, IJClab, LPNHE)**

- PCB metrology
  - Bef. & After curing & soldering
- Glue formula & preparation
- Gluing methods
  - Robot
  - Stencil
- Reenforcement
  - Filling glue
  - Adhesive films

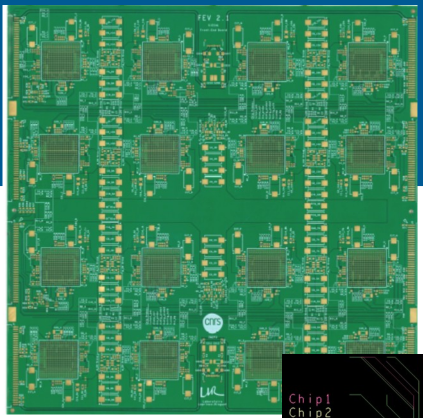






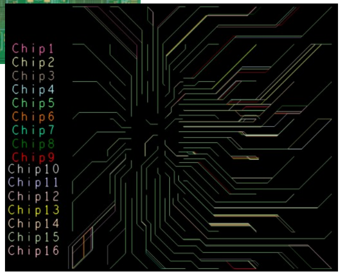


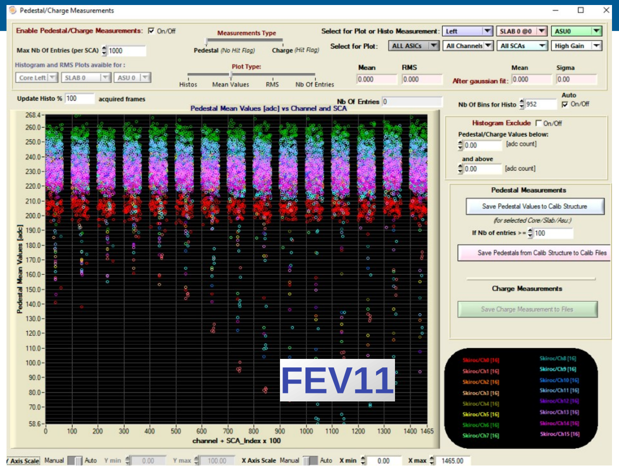
# New FE boards



**Improvements:**

- Power distributions
  - Local power regulation: LDO's
  - Local High Voltage filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing



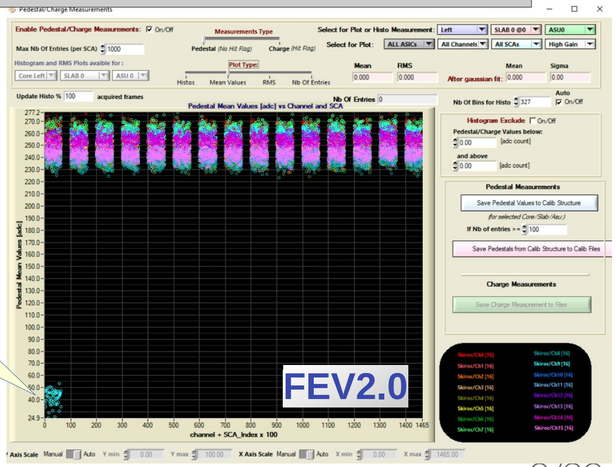




Pedestal measurements vs. Ch# + Mem#×100)

**Status:**

- pre-version 2.0 tested, minor corrections needed
  - Noise uniformity dramatically improved (ex: outliers in thr. / 20 !)
- version 2.1 produced, … in metrology
  - before cabling, 2nd metrology, gluing, …
  - All material available : ASICs being tested
- Beam test of a few layers @DESY, June 2024

SIngle channel → the fault on the ASIC/packaging



# Detector optimisation for Higgs Factories

## Low energy (90 GeV)

- Lower energy – less focused jets
  - Lower granularity needed (1–2 cm OK ?)
  - Lower dynamic range ? ✗

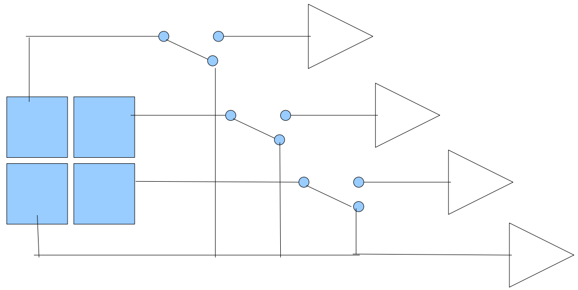
**… but not so for the rest (≥ ~250 GeV)**

## Reduce the number of layers + thicker sensors

- See “Small ILD” model
- 6’’×500µm wafers ➡ 8’’ × 725 µm ( resolution $1/\sqrt[5]{d}$ )

## One size fit all ?

- Have a dynamic granularity ?



- Have a semi-digital readout ?
  - Hit counting for low energy
  - E measurement for high energies

# Going from 30 to 26 Layers: performances

**Going from 30 to 26 layers**

– Reduction of cost; increase of Energy resolution
  - keep 24$X_0$ (84mm) of Tungsten

**Increasing the Si thickness to 725µm**

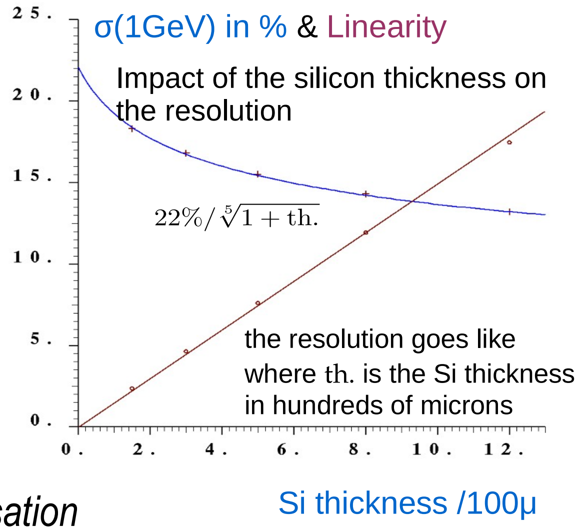
– GR width ↗ ⇒ go to 8" wafers, new design

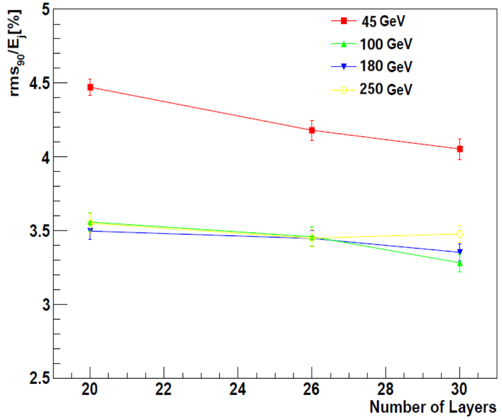
**Energy resolution σ(E)/E:**

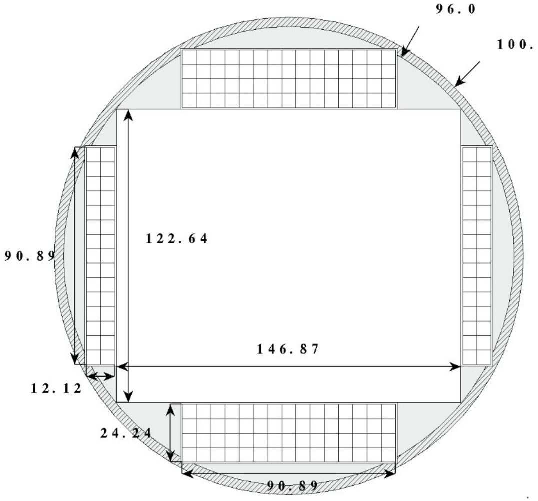
– for 26 layers w.r.t. 30: ↗ +8.5%

– with 725µm w.r.t 500µm : ↘ –6.6% (-8.7% wrt to DBD 300µm)

*near compensation*



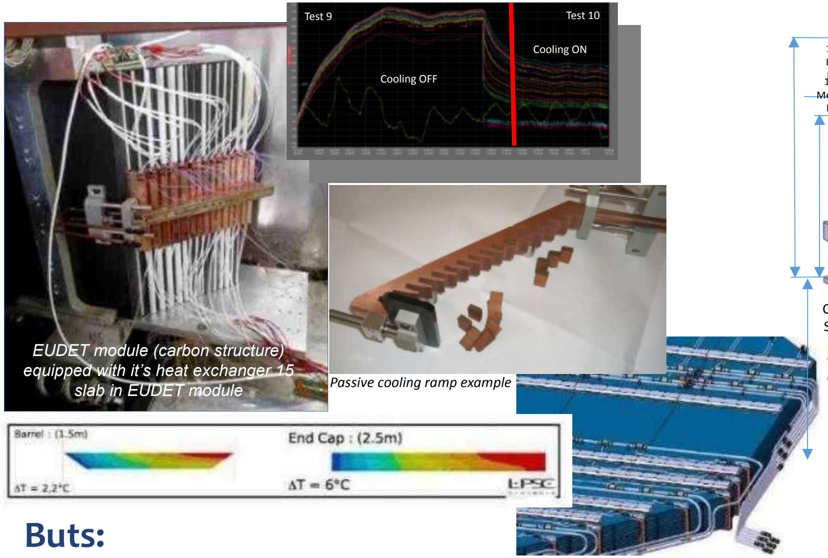




**Study needed on dead zones (larger GR…), separation, resolution and efficiency performances at low energy.**

– eg: JER : $\sigma(E_J)/E_J$ +6% for 26 layers (500 µm) to be redone… *Shown @ 6th ILD Optim meeting (16/07/2014) [link]*

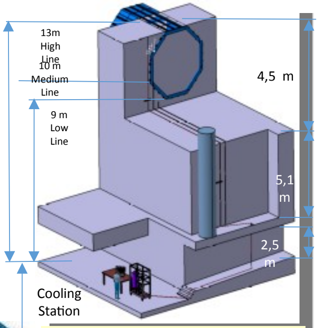
# Leakless Water cooling system

## Thermique/Intégration




*EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module*

*Passive cooling ramp example*




*LPSC cooling test area* with a drop of 13 m

Cooling station

**Buts:**

- Heat evacuation at end of slabs
- Caloduc compatible with ECAL–HCAL spacing (3 cm)
- Leakless (depression)

**Modèle : sur module pilote**

**Maquette 1: 1:1**

- simple circuit

**Maquette 2: 3:4**

- heat model in C-W structure

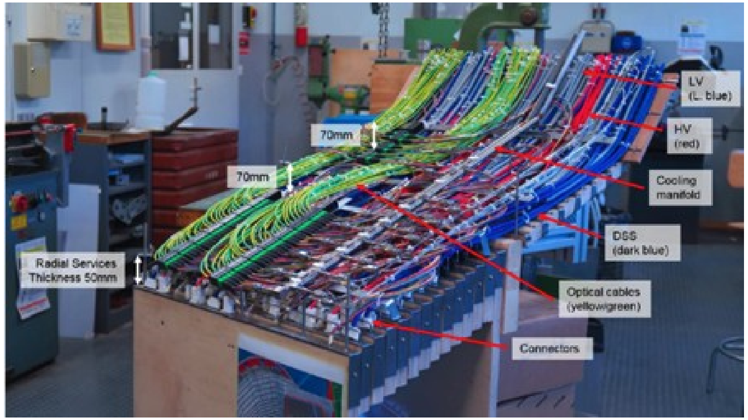
**To Do:**

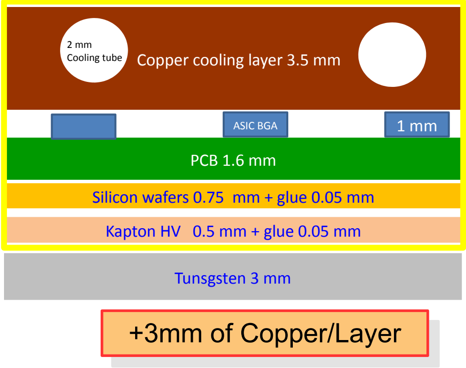
- **Test sur on a full ECAL module**

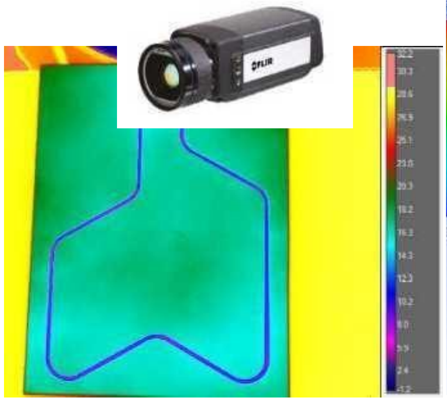
**For FCC-ee:**

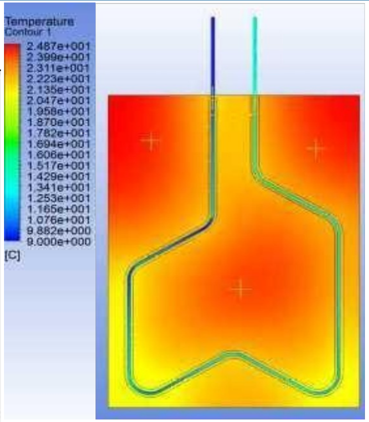
- 1) Dimensioning for continous working, if possible, without active cooling
- 2) if not, include a active cooling $CO_2$ (in Cu or W)

# Services: integration & cooling



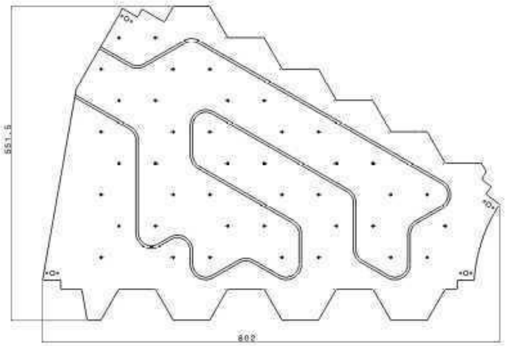



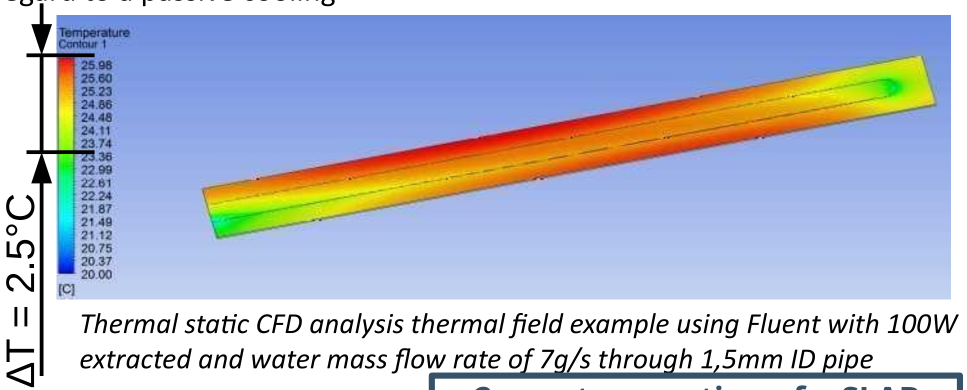






Pipe insertion on a cooling prototype

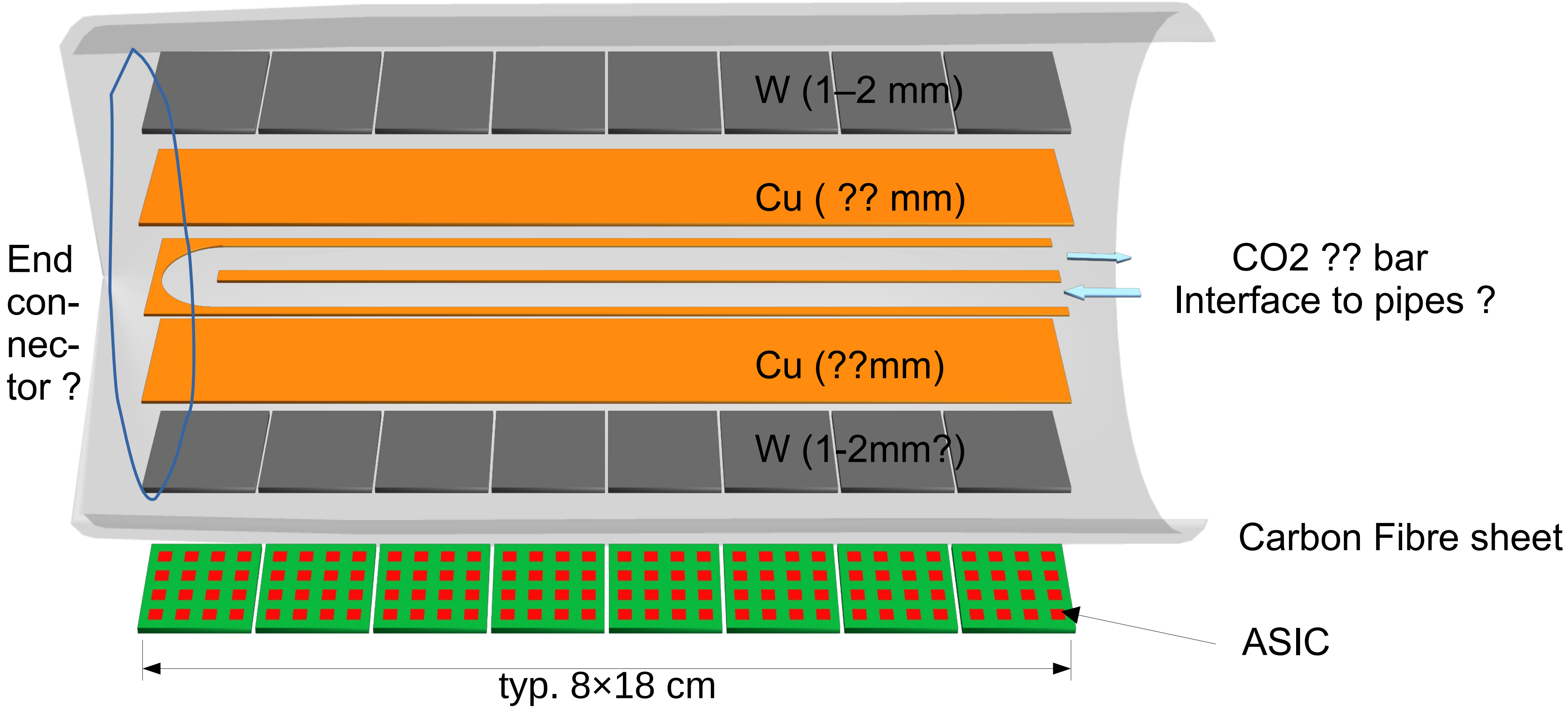
- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling






*Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe*

**= 2× cont. operation of a SLAB, with 5 mW/ch × 5×5 mm²**

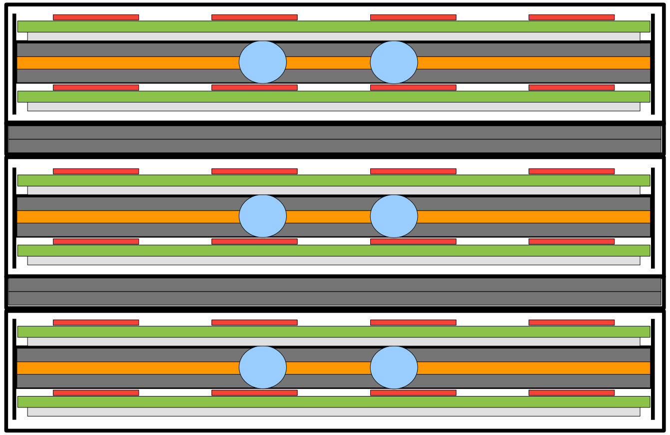

W (1–2 mm)
Cu ( ?? mm)
End
con-
nec-
tor ?
CO2 ?? bar
Interface to pipes ?
Cu (??mm)
W (1-2mm?)
Carbon Fibre sheet
ASIC
typ. 8×18 cm

# Where to put the cooling layers ?

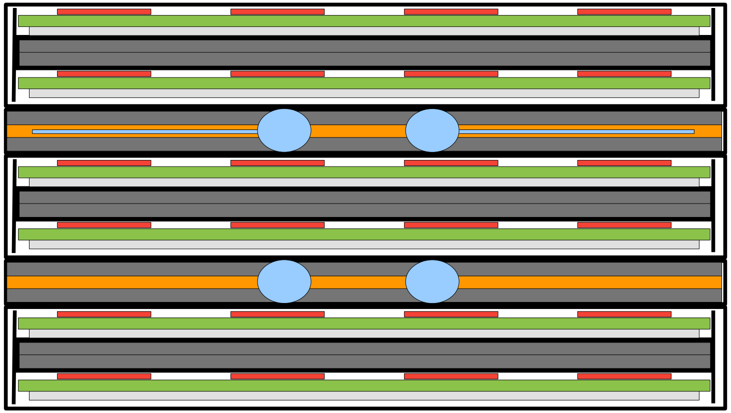
## In-slabs :

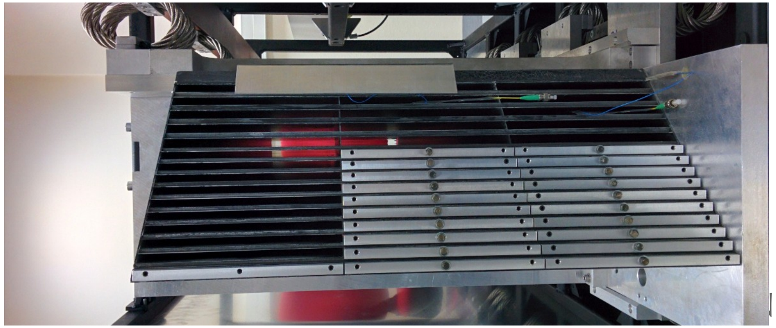
Opt. Up

Opt. Down



## in-structure



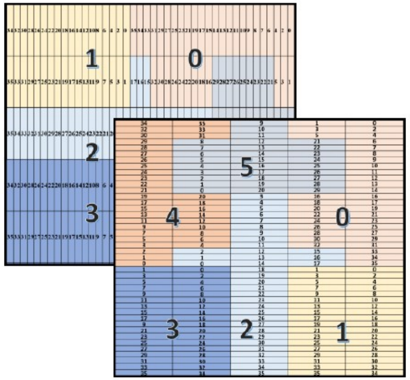


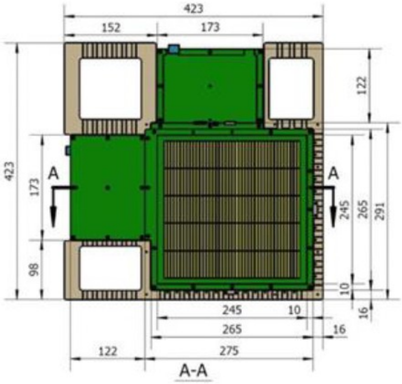
# SciECAL

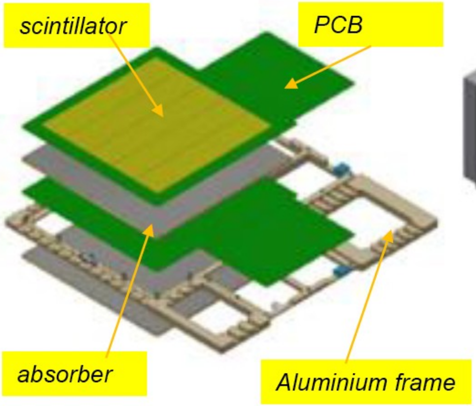
# SciECAL technological prototype

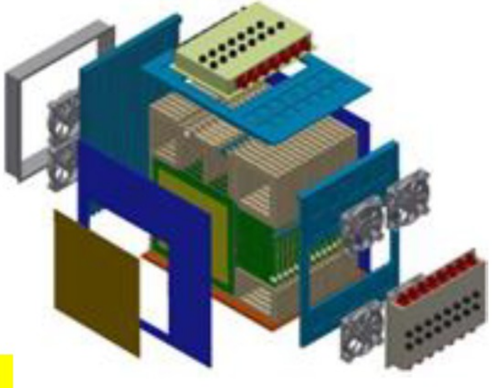
## Sci-ECAL technological prototype

- High granularity calorimeter
  - Adjacent layers are of orthogonal placement ➔ 5mm*5mm virtual cell
  - Two layers get integrated into one superlayer
  - 16 superlayers are assembled in ECAL Aluminium frame
- All channels' signal could be readout individually at the same time
  - 6720 electronics channels



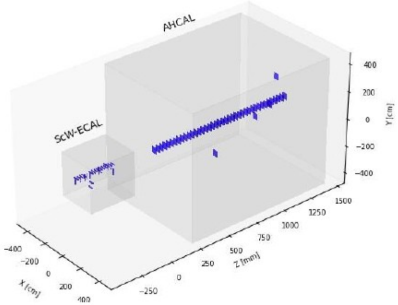



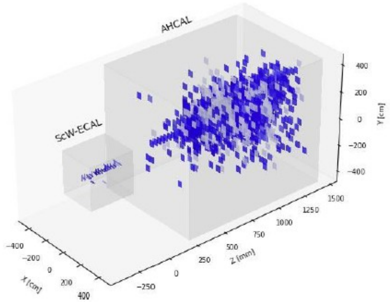
# SciECAL technological prototype

## Beam test @CERN

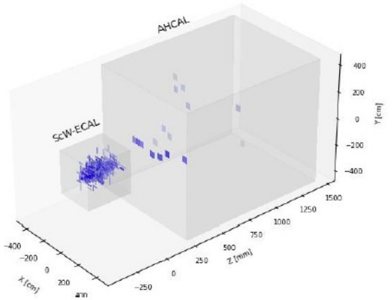
- ECAL Beam test : Sci-ECAL + AHCAL
  - SPS : H8 beamline, Oct 19 – Nov 2, 2022
    - mu+ : 108GeV/c(inadequate)
    - pi+ : 10, 15, 20, 30, 40, 50, 60,80, 100, 120GeV/c (~150K events each point)
    - e+ : 10, 20, 30, 40, 50, 100GeV/c (~150K events each point)
  - SPS : H2 beamline, Apr 26 – May 10, 2023
    - mu- : 100GeV, 120GeV (>3M events)
    - pi- : 10, 15, 20, 30, 40, 50, 60, 70, 80, 100, 120GeV/c (>100K events each point)
      350GeV/c
    - e- : 10, 20, 30, 40, 50, 60, 70, 80, 100, 120GeV/c (>100K events each point)
      150, 200, 250GeV/c
  - PS : T9 beamline, May 17 – 31, 2023
    - mu- : 10GeV/c
    - pi- : 1, 3, 5, 8, 10, 12, 15GeV/c
    - e- : 0.5, 1, 2, 3, 4, 5GeV/c




100GeV muon




350GeV pion




60GeV electron

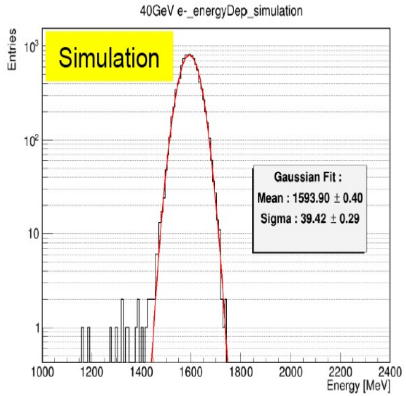
# SciECAL technological prototype

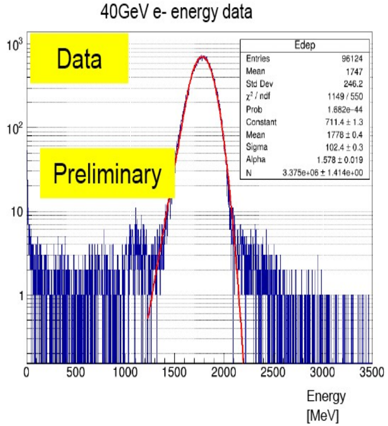
## Calibrations:

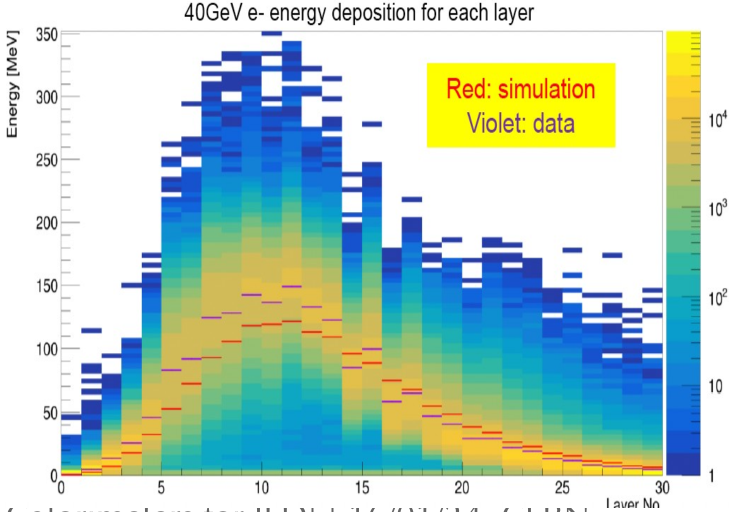
- Pedestal calibration
- High- & Low-gain intercalibration
- LED:
  - SPS: before, middle, after
  - PS: Everyday
  - HV adjusted ↔ temperature
- MIP (Muons)

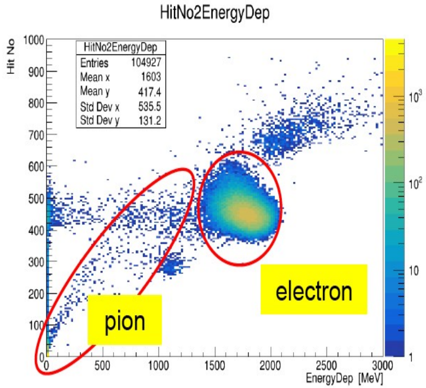
## Energy response

- 40GeV/c electron data from SPS H2
  - Calibrated with 100GeV muon data
  - Threshold: 0.5 MIP
  - No obvious energy leakage
  - Still contamination
- More effort to match data and simulation …



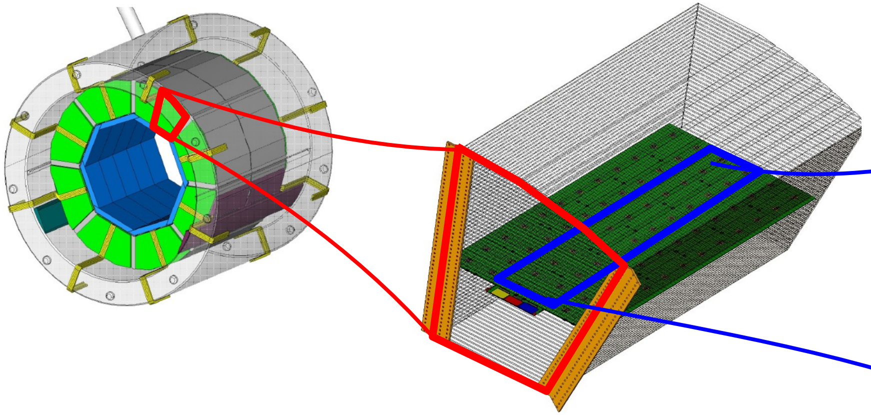



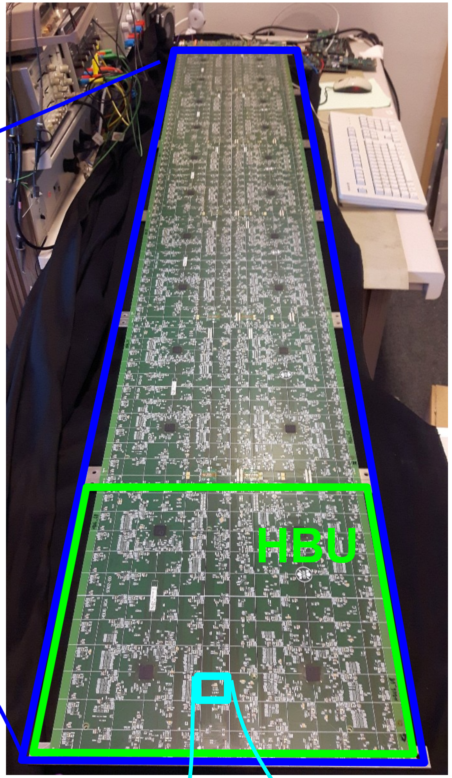



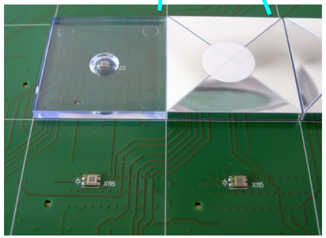



# AHCAL

# AHCAL Technological Prototype



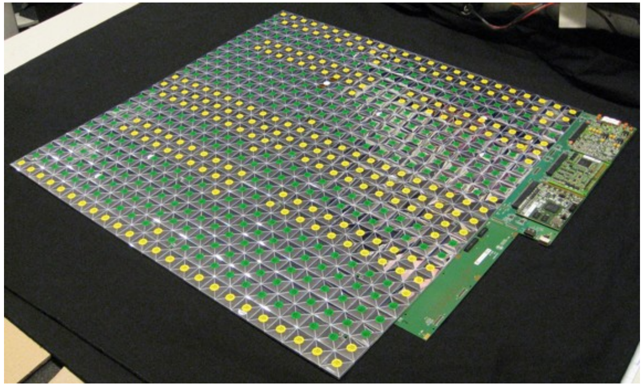


- highly granular scintillator SiPM-on-tile hadron calorimeter, 3*3 cm² scintillator tiles optimised for uniformity
- **fully integrated design**
  - front-end electronics, readout
  - voltage supply, LED system for calibration
  - no cooling within active layers -> **power pulsing**
- **scalable** to full detector (~8 million channels)
- geometry inspired by ILD, similar to SiD and CLICdp
- HCAL Base Unit: 36*36 $cm^2$, 144 tiles, 4 SPIROC2E ASICs
  - slabs of 6 HBUs, up to 3 slabs per layer

# AHCAL Technological Testbeam Prototype

- Large enough to contain hadron showers
  - 38 active layers of 72*72 cm²
  - 4 HBUs per module
  - in total: 608 SPIROC2E ASICs, ~22000 channels
  - SiPMs: Hamamatsu S13360-1325PE
- All modules interchangeable
- Built with scalable production techniques in ~2 years
- Operated in beam tests with muons, electrons and pions at CERN SPS in 2018
  - 3 weeks of beam time
  - Collected O(100) mio events
  - Very stable running
  - Nearly noise free
  - < 1 per mille dead channels

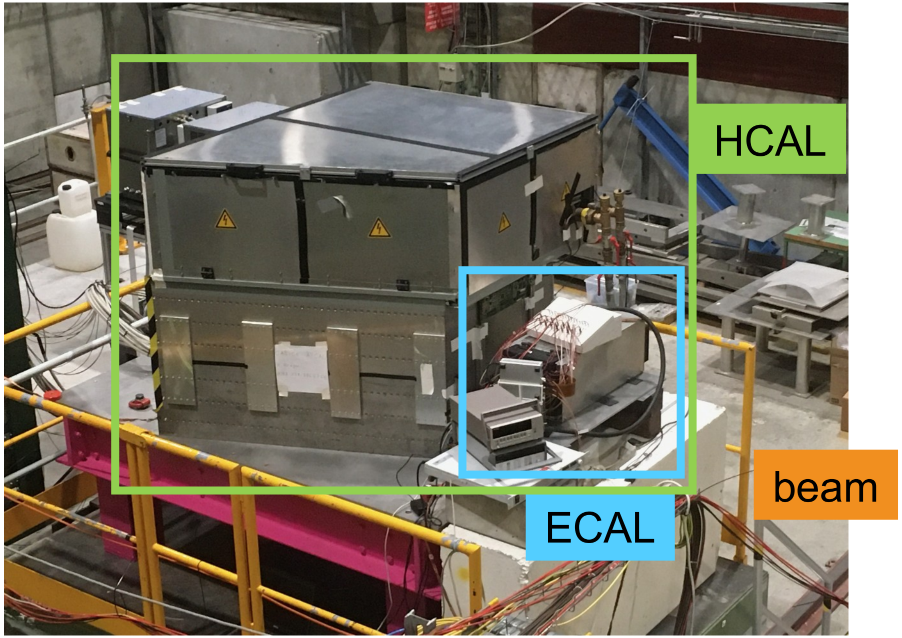


# Combined testbeam with CALICE SiW-ECAL

## 2 weeks of beam test at CERN SPS: 8-22 June 2022

- First common running of technological prototypes of SiW ECAL and scintillator AHCAL
  - 15-layer ECAL prototype, 5×5 $mm^2$ cells
  - 38-layer HCAL prototype, 30×30 $mm^2$ cells
- Successful synchronized data taking
- Muon data for calibration
- Energy scans for electrons and hadrons

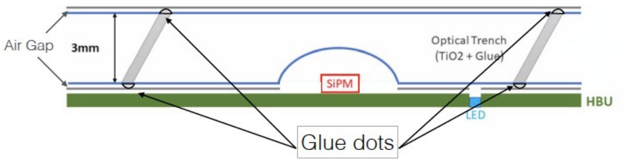
- Milestone in our program reached!
- Future beam test program to be defined
  - Tungsten stack available

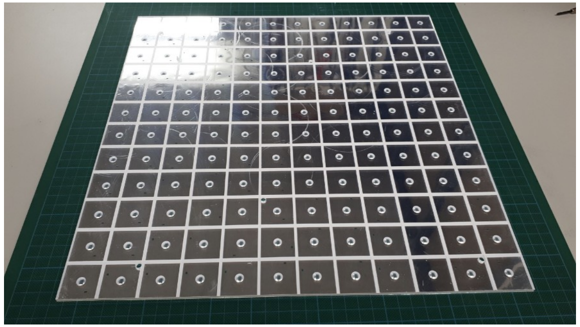


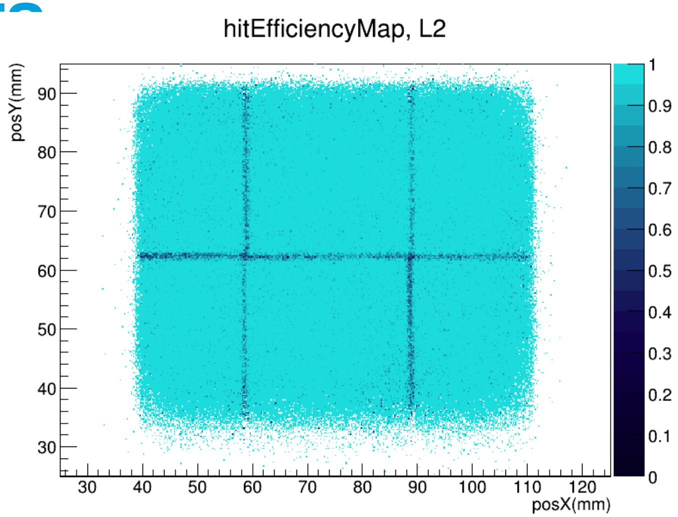
# AHCAL Plans: Hardware Developments

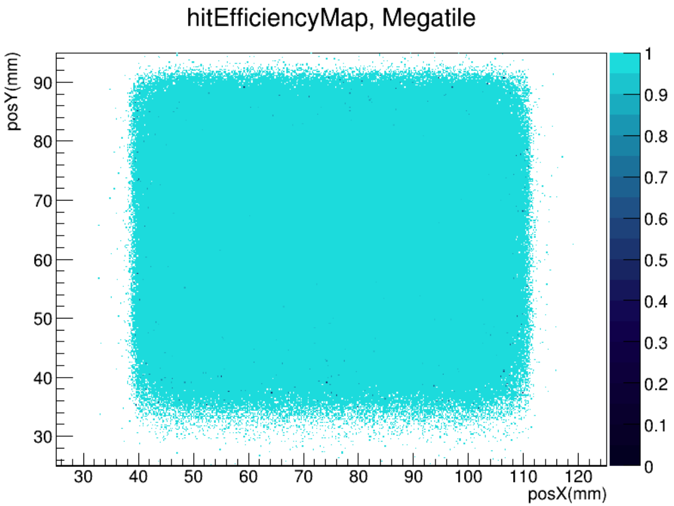
## Alternative scintillator geometry

- ILD will require two orders of magnitude more tiles than AHCAL prototype, one order more than CMS HGCAL
- Megatiles would allow larger units for mechanical assembly
- Challenge: reach good uniformity while keeping the cell-to-cell light cross talk small
- Status:
  - Several generations of Megatiles produced
  - Last one shows reasonable uniformity and light yield, working on optimization of edge cells
  - One Megatile HBU included in 2022 testbeam setup
  - Plan to build a 2*2 HBU layer to study also Megatile-Megatile transition region





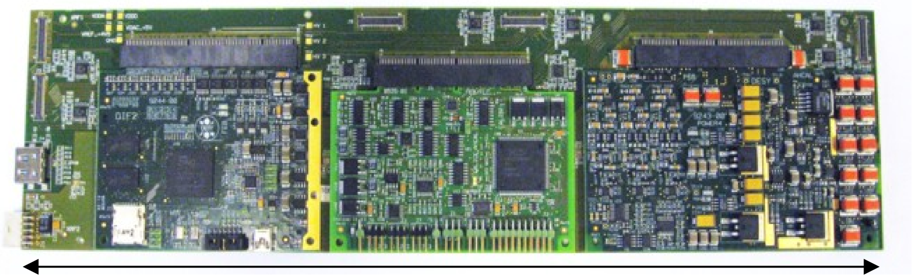



# AHCAL Plans: Hardware Developments

## Common Readout

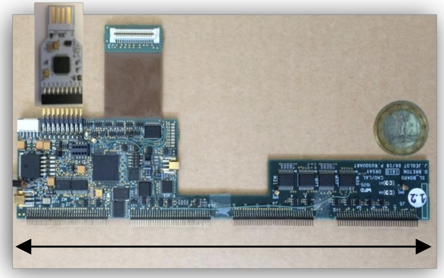
- Harmonise readout between CALICE SiW ECAL and AHCAL
- Reduce size of AHCAL interface boards
  - Current design is from 2007
  - Focus was on modularity
  - New SiW ECAL interface board (SL board) optimized for compactness
  - Plan to follow SiW design as much as possible
    - Some differences in powering concept
    - Additional LED calibration system in AHCAL
- Status: just started

AHCAL interface boards



36 cm

SiW ECAL SL board



18 cm

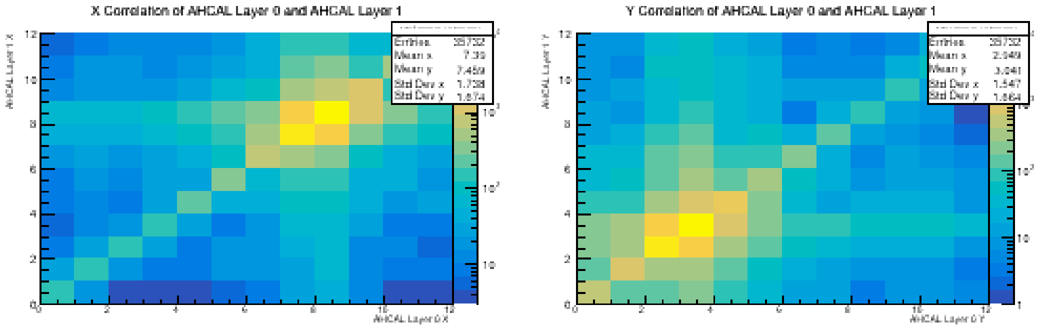
AIDA innova

# AHCAL Plans: Hardware Developments

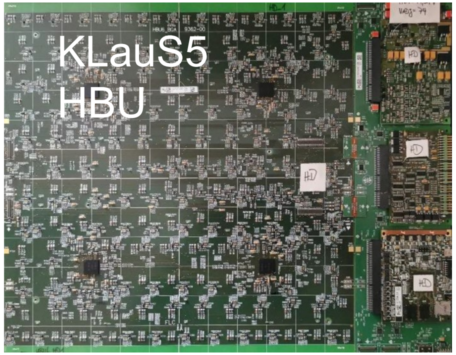
## Alternative Readout ASIC (KLauS)

- Wide range of applications
- Possible application at circular Higgs factories
- Optimised for SiPMs with small pixels (10µm) -> possible application in scintillator ECAL
- Status:
  - First HBU with KLaus5 operated within AHCAL DAQ
  - KLauS6 with full functionality available


SPIROC HBU




KLauS HBU



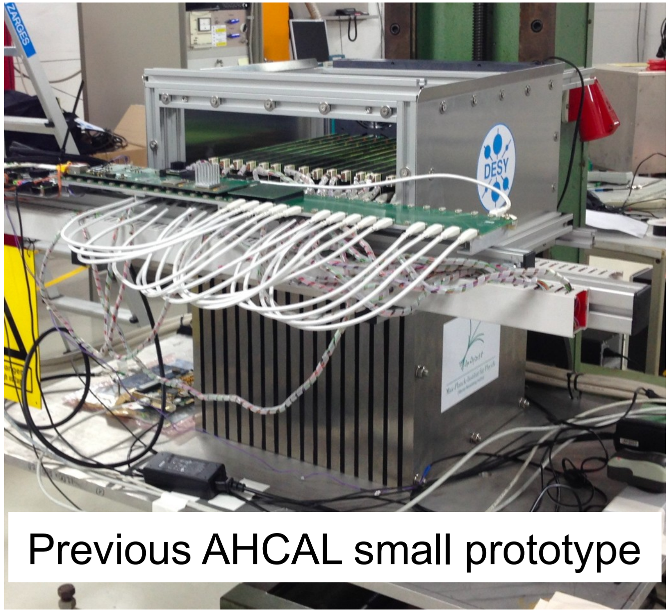
# AHCAL plans: towards continuous readout

- Main R&D topics: Re-design of the full readout and powering chain for continuous read-out, data rates and possible trigger requirements of circular Higgs Factories
- development of appropriate electrical, thermal and mechanical integration concepts.
- Tentative timescale
  - Concept for continuous readout 2024
  - First layer with continuous readout 2025
  - EM prototype demonstrating system aspects 2026
  - Full-size layer and multi-layer demonstrator >2026
  - Engineering prototype >2026

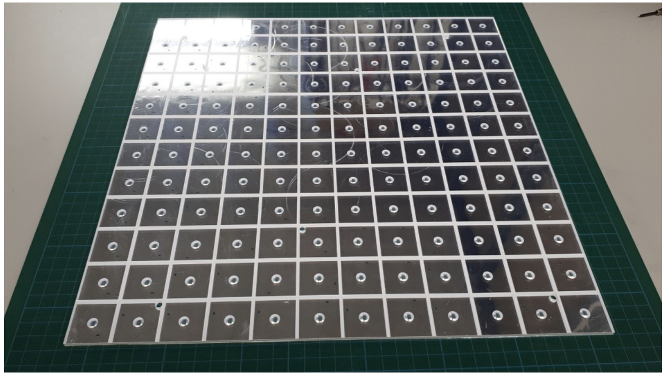
# DRD plans for AHCAL

- Build a small AHCAL prototype with continuous readout with hit timing capability

- Task sharing between institutes working on AHCAL
  - Front-End ASIC (HD)
  - Back-End / DAQ (KIT, Mainz)
  - Megatiles (Mainz)
  - Mechanics & Cooling (Mainz, HD, DESY)
  - Common tasks: software, testbeams, analysis, …



Previous AHCAL small prototype

# T-SDHCAL

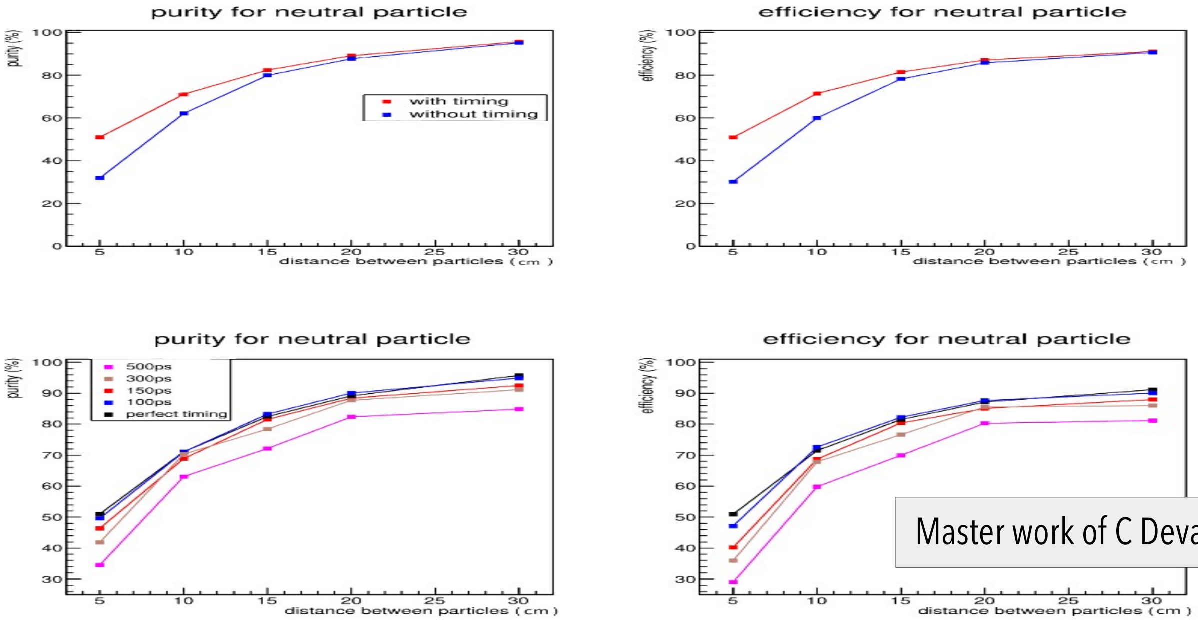
# SDHCAL → T-SDHCAL

## Power issues ?

- RPC :
  - Rates OK for RPC ?
  - Cooling possible with gas
    - (flow to be determined from uniformity of response :
    - heat/laminar flow )

## Timing

- recent studies show time information could improve significantly hadronic showers separation at lower distances.




Master work of C Devanne

# SDHCAL → T-SDHCAL

It consists of a few steps:

1) Replacing the RPC with **MRPC:**

Low resistive materials could /should be used to increase the rate
(Low resistivity glass, PEEK doped with CarbonNanoparticles)

→We need to study how many gaps taking into account the cost on the cassette thickness

2) Replacing the Hardroc with a new ASIC (continuous readout + Internal TDC)

→We started with PETIROC but we need to go further (Liroc+TDC)

3) Developing a cooling system.
The cooling system should not add too much dead zone.
Could we use it with the present SDHCAL mechanical with limited efforts?

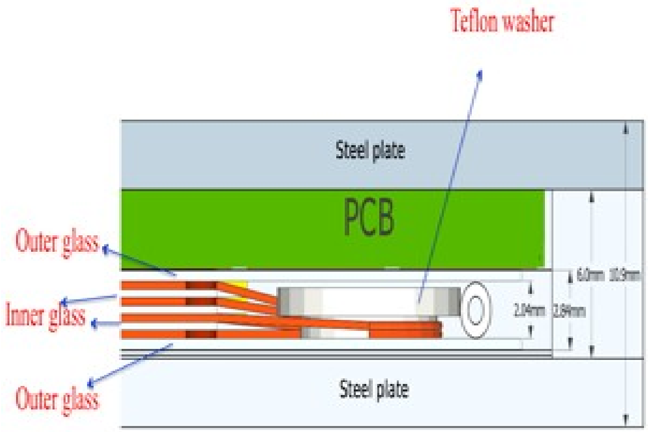
→ we have already some studies on this topic

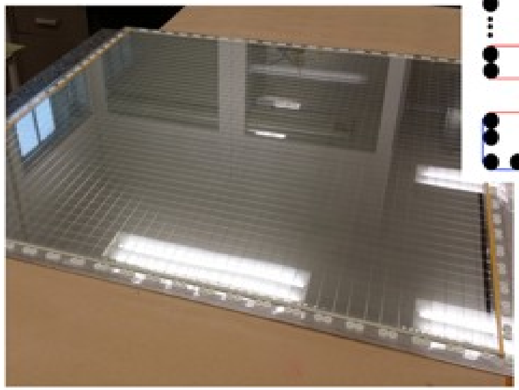
# SDHCAL: MRPC's

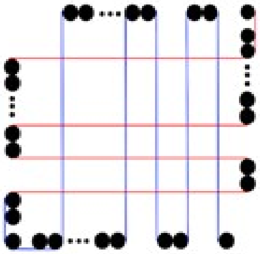
We built small and large 4-gap RPC of 1 m2 using fishing lines. Efficiency > 92%

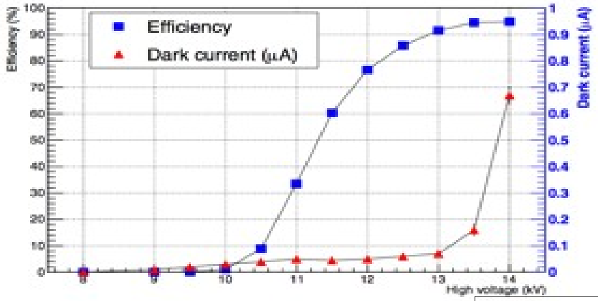
We built small and large 4-gap RPC of 1 m2 using a new technique that renders the fabrication process if very easy.  First results show good efficiency (> 90%)

Excellent time resolution obtained with small size MRPC (Guillaume's talk) using eco-friendly gas mixture








Threshold sets at 114 fC

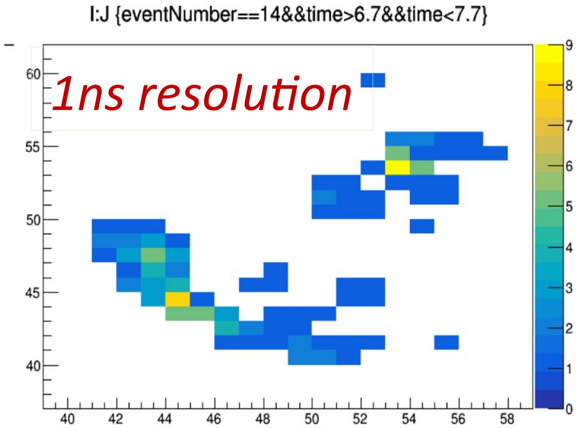
HV / kV

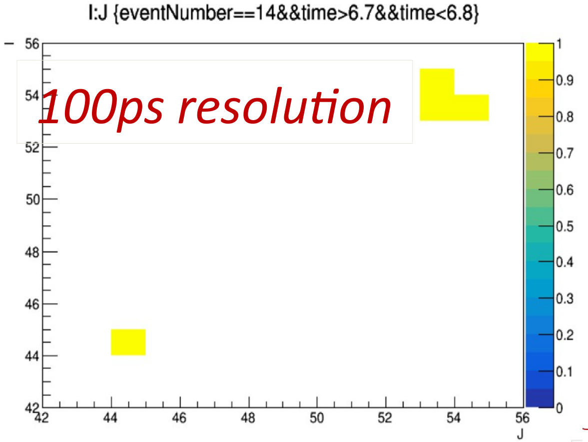
# Introduction of Timing Electronics

- Timing information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.
- Method: Adding some mRPC layers in the SDHCAL
- Front-End Electronics for mRPC readout
  - **High resolution timing measurement**


- Time measurement with 10 bits TDC interpolating 40MHz clock
- Timing resolution below 40 ps
- 32 input channels
- Power consumption: ~6mW/channel

Example: Pi-(20 GeV), K-(10 GeV) separated by 15 cm



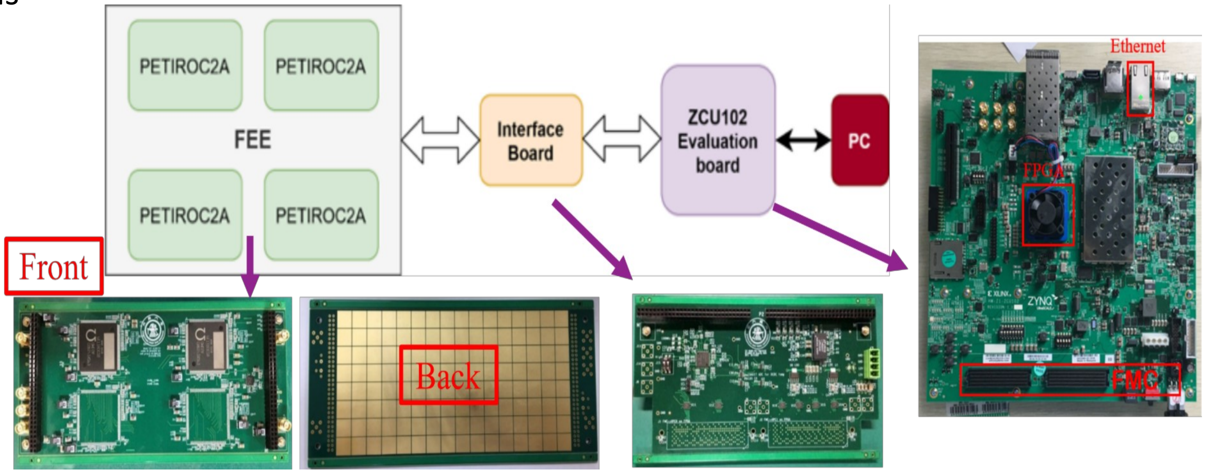



# T-SDHCAL: Readout electronics

**PETIROC** was proposed for iRPC@CMS. Excellent performances are obtained with doublet RPC using pickup strips

We designed small ASU with pickup pads ($1 \times 1$ cm$^2$):
$\sigma(t)$ ~ 50 ps on injected signals and 2 small MRPCs coincidence obtained at SJTU
see presentation of Weihao Wu, CALICE sept 2023 @ FZU for details

Larger ASUs hosting PETIROC have been designed and will be soon be produced with ($1.5 \times 1.5$ cm$^2$) pads



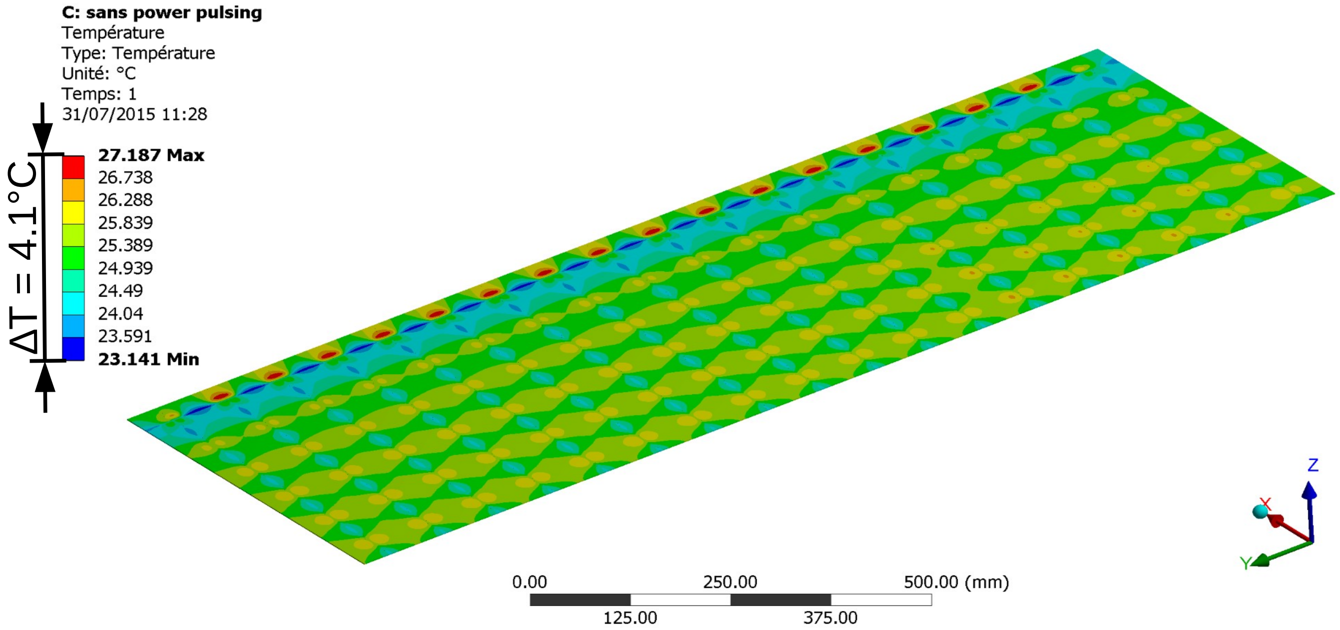

Within the DRD6 project we would like to develop the **Liroc+internal TDC**

# T-SDHCAL: cooling & rates

**Cooling:**

Previous studies were performed on Hardroc (full regime)

We have to do the studies with the new ASICs and the mechanical structure in mind




**High-rate capability**

Low resistivity materials

Low-resistive PEEK ($10^9\ \Omega\cdot$cm)

# SDHCAL: next steps (2024)

Large MRPC equipped with PETIROC (1 or 2 $m^2$)

Cooling system

New cassette

Also find resources to finalize DAQ system for HR3.

# Conclusions

**Work has started in many places:**

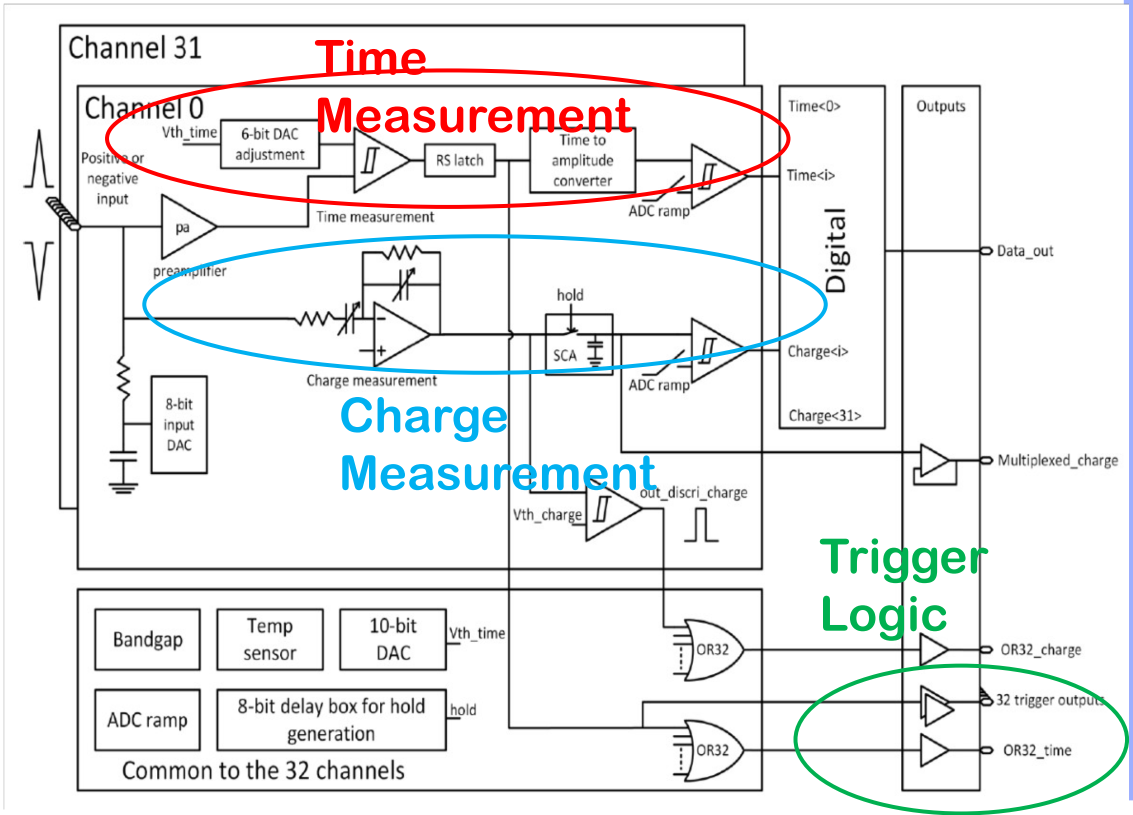
1) Electronics [see Christophe presentation] and AHCAL
2) Estimation of rates
   ➞ dynamic ranges, DAQ scaling, power due to data handling (conversion, storage, transfer)
3) PFA with timing
   1) Precision to be optimised wrt physics performance; check work done for CEPC CDR
   2) Funding in France (ANR) and Germany (DPG) for studies ➞ next 3 years
4) Cooling schemes :
   1) Diphasic CO2 in ECAL ?
   2) Gas in T-SDHCAL ?
   3) Water in AHCAL ?

   Exact scaling depends on electronics, granularity, precision

   What are the constraints on $\Delta T$ from tracking (TPC) ?

# Extras

# Petiroc2B ASIC




*from Petiroc datasheet v2.5a

- A 32-channel front-end ASIC designed for SiPMs readout (mRPCs as well).
- Charge and timing measurement
- 40 ps bin size of on-chip TDC
- Readout time: 12us
- Fast trigger line
- Dynamic Range 0-480 pC i.e. 3000 photoelectrons @ 10^6 SiPM gain
- Fast fixed gain (40) inverting voltage preamplifier
- Slow shaper with adjustable shaping time from 25 to 100 ns
- Charge measurements by Track&Hold
- Power consumption 6mW/channel