Adapting the ILD vertex detector to FCCee context and related R&D

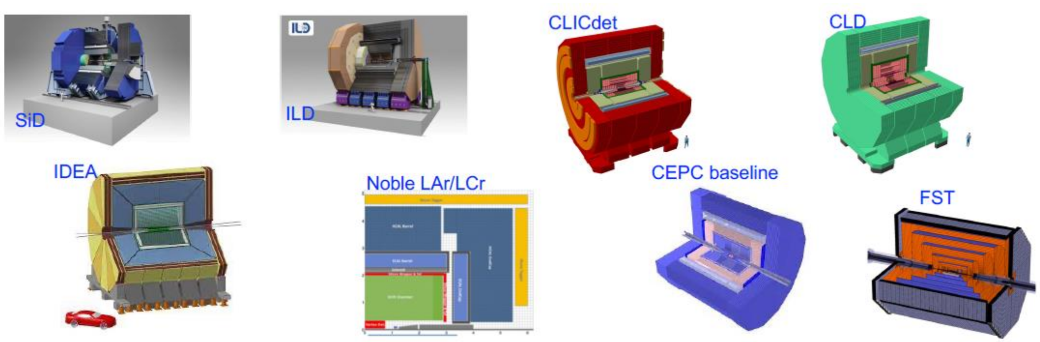
FCCee requirements and needed changes

Comparison with other concepts

R&D within DRD3/7 framework

Tracking/vertexing detectors in future e^+e^- colliders

Collider	ILC		CLIC	FCCee			CEPC	
Bunch separation (ns)	330/550		0.5	20/990/3000			25/680	
Power Pulsing	yes		yes	no			no	
beamstrahlung	high		high	low			low	
Detector concept	SiD	ILD	CLICdet	CLD	IDEA	Lar	Baseline	IDEA
B Field (T)	5	3.5	4	2	2	2	3	2
Vertex	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel	Si-Pixel
Vertex Rmin (mm)	16	16	31	~12	~12	~12	16	16
Tracker	Si-strips	TPC	Si-Pixel	Si-Pixel (+RICH ?)	DC/Si-strips	DC/Si-strips or Si-Pixels	TPC or Strips	DC/Si-strips
Tracker Rmax (m)	1.25	1.8	1.5	2.2	2.0	2.0	1.8	2.1
Disks layers	4 + 4	2 + 5	6 + 7	3 + 7	3 (150 mrad)		2+6	

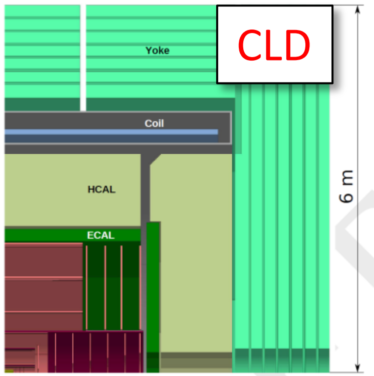


(From D. Dannheim)

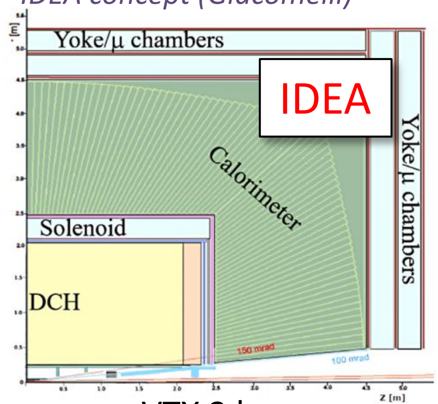
Large similarities between the concepts but also significant differences

Detector concept & vertexing/tracking

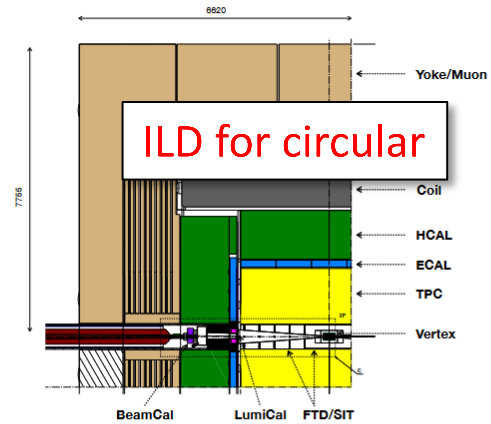
ILD & CLD concepts (Poeschl)



IDEA concept (Giacomelli)



ALLEGRO concept (Aleksa)



- Inspired from CLICdet
- « Full Silicon »
- Possibly + RICH
- Calo. inside coil

- VTX 3 layers
- Calo. outside coil
- Drift Chamber
- Si wrapper

- VTX: 3 double layers
- Calo. inside coil
- TPC ?

- VTX ⇨ Silicon pixels (CMOS-MAPS)
- Added dedicated timing layer ?
- Shared concerns: MDI, beam background, integration, cooling, etc.

Physics program priorities
√s

Defining the figure of merits

Vertexing
Tagging capabilities (b,c, τ, s)
Impact parameter resolution
Standalone tracking capabilities
Low pT tracking
Vertex charge determination
Hit/track separation
Displaced vertex (LLP, etc.)
Acceptance

Tracking
Tracking efficiency/fake tracks
Momentum resolution
Charge determination
Robustness/redundancy
Association with calo. clusters

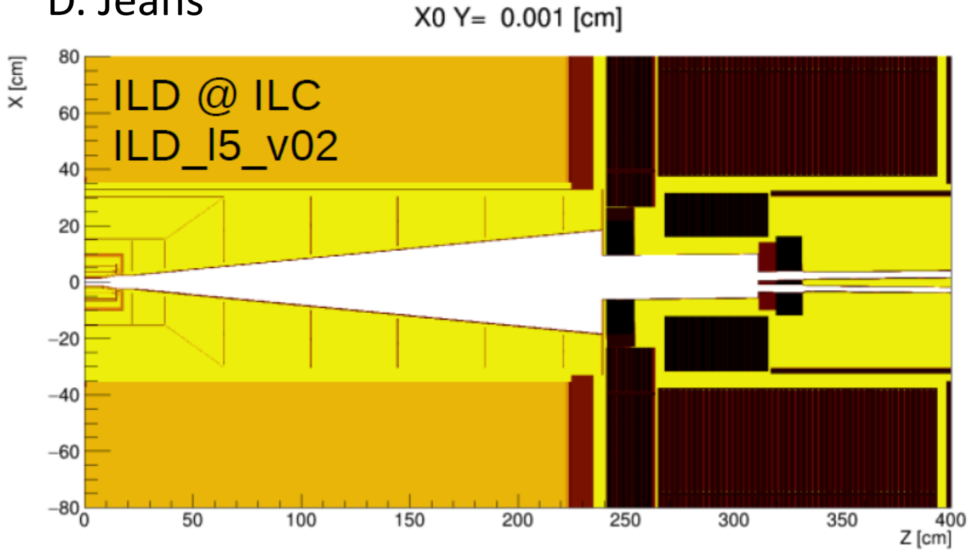
Particle ID
dEdx
Timing measurement
RICH

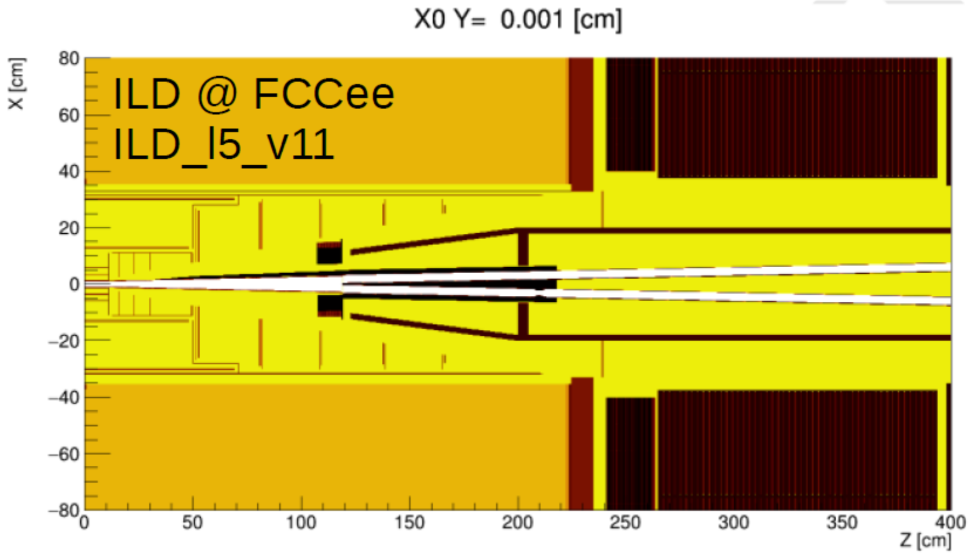
Vertex/inner tracker main differences between ILC and FCCee

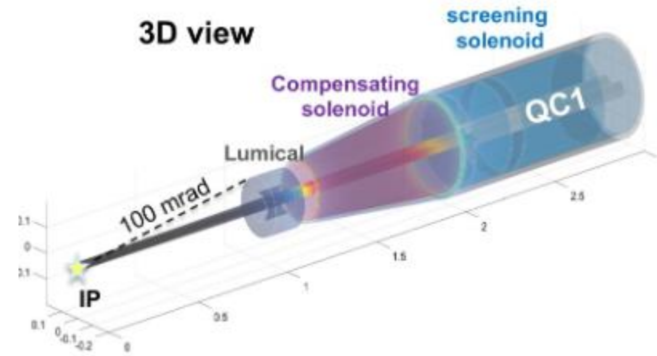
	ILD in ILC	FCCee	Consequence
Magnetic Fields	3.5 T +anti-DID ?	2 T (mandatory @√s=90GeV)	• pT resolution • Min pT to reach layers • Level arm optimization ?
Beam time structure	2 ms between trains	~ Continuous	• No Power Pulsing allowed ⇨Power management more challenging
BX time	~300 ns	20 ns (90GeV) / 1 µs (250 GeV)/ 3 µs (350GeV)	• Single bunch timing capabilities depend on √s
Beam background	e+e- pairs drive occupancy Cryostat + Faraday cage	Lower beamstrahlung rate Higher Synchrotron radiation	• Time resolution not driven by beam background • Allows beam pipe radius reduction • Cooled beam pipe + Gold coating • Remove Cryostat ?
Beam pipe radius	~15 mm	~10 mm ?	• Lower radius can compensate thicker beam pipe
L* (IP-Quad magnet distance)	4.1 m	2.2 m	• Forward tracker geometry • Former worse forward tracker acceptance @FCCee now compensated by reduced beam pipe radius
Crossing angle	14 mrad	30 mrad	
Forward tracker acceptance	~ 90 mrad	150 mrad ⇨ ~ 100 mrad	
Z pole running ? # of detectors	Optimized for √s = 250 GeV and beyond	Different possible √s optimizations	• @ Z pole, Very small stat. Uncertainties call for very small syst. Uncertainties • Large physics event rate (100 kHz)

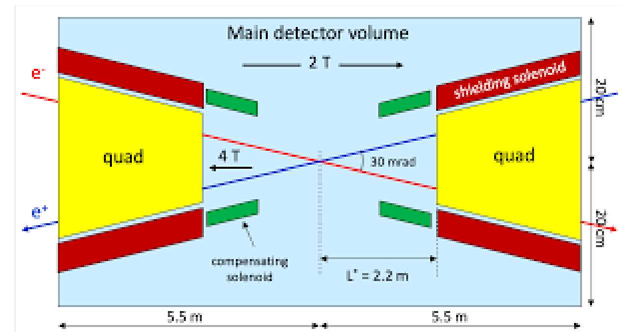
MDI – Forward region

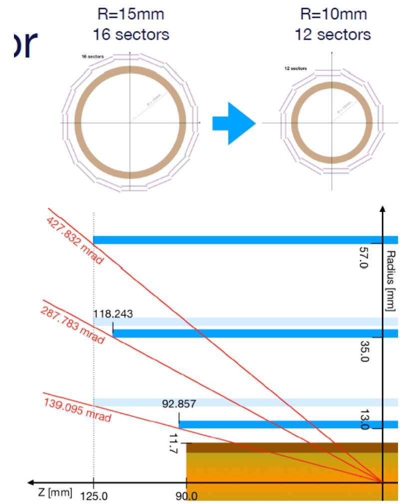
D. Jeans







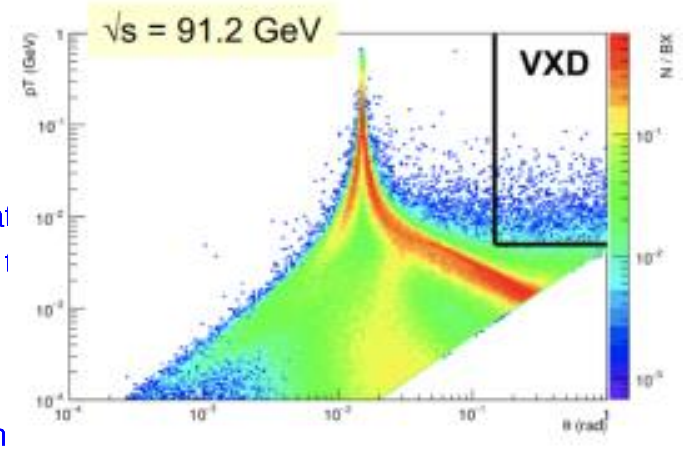




- Common constraints for all detecto concepts
- Forward tracker acceptance fixed @ ~100 mrad ?
- Disk geometry modified
- Barrel/disk border modified by beam radius reduction

Beam related Background

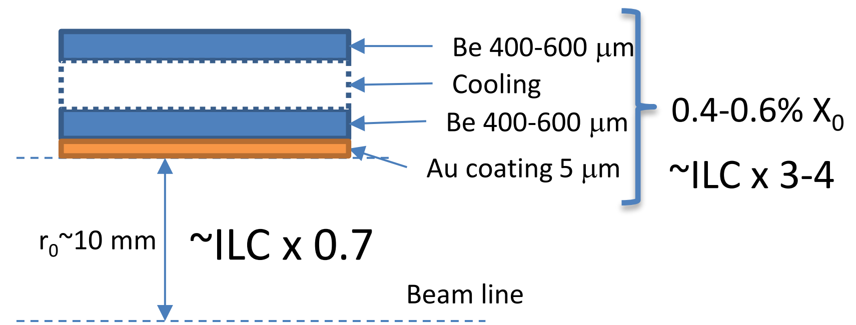
- Usually one considers that occupancy ~< 10^{-2}-10^{-3} is safe for tracking/vertexing
- FCCee rate estimate
  - ✓ Gold coating + beam pipe cooling necessary to cope with synchrotron radiat
  - ✓ e+e- pairs occupancy (with 1 μs time resolution) ~< 10^{-4} (possibly higher at t pole)
    - Less severe for circular (⇨Rmin reduction ~10mm))
- Experience from ILC studies over 20 years
  - ✓ Any modification in the Interaction region (beam scheme, beam pipe design field) might bring surprises
  - ✓ One should not consider that a 10^{-4} occupancy estimation means that there is no issue.
    - The robustness is questionnable
    - Large possible variations in some acceptance corners (asymmetries in φ or z)
    - Safety factor absolutely mandatory
    - 2 independant simulation tools would be welcome (GuineaPig, Fluka, etc.)
- Experience from Belle-2
  - ✓ Discrepancies observed between simulations and first collisions
    - (cf. backup slides)
- Direct beam background vs backscattered background
  - ✓ Generally the backscattered ones are more sensitive to any MDI change.
- What about timing information to reject background ?
  - ✓ Need ~ 5 ns to reject backscattered particles
  - ✓ Is it worth paying the price in terms of additionnal power ?
- What about cluster shape to reject background ?
  - ✓ Need very good sensitive thickness/pitch ratio (> 2)



$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.\,sin^{3/2}\theta}\right)^2$$

$$a \sim \sqrt{r_0}$$

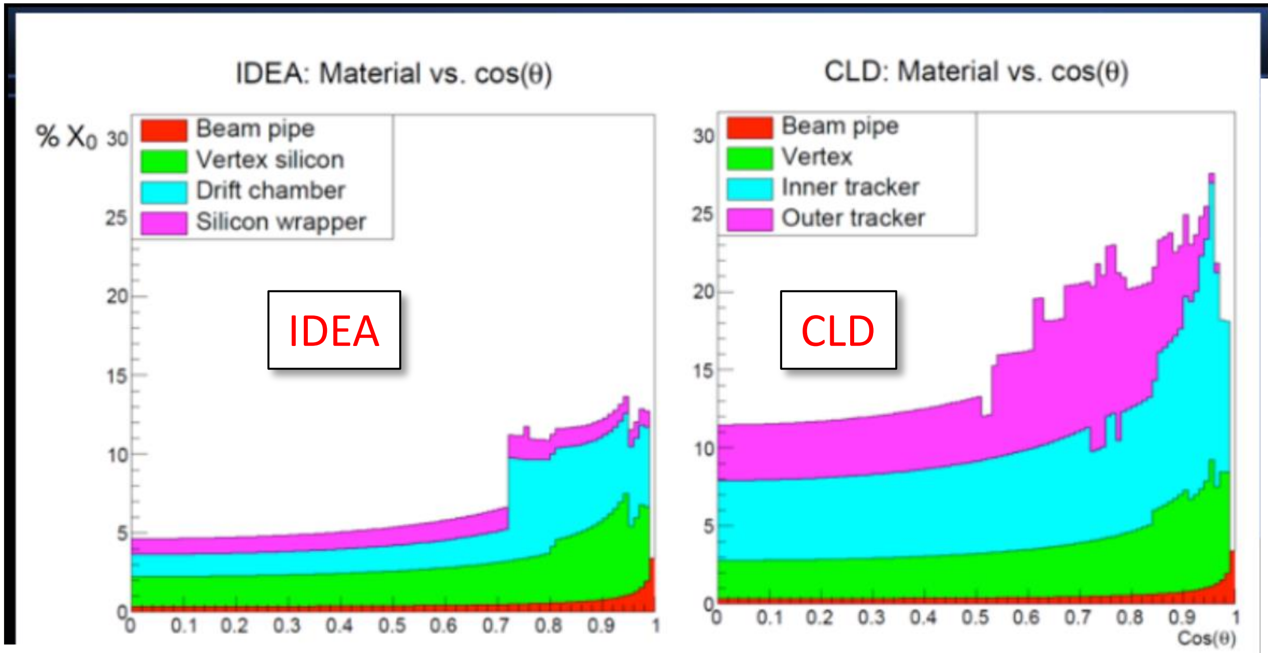
$$b \sim r_0\sqrt{material}$$



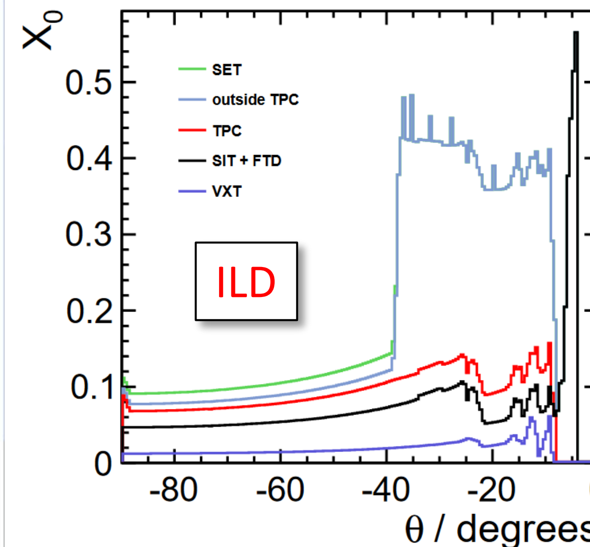
$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}} \sqrt{1 + \frac{1}{2}\left(\frac{r_0}{L_0}\right) + \frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}} \sqrt{1 + \frac{8r_0}{L_0} + \frac{28r_0^2}{L_0^2} + \frac{40r_0^3}{L_0^3} + \frac{20r_0^4}{L_0^4}}$$

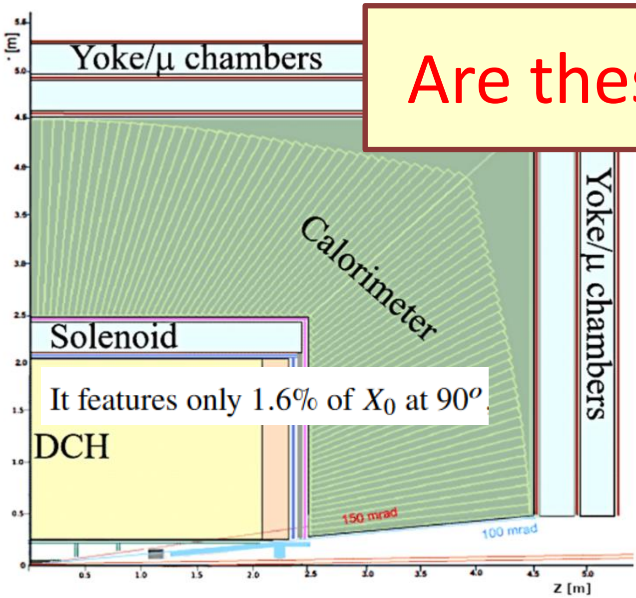
Material budget discussion

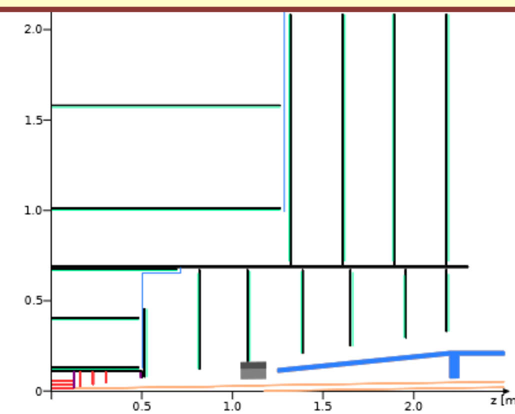


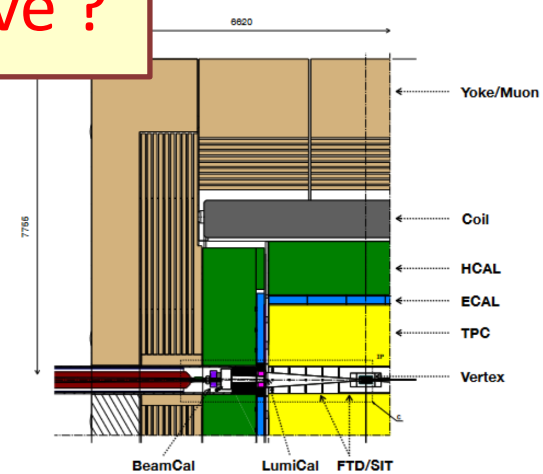
ILD material



Are these estimates conservative ?







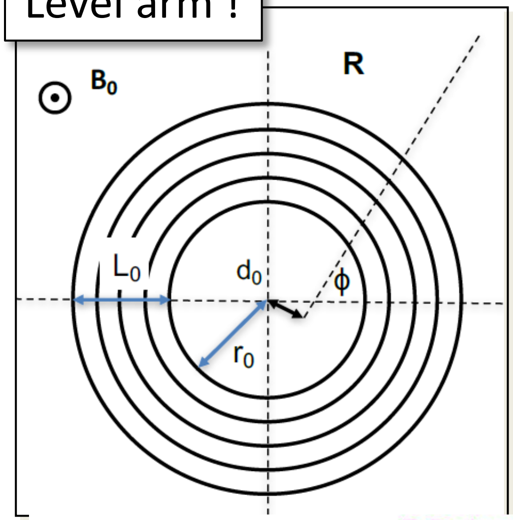
https://pos.sissa.it/414/337/pdf

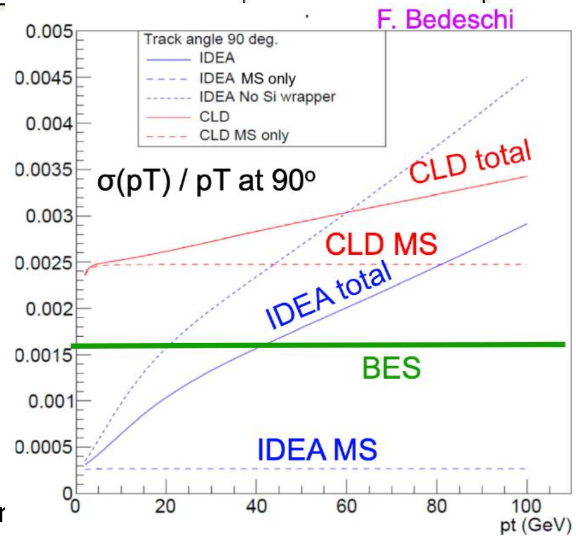
Tracker requirements

Expected performances

$$\frac{\sigma_{p_T}}{{p_T}^2} \sim 2 \times 10^{-5} GeV^{-1}$$

Level arm !





Physics
- ⇨ Momentum resolution
- ⇨ Tracking efficiency
- ⇨ Track separation, low fake tracks
- ⇨ Etc.

- Level arm also plays a crucial role for the VTX

- Material budget vs intrinsic resolution
  - ✓ Typically σ_{sp} ~5-10 μm/layer ; material ~1-2% X_0/layer ; Power ~< 100 mW/cm²
  - ✓ Low momentum vs high momentum ⇦ physics input
- 2 main options:
  - ✓ All silicon (CLD, CLICdet, SiD)
    - Few high resolution layers
    - Possibly timing capabilities
  - ✓ Silicon + Gazeous detector
    - TPC (ILD) / Drift Chamber (IDEA) / RICH (CLD ?)
    - dEdx/dNdx capabilities,
    - More hits, overall less materials
    - TPC: Ion back flow issue for circular colliders
- PID Strategy to be included (RICH, timing, dEdx, etc.)

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

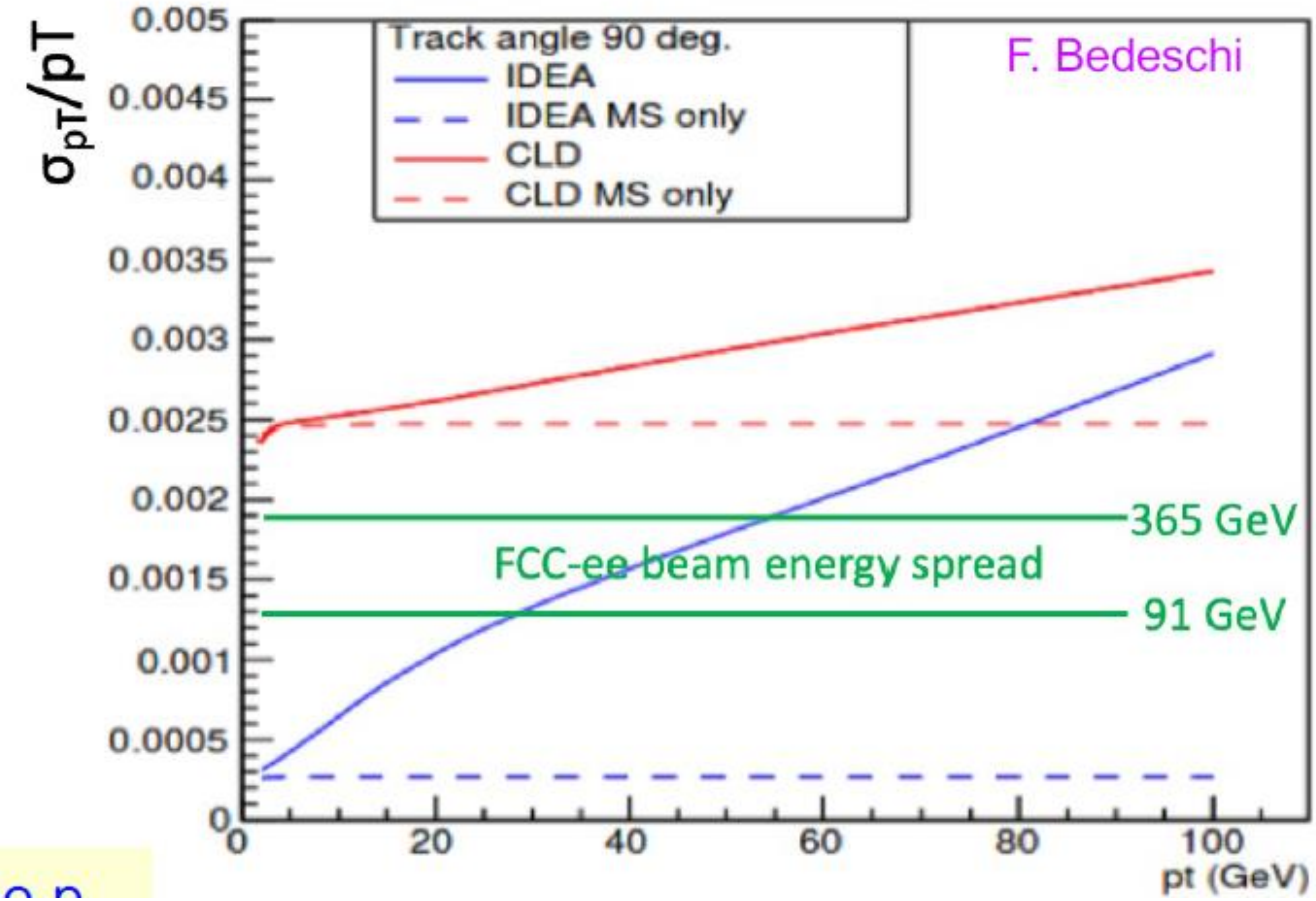
$$d_{tot}/X_0 = (N+1)d/X_0.$$

d = layer thickness, N = # layers

$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{0.3\beta\,B_0 L_0}\sqrt{\frac{d_{tot}}{X_0\,\sin\theta}} \qquad \frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\,p_T}{0.3\,B_0 L_0^2}\sqrt{\frac{5}{N+5}}$$

m.s. term dominates for pT ~< O(100) GeV/c

CLD / IDEA



Are these estimates comparable ?

Feasibility studies @FCCee

Vertex detector: work ahead & preliminary conclusions

Work in progress: requirements from heavy-quark EW measurements

L. Rohrig,
S. Monteil

Preliminary conclusions

- Two examples have been shown where the physics outcome of FCC-ee would gain from having better vertex detector performances than the one provided by the baseline detectors considered so far.
- Engineering studies indicate that the material of the vertex detector layers, compared to that of the baseline IDEA detector, can realistically be achieved. Special care is taken in designing the beam-pipe and its cooling system, in order to minimise the amount of material in front of the vertex detector [164, 826]. Ongoing R &D efforts to decrease the material budget are starting and will be ready for the final report – for example, the ITS3 design [843] indicates that reducing further the material is possible.
- It should be noted that these requirements, tighter than the ones presented for a linear collider detector, will have to be reached despite the additional constraints set by the FCC-ee environment on the readout electronics of the detector: (i) its power budget is tighter than for a detector operating at a linear collider (since power-pulsing the electronics is not possible with collisions occurring every ~ 20 ns); and (ii) it should be fast enough, better than about 1 µs, such that the integrated background remains negligible [826].

22.11.23 8 E.Perez

Preliminary conclusions

The performance of a gaseous tracker and of a full silicon tracker have been shown and quantified in several examples.

- Having a very large number of measurement points along the tracks, as offered by a gaseous tracker, is crucial for an efficient reconstruction of K_s, Λ's or other long-lived particles that decay into charged particles, and will be a clear bonus for an experiment with a stronger focus on flavour or BSM physics.

The momentum resolution offered by both designs looks adequate for Higgs measurements. This statement probably holds as well for most electroweak measurements, with the notable exception of the Z width measurement. For flavour physics at the Z peak, where lower momenta tracks are involved, a low mass, gaseous tracker is advantageous since the momentum resolution is minimally affected by multiple scattering.

Optimisation studies are ongoing to further improve the momentum resolution of the CLD tracker.

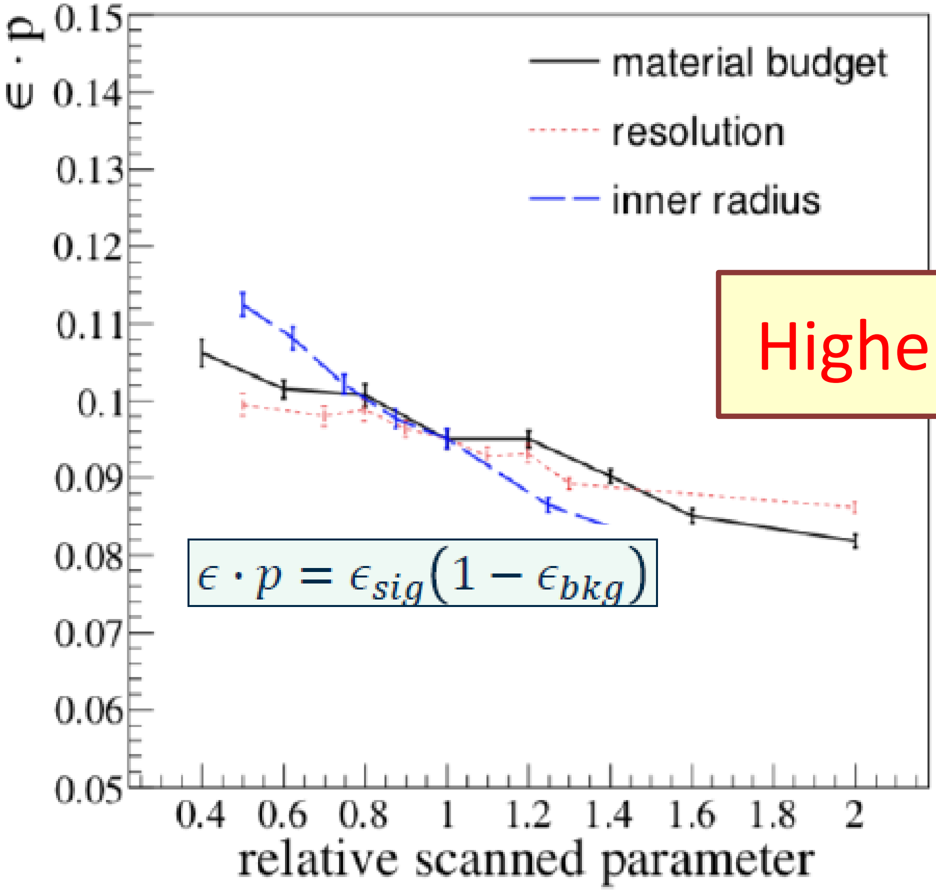
The tracker volume, that extends to a radius of about 2 m, may have to be reduced a little in order to free some space to accommodate a dedicated detector for charged-hadron particle identification (see Section 8.4.6), in particular for the CLD tracker. A reduction by $\mathcal{O}(20)$ cm would have some impact on the momentum resolution, which may be partly compensated by reducing the amount of material in the CLD tracker layers.

2.11.23 13 E.Perez

expected Recommandation: focus on material budget

CEPC vertex detector optimization

c-tagging: Detector optimization for CEPC

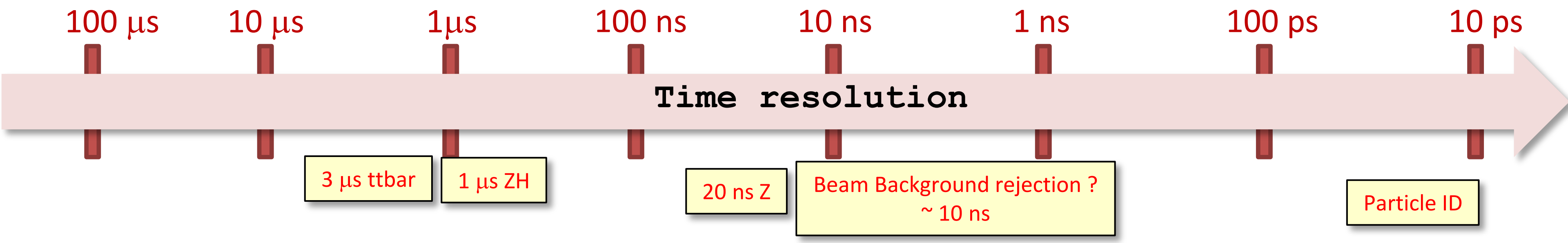


Higher dependance to mat. budget

M. Ruan, **ECFA WG3: Topical workshop on tracking and vertexing**

https://indico.cern.ch/event/1264807/contributions/5344222/attachments/2655752/4599314/ECFA-2.pdf

Timing & 4-D tracking



- Time resolution Δt
  - ✓ Bunch separation (3 μs / 1 μs / 20 ns @ FCCee)
  - ✓ Background rejection ? (1-10 ns range)
  - ✓ Particle ID (10-100 ps)
- Usual drawbacks to go faster
  - ✓ Power consumption
  - ✓ Active Cooling & geometrical acceptance due to services
  - ✓ In pixel circuitry ⇨ larger pixels (or multipixels)
  - ✓ Fill factor, dead time
  - ✓ PID Restricted to low momentum particles (~< few GeV/c)
- Still
  - ✓ Forward region not covered by a central gazeous detector (TPC)
  - ✓ Added value for intermediate radii (e.g. LLPs ?)
- Specialized layers
  - ✓ Doesn't compromise the other requirements (material budget and granularity)
    - Probably not in the most inner layers

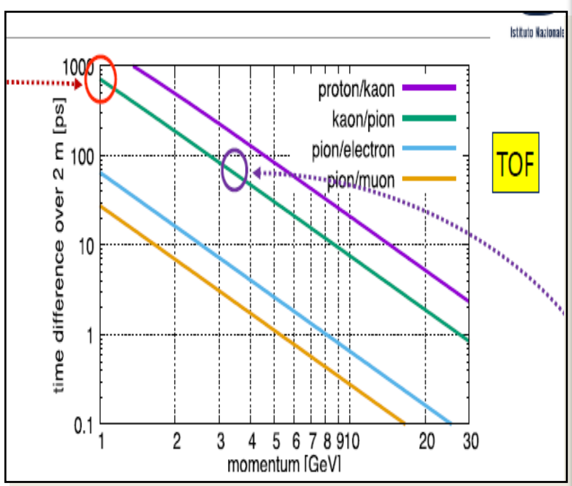
Particle ID and time resolution DRD4 & 1/3

More details here: https://indico.cern.ch/event/1202105/contributions/5402790/attachments/2662086/4612032/FCC-DRD4.pdf

- Goal:
  - ✓ K/π, π/e⁻ separation, etc. ⇨ Interest to push beyond 10 ps resolution
  - ✓ Even more important for the physics program @ Z peak

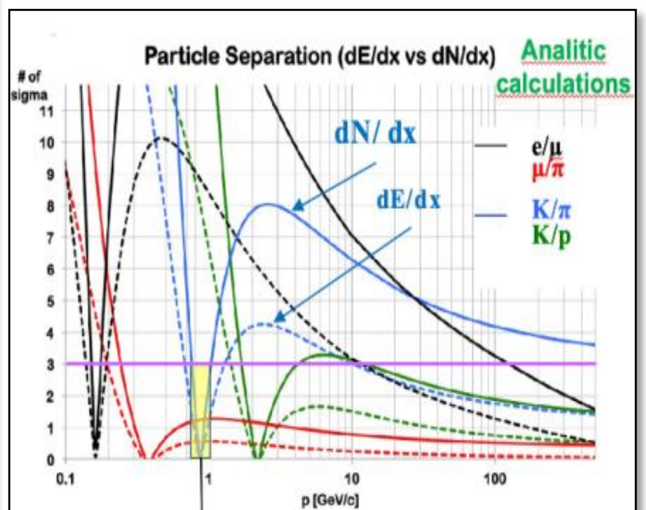
Fast timing (<100 ps) Solid state (pixelated) detector (DRD3)	dE/dx + dN/dx Mainly gazeous detector, e.g. TPC, DC, RICH (DRD1)

Time difference (ps)



Time of Flight

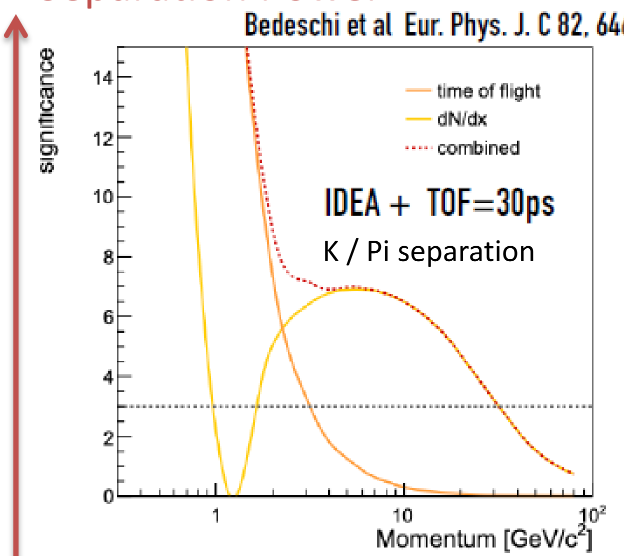
Separation Power (significance)



dE/dx – dN/dx

Separation Power

Bedeschi et al Eur. Phys. J. C 82, 646



Combined measurement

Momentum (GeV/c)

Particle ID and time resolution DRD4 & 1/3

More details here: https://indico.cern.ch/event/1202105/contributions/5402790/attachments/2662086/4612032/FCC-DRD4.pdf

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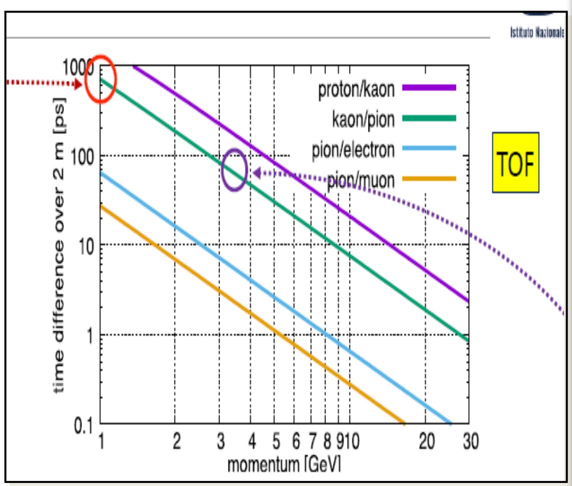
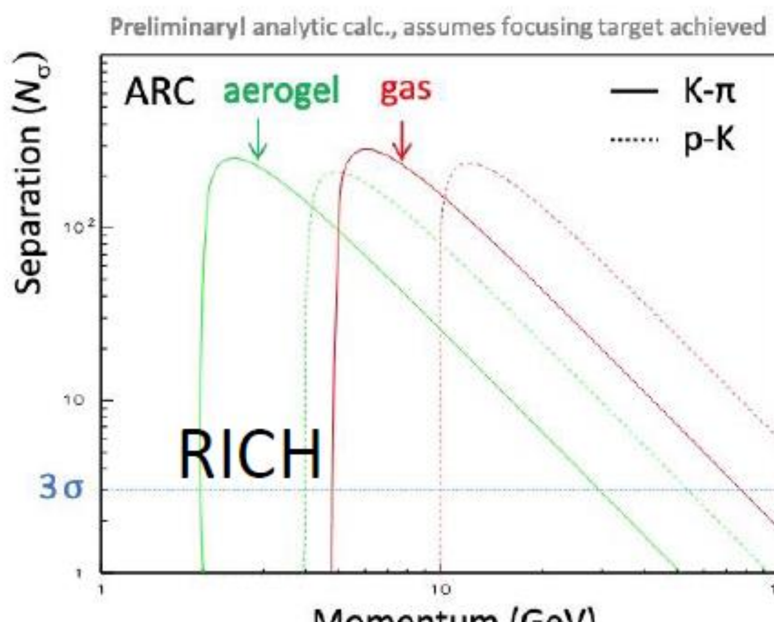
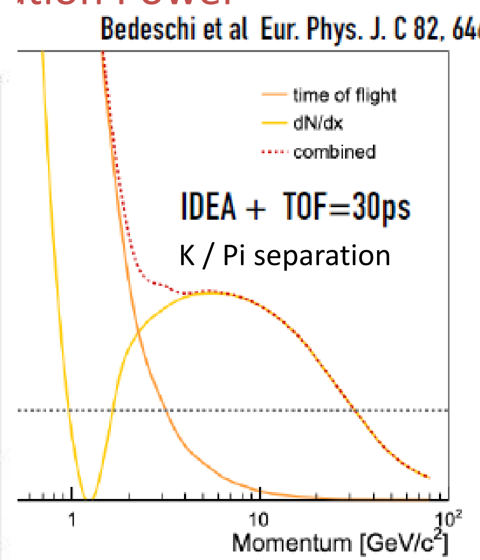


Time of Flight

Separation Power

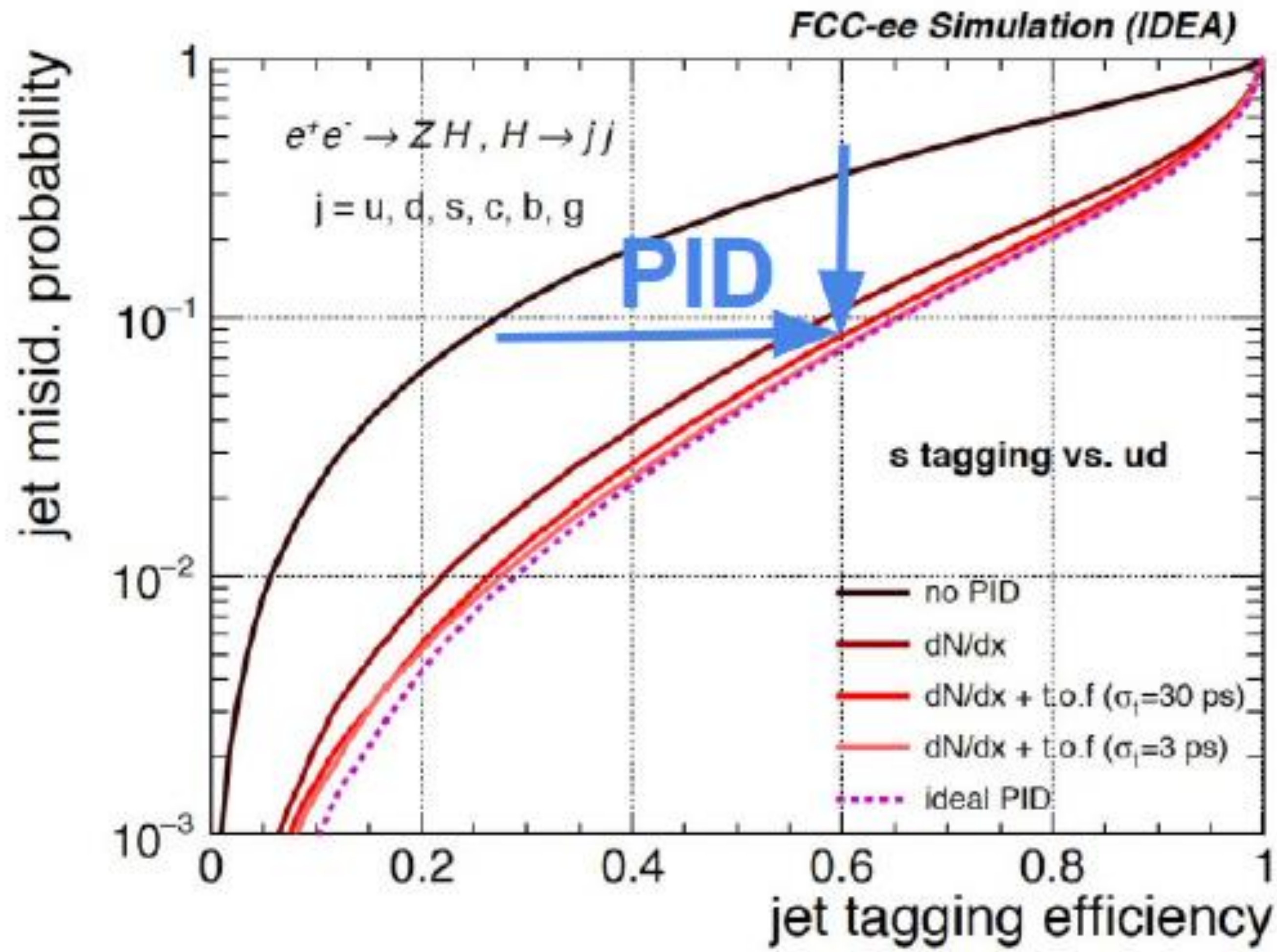




Combined measurement

Particle ID has to be integrated in the VTX/TRK concept

s-tagging ?



s-tagging in ILD ?

IDEA

- Fast sim
- Different scenarios

Name	Beam pipe radius [cm]	VTX layer$_1$ radius [cm]	Thickness of first 3 VTX layers [μm]	Thickness of 8 VTX disc layers [μm]
standard IDEA	1.5	1.7	280	280
+R1.3	1	1.3	280	280
+w100	1	1.3	100	280
+w50	1	1.3	50	280
+w30	1	1.3	30	280
+w100_DSK	1	1.3	100	100
+w50_DSK	1	1.3	50	50
+w30_DSK	1	1.3	30	30
+L1_w30	1	1.3	layer$_1$ = 30, layer$_{2,3}$ = 280	280

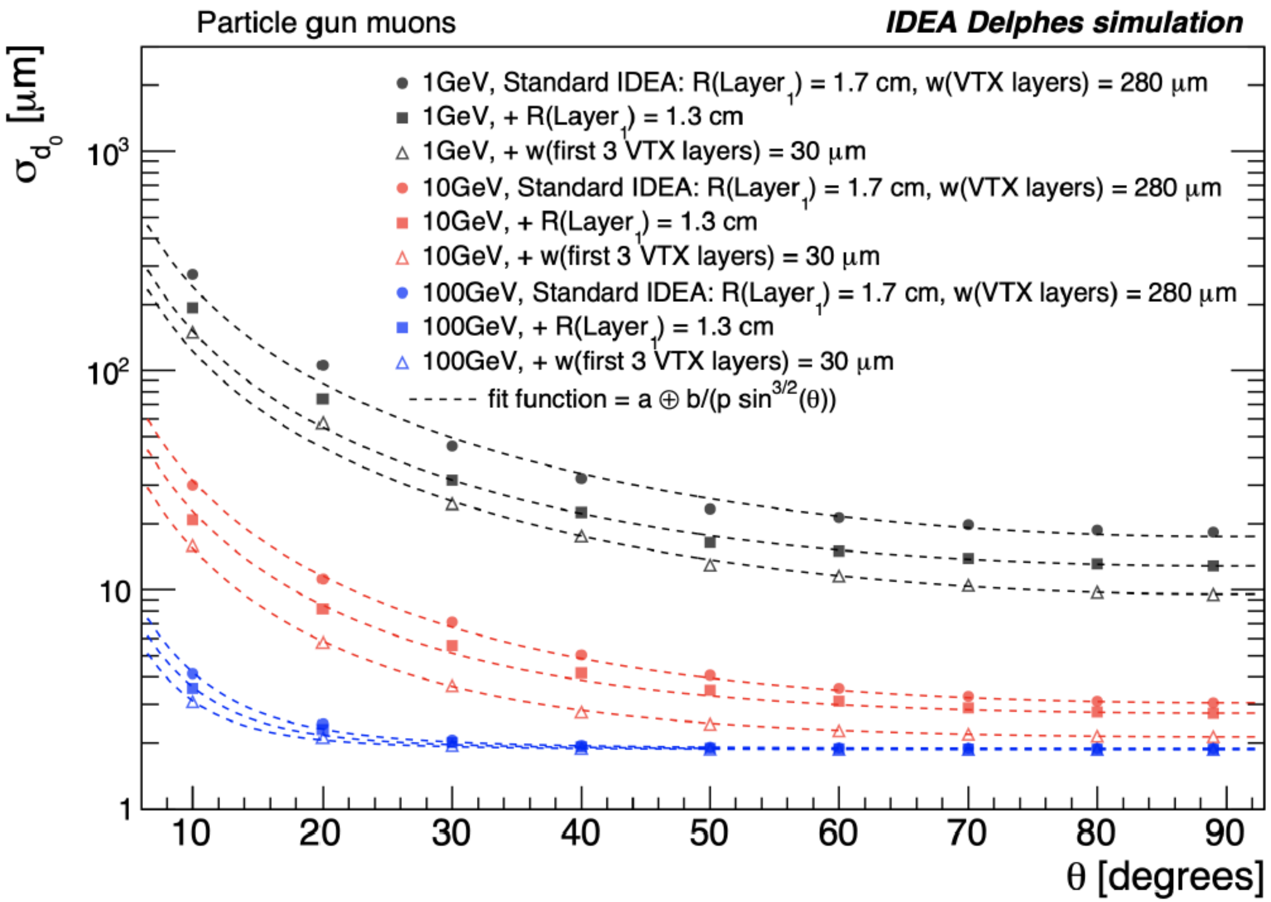
Progress on IDEA vertex detector in full simulation ...

Armin Ilg, University of Zürich

... and performance of an ALICE ITS3-like vertex detector for FCC-ee

Leila Freitag, University of Zürich

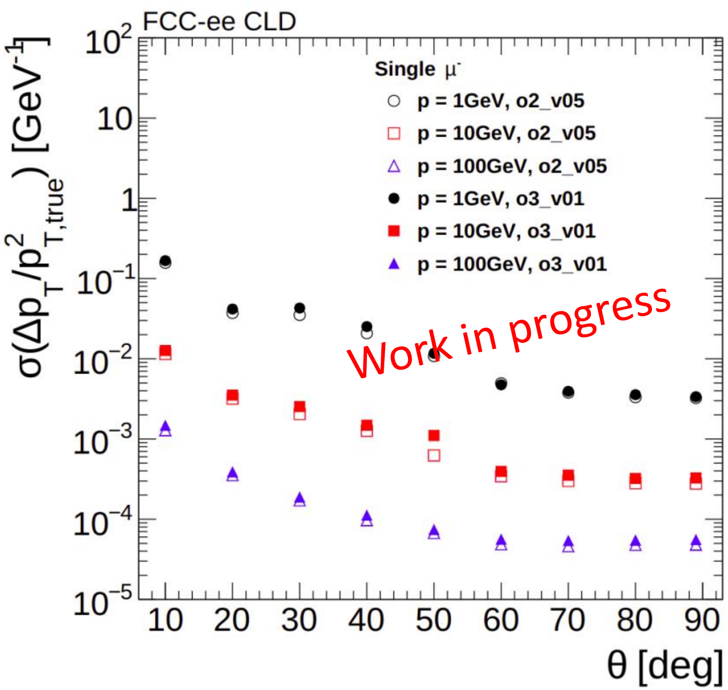
[6th FCC physics workshop]

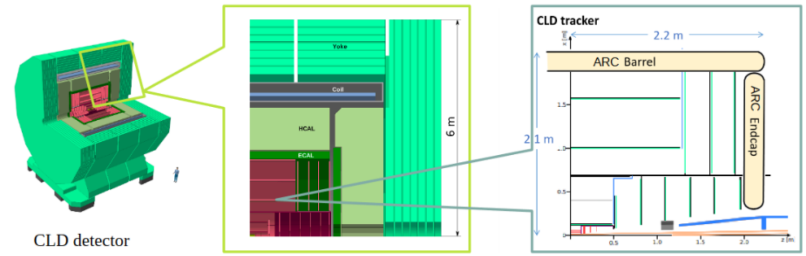


J. Andrea, G. Sadowski (PhD), Z El Bitar

An example of Full sim performances in CLD

- CLD_01_v04 = former geometry
- CLD_02_v05 = new beam pipe radius & material budget
  - ✓ 5 μm Au + 2 x 350 μm layers of BeAl + liquid parafin ~ 0.6 % X_0 ⇨ mat. Budget +33%
  - ✓ Inner radius: 15 mm ⇨ 10mm
- CLD_03_v01 = Adding a RICH
  - ✓ + Array of RICH Cells (ARC)





D0 resolution – single μ^- – CLD_o1_v04

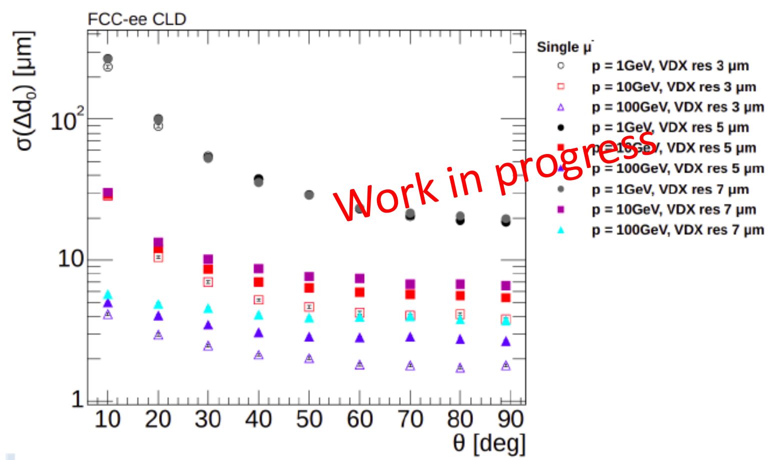
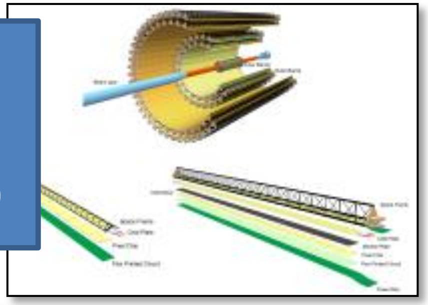


Figure: D0 resolution (10k events)

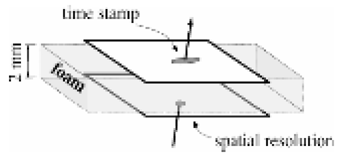
- Need to reassess the performances plots optimization for FCCee with respect to ILC context.
- Comparing resolutions between detector concepts has to be taken with caution (Different level of realism and conservatism on the technologie future performances)

Material budget: starting from the layers

Classical single sided layers (e.g. ALICE ITS-2)



Double sided layers

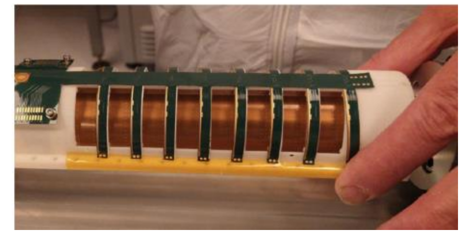


PLUME
(Bristol, DESY, IPHC)

Double sided ladders with minimized material budget
0.35% X_0 reached ⇨ ~0.3 X_0 doable (with air flow cooling)

Pseudo stitching + bent sensors (superALPIDE)

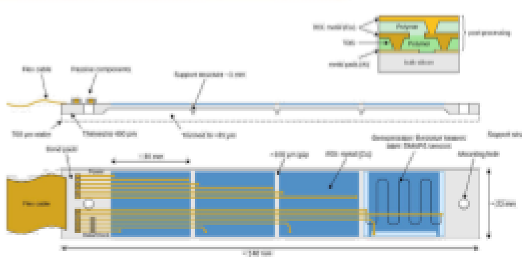
- 1 silicon piece cut from one ALPIDE wafer (9x2 dies, ~1/2 of layer 0)



Integration !

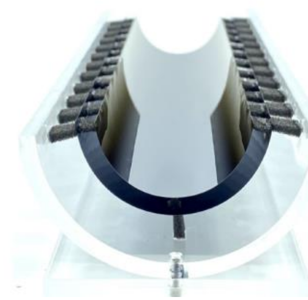
Self supported silicon (Belle-2 upgrade)

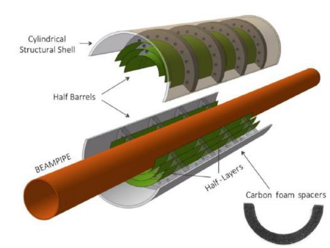
7.1x1.5 cm²
Thickness (edge/center) 430/90 µm
Planarity ~17 µm



Stitching + bent sensors ALICE-ITS3

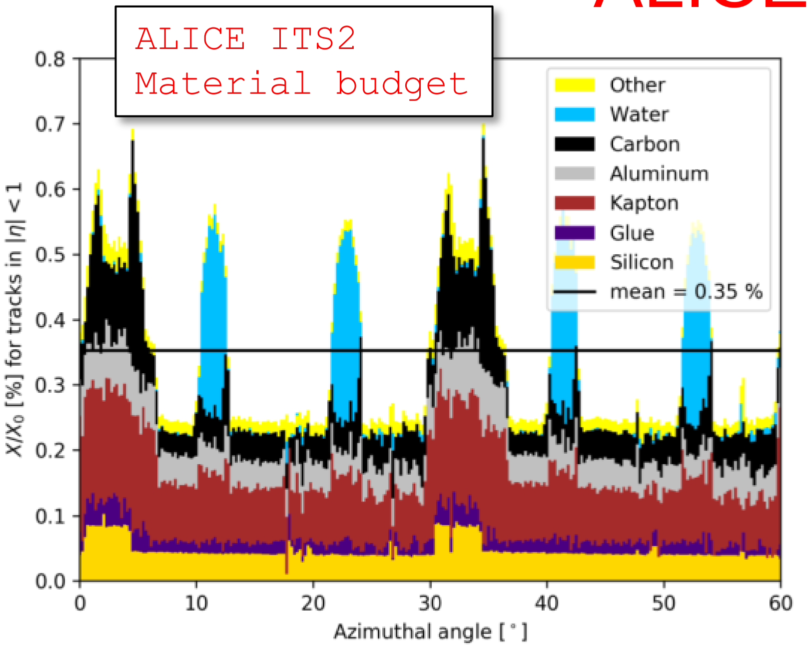
Layers 2+1

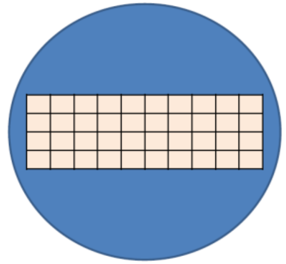


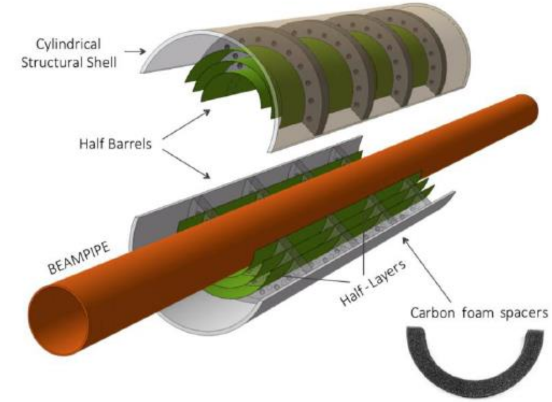


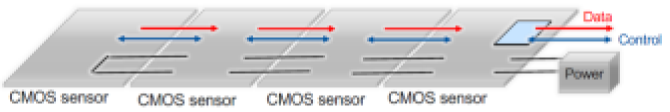
Inputs for engineering studies

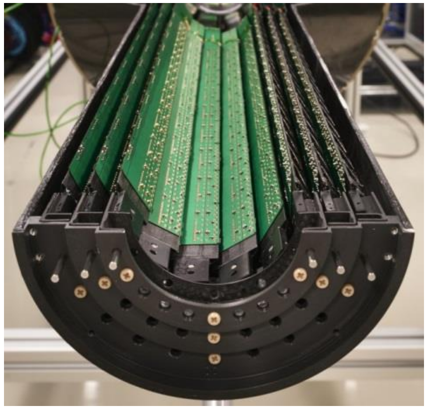
ALICE ITS-3 (Run4)





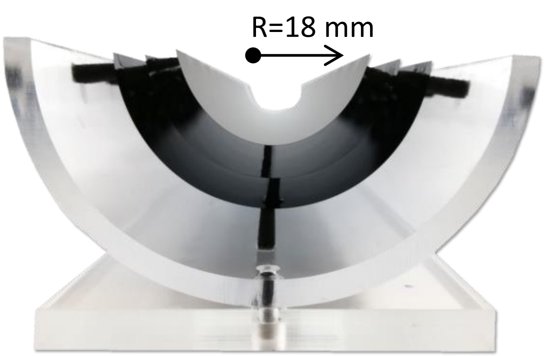






ITS2:

- 7 layers of MAPS
- TJ 180 nm CMOS
- 12.5 Giga pixels
- Pixel size: 27×29 µm^2
- Water cooling
- **0.3 % X_0 / inner layer**



ITS3:

- 4 outer layers of ITS2
- 3 new fully cylindrical inner layers
  - Sensor size up to 27×9 cm
  - Thickness 30-40 µm
  - No FPCs
  - Air cooling in active area
- **0.05 % X_0 / inner layer**

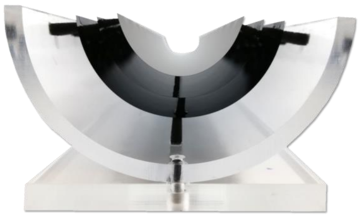
⇨ ALICE ITS-3 paves the road for the stitched sensor approach

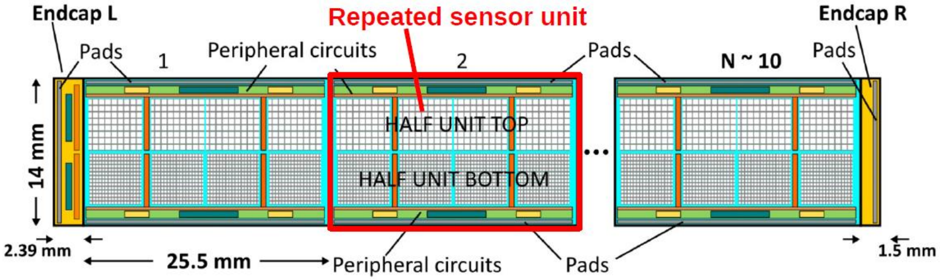
Cf. M. Winter presentation: CMOS technology Overview

How to adapt ITS-3 approach to FCCee ?

- ALICE-ITS3/CERN drives the R&D on stitching + bent sensors:
  - ✓ Sensor part ~15% of total material budget
  - ✓ Sensors thinned down to 50 μm or less ?
    - Tests performed by ALICE (to be shown in the ITS3-TDR)
  - ✓ Minimizing overlapping regions,
  - ✓ minimizing minimal radius around the beam pipe
- Challenges and caveats (for e^+e^- colliders)
  - ✓ Mechanics ? Bonding ? Air cooling only ?
  - ✓ Power dissipation map could be a challenge
  - ✓ Design: Minimizing peripheral circuits (Fill factor ~90%)
  - ✓ Bent sensor performances ? Yield ? Radiation hardness ?
  - ⇨ design rules constraints the minimal pitch (~22 μm)
  - ✓ ITS-3 do not have disk (chip periphery adds Z position constraint)
  - ✓ Approach validated in a limited radius range (R> 18mm) ?
    - Trials performed by ALICE down to R = 10mm (thickness 30-50 μm)

Figure 4.42: Setup for the bending strength measurements.



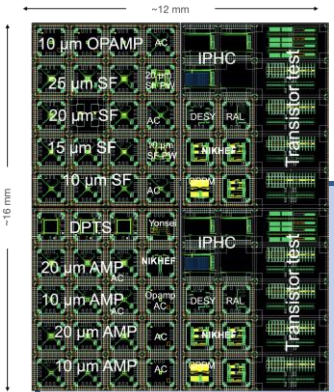


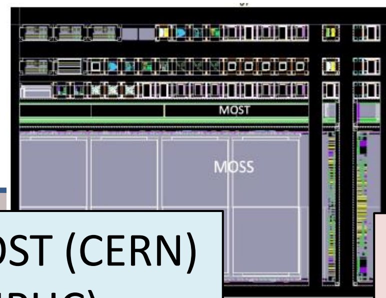
CMOS technology: moving from 180 nm to 65 nm

Technology	TowerJazz 180 nm	TPSCo 65 nm
Available since	2013 (mature technology)	2020 (access through CERN)
Large surface projects	• ALPIDE for ALICE ITS-2 • MIMOSIS for CBM-MVD • OBELIX for Belle-II upgrade	• MOSAIX for ALICE ITS-3 • DRD3/7 R&D ?
Price	affordable	More expensive
Wafer	• 8 inches (20 cm)	• Larger: 12 inches (30cm) ⇨ stitching + bent sensors
Epitaxial layer thickness	• 18/25/30/40/50 μm	• 10
Process options	• « standard » • « modified », « gap »	• « standard » • « modified », « gap »
Technology	• Feature size (180 nm) • V (1.8V) • 6 Metal Layers	• Feature size (65nm) • Lower V (1.2 V) • 7 Metal layers ⇨Pitch reduction, power saving, more functionnalites, etc.

⇨ Strong motivations to switch to a smaller feature size to increase the performances space

TPSCo 65nm Submissions





- MOSS/MOST (CERN)
- CE65_v2 (IPHC)
- Etc.

- MOSAIX (CERN)
- SPARCS ? (IPHC)
- Etc.

ALICE ITS-3

MLR1 (2020) → ER1 (2022) → ER2 (2024) → ER3 (2025?)

2020	2021	2022	2023	2024	2025	2026	2027	2028	2029

- CE65_v1 (IPHC)
- DPTS (CERN)
- APTS (CERN)
- TANGERINE (DESY)
- Ring oscillators (CPPM)
- Etc.

ER1 → MPR2 (2025) → MPR3 (2027?)

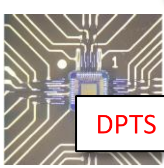
- Fine pitch demonstrator
- Architectures exploration

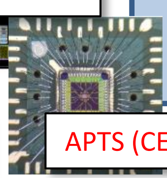
- Fine pitch telescope
- Fast timing ?
- Power optimization ?

Generic R&D via DRD3/7

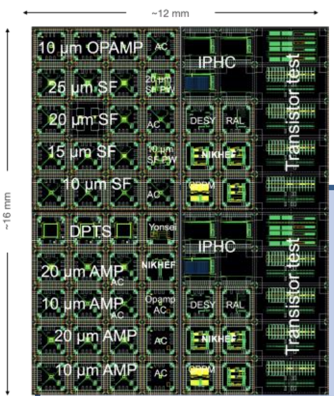

Ring oscillators

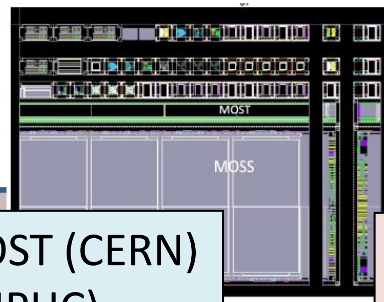

CE65


DPTS (CERN)


APTS (CERN)

TPSCo 65nm Submissions





- MOSS/MOST (CERN)
- CE65_v2 (IPHC)
- Etc.

- MOSAIX (CERN)
- SPARCS ? (IPHC)
- Etc.

ALICE ITS-3

MLR1 (2020) → ER1 (2022) → ER2 (2024) → ER3 (2025?)

2024 | 2025 | 2026 | 2027 | 2028 | 2029

DRD project: Fine-pitch CMOS pixel sensors with precision timing for vertex detectors at future Lepton-Collider experiments

DRD technology area

DRDT 3.1 - Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors.

Proposing participants

Institute	Contact	Foreseen main areas of contribution
APC Paris	M. Bomben	Simulations, testing
CERN	D. Dannheim	Testing, DAQ, ASIC design support
DESY	S. Spannagel	ASIC design, testing, DAQ, simulations
IPHC Strasbourg	A. Besson	ASIC design, testing
Oxford University	D. Hynds	Testing, simulations
Zurich University	A. Macchiolo	Testing, DAQ, simulations

→ MPR2 (2025) → MPR3 (2027?)

...ne pitch demonstrator
...rchitectures exploration

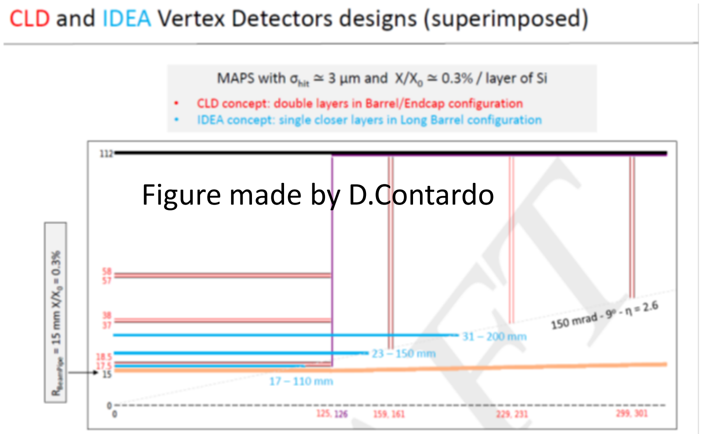
- Fine pitch telescope
- Fast timing ?
- Power optimization ?

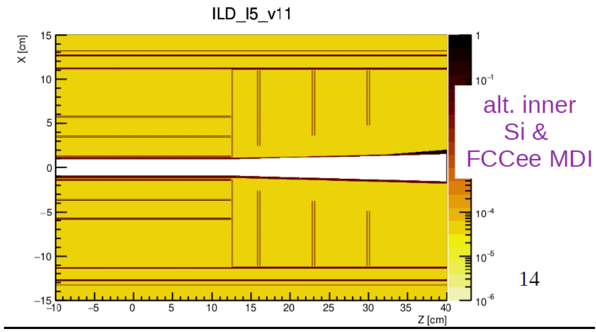
Generic R&D via DRD3/7

DPTS (CERN)
APTS (CERN)

Vertex detector proposal @ ILD for FCCee

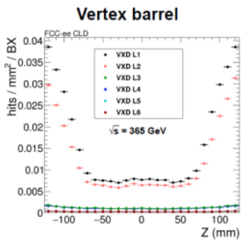
- Technology: CMOS pixel sensor as a baseline
  - ✓ (probably the generation after TPSCo 65nm)
- MDI constraints (implemented by D. Jeans in the simulation)
  - ✓ Inner layer as close as possible to the beam pipe: Rmin ~12 mm
- Geometry partly determined by the main tracker
  - ✓ Adaptable to any detector concept
- Requirements
  - ✓ Minimized material budget (~< 0.15% X_0 per layer)
    - Beam pipe radius/mat. budget fixes the requirement
  - ✓ Spatial resolution ~3 μm / layer
  - ✓ Time resolution: ~ 500 ns
  - ✓ Moderate Power dissipation (~< 50 mW/cm²) allowing for air flow cooling
  - ✓ 5-6 layers in the inner radius (~< 6-10 cm)
    - Robustness / standalone tracking (≠ IDEA choice)
    - Double sided option still considered but not easily compatible with a stitched approach
    - « long barrel » preferable ⇨ minimize the distance between IP and the first hit
    - Low momentum tracking capabilities
    - Track seeding @ different radii : e.g. FIPs, highly ionizining particles, LLPs, etc.
  - ✓ « merge » VTX and SIT ?
    - Same technology ? ⇨ Power dissipation optimization
  - ✓ Other pixel layers close to the main tracker
  - ✓ Stitched sensor: very promising approach by ALICE ITS-3
    - At least in the z dimension
    - Bent sensor considered (caveat: acceptance)
- Timing measurement capabilities (< 100 ps)
    - Either in a specialized/dedicated layer
    - Or preferably included in the same technology if R&D allows it

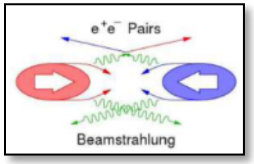




D.Jeans

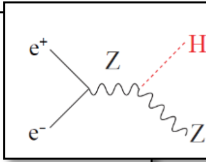
backup





Vertex detector requirements (ILC/FCCee)

Physics
- ➪ Flavour tagging
- ➪ Low pT tracks
- ➪ Vertex/Jet charge determination
- ➪ Track seeding

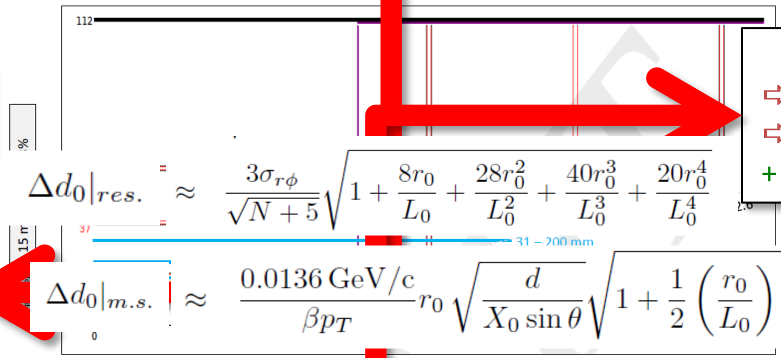


Physics O(Hz/cm²)

Beam background O(10-50 MHz/cm²)

CLD and IDEA Vertex Detectors designs (superimposed)

MAPS with $\sigma_{hit} \simeq 3$ µm and $X/X_0 \simeq 0.3\%$ / layer of Si
- CLD concept: double layers Barrel/Endcap configuration
- IDEA concept: single closer layers in Long Barrel configuration



$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV}/c}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

(Figure: D. Contardo)

Vertex reconstruction
- ➪ granularity
- ➪ Pitch ~17-20 µm
- ➪ (σ_{sp} ~3-4 um)

Material Budget
- ➪ ~ 0.15% X_0 / layer
- ➪ < 1% X_0 for the whole VTX
- + ~0.4-0.6 % X_0 for the beam pipe

Beam background

Radiation hardness
O(100kRad/yr) & O(10^{11})n_{eq}/yr

Rad.Tol. devices

Time resolution
O(100ns-1 µs)

O(10ns)@CLIC

Power consumption
~< 50mW/cm²

Fast read-out & low Power Architectures (~ 20-50 mW/cm²)

No Power pulsing @FCCee

Cooling
Stiffness / Alignment

Low material detectors & supports structures

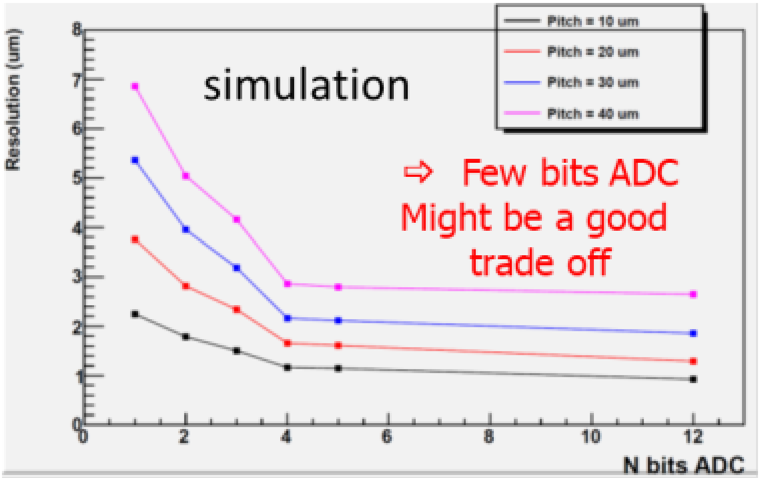
$$\sigma_{d_0} = a \oplus \frac{b}{p\sin^{3/2}\theta}$$

$a \simeq 5\,\mu m$ $\quad b \sim 10-15\ \mu m.GeV$

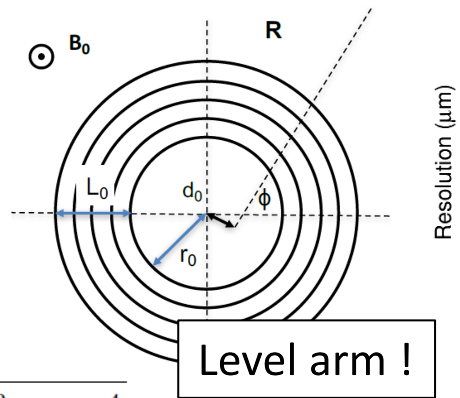
- Design: 5 single layers or 3 double layers ? Inner and outer radius ? Etc.
- R&D: ➪Keep excellent spatial resolution, low material budget, moderate Power consumption and push towards better time resolution (BX)

Spatial resolution in Higgs factories

- Typical targets:
  - ✓ σ_{sp}~3 µm for the vertex layers
  - ✓ σ_{sp}~5-10 µm for the outer tracker layers
- Resolution in each layer depends on
  - ✓ Pitch
    - In conflict with the functionnalities inside the pixel
    - Favored by small feature size technology
  - ✓ Charge deposition
    - Sensitive layer thickness
  - ✓ Charge sharing (SNR vs resolution)
    - Depletion:
    - Staggered pixels
  - ✓ Charge encoding
    - Binary output / ADC / Tot / etc.



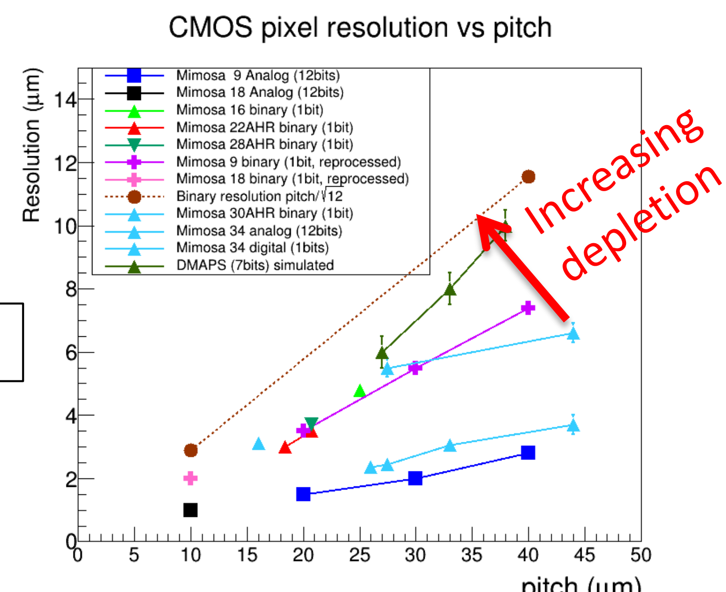
$$\sigma_{d0}{}^2 = a^2 + \left(\frac{b}{p.sin^{3/2}\theta}\right)^2$$



$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}}\sqrt{1+\frac{8r_0}{L_0}+\frac{28r_0^2}{L_0^2}+\frac{40r_0^3}{L_0^3}+\frac{20r_0^4}{L_0^4}}$$

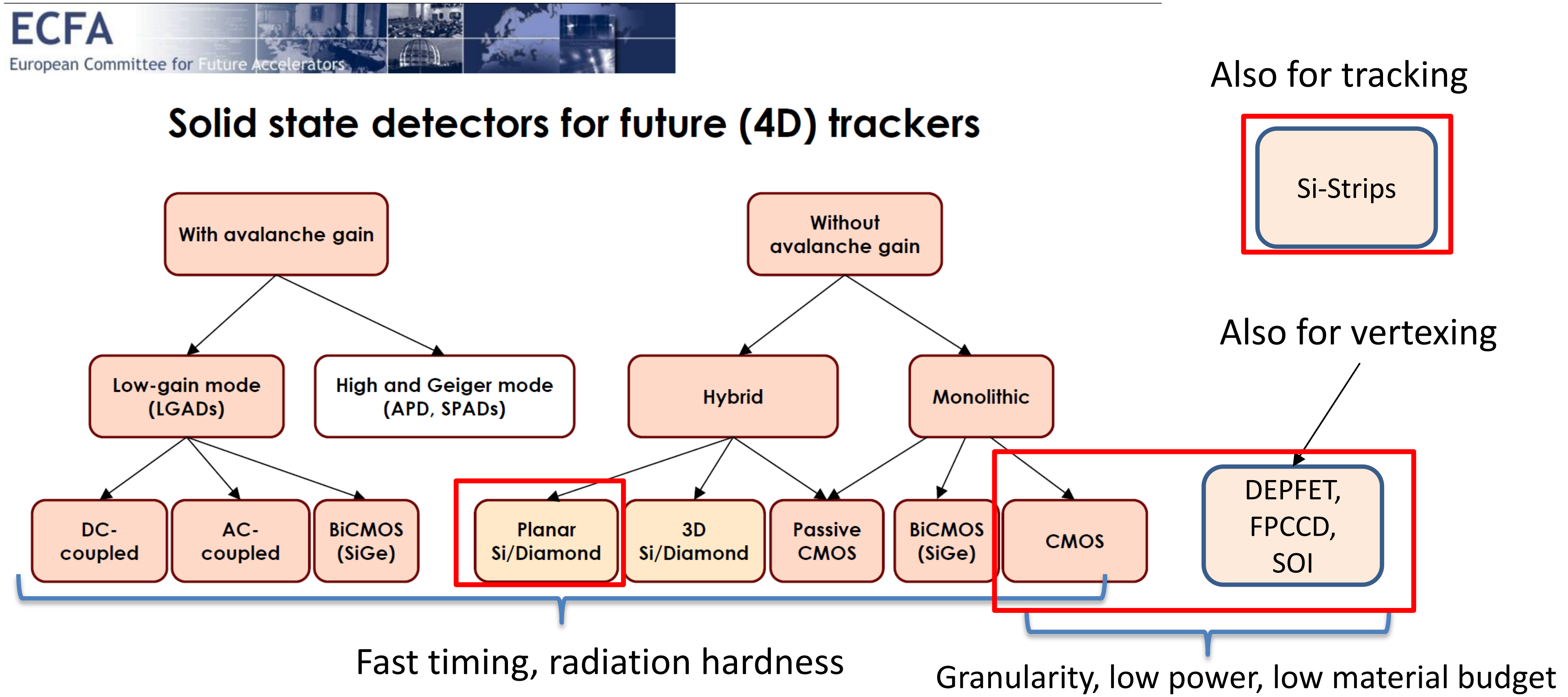
$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}}\sqrt{1+\frac{1}{2}\left(\frac{r_0}{L_0}\right)+\frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$

d = layer thickness, N = # layers



⇨ σ_{sp} ~ 3 µm ⇔ pitch ~ 15-20 µm
(assuming binary output, ~20 µm epi.thickness & large depletion in 180nm tech.)

Pixel detectors landscape for FCCee detectors



- VTX hierarchy of the driving parameters
  - ✓ Granularity & material budget > Power > time resolution > Radiation hardness
- Outer tracker
  - ✓ Material budget still a must. Relaxed granularity ⇨ possible focus on Power, time resolution
- Specialized timing layers
  - ✓ Timing layer ⇨ Price to pay: granularity and/or Power
- R&D needed to improve the parameter space

Power vs fast timing vs pixel size

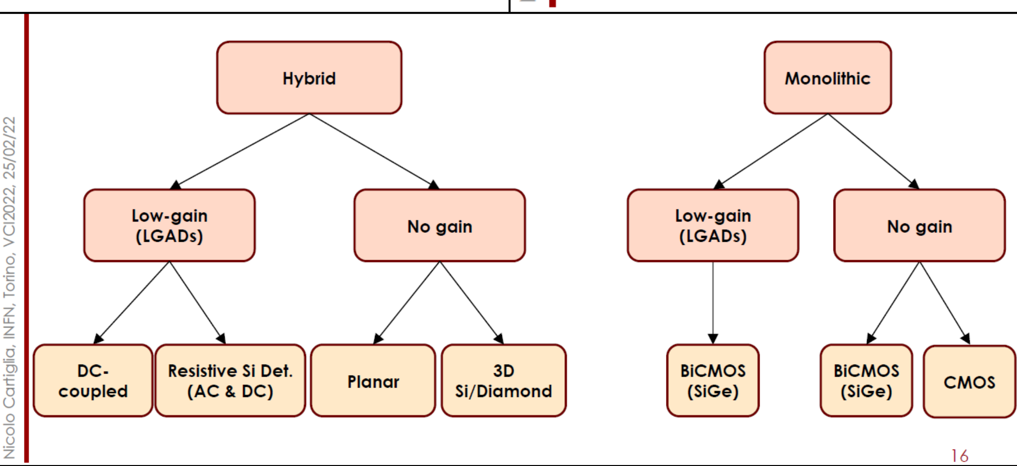
Brief considerations about electronics: power

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

Name	Sensor	node	Pixel size	Temporal precision [ps]	Power [W/cm²]
ETROC	LGAD	65	1.3 x 1.3 mm²	~ 40	0.3
ALTIROC	LGAD	130	1.3 x 1.3 mm²	~ 40	0.4
TDCpic	PiN	130	300 x 300 μm²	~ 120	0.45 (matrix) + 2 (periphery
TIMEPIX4	PIN, 3D	65	55 x 55 μm²	~ 200	0.8
TimeSpot1	3D	28	55 x 55 μm²	~ 30 ps	5-10
FASTPIX	monolithic	180	20 x 20 μm²	~ 130	40
miniCACTUS	monolithic	150	0.5 x 1 mm²	~ 90	0.15 – 0.3
MonPicoAD	monolithic	130 SiGe	25 x 25 μm²	~ 36	40
Monolith	LGAD monolithic	130 SiGe	25 x 25 μm²	~ 25	40

45

Nicolo Cartiglia, INFN, Torino, VCI2022, 25/02/22

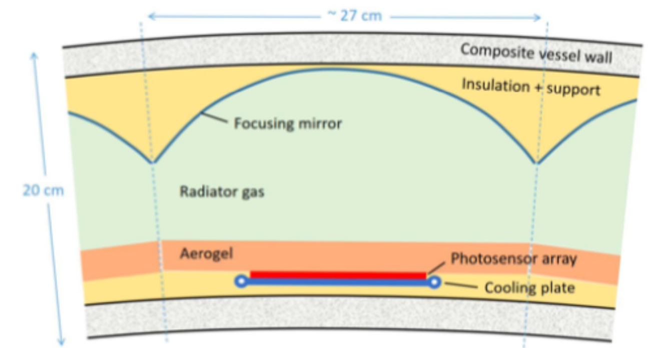


Price to pay: additionnal cooling system (addtionnal material)

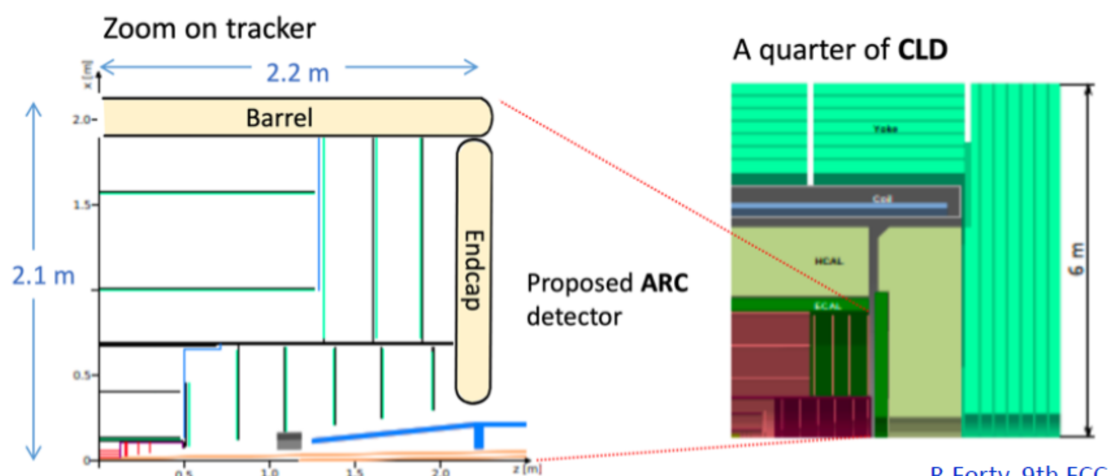
From M. Dam

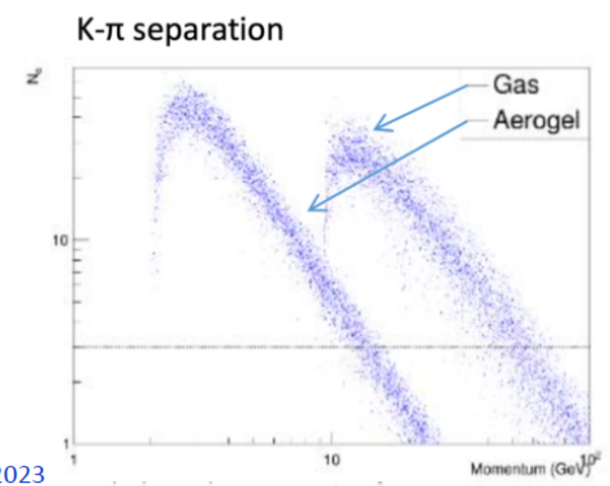
Compact RICH detector for FCC-ee

- Design goal: Compact design, max 20 cm depth, few % X_0
- Use spherical focussing mirrors, *r* = 30 cm, for radiator thickness of 15 cm
- Two radiators
  - Aerogel
  - Gas
    - Unpressurised C_4F_{10} gives good momentum range for K-π separation, with acceptable photon yield
    - Pressurised Xenon may provide similar performance if fluorocarbons unacceptable



ARC detector (one cell)



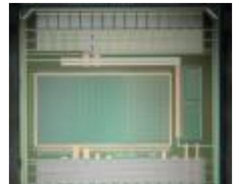


R.Forty, 9th FCC Week, 2023

CE65_v1

- CE_65v1 (MLR1 submission)
  - ✓ prototype designed @IPHC
  - ✓ Analog output, various designs (pitch, amplification)
- CE_65v2 (ER1 submission)
  - ✓ 18/22 μm pitch, hex design
  - ✓ Test beam next week @ DESY

✓ More results: PSD13, Oxford, El Bitar



CE-65 (IPHC)

PICSEL

C4PI-Platform

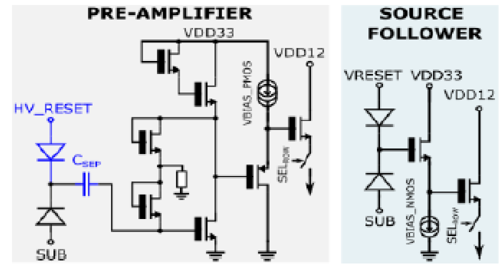
CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

iPHC Institut Pluridisciplinaire Hubert CURIEN STRASBOURG

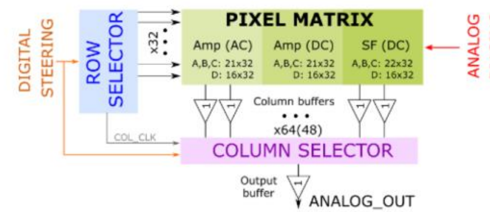
eurizon European network for developing new horizons for RIs

AIDA innova

cnrs IN2P3 Les deux infinis



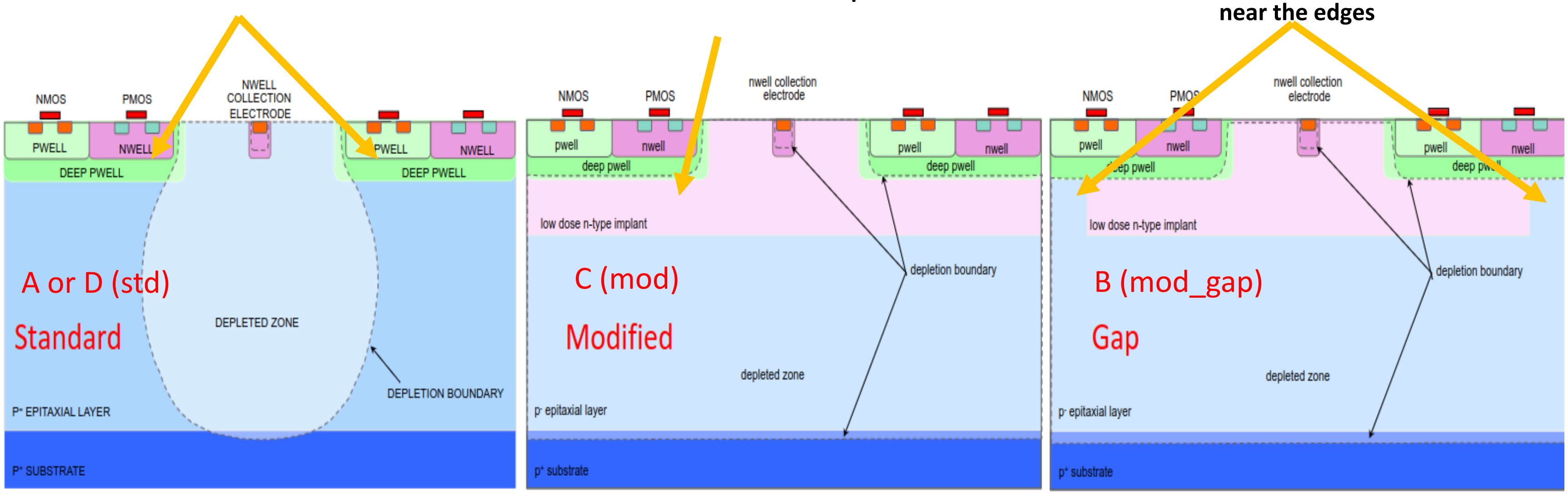
Variant	Process	Pitch	Matrix	Sub-matrix
CE65-A	std	15μm	64×32	AC/21, DC/21, SF/22
CE65-B	mod_gap	15μm	64×32	AC/21, DC/21, SF/22
CE65-C	mod	15μm	64×32	AC/21, DC/21, SF/22
CE65-D	std	25μm	48×32	AC/16, DC/16, SF/16



Prevent circuitry's nwells from collecting charge

To obtain a full depletion

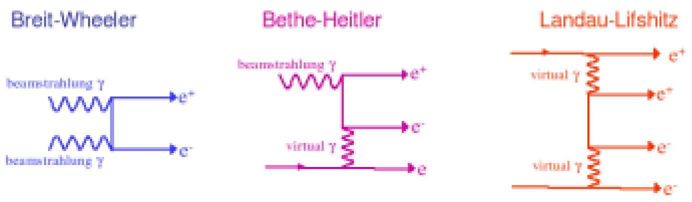
To overcome the weak electric field near the edges



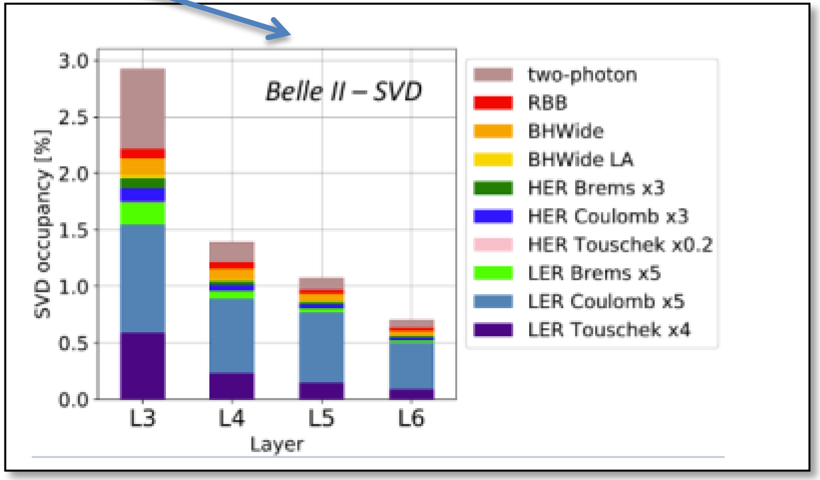
https://doi.org/10.1016/j.nima.2017.07.046

https://iopscience.iop.org/article/10.1088/1748-0221/14/05/C05013

Challenge: understand beam related backgrounds

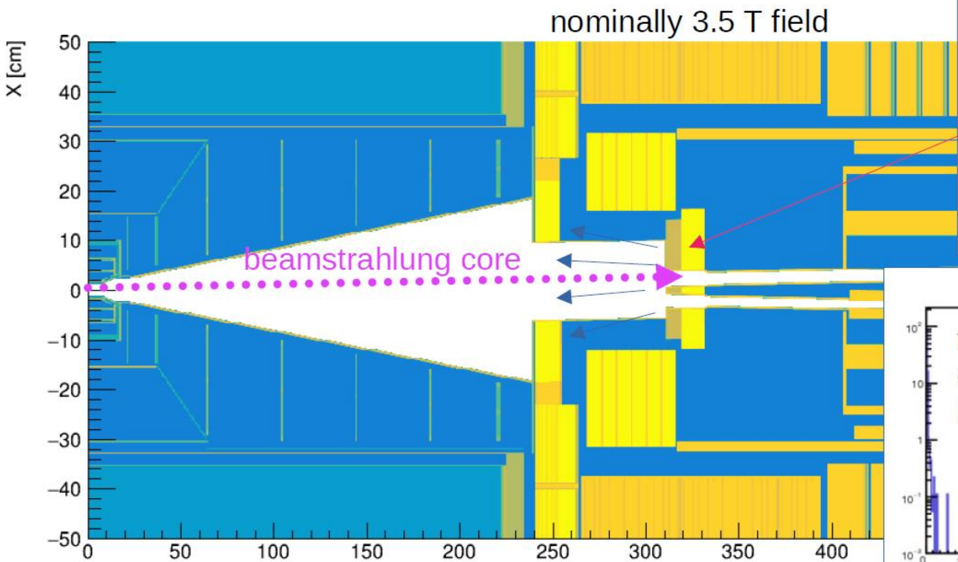


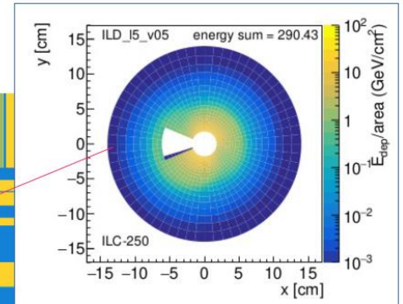
- Sources:
  - ✓ Incoherent pairs (« beamstrahlung »)
  - ✓ Synchrotron
  - ✓ Beam loss (circular machines)
  - ✓ Radiative bhabha
  - ✓ Beam gas, etc.
- Usually one considers that occupancy ~< 10^{-2}-10^{-3} is safe for tracking/vertexing purposes
- Experience from ILC studies over 20 years
  - ✓ Any modification in the Interaction region (beam scheme, beam pipe design, B field) might bring surprises
  - ✓ One should not consider that a 10^{-4} occupancy estimation means that there is no issue.
    - The robustness is questionnable
    - Large possible variations in some acceptance corners (asymmetries in φ or z)
    - Safety factor absolutely mandatory
    - 2 independant simulation tools would be welcome (GuineaPig, Fluka, etc.)
- Experience from Belle-2
  - ✓ Discrepancies observed between simulations and first collisions
- Direct beam background vs backscattered background
  - ✓ Generally the backscattered ones are more sensitive to any MDI change.
- What about timing information to reject background ?
  - ✓ Need ~ 5 ns to reject backscattered particles
  - ✓ Is it worth paying the price in terms of additionnal power ?
- What about cluster shape to reject background ?
  - ✓ Need very good sensitive thickness/pitch ratio (> 2).
  - ✓ Charge information helps.
  - ✓ (you actually reject very low pT particles)

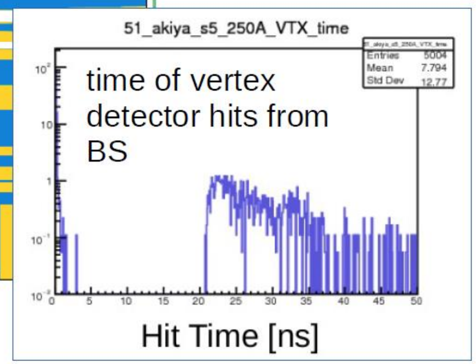


Example of background study: ILD, from linear to circular

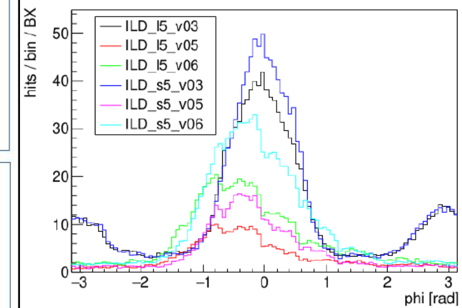
simulation model of ILD @ ILC





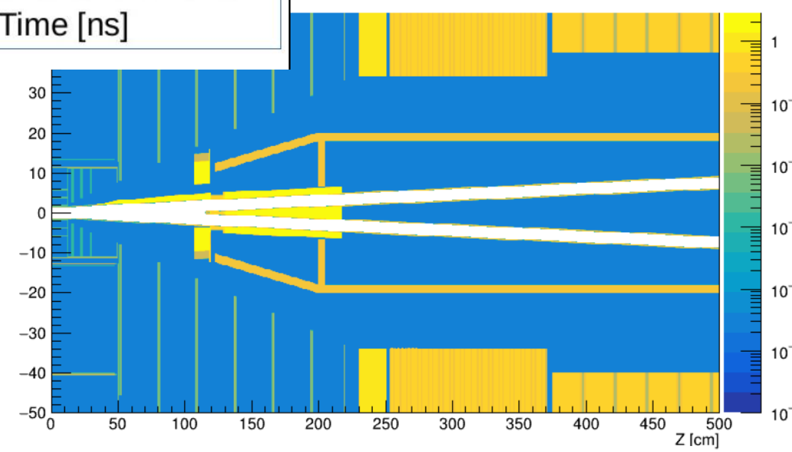


[D. Jeans LCWS2023]



Adapt MDI, B = 2T,
Sensitive to precise B-field map
Adapt Beam structure
Effect in TPC also being studied

at FCCee,
quasi-continuous ion cloud from ~14M bunch crossings

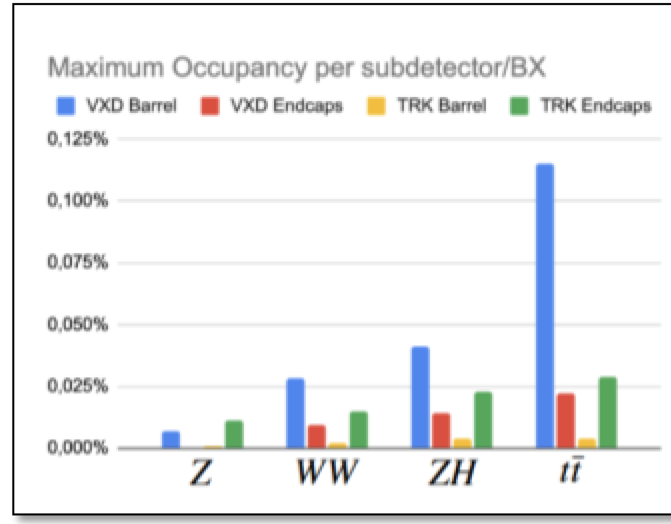


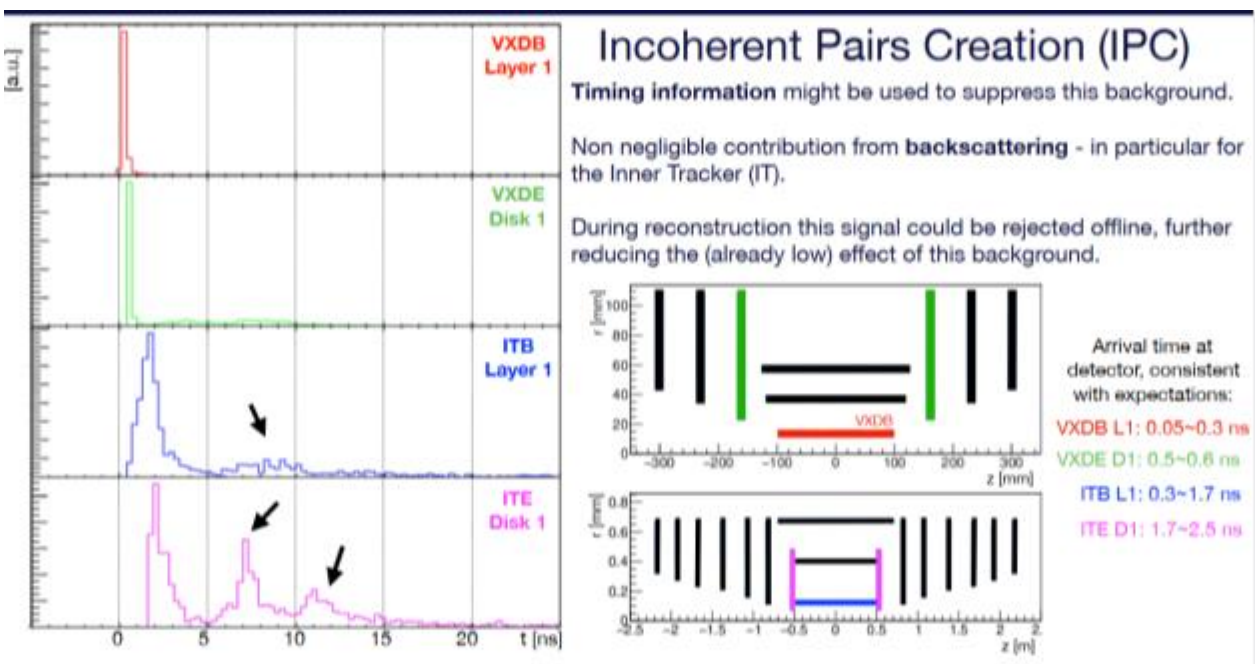
- at FCCee, MDI extends to ~1m from IP
  → 6 times more beamstrahlung background hits in TPC

Example of study in CLD

	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

US FCC workshop 25/04/2023 Ciarma





BX rate might be an issue at the Z-pole

Timing resolution range to reject background ~ 1 ns