CMOS PIXEL SENSORS for TRACKING DEVICES at FUTURE HIGGS-TOP-EW FACTORIES : WHERE DO WE STAND ? WHAT CAN WE ANTICIPATE in PERSPECTIVE of ILC ?

Marc Winter, IJCLab-Orsay, IDT-WG3 meeting, 26th April 2024

Reminder:

- some characteristic features of CMOS Pixel Sensors (CPS)
- illustrative set-ups/concepts based on CPS

Most advanced CMOS process: TPSCo 65 nm imaging technology

Generic development of the 65 nm sensors:

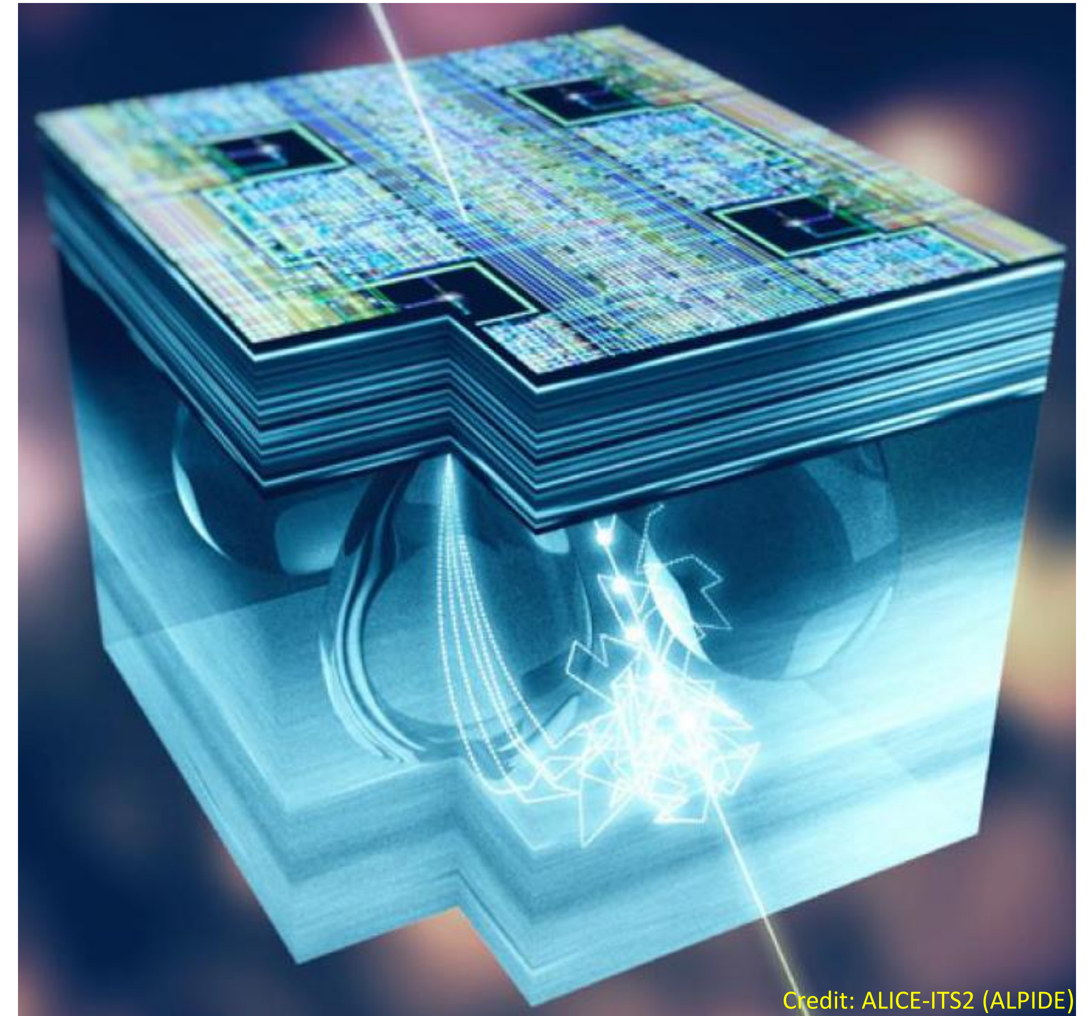
- R&D for fast and radiation tolerant sensors
  (main drivers: HL-LHC → FCChh)
- R&D privileging spatial resolution & suppressed material budget
  (main drivers: H.I. e.g. ALICE-ITS3, CBM-MVD, Belle-II → Higgs-Fact)

ALICE-ITS3 project:

- Sensor developed for the ITS3 vertex detector
- **Salient features coming out from R&D on:**
  CMOS-65 (vs CMOS-180), stitching, system integration

Other collaborative frameworks of R&D:

- DRD-TF*X* = 3, 7.6, 8 ; CERN-EP WP 1.2, 4 , …
- CBM, Belle-II, Mu3e, eIC, …, ***ALICE3***


Credit: ALICE-ITS2 (ALPIDE)

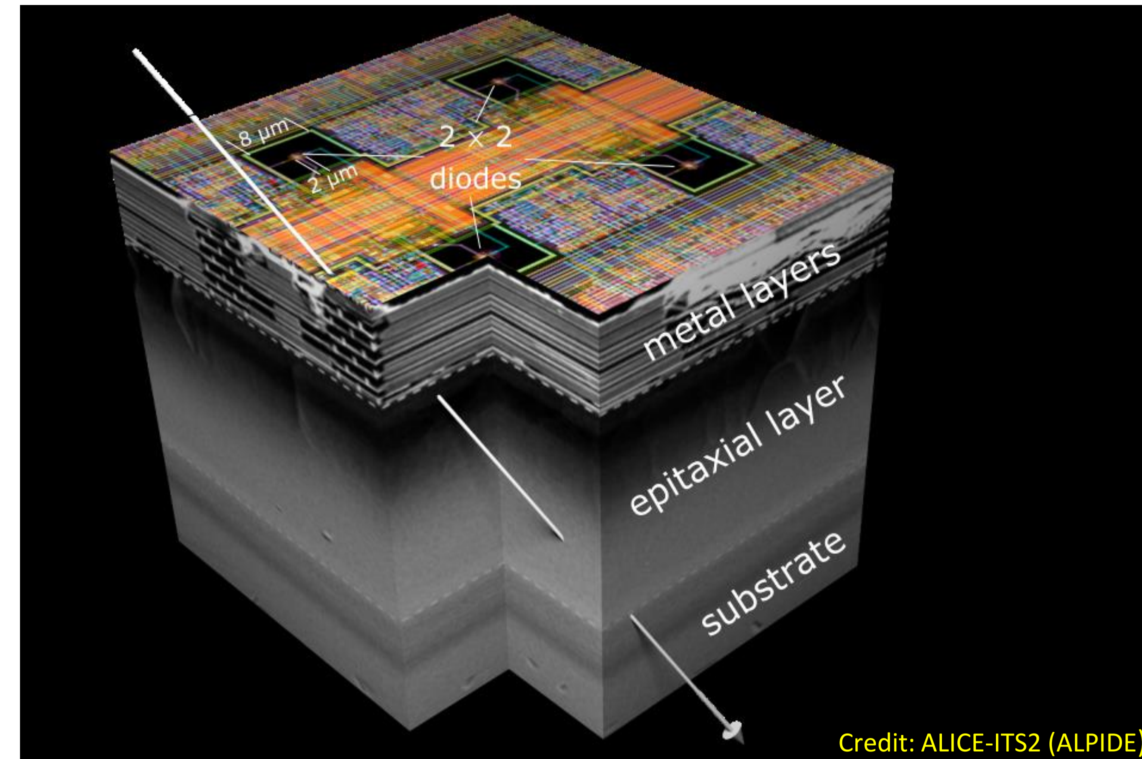
Numerous CMOS sensors in use or development: some general features

- **Main asset:** µ-circuits (steering, r.o., slow control) integrated on thin sensing substrate ➔ Monolithic & Thin (& T_{room})
- Numerous developments of **custom design** CMOS Pixel Sensors (CPS) on-going for vertexing and tracking devices foreseen to equip experiments at existing infrastructures (LHC, KEK, PSI, …) and future colliders (eIC, FAIR, FCCee, CEPC, C3, ILC, CLIC, …)
- Some R&D for ECAL
- Optimisation imposes hierarchising conflicting requirements:

  Spatial resol. / Timing / Mat. budget (power) / Rad. Tol. / Hit rate
- Dependence on CMOS process (foundry) characteristics
- Frameworks: CERN-EP, DRD, ALICE-ITS3, … (main driver for

  Higgs factories: 65 nm techno with stitched curved sensors)
- 3 predominent foundries: TJsc, TPSCo, L Foundry
- System Integration is crucial for realistic detector optimisation:
  - Air cooling at which price ?
  - Services ➔ impact on FW region ?
  - Impact on choice of sensor technology and design ?

Modify design ?



Evolution of the Performances in Terms of Spatial & Time Resol. / Power / Hit Rate

Sensor/time → (2007 -> 2024)	MIMOSA-26 -> EUDET, …	MIMOSA-28 -> STAR-HFT, …	ALPIDE -> ALICE-ITS2, …	MIMOSIS -> CBM-MVD	MOSAIX -> ALICE-ITS3
CMOS techno.	AMS/**350** nm	AMS/**350** nm	TJsc/**180** nm	TJsc/**180** nm	TPSco/**65** nm
Hit rate [MHz/cm²]	≤ 1 MHz/cm²	≤ 1 MHz/cm²	> 1 MHz/cm²	< 100 MHz/cm²	O(10) MHz/cm²
Pixel dim. [µm]	18.4 x 18.4	20.7 x 20.7	≈ 27 x 29	26.9 x 30.2	20.8 x 22.8 (tbc)
Discri. µcircuit	End-of-col.	End-of-col.	In-pixel	In-pixel	In-pixel
σ_{sp} [µm]	≥ 3.1 µm	≥ 3.7 µm	≥ 5 µm	≥ 5.5 µm	≈ 5 µm
Δ_t [µs]	115 µs	185 µs	≤ 10 µs	≤ 5 µs	2 – 10 µs
Power density	250 mW/cm²	170 mW/cm²	≤ 50 mW/cm²	< 200 mW/cm2	50/900 mW/cm²

From < 2008 to > 2024:

- CMOS technology feature size has decreased : 350 nm ↘ 65 nm
- Expts hit rate (& rad. tol.) requirements became more severe : < 1 MHz/cm² ↗ O(100) MHz/cm²

→ **Global consequence:** (binary) **spatial resolution has degraded despite the steady feature size reduction**

⇨ Achieving ≤ 3 µm resol. for a vertex detector suited to Higgs fact. running conditions is a challenge (in part. for circular machines) but several potential sol. remain unexplored

Numerous CMOS Sensors in Use or Development (illustrative sub-sample)

Name	Expt	Sub-syst	Area	Δ Pos., Time	Power (fid.)	Technology	Comment
ALPIDE	ALICE-ITS2	Vx & In. Trkr	10 m²	5 µm, ≤ 10 µs	≤ 50 mW/cm²	TJsc 180 nm EPI	In operation
MOSAIX	ALICE-ITS3	Vx only	0.12m²	5 µm, 2-10 µs	≤ 50/900 mW/cm²	TPSco 65 nm EPI	Wafer scale CPS
FASTPIX	→ HL-LHC	Demonstr.		≥ 1 µm, ≤ 100 ps	+++	TJsc 180 nm EPI	Timing & Rad. Tol.
MonoPix	→ ATLAS	ITk	few m²	< 10 µm, ≤ 20 ns	> 0.5 W/cm²	TJsc 180 nm EPI	Not retained
CACTUS	FCC, eIC, …	Timing det.		< 100 ps	300 mW/cm²	LF 150 nm	R&D proto.
MALTA	HL-LHC, …	Fast det.	few m²	36x40 µm², 25 ns	> 100 mW/cm²	TJsc 180 nm EPI	512x512 pixels
MIMOSIS	CBM/FAIR	Vx & In. Trkr	0.16 m²	5-6 µm, 5 µs	< 100-200 mW/cm²	TJsc 180 nm EPI	Fixed target HI expt
TaichuPix	CEPC	Vx & In. Trkr		≤ 5 µm	90-160 mW/cm²	TJsc 180 nm EPI	8x8 µm² n-well
NAPA	SiD/C3	Trkr, (calo.)		7µm pitch, O(ns)	20 mW/cm²	TPSCo 65 nm EPI	Target values
ARCADIA	IDEA/FCCee	Vx & In. Trkr		10-50 µm		LF 110 nm	Working horse
CLICpix	CLICdp	Vx & In. Trkr		25 µm pitch, 10 ns		TPSCo 65 nm EPI	Follows TimePix
OBELIX	Belle-II	Vx (7 layers)	O(1) m²	≤ 10 µm, ≤ 100 ns	≈ 200 mW/cm²	TJsc 180 nm EPI	Follows MonoPix
MuPix	Mu3e expt	Vx & Trkr		≤ 30 µm, ≤ 20 ns	≤ 350 mW/cm²	HV TJsc 180 nm	Muon decay expt

N.B.: list is not supposed to be complete but illustrative

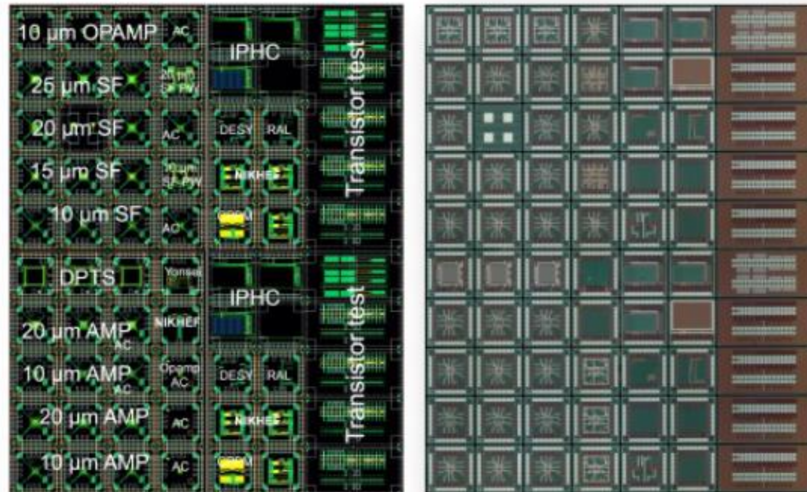
TPSCo 65 nm Technology

ECFA
European Committee for Future Accelerators

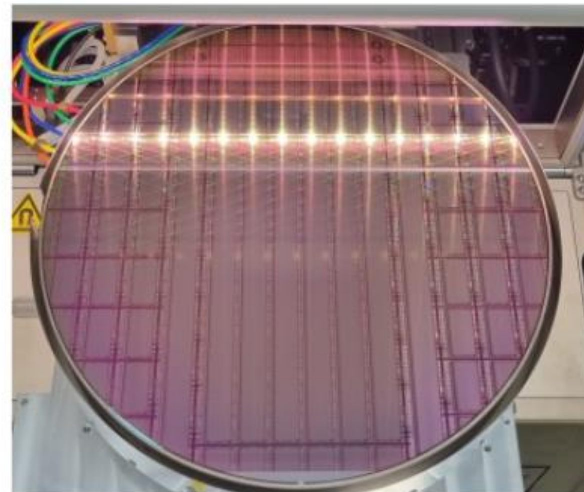
DRD7.6

TPSCo 65nm

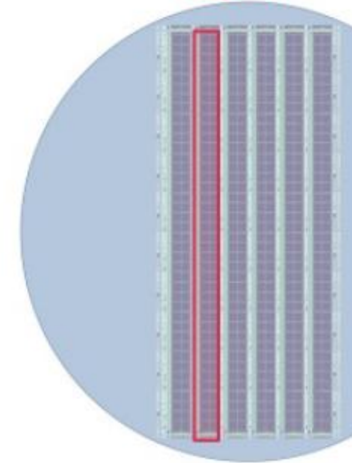
- Currently in use for ALICE ITS3 and EP R&D WP1.2
- Joint runs already carried out – MLR1, ER1
- CERN, IPHC, INFN, NIKHEF, STFC, SLAC, DESY, SLAC, Yonsei…



MLR1 (December 2020): 1.5 x 1.5 mm^2 test chips



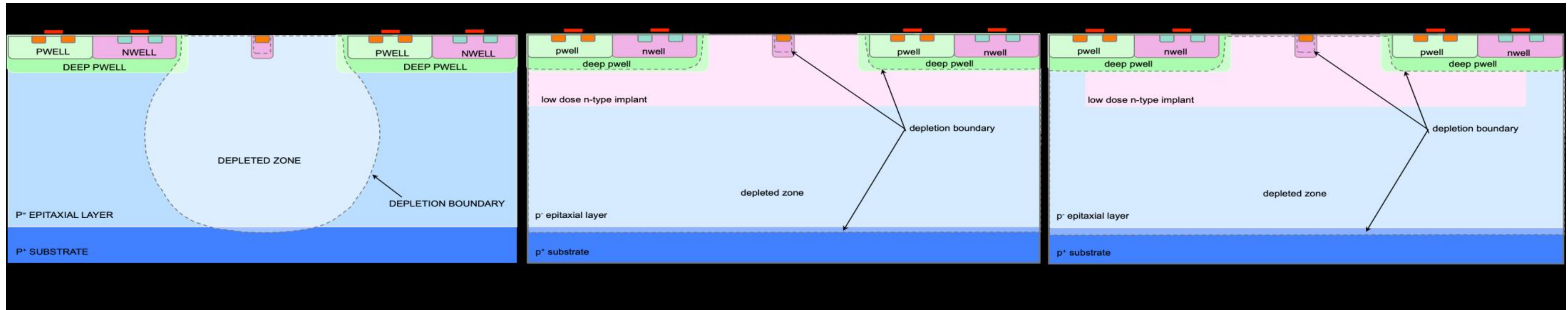
26cm long single silicon object



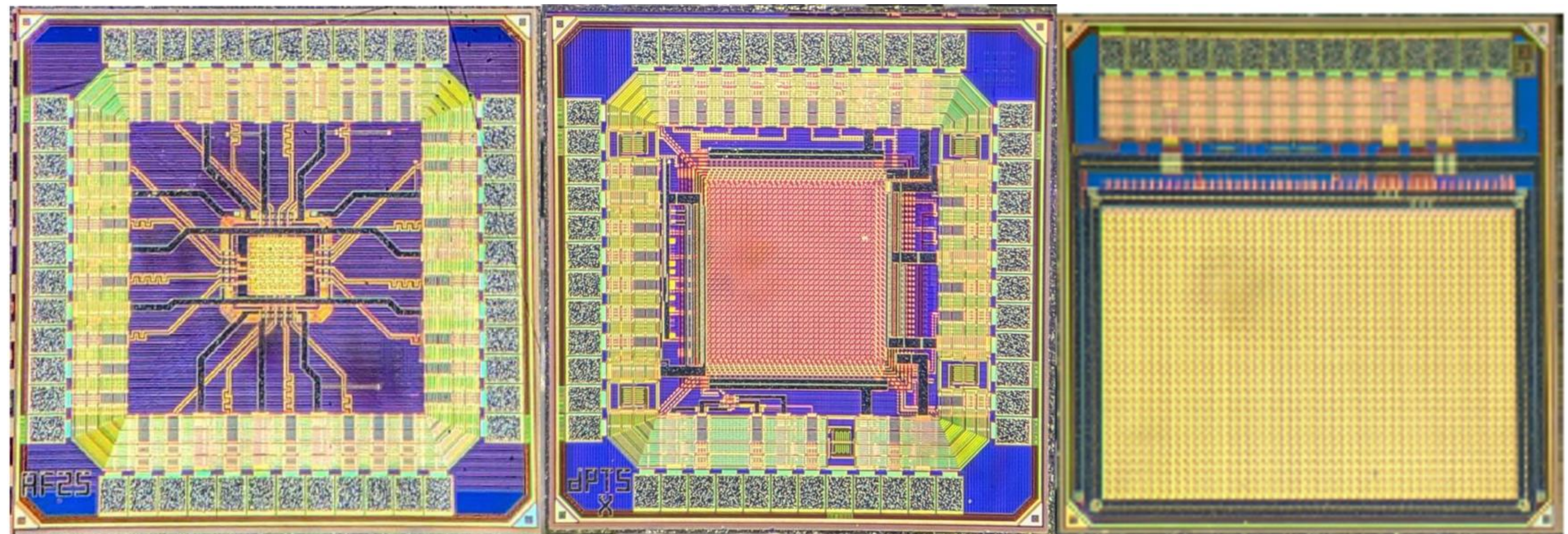
ER1 (December 2022): stitching

TPSCo 65 nm Prototyping for the ALICE ITS-3 Vertex Detector

MLR-1 run (2021): Analog & Digital output prototypes with 10-25 µm pitch & 3 epitaxial layer doping profiles



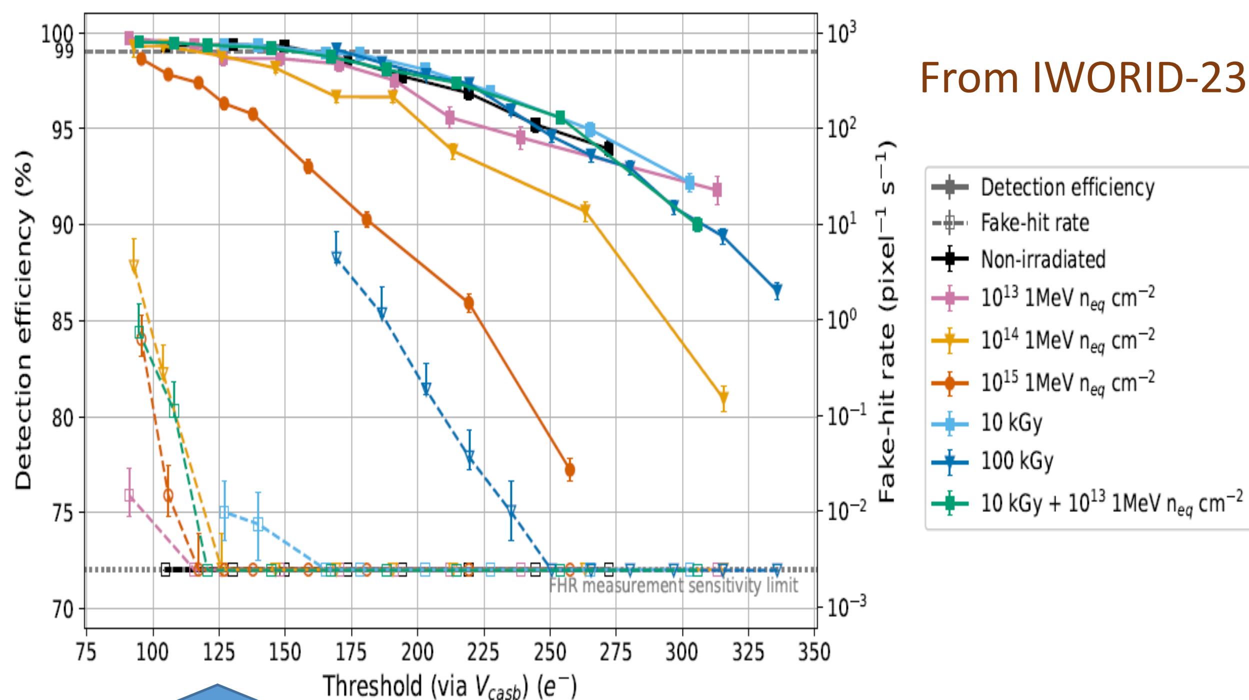
Technology validation & Detection Performance assessment based on 3 different Mini-sensors & various Test structures



APTS: analog output **DPTS**: digital output CE-65: analog output

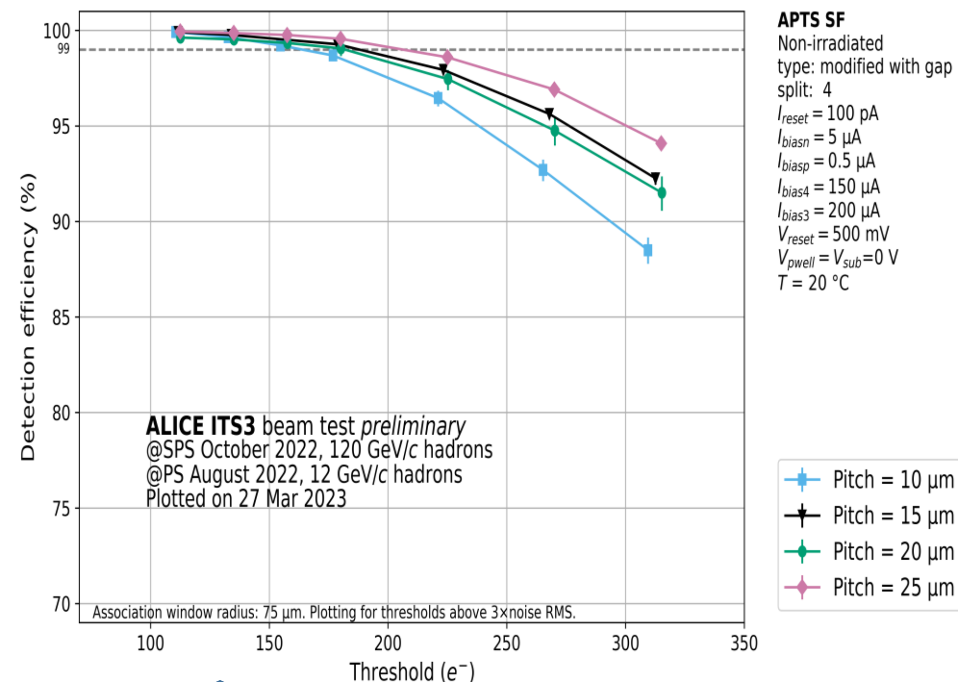
MLR1 TEST RESULTS

DPTS (15 µm pitch) Detection Efficiency versus NIEL and TID



Operation regime

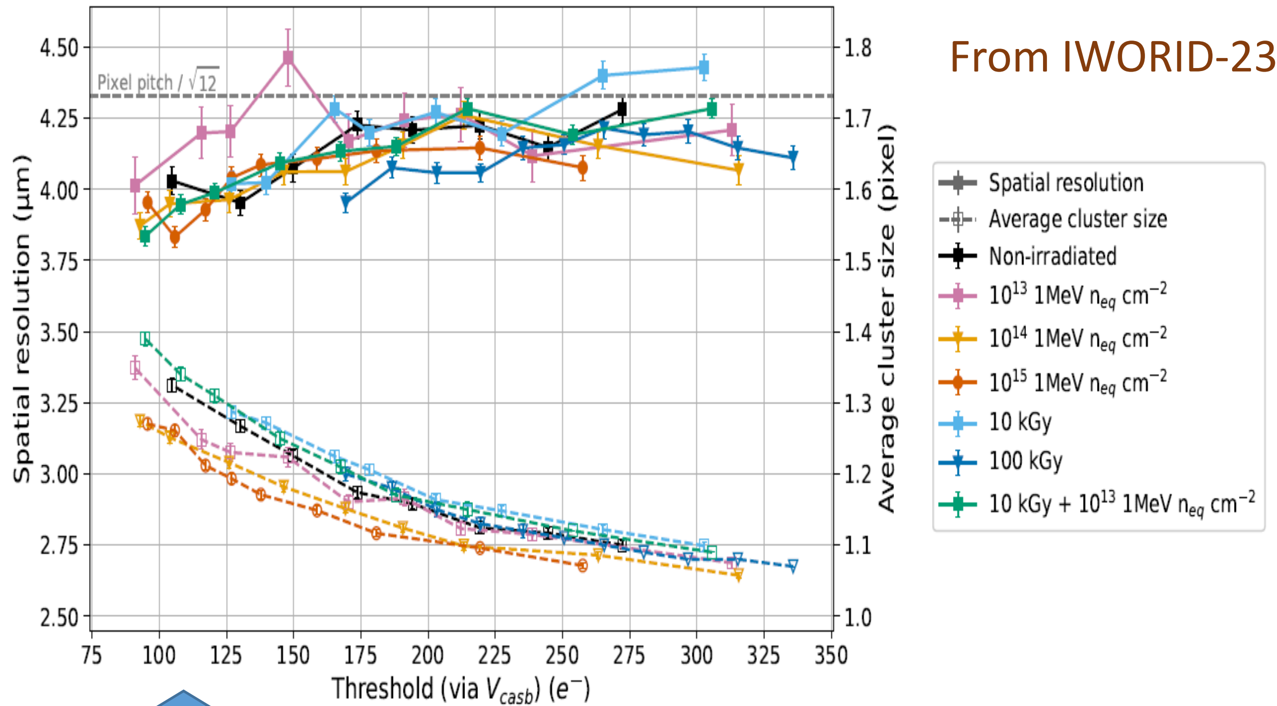
APTS Detection Efficiency for a pitch of 10, 15, 20, 25 µm



Operation regime

MLR1 TEST RESULTS: Spatial Resolution & Cluster Size

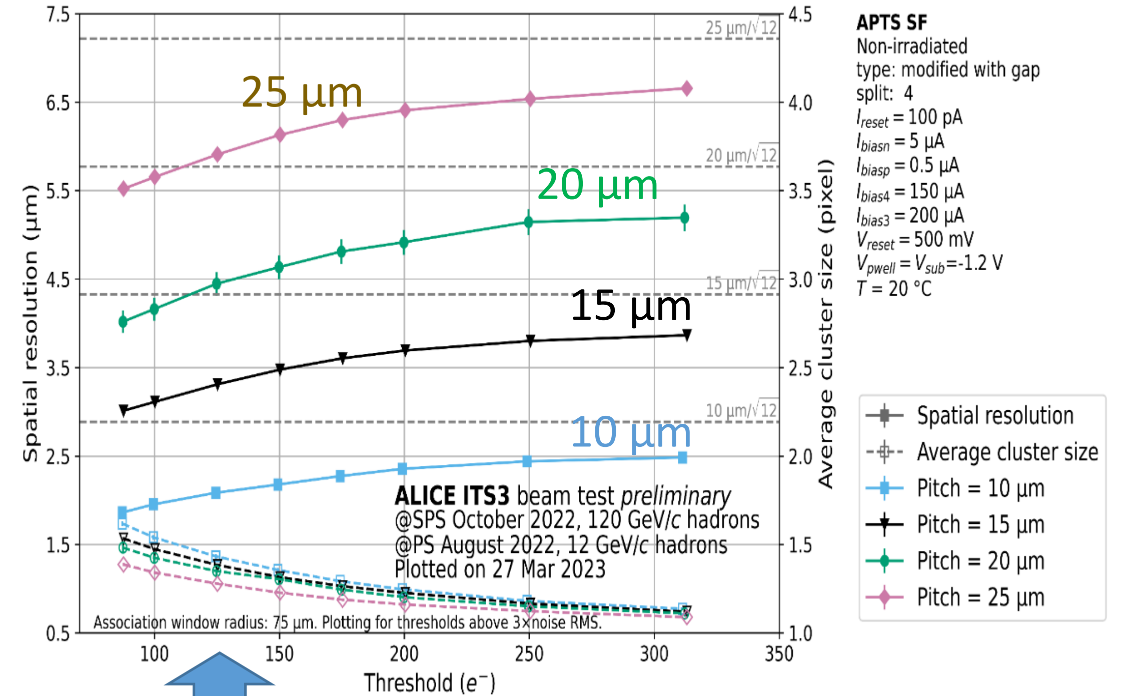
DPTS (15 µm pitch) vs NIEL and TID



From IWORID-23

Operation regime

APTS (10, 15, 20, 25 µm pitch)

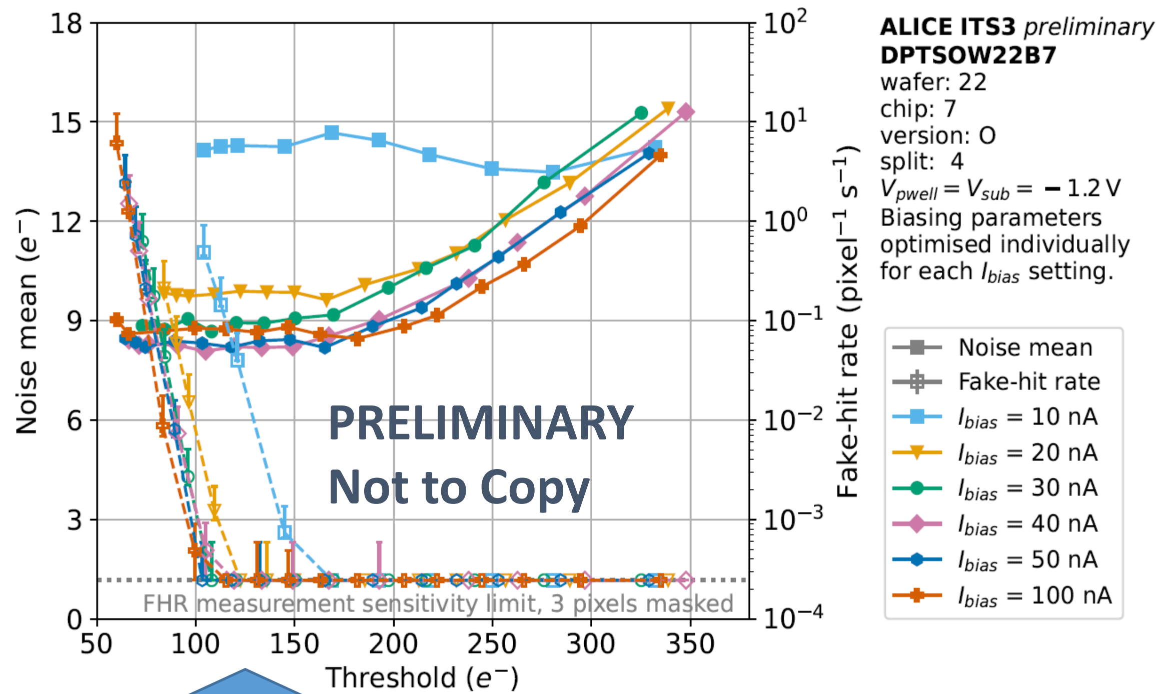


Operation regime

Binary resolution slightly better than pitch / √12 (impact of thin EPI ?)

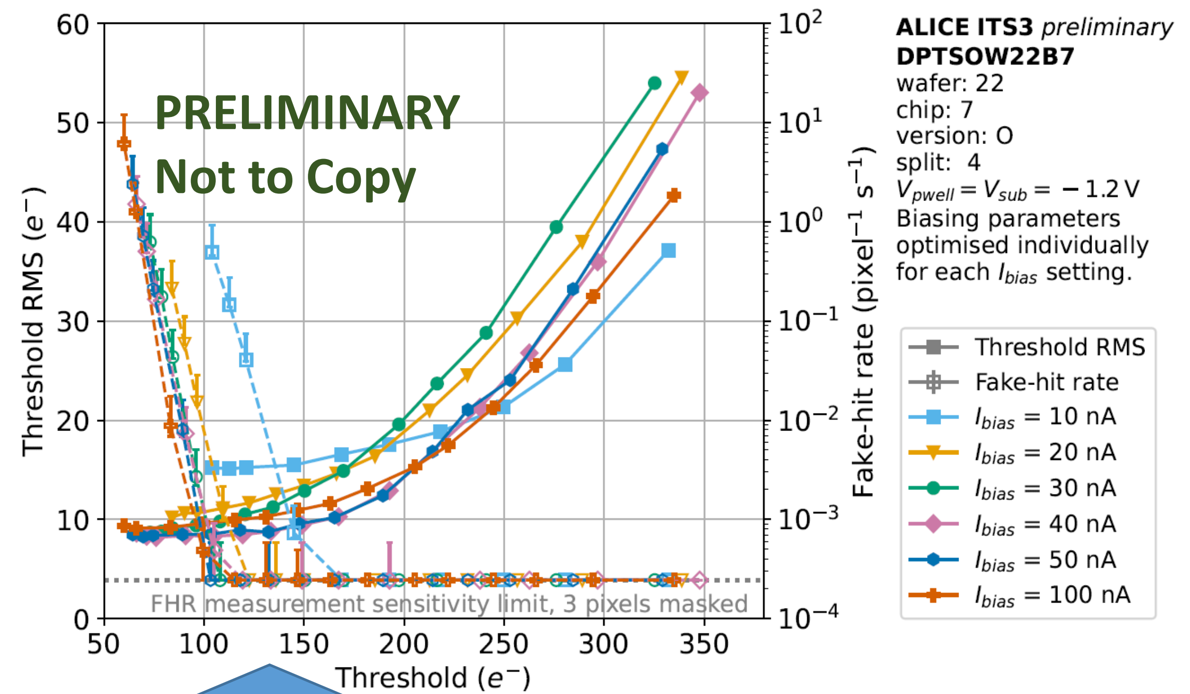
MLR1 TEST RESULTS (soon to appear in ITS-3 TDR):
Pixel Noise, Threshold Dispersion, Fake Hit Rate

DPTS (15 µm pitch): Pixel Noise



Operation regime

DPTS: Discri. Threshold Dispersion

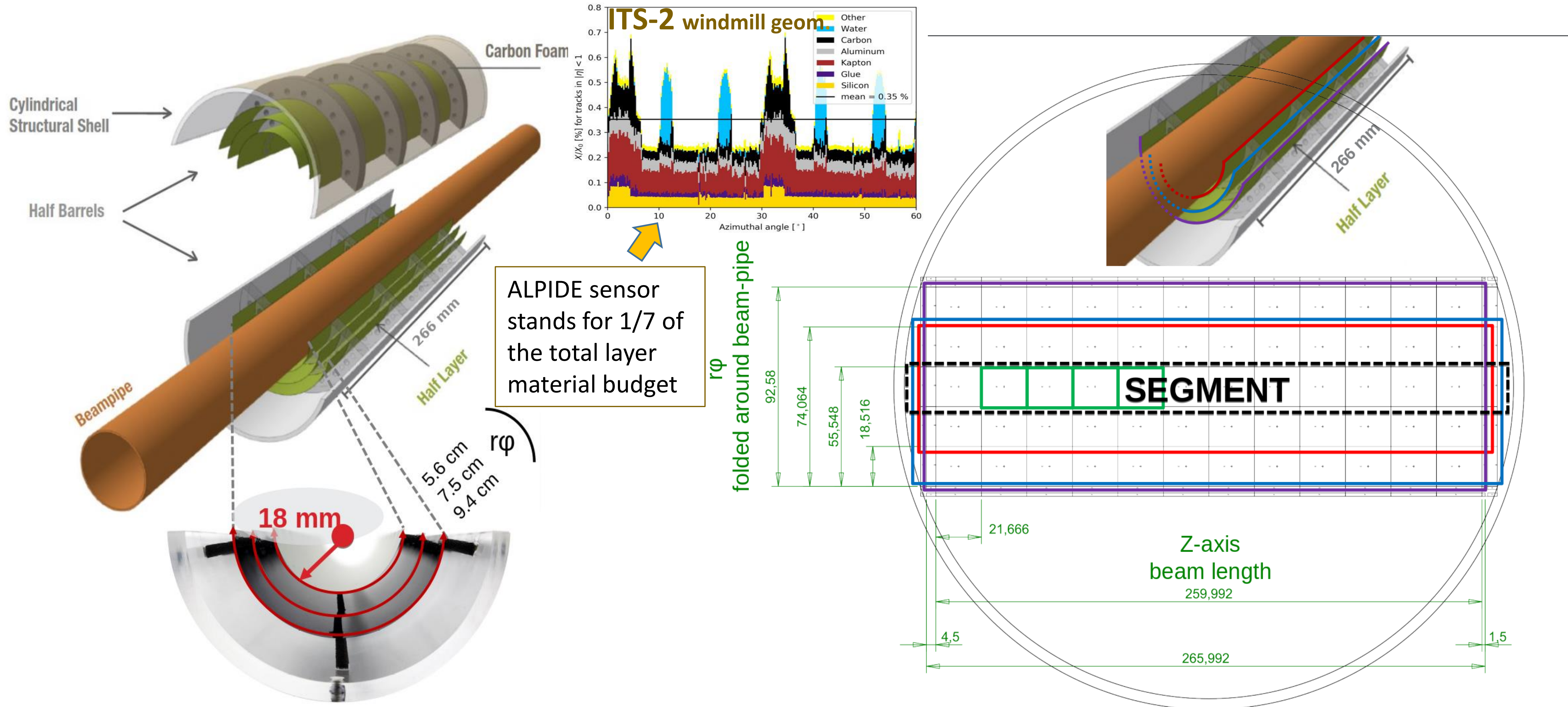


Operation regime

ITS3 TDR (draft): private communication

LARGE STITCHED CMOS SENSORS DEVELOPED FOR THE ITS3

ITS3: multi-reticle (stepping), thin (≤ 50 µm), curved sensors to reach ≤ 0.1 % X_0/ layer → stitching design rules



P
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2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
MLR 1		ER1	ER2	ER3	Commissioning			Run 4			

ER1 Submission

Aim at learning and proving **stitching**, submitted in December 2022

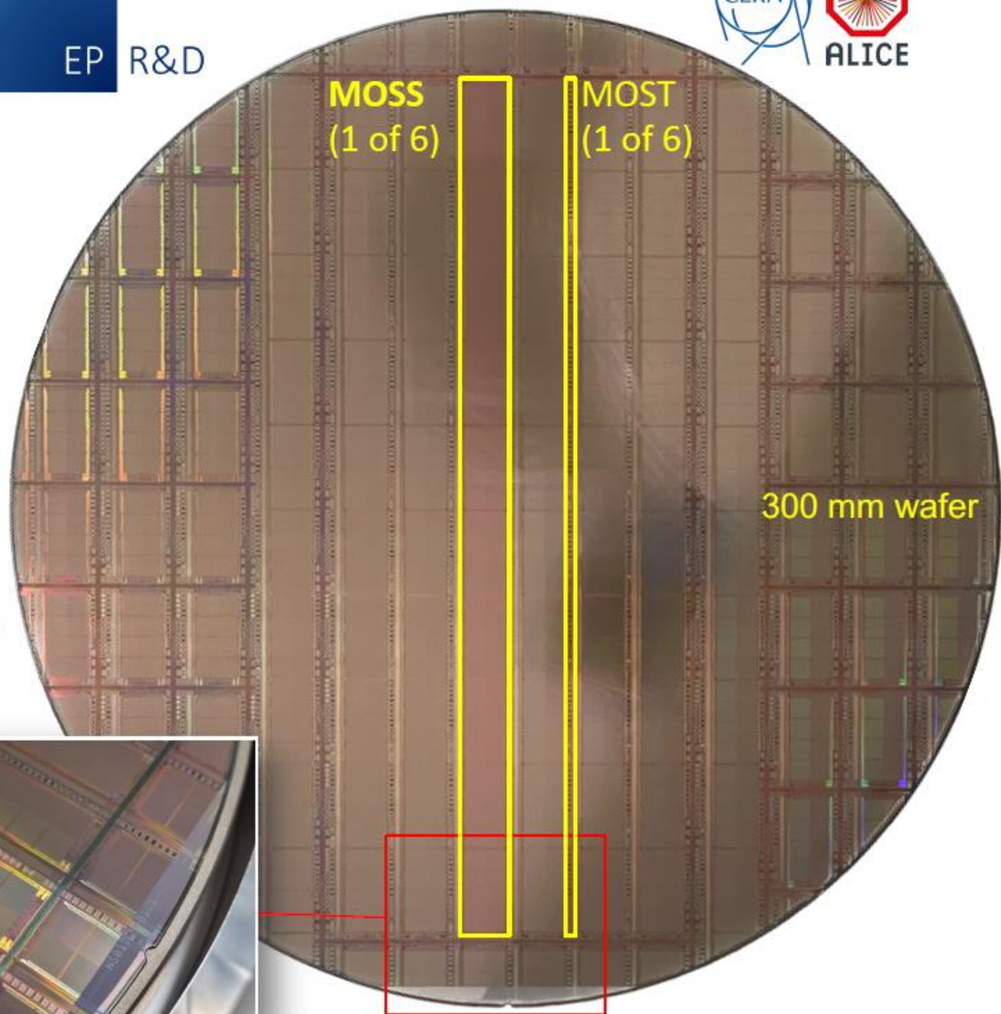
65 nm CMOS Imaging Technology

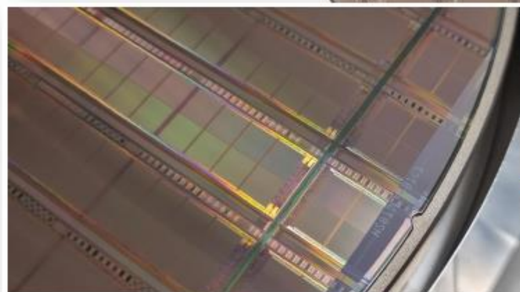
Design activities framed within **CERN EP R&D WP1.2**

- Large effort of several teams and institutes

Two wafer scale stitched sensor chips (MOSS, MOST)

- Different design approaches for resilience to manufacturing faults

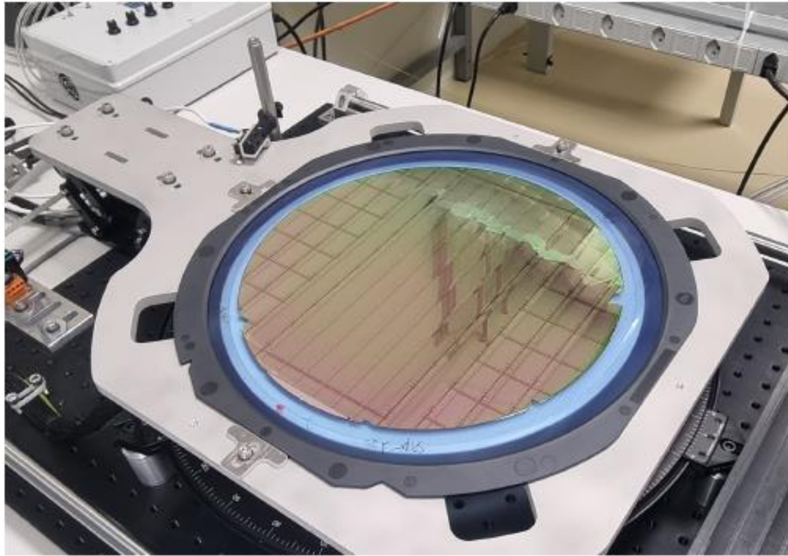


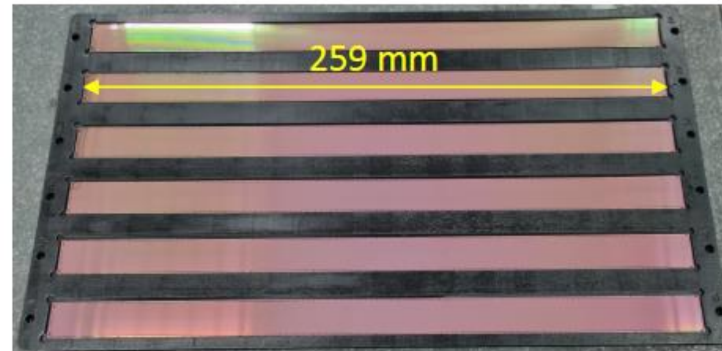


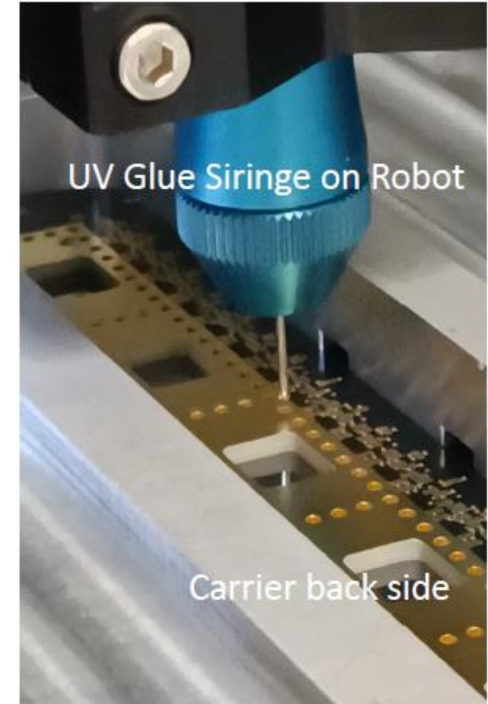
MOSS and MOST Tests on-going

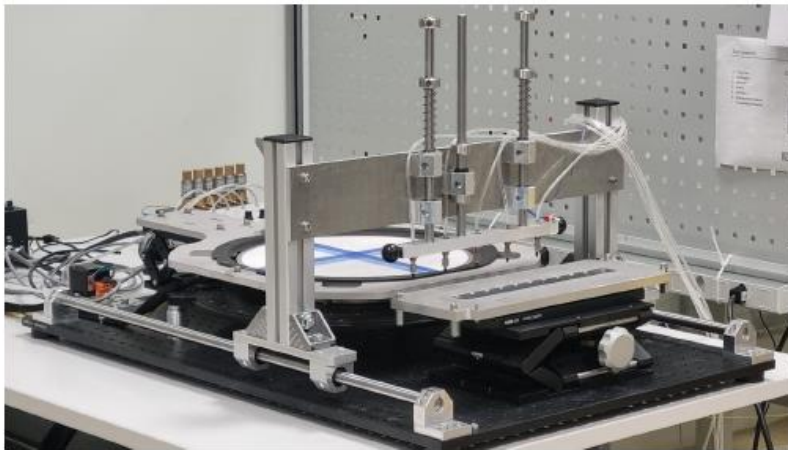
MOSS PROTOTYPE HANDLING

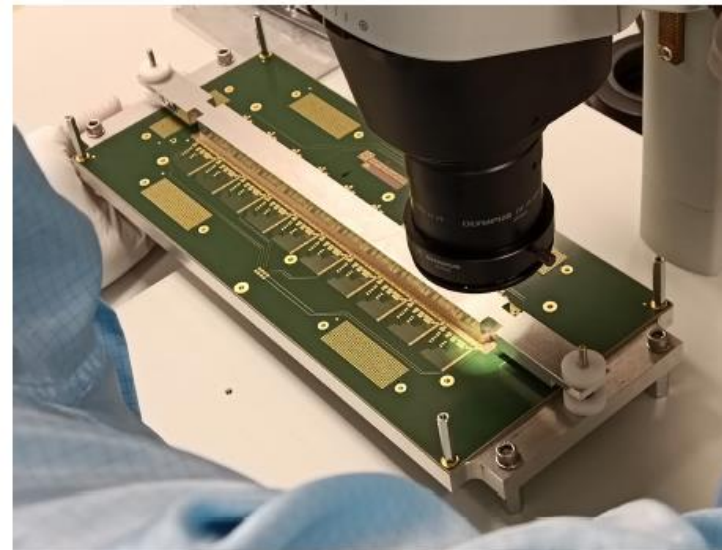
Pick, Align, Glue MOSS on Carrier

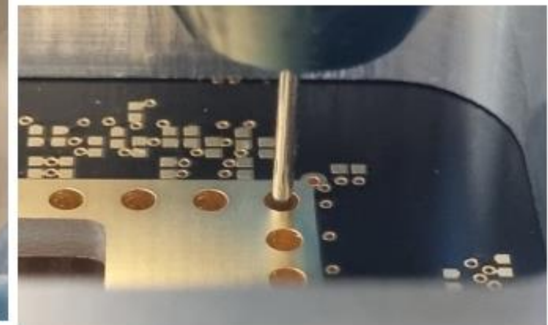




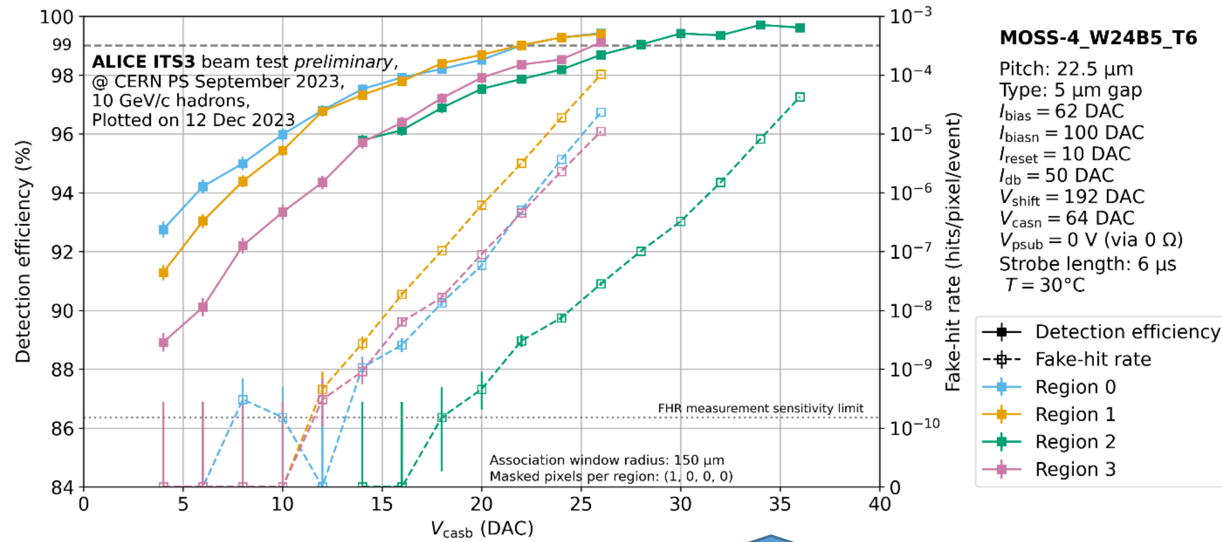


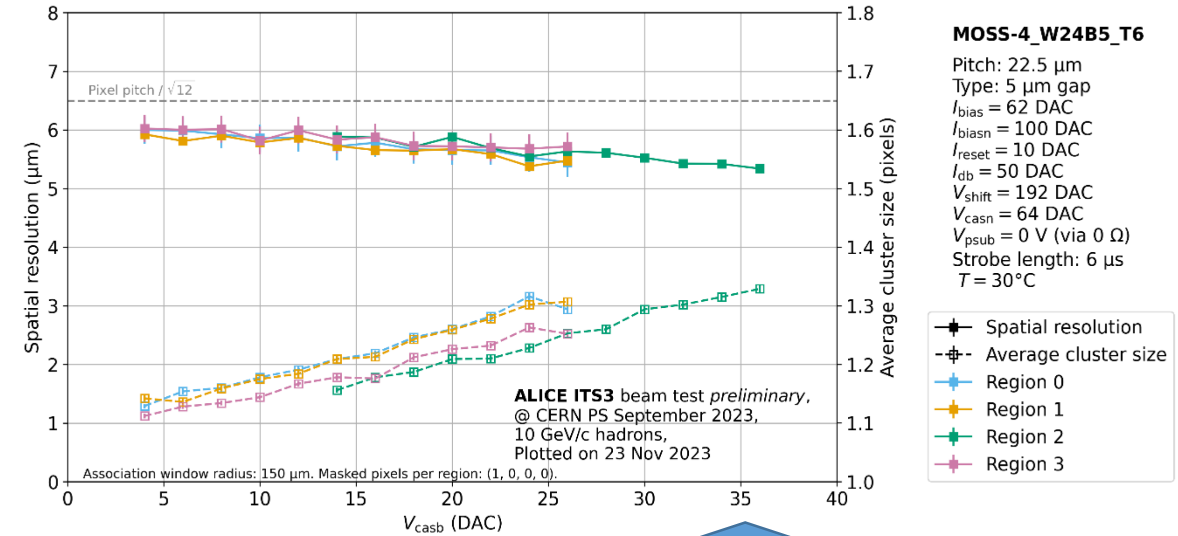






ER1: MOSS SENSOR TEST RESULTS





Operation regime

Operation regime

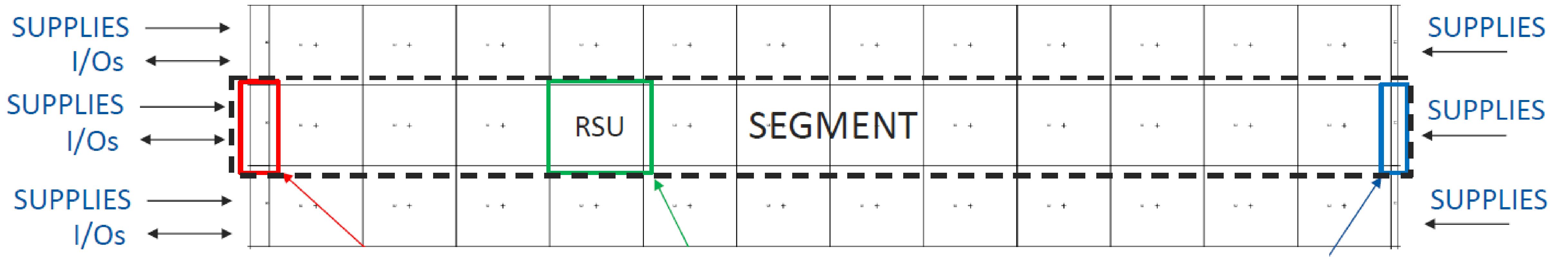
MOSS beam tests: 1st analyses indicate a spatial resolution ≈ 5 – 6 µm (binary charge encoding), close to pitch/√12

→ follows from pixel dimensions (22.5 µm x 20.8 µm) constrained by stitching rule induced system architecture design

→ shorter sensors (e.g. 12 cm long) may allow for (somewhat) smaller pixels, i.e. better spatial resolution (tbc)

Emblematic illustration of the necessity of a global approach when designing a sensor (experienced designers needed)

ER2: MOSAIX PIXEL SENSOR OVERVIEW



Control effects of yield, ageing, etc. ➡ **segmented pixel array**

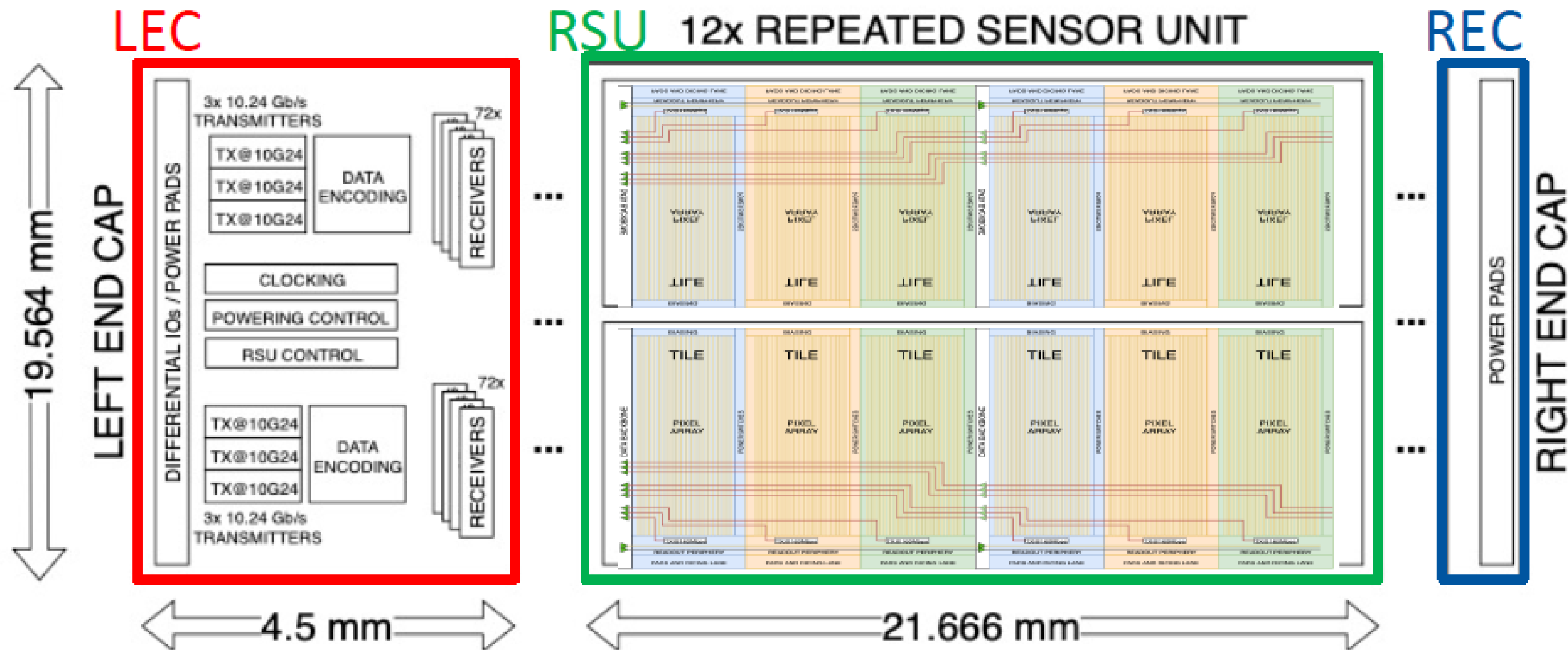
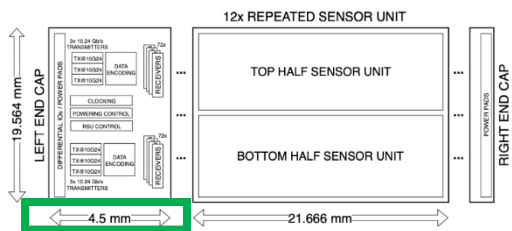


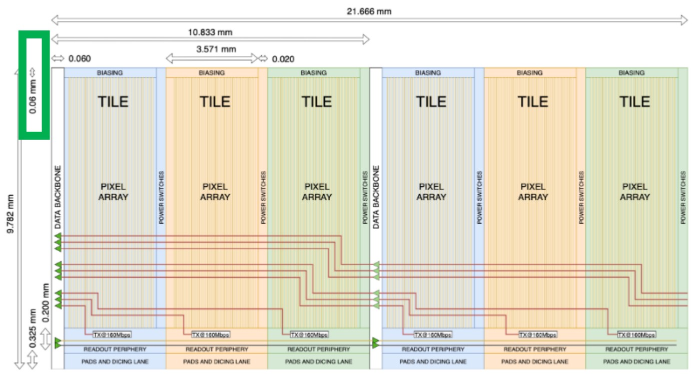
Figure 3.34: Block diagram of the sensor segment.

Courtesy of Gianluca Aglieri

Thermal analysis: Simulations with updated layout and heat map



Block diagram of the sensor segment (G.Aglieri)



Architecture of the bottom half sensor unit (not to scale)

	Power density [$mW\ cm^{-2}$]		
	Expected 25 °C	Max 25 °C	Max 45 °C
Left End Cap (LEC)		791	
Active area (RSU)	28	44	62
Pixel matrix	15	32	51
Biasing	168	168	168
Readout peripheries	432	457	496
Data backbone	719	719	719

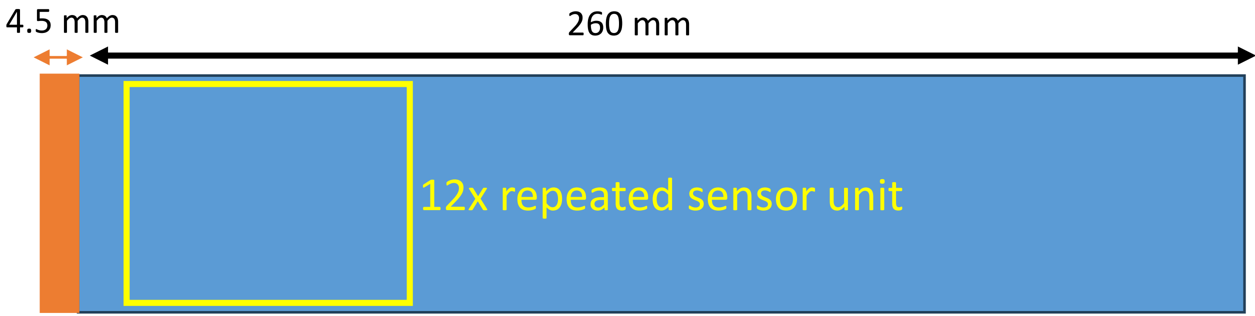
Estimates of power consumption

Total power dissipated by the 3 layers inside ITS-3 fiducial volume (1200 cm^2):

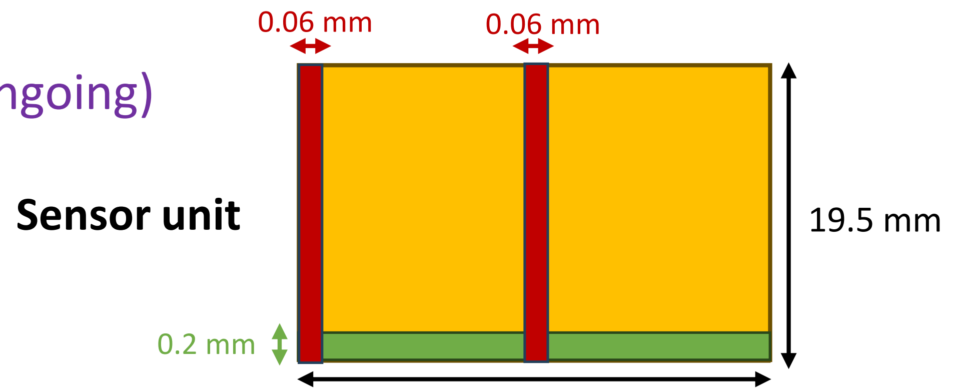
Ptot (fid. vol.) ≈ 50 W

- Update of the thermal simulation model with latest modifications
  1. Layout of L0 = 19 mm, L1 = 25.2 mm, L2 = 31.5 mm
  2. Heat map with all relevant components and power dissipations
- Pixel matrix power dissipation value not fixed → Simulations will be performed with 15 and 30 mW/cm^2

Computational model (ongoing)



End Cap, 800 mW/cm^2



21.6 mm

Matrix, 15 - 40 mW/cm^2

Periphery, 450 mW/cm^2

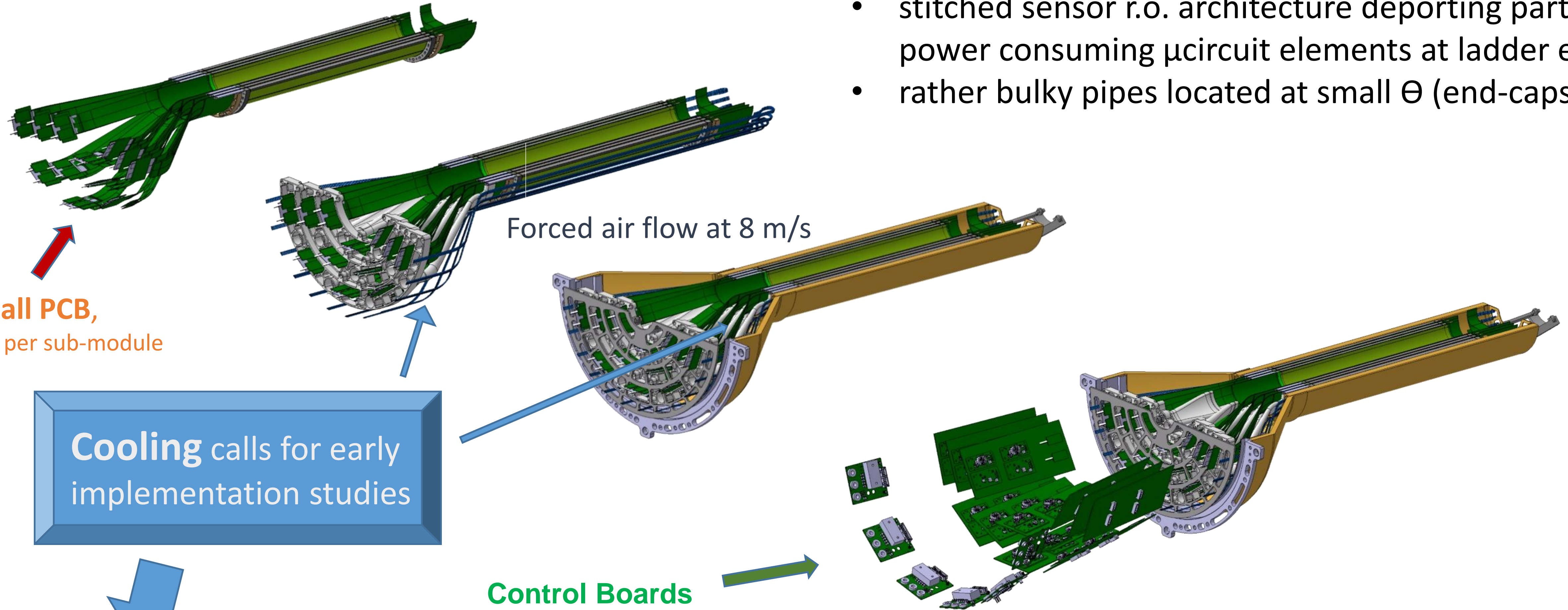
Data backbone, 700 mW/cm^2

From C. Gargiulo

ITS-3 SYSTEM INTEGRATION STRATEGY and PROCEDURE

Air Cooling inside sensitive volume achieved with

- stitched sensor r.o. architecture deporting part of power consuming μcircuit elements at ladder end
- rather bulky pipes located at small ϴ (end-caps)



Control Boards

Contains all the remaining electronics
It is divided in several segments avoiding acceptance cone
Different layouts under study

Impact on choice of sensor technology and design

ITS-3 SYSTEM INTEGRATION PROCEDURE

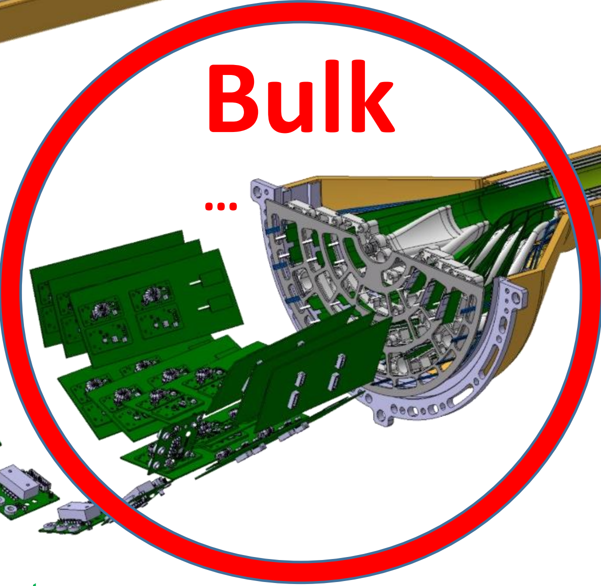
Services are of prime relevance, in particular for the FW and BW regions

Small PCB,
one per sub-module

Forced air flow at 8 m/s

Cooling calls for early implementation studies

Impact on choice of sensor technology and design



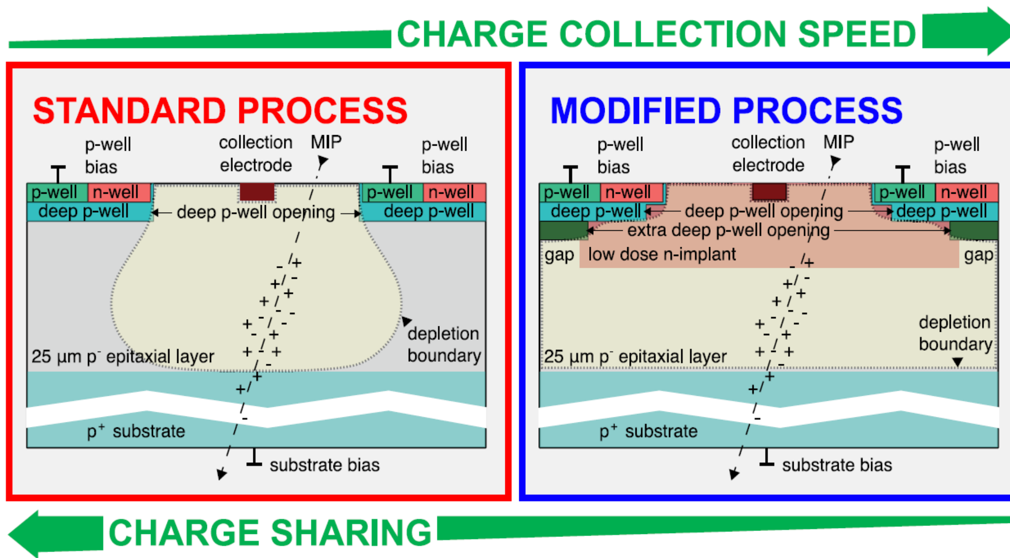
Merge with CLD cooling concept ?

Control Boards
Contains all the remaining electronics
It is divided in several segments avoiding acceptance cone
Different layouts under study

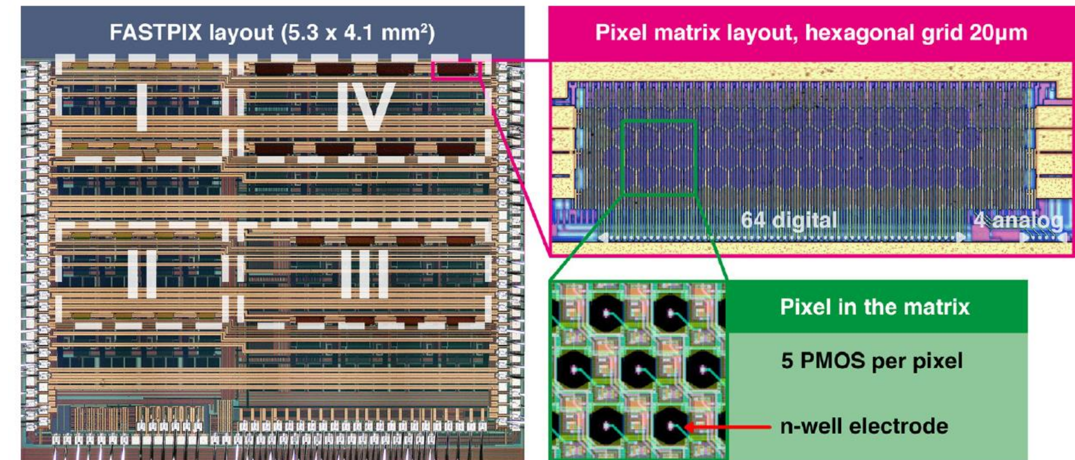
FAST CMOS SENSOR R&D

R&D objectives:

- different for BG rejection and PID (ToF)
- depend on radius/surface (small vs large) of the detector to equip
- overlaps slightly (CMOS-)LGAD development



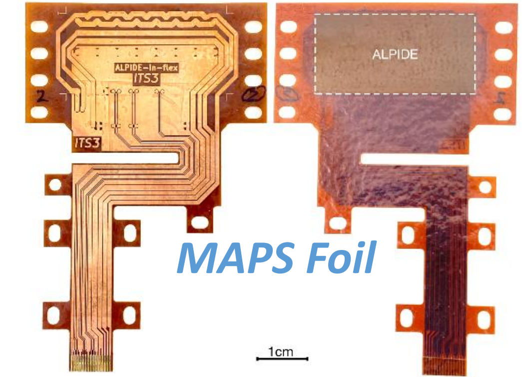
FASTPIX NIM A 1256 (2023) 168641



- FASTPIX: exploratory chip in TJsc 180 nm achieved O(100) ps time resolution with modified EPI
- Several prototypes fabricated in MLR-1 (TPSCo 65 nm) addressing HL-LHC and FCChh
- NAPA : CPS in TPSCo 65 nm for the C3 Higgs-Factory (goal ≈ 1 ns resolution with 25 µm pitch)
- ARCADIA: proto. device (CMOS LF-110) exploring r.o. circuitry options for future fast sensors equiping IDEA/FCCee

SUMMARY -- OUTLOOK

- **Significant progress during last years in the development of CPS & their use in expts (up to 10 m²):**
  - TJsc 180 nm process:
    - gets more (full custom) applications beyond ALICE-ITS2 (ALPIDE): CBM/FAIR, Mu3e, *Belle-II*, … : MIMOSIS-II for CBM may be a good seed for ILC
    - also considered for sub-nanosecond sensor design (FastPix)
    - used to investigate curved dices sensor mosaics (SuperAlpide) & embedded sensor blades



  - TPSCo 65 nm process seems validated for tracking devices, with limitations:
    - small signal amplitude (thin EPI)
    - spatial (& time ?) resolution, fill factor, yield with stitched sensors (for extra-low mat. budget)
- **Most of the progress was achieved within the ITS-3 project:**
  - Validation of new CMOS technology (TPSCo-65) and assessment of its limits/consequences
  - Pioneering design methology of wafer scale sensors using stitching rules of foundry (25 cm long CPS),
  - Validation of curved, wafer-scale, thin sensor concept (material budget < 0.1 % X_0 / layer),
  - Realisation of complete, very light, vertex detector design (mechanics, cooling) ⟹ impact on FW/BW regions
- **Ccl:** $\sigma \approx 3$ µm, < 0.1 % X_0/layer, < 50 mW/cm², $\Delta t \approx O(100)$ ns **in a single sensor** is still a challenge (next slide)
- **Sub-ns CMOS sensors:** still in early stage of R&D (no large sensor), but promising perspectives identified
- **CPS for calorimetry:** R&D with TPSCo-65 pursued by several groups (prominent challenge: power suppression)

COMMENT on SENSOR OPTIMISATION for the EW RUN

- **Achieving simultaneously** $\sigma \approx 3$ µm, < 0.1 % X_0 / layer, < 50 mW/cm^2, $\Delta t \approx O(100)$ ns within a single sensor seems unlikely with currently available CMOS technologies

  ➡ which parametres could be relaxed to preserve the most essential ones for phys. ?

- **Spatial resol. vs mat. budget**: shorter sensors suspected to allow $\sigma \approx 4.x$ µm (?) while preserving the asset of large stitched sensors to achieve < 0.1 % X_0 / layer (tbc)

  ➡ should trigger R&D interest in the ILC community

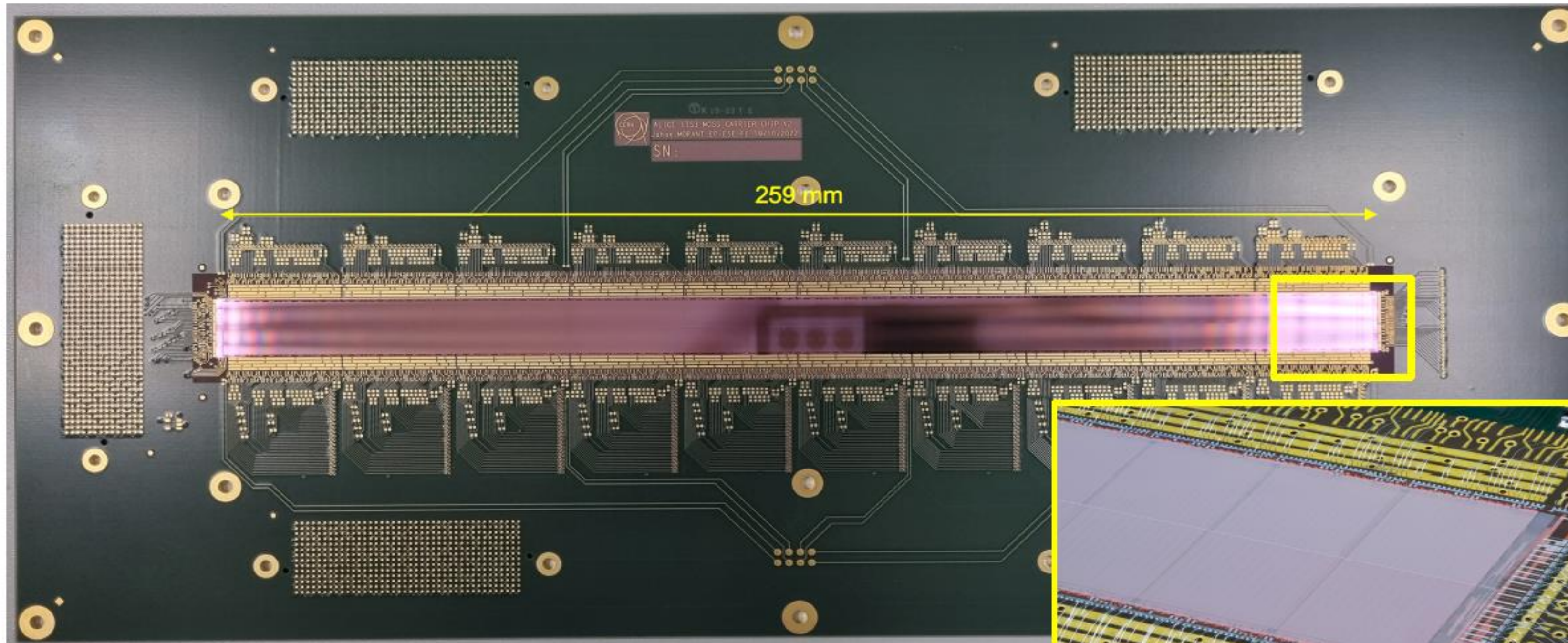
- **Power vs Δt** for the sake of air cooling at $\sqrt{S} <$ HZ threshold:
  - Higgs-top-EW factory ➡ Higgs, top, Z & T/QGC studies (HF comes in addition)
  - EW running conditions at FCCee and Giga-Z (polar) are quite different because of the different beam time structures ➡ low machine duty cycle (e.g. Giga-Z) allows to circumvent the conflict
  - Double-sided ladders : spatial / time resol. optimised on either side at the expense of mat. budget

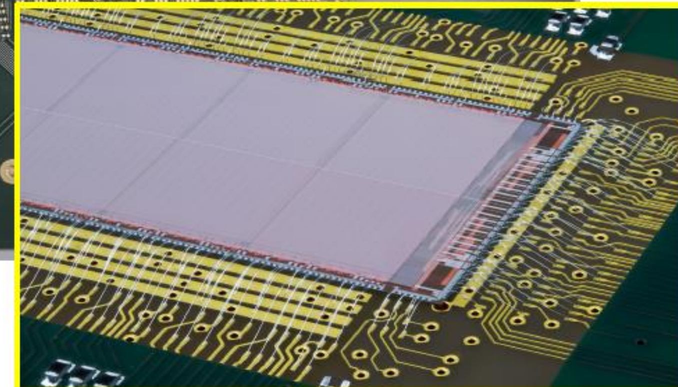
- R&D for the ALICE-3 project should provide valuable guidance

- Extensions of CMOS technology :
  - 3D-sensors (stacking) for small areas (cost, yield !) but extra mat. budget (no bending ?)
  - More advanced CMOS process: e.g. 28 nm ?

BACK-UP SLIDES

Wire Bonding MOSS on Carrier





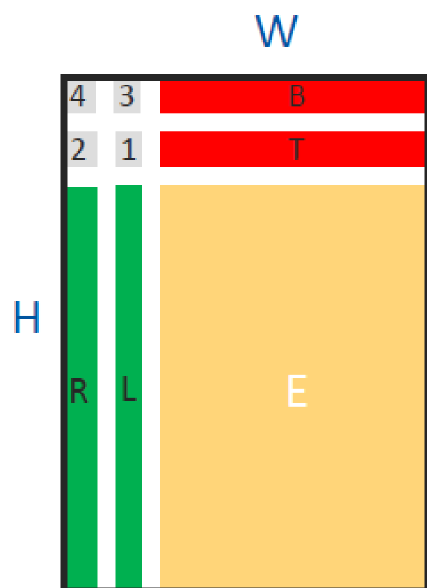
2192 bonding wires in two steps (1140+1052)

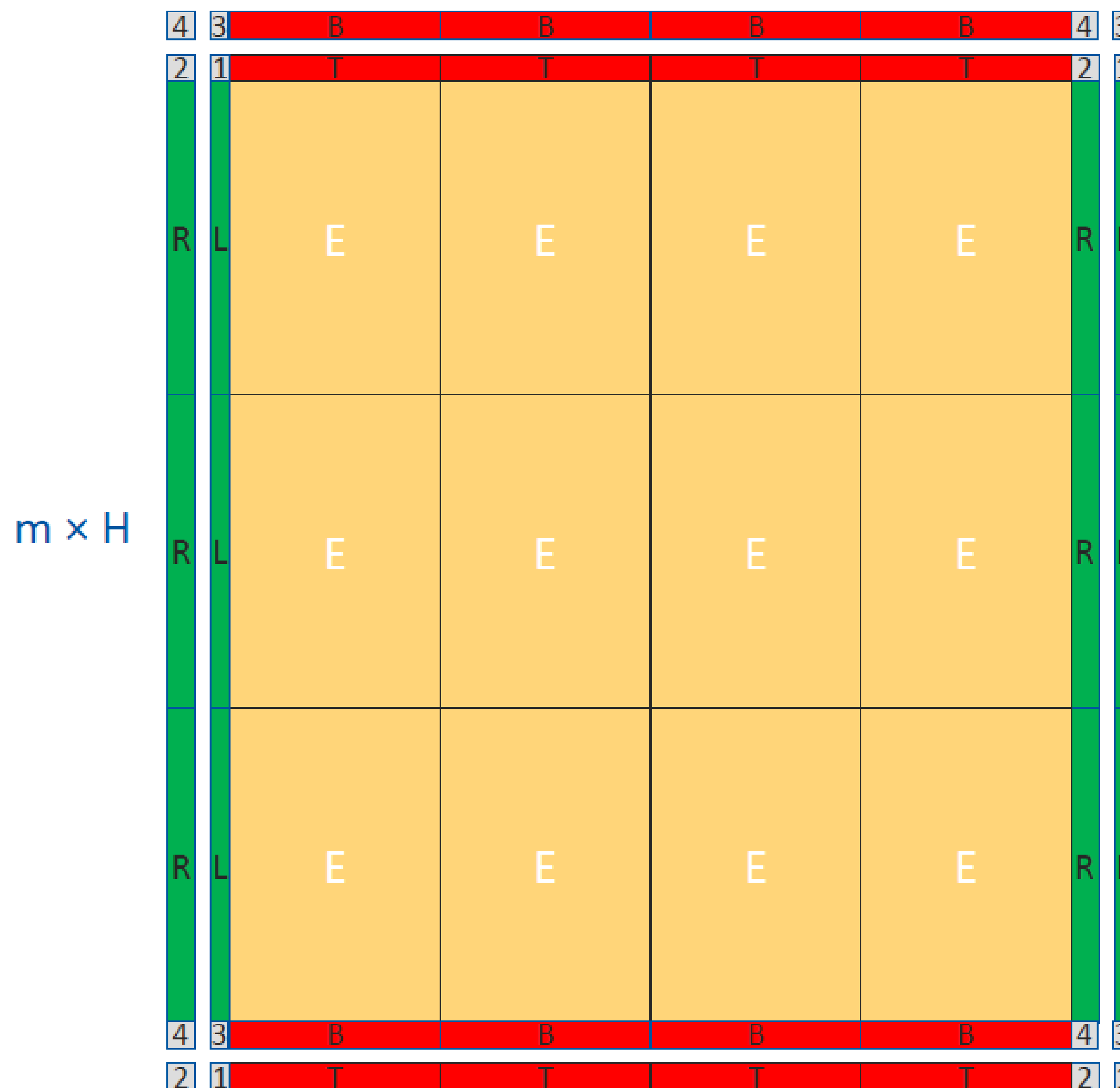
MOSS beam tests: 1st analyses indicate a spatial resolution ≈ 5 – 6 µm (binary charge encoding), close to pitch/$\sqrt{12}$

- → follows from pixel dimensions (22.5 µm x 20.8 µm) constrained by stitching rule induced system architecture design
- → shorter sensors (e.g. 12 cm long) may allow for (somewhat) smaller pixels, i.e. better spatial resolution (tbc)

Emblematic illustration of the necessity of a global approach when designing a sensor (experienced designers needed)

Stitching





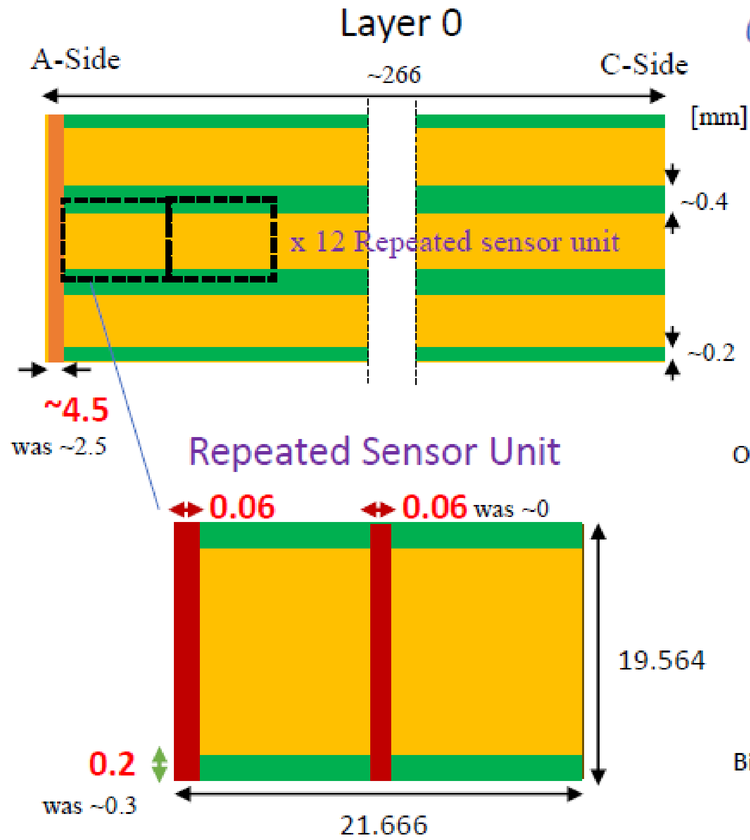
Courtesy of G. Aglieri

Thermal analysis: updating layout and power dissipation map

- Update of the thermal simulation model with latest modifications
  1. Carbon foam position and half-layer dimension.
  2. Power dissipation map with all relevant components.

Updated power dissipation map

@Collaboration with WP2



Estimates of power consumption

Operative temperature →

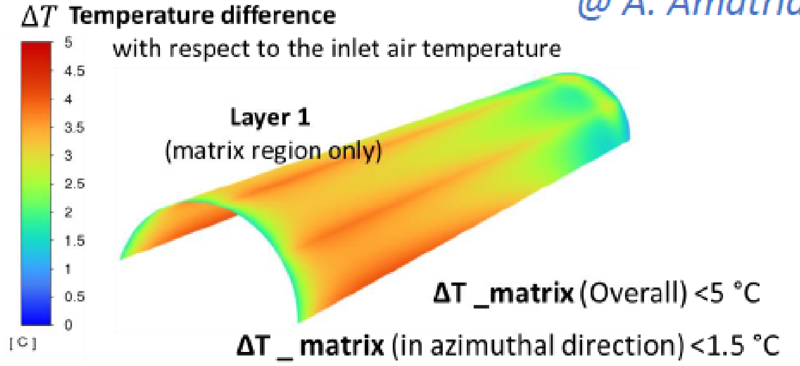
	Power density [mW cm^{-2}] Expected 25 °C	Max 25 °C	Max 45 °C	Latest assumption
Left End Cap (LEC)		791		~~1000~~
Active area (RSU)	28	44	62	
Pixel matrix	15	32	51	~~20~~
Biasing	168	168	168	
Readout peripheries	432	457	496	~~500~~
Data backbone	719	719	719	~~0~~

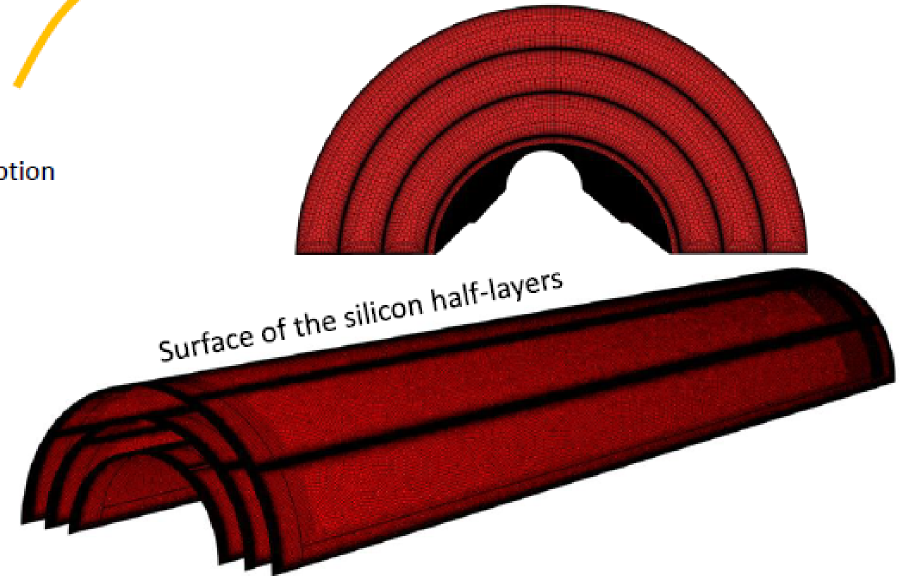
Biasing (0.06 mm, 150 mW/cm2) has been disregarded.

Computational model (ongoing)

- Pixel matrix power dissipation is temperature dependent
  → Simulations will be performed

@ A. Amatriain



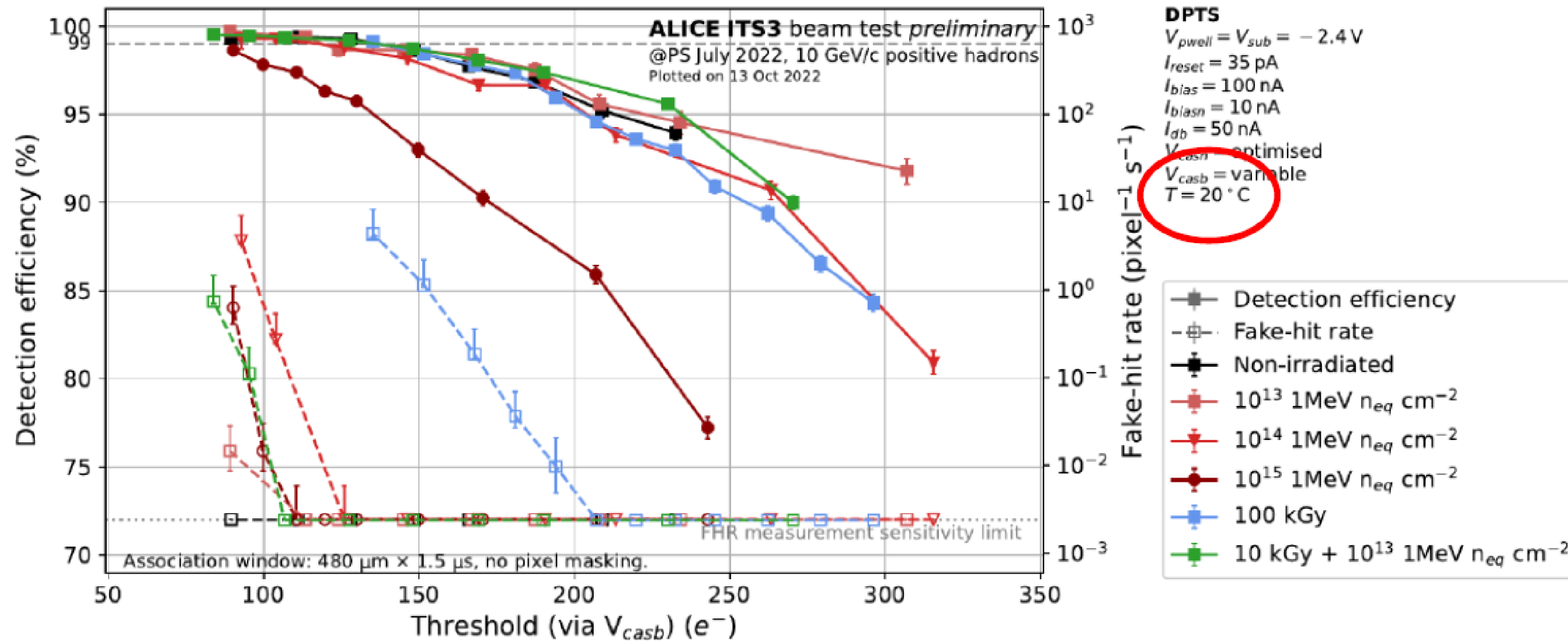


A compromise is going to be made (Mesh size Vs non-relevant area).

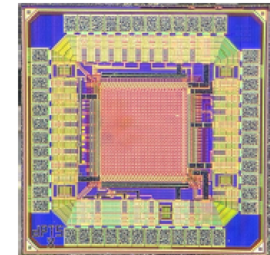
DRD7.6

doi: 10.1016/j.nima.2023.168589

TPSCo 65nm : qualified for HEP (synergy between ALICE ITS3 and WP1.2)



DPTS



15 x 15 µm^2 pixel

- Fully efficient after 10^{15} 1MeV n_{eq} cm^{-2}… at room temperature
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- Many features not yet explored (wafer stacking, special imaging devices…)

ALICE ITS3 REQUIREMENTS

3 Cylindrical layers

Made with **6 curved wafer-scale single-die** Monolithic Active Pixel Sensors

Radii 18/24/30 mm, length **27 cm**

Thinned down to **<50 µm**

Position resolution ~5 µm

-> Pixels **Θ(20 µm)**

Electro-mechanical integration

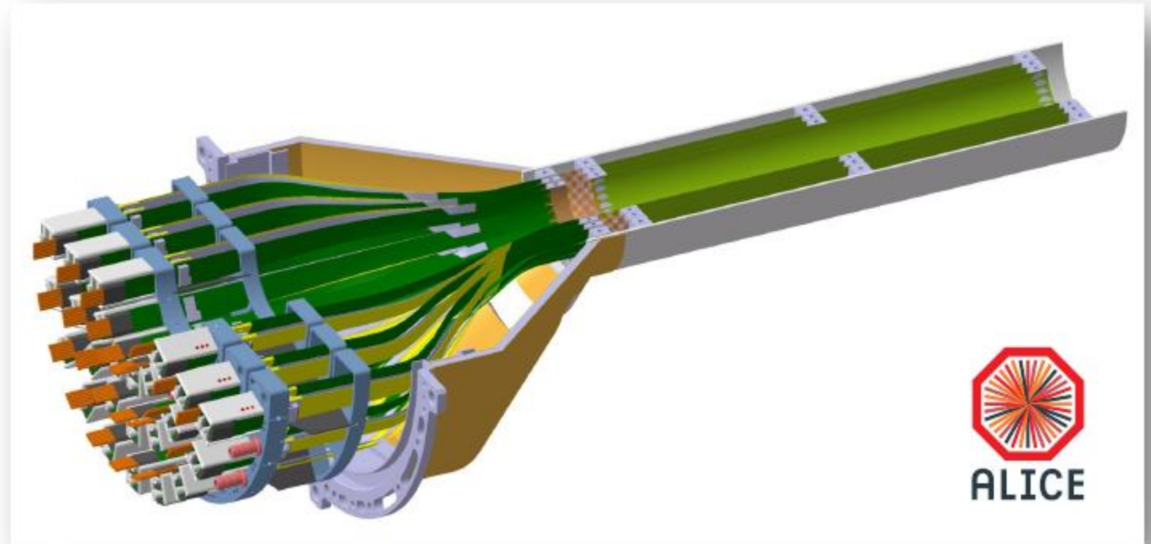
No flexible circuits in the active area

-> Distribute supply and transfer data on chip to the short edge

Cooling by air flow

-> Dissipate less than *20 mW/cm²* (in sensitive area)

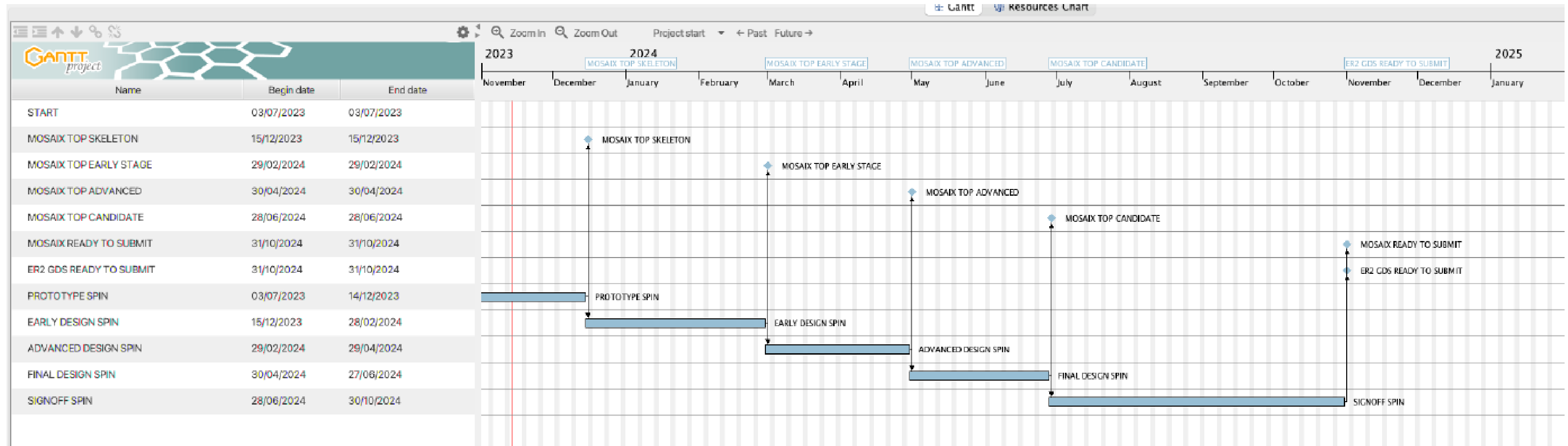
ALICE ITS3 LoI CERN-LHCC-2019-018 / LHCC-I-034



Pb-Pb Interaction Rate	50 kHz
Particle Flux	2.2 MHz/cm^2
Integration time	< 10 µs
TID	<10 kGy
NIEL	1×10^{13} 1 MeV n_{eq} cm^{-2}

Courtesy of Gianluca Aglieri

MOSAIX DESIGN MILESTONES



Design completion (full GDS): 28/06/2024

Final signoff spin and corrections: July-October

Submission: October 2024