



Contribution ID: 142

Type: Talk

Suitability of a 65 nm CMOS imaging process to reach the position resolution required by a vertex detector at an e^+e^- future collider

Tuesday 21 October 2025 12:55 (17 minutes)

The performance of monolithic CMOS pixel sensors strongly depends on the fabrication process, particularly on the feature size, which directly impacts the achievable pixel pitch.

A consortium led by the CERN EP R&D program, the ALICE experiment, and various European projects (AIDAInnova, EURIZON) is investigating the benefits of a 65 nm CMOS imaging process to design a new generation of pixel sensors. These developments enabled the upgrade of the inner layers (ITS3) of the ALICE experiments and are fostering further studies for detectors including those for future e^+e^- colliders that are still currently unmatched by any technology.

Three fabrications of a variety of prototype sensors already took place, in 2020, 2022, and 2023. The present contribution reports on the characterization of the second version of the CE-65-v2 (Exploratory Circuit) sensor family. The CE-65-v2 sensor includes AC-coupled and analog output pixels exclusively in a squared or staggered arrangement. They include analog output matrices featuring 48×24 (1152) pixels with either 15- μm , 18- μm or 22.5- μm pixels. Three versions of the sensing node were fabricated to modify the charge sharing between pixels. Illumination with ^{55}Fe source allowed us to estimate the equivalent collection node capacitance and its pixel-to-pixel fluctuation, as well as the leakage current before and after irradiation. Non-irradiated sensors were tested in a 4 GeV electron and 120 GeV mixed hadrons beam to study in detail the charge sharing among pixels and extract the sensor detection efficiencies as well as their position resolutions.

In this work, we focus on the performance of matrices with 18- μm and 22.5- μm pixels, emphasizing an original hexagonal staggered layout. This design offers potential advantages in terms of symmetry and charge collection, and represents a significant innovation compared to the conventional squared pattern, also studied for reference. The evaluated pixels were implemented in three design variants: blanket, standard, and gap. The evolution of the latter with digitization strategies, simulated from the data, was also investigated to explore the potential of pixels with binary or few bits output, designed in this 65-nm process, to match the excellent resolution expected for the inner layers of an e^+e^- detector. We pursue to continue developing the 65-nm process with the goal of fulfilling all e^+e^- vertex detector requirements and improve upon them.

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Session Classification: Tracking, vertexing and timing

Track Classification: Detector: Tracking, vertexing and timing