SiW-ECAL in 2026

Vincent Boudry for the SiW-ECAL groups

Institut Polytechnique de Paris

LCWS2026, KEK, 11/11/2026

SiW-ECAL : a Design for Higgs Factories

ASU = most critical element (~100k pieces)



HCAL

Endcap2

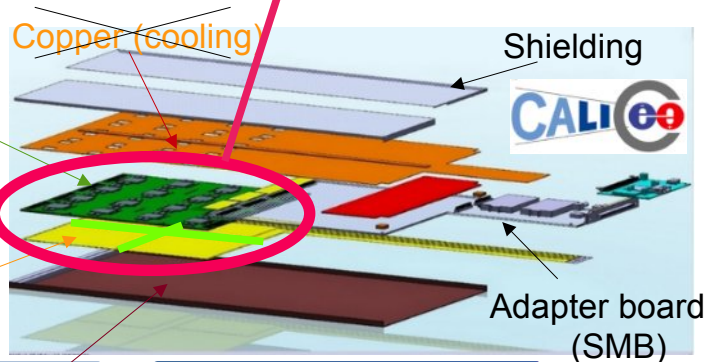
Endcap1

Barrel

ECAL

B = 2 – 3.5 T

PCB (FeV)
16 SK2 ASICs
1024 channels
ASU
Wafer (4)

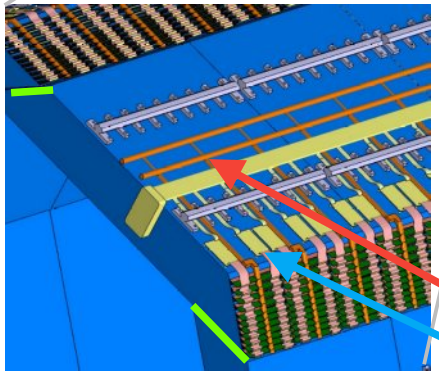


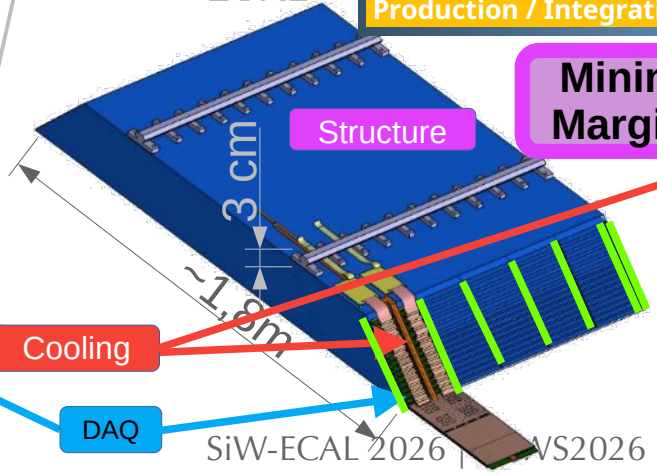
Carbon+W

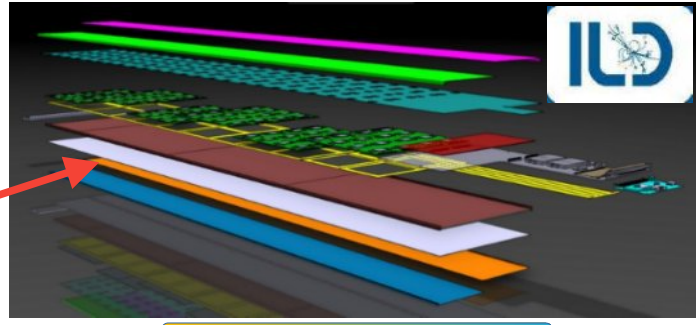
U layout of a **short slab**

- Physical
- Instrumental
- Electronics
- Mechanical
- Thermal
- Production / Integration

Mininal Margins







U layout of a **long slab**

+ timing

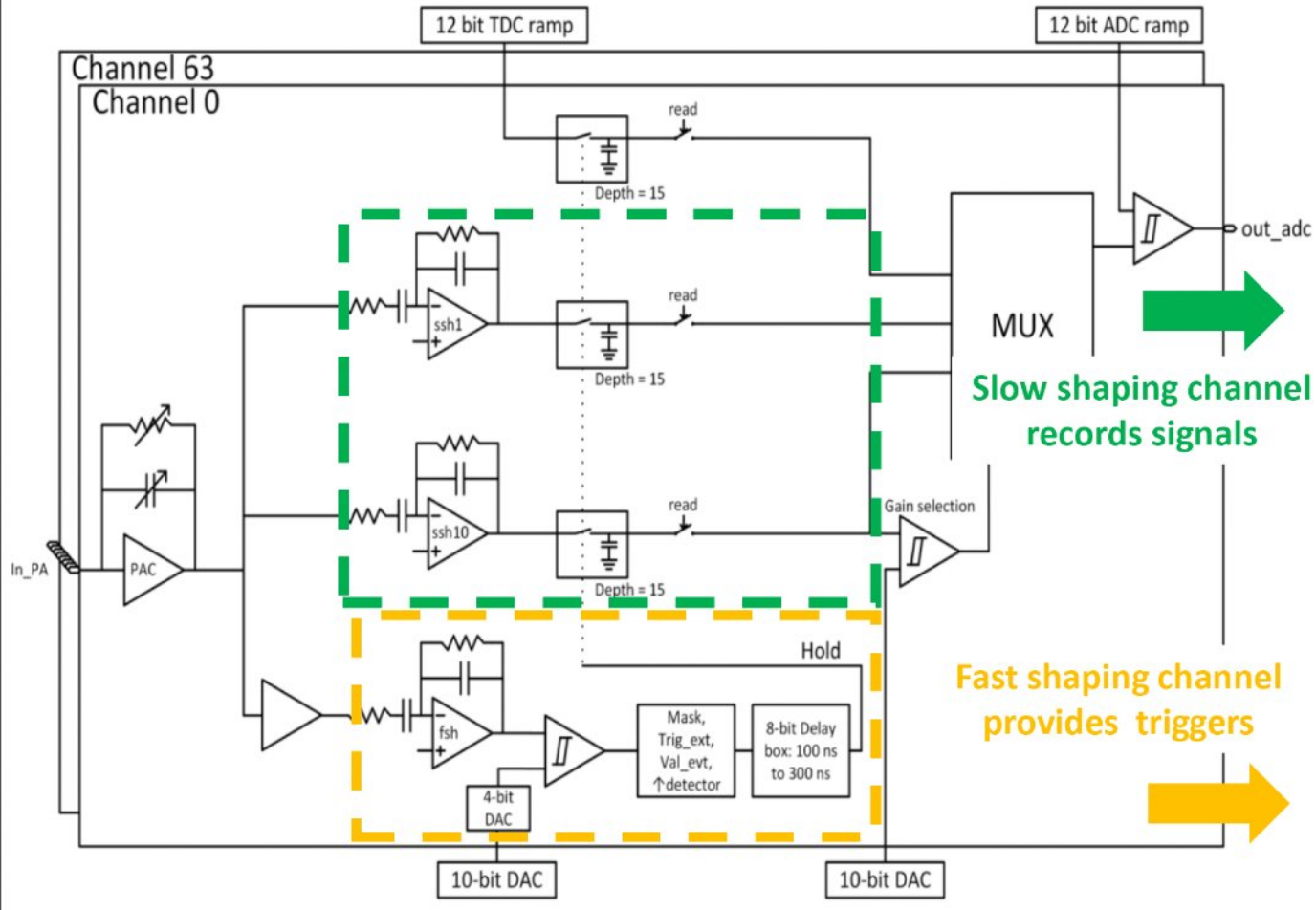
Cooling

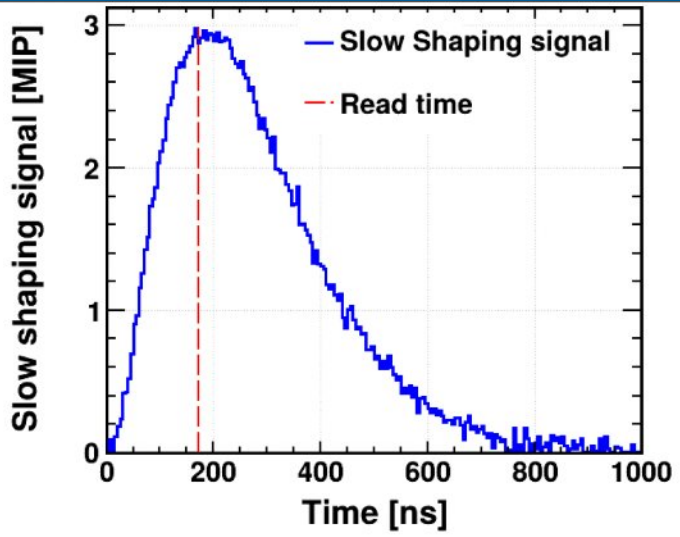
DAQ

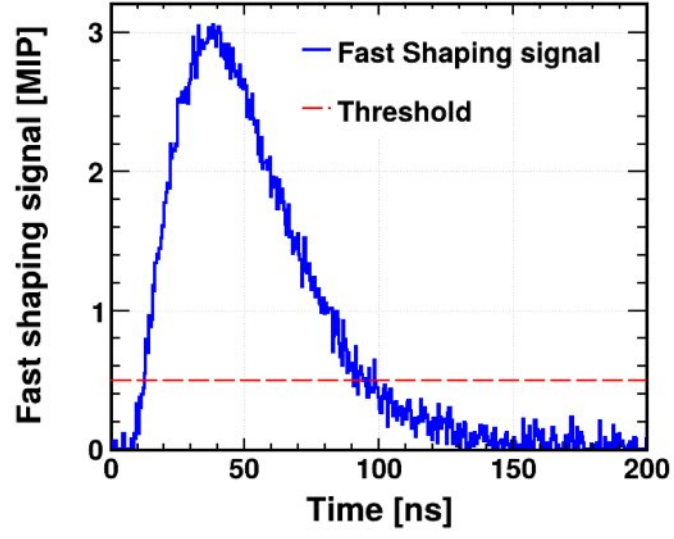
PP ↔ Cont



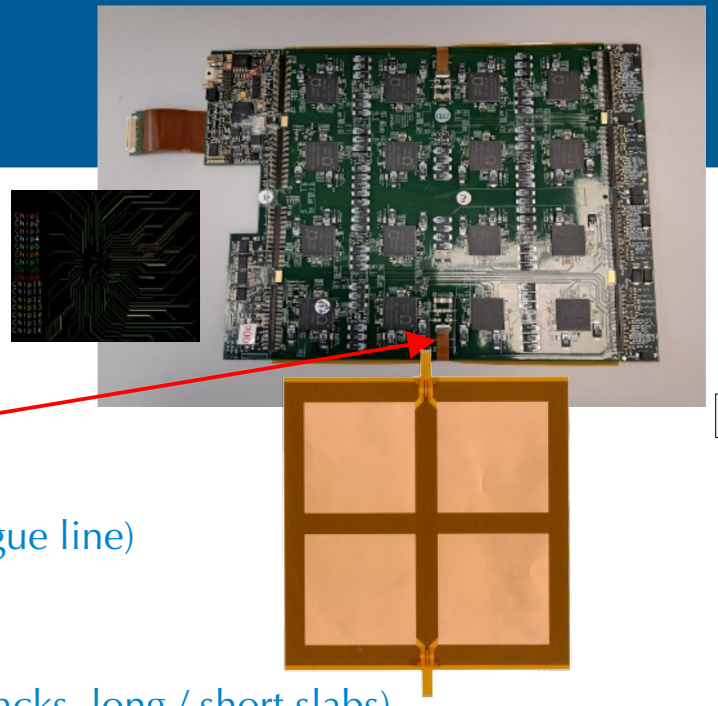
SKIROC chips

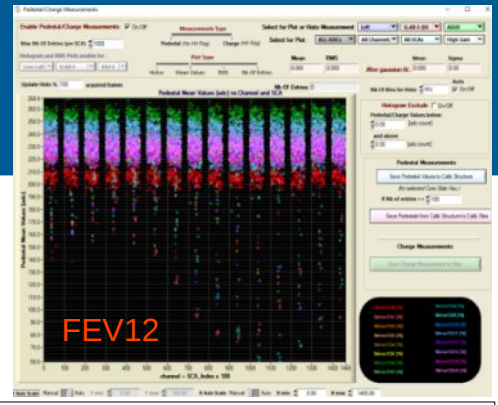




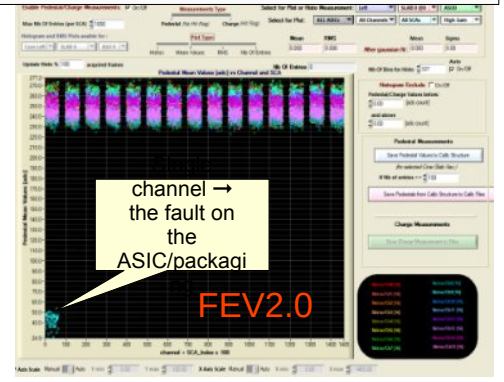


“ultimate” ASU2.1 (2023) SLBoard and DAQ





Pedestal measurements vs. Ch# + Mem#×100)



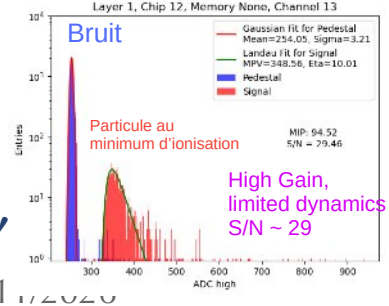
Improvements wrt FEV11/12/13

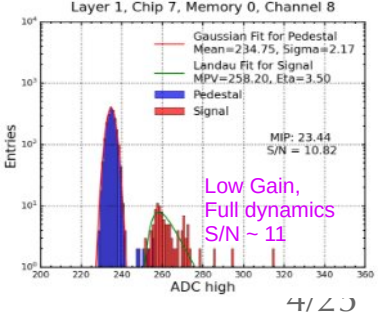
- Power distributions
  - Local LV power regulation: LDO’s
  - Local HV filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing streamlined
- Stand-alone HV distribution
  → **flexibility** (testing, reuse for ≠setups: stacks, long / short slabs)

Status:

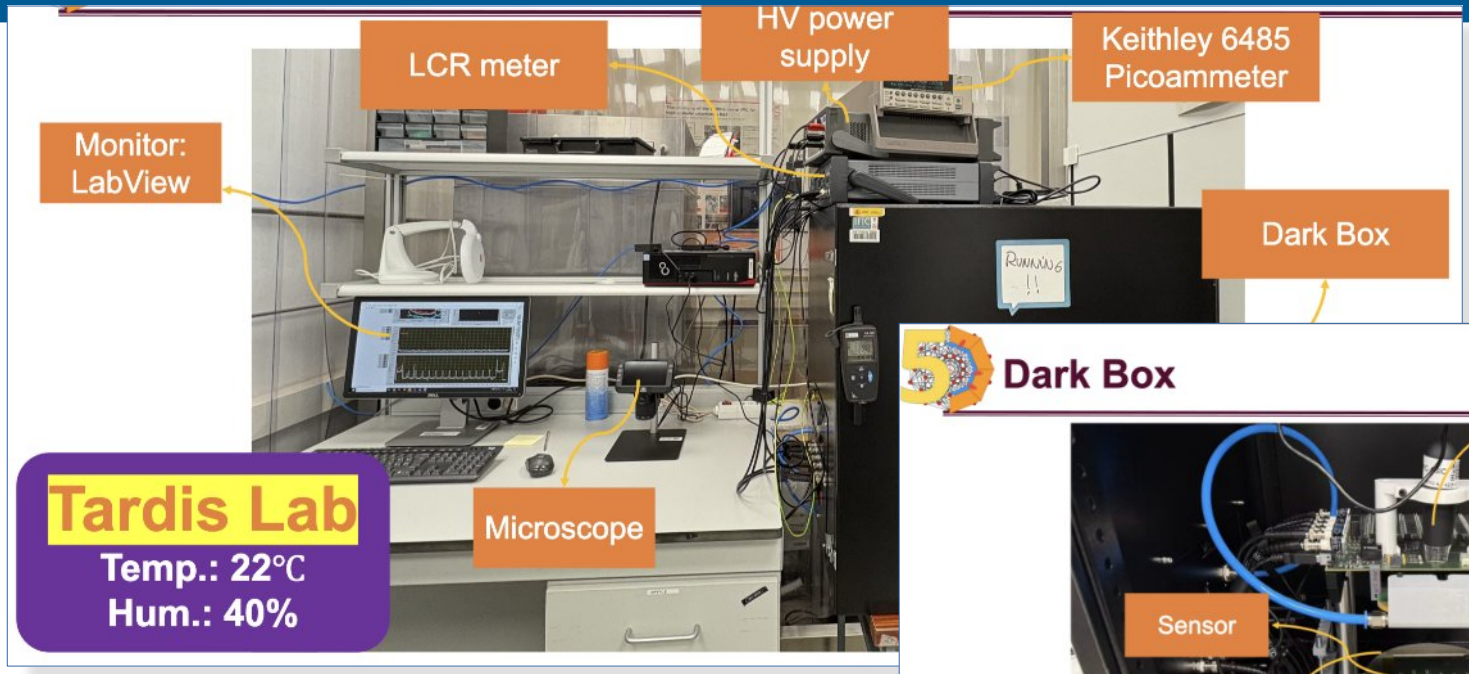
- Noise uniformity dramatically improved
  (ex: outliers in thr. / 20)
- version 2.1 produced
  - 15 cabled, 2nd metrology, 15 equiped with sensors (beg 2026)

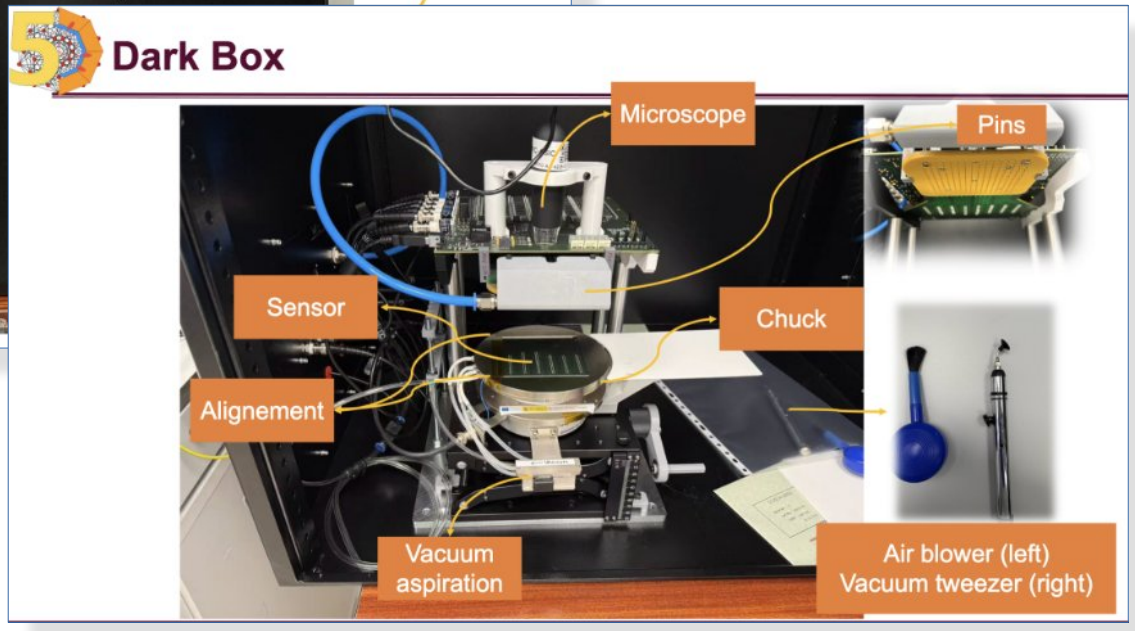
BT DESY 2025 → Possibility to run “low gain, full dynamics”

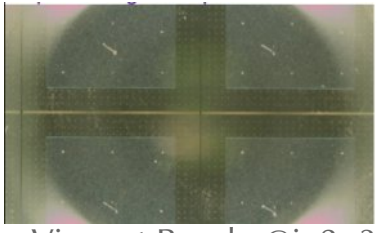


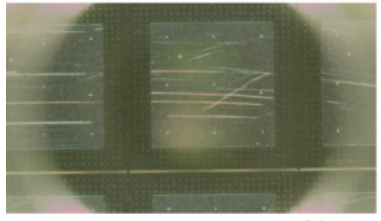


Wafer Testing at IFIC, Valencia



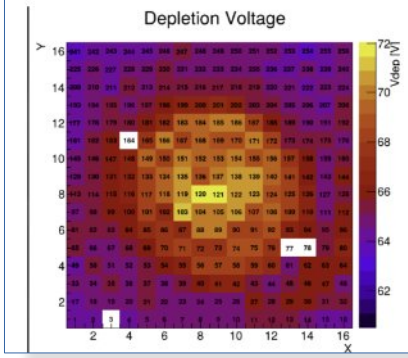


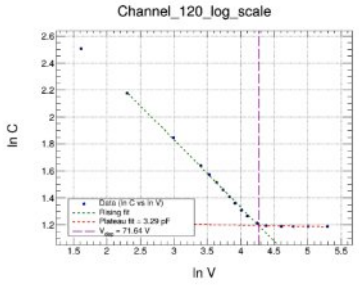




Wafer Testing at IFIC, Valencia

Sensor 43 (from old batch of Taikan)





Sensors

Status in Feb 2026

Sensors at IFIC. Green means tested at IFIC. Red means bad.

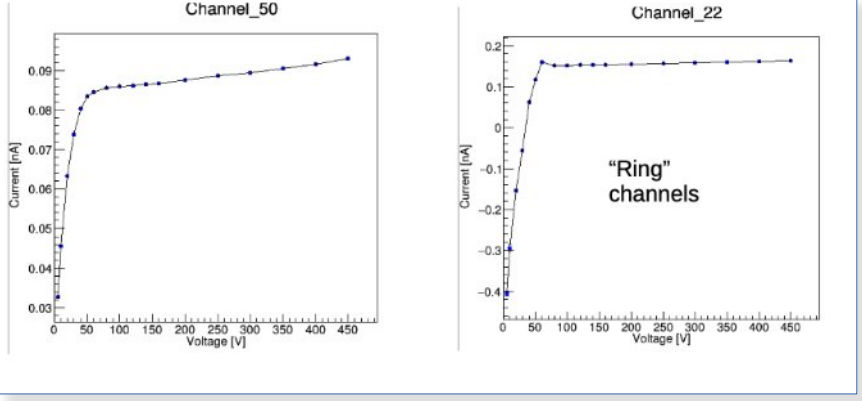
S12834_0850	54	no	500um, no GR	KEK/Utokyo	
S12834_0850	55	no	500um, no GR	KEK/Utokyo	
S12834_0850	56	no	500um, no GR	KEK/Utokyo	
S12834_0850	57	no	500um, no GR	KEK/Utokyo	
S12834_0850	58	no	500um, no GR	KEK/Utokyo	
S12834_0850	59	no	500um, no GR	KEK/Utokyo	
S12834_0850	60	no	500um, no GR	KEK/Utokyo	
S12834_0850	61	no	500um, no GR	KEK/Utokyo	
S12834_0850	62	no	500um, no GR	KEK/Utokyo	
S12834_0850	63	no	500um, no GR	KEK/Utokyo	
S12834_0850	64	no	500um, no GR	KEK/Utokyo	
S12834_0850	65	no	500um, no GR	KEK/Utokyo	
S12834_0850	66	no	500um, no GR	KEK/Utokyo	
S12834_0850	67	no	500um, no GR	KEK/Utokyo	
S12834_0850	68	no	500um, no GR	KEK/Utokyo	not tested
S12834_0850	69	no	500um, no GR	KEK/Utokyo	not tested
S12834_0850	70	no	500um, no GR	KEK/Utokyo	not tested
S12834_0850	71	no	500um, no GR	KEK/Utokyo	not tested
S12834_0850	77	no	500um, no GR	IFIC	
S12834_0850	78	no	500um, no GR	IFIC	
S12834_0850	79	no	500um, no GR	IFIC	
S12834_0850	80	no	500um, no GR	IFIC	
S12834_0850	81	no	500um, no GR	IFIC	
S12834_0850	82	no	500um, no GR	IFIC	
S12834_0850	83	no	500um, no GR	IFIC	
S12834_0850	92	IJCLab + YES- IFIC	500um, no GR	IJCLab	
S12834_0850	93	IJCLab	500um, no GR	IJCLab	
S12834_0850	94	IJCLab	500um, no GR	IJCLab	
S12834_0850	95	IJCLab YES- IFIC	500um, no GR	IJCLab	

19 from Taikan
4 from Roman
7 from Adrian
=30 at IFIC

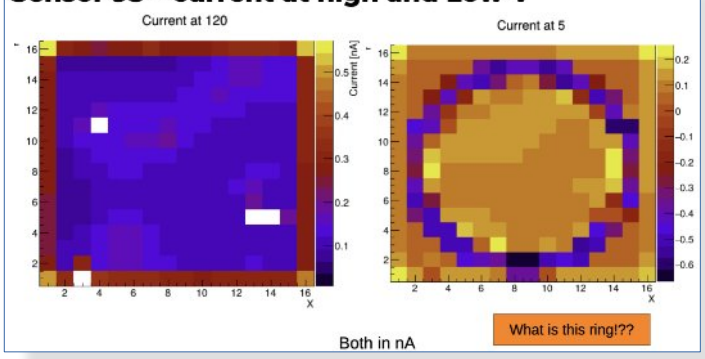
Plus 22 at LLR

52 in total
For 13 modules

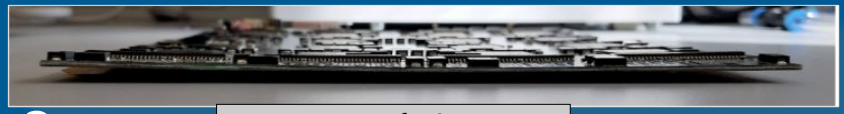
(plus 2 produced in 2025)



Sensor 95 – current at high and Low V



Hybridization studies (2024): How to assemble silicon sensors & PCB ?

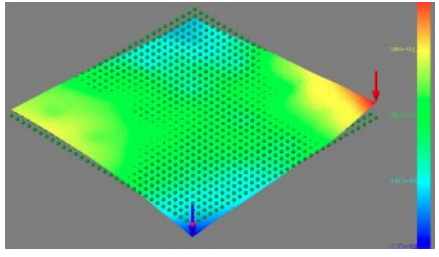


Worst case of a bent FEV

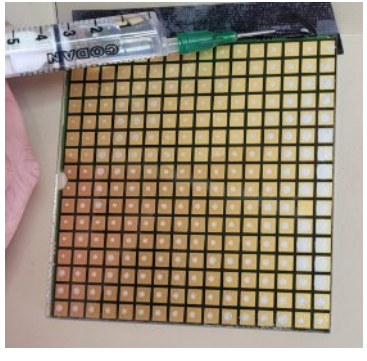
Revisiting gluing (IFIC, IJClab, DMLAB)

- PCB metrology
  - Before & After curing & soldering
- Glue formula & preparation
- Gluing methods
  - Robot
  - Stencil
- Reinforcement
  - Filling glue
  - **Adhesive films (chosen)**

IJClab (méca)

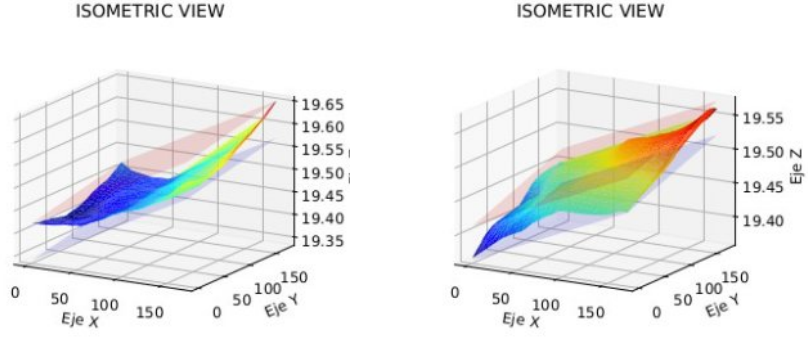


Conductive glue + filling (~invisible) on a glass plate





Flatness of PCB



Same PCB before / after 10-day dry storage



Measurements by C. Orero, IFIC



Puncturated adhesive film (**DMLab**) + conductive glue dots

Assembly chain (Mostly IFIC)



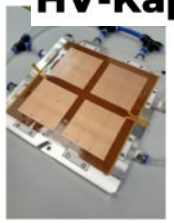
Metrology of PCBs

IFIC

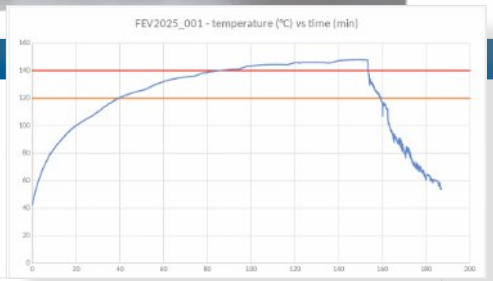
▷ **We could not do conclusive metrologies of the PCBs upon reception**

- Small differences between FEV2.0 and 2.1 and w/ w/o components which make the tools available not suitable… we aim for precision mechanics, we require detailed mechanics models and designs
- At arrival + after drying, requires at least 1 month of time for the full process. → so we decided to dry them before having the definitive tooling (which took some time to be produced)

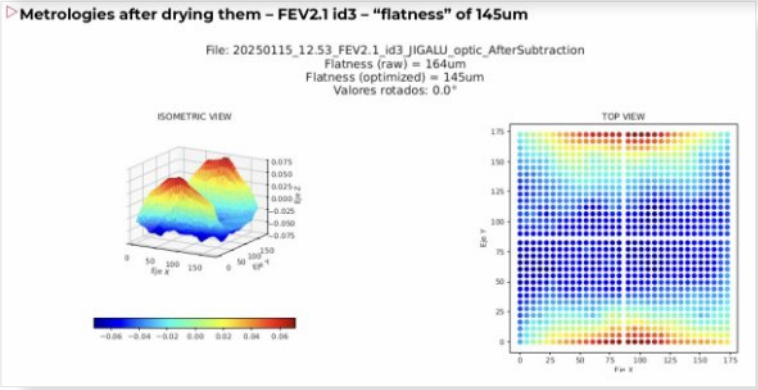
HV-Kapton



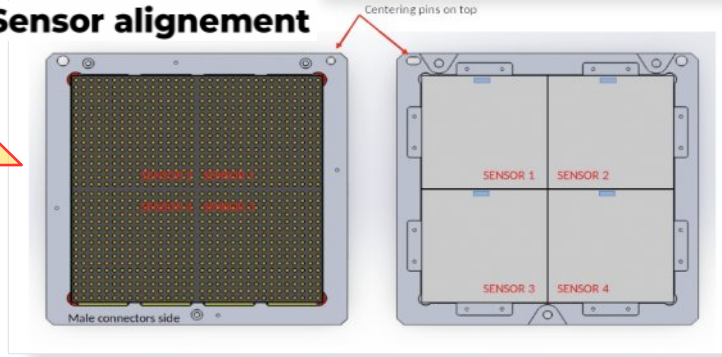




▷ **Metrologies after drying them – FEV2.1 id3 – "flatness" of 145um**



Sensor alignement



PROCEDURE - 3D robot and precifluid v0.odt

PROCEDURE - CALICE ASU gluing_alignment v0.odt

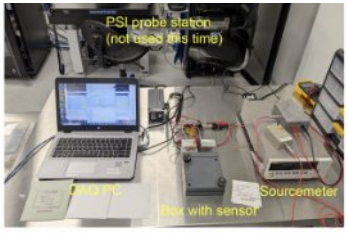
PROCEDURE - CALICE ASU gluing v0.odt

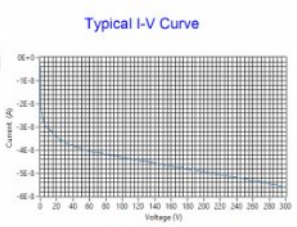
PROCEDURE - H20E preparation v2.odt

PROCEDURE - HV-K… to ASU v0.odt

Sensor and electronics cleaning

Sensor characterization

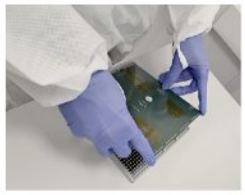


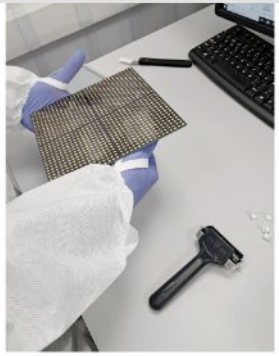


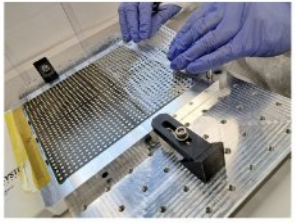
- Reasonable I-V curve though leakage current ~ factor two lower than in HPK data sheet
- Tests allow to validate that there is no major problem with sensors

J. Jeglot, A. Torento, R.P., (R. Cornat)







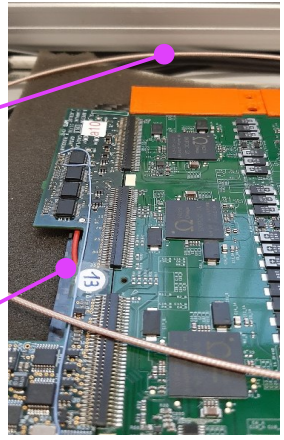


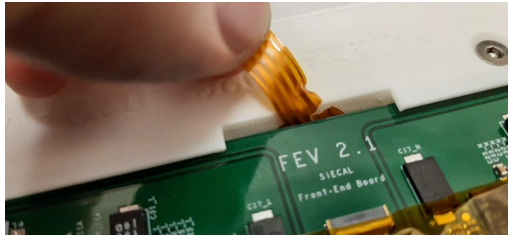
3M tape

Integration at IJCLab

Many “small” operations

- But with high risks
  (= not for physicists)
- Metrology of PCBs and
  3D printing of individual rails
  adapted to the curvature of PCBs
  and W thickness
- Adaptation of the SLBoards, DAQ
- Repairs, e.g. the HV
  (ripped Kapton in operation)

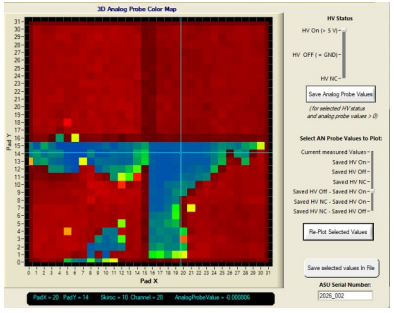




Check with 90Sr of the response

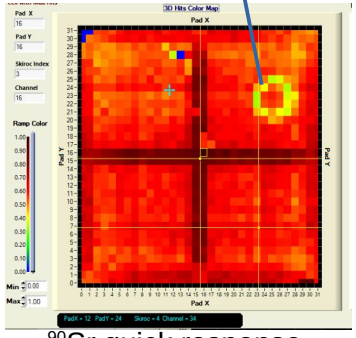
- Online histograms:

Delaminated board



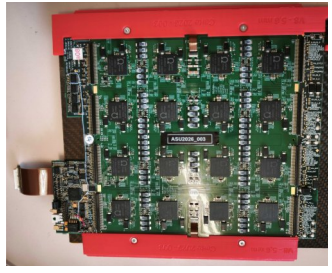
“HV-on – HV-off” map

Roman’s wedding ring



^{90}Sr quick response
(Hit map, 5 mins)

Integration

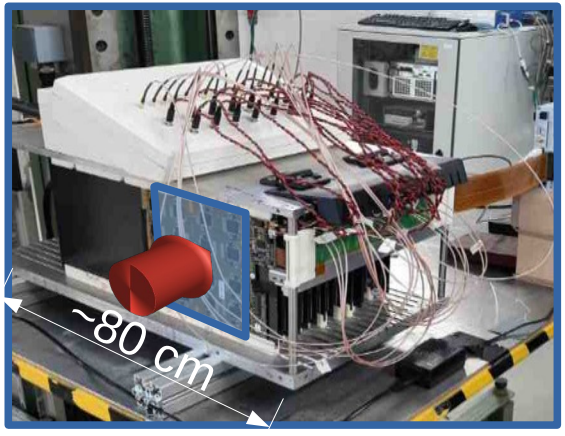




(Almost) Uniform Prototype

A Stack of 15 uniform sensor layers, separated by W absorbers (non-uniform)

- 15 Sensor layer made of :
  - 4 wafers [500 µm × (16×5.5mm)² Si PIN Diodes] ⇒ 18×18 cm²
  - 1 PCB (FEv2.1)
  - 16 ASICs (SKIROC2a)
- Tungsten absorbers:
  - 8 × **4.2 mm** [1.2 X_0] + 7 × **5.6 mm** [1.6 X_0]
    Total= 20.8 X0
- Missing channels: bad connexion, ASIC, noise: ~4%





10 days in June 2026 at the CERN SPS:

- **very smooth running**
  - Muon position scans (0 & 45°)
  - e+ Energy & angular scans (10–99 GeV; 0-45°)
  - Low-E π samples
  - Electronics modes ⊃ TDC

See update (T. Kamiyama): Performance Evaluation of the 15-Layer SiW-ECAL Technological Prototype with CERN SPS Beam Test Data

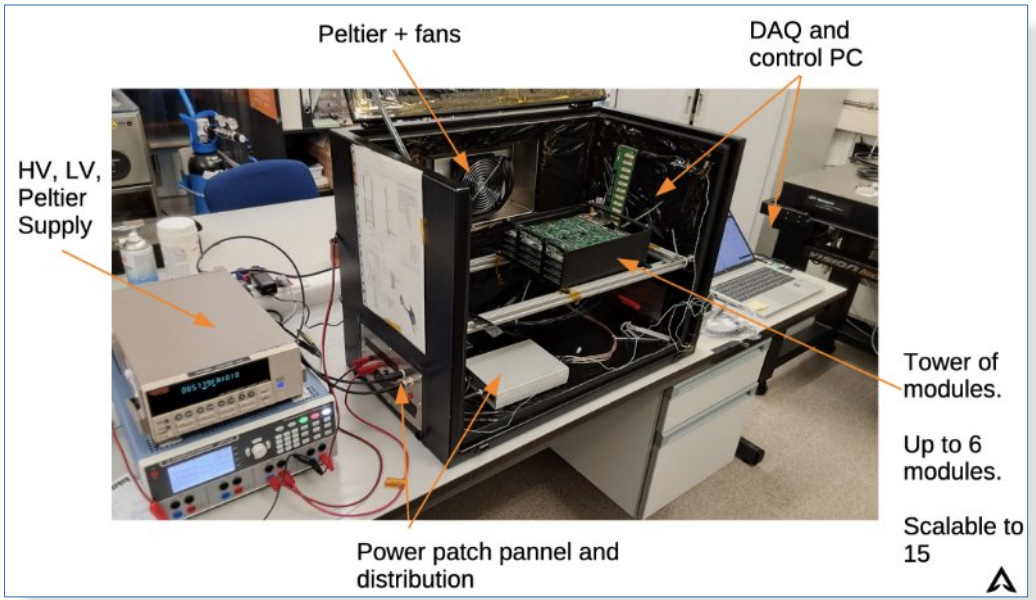
Prototype Exploitation

1) Test on environmental conditions at IFIC: temperature

- Just started
- Hints at a sizable effect
  - (June 2026 BT were not in a cool environment)

Study and reports made by (AI)²

(AI)² = (Adrián Irles x OpenAI)



2) Complement the energy scans (7.5–99 GeV e–) at low-E (1–5 GeV) → DESY in 2027 ?

Prototype Application: EBES

ICEPP The University of Tokyo KEK

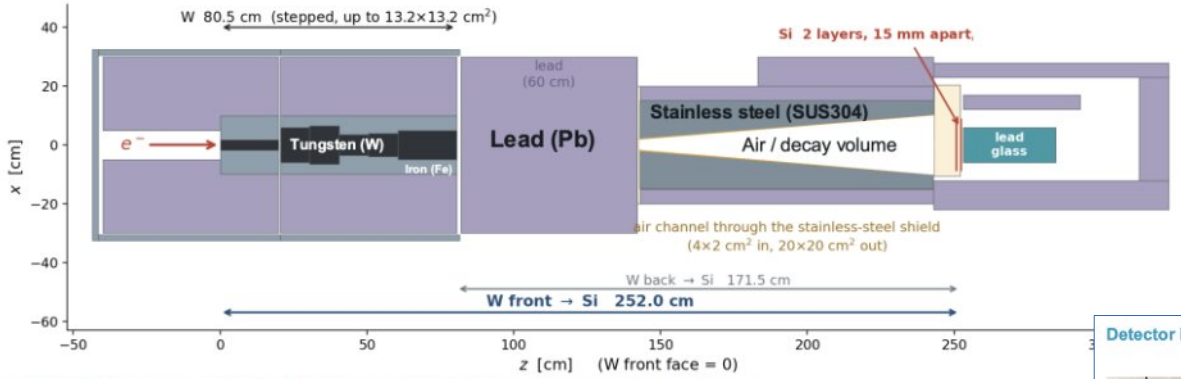
Search for Axion-like Particles in the EBES Experiment at KEK LINAC

Background Evaluation Using Silicon Pad Sensors and Simulation

ASU → estimate the muon background vs neutron

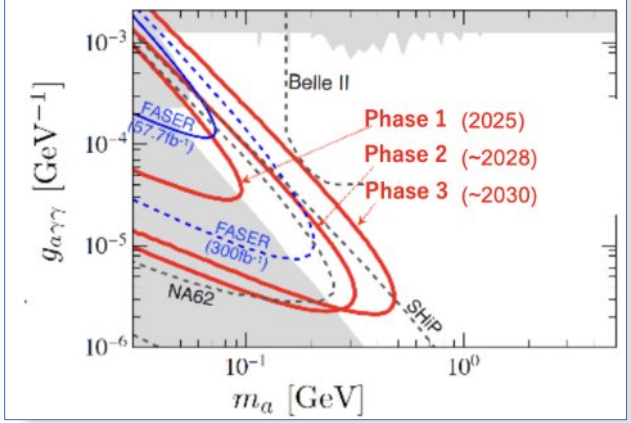
Phase 1 setup for the October 2025 run

- W target: ALP production via bremsstrahlung photons. Lead shield: suppression of secondary particles.
- Hollow stainless-steel shield reduces backgrounds such as neutrons. The ~1 m cavity is the ALP decay volume.
- Two Si layers: charged-particle positions and times. Lead glass: energies of photons from ALP decays.

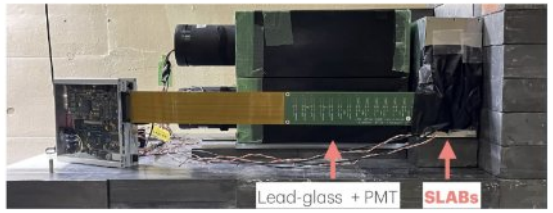


Phase 1 (2025): two silicon layers added for background studies

Projected ALP sensitivity



Detector installation at KEK LINAC SY3



Prototype Application: LUXE

Physics:

- QED in High Fields: $e+n\gamma_{vis}$ γ $_{HE}e$, $\gamma_{HE}+n\gamma_{vis} \rightarrow ee$
  - Schwinger's limit
- BSM: Axions Like Pseudo Scalar, …
- ≥ 202? at DESY/XFEL?

Beams:

- XFEL beam 10 Hz, $1.6 \cdot 10^9$ e–, $E_e \leq 17.5$ GeV
- Laser : 40–350 TW, 30 fs, 1 Hz → $1.5 \cdot 10^{20}$ W/cm³

ECAL's:

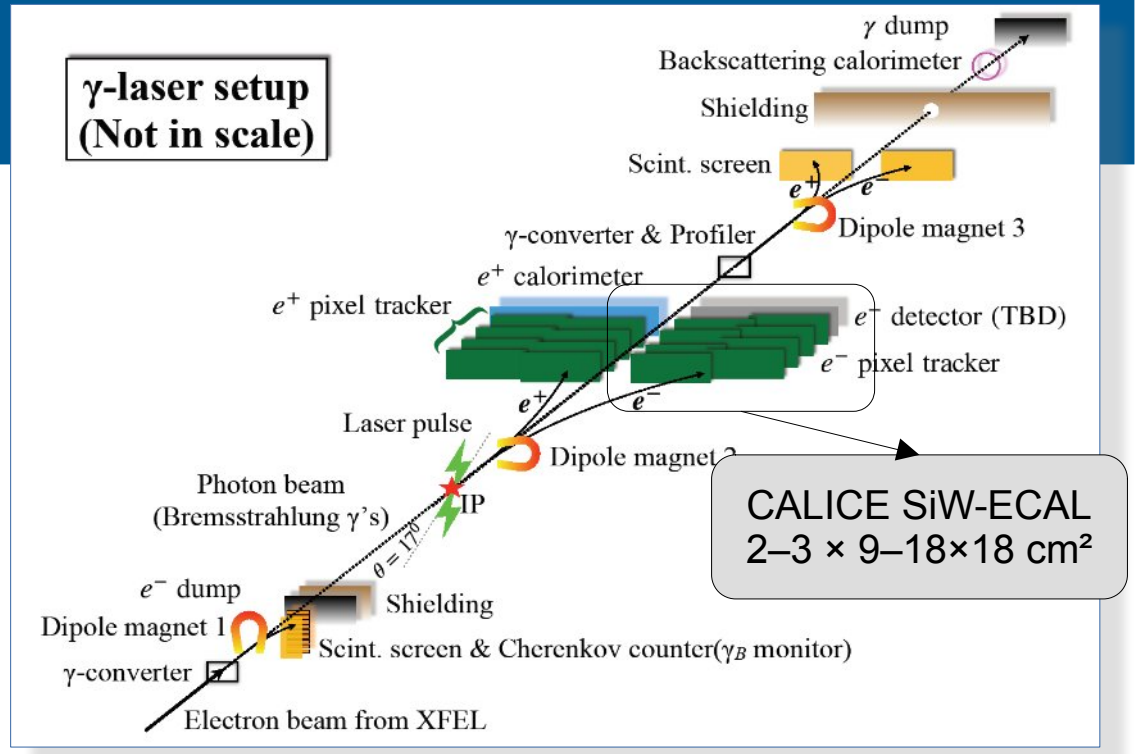
- 5×5 mm² cells, 20 X_0, 12⁺ layers, 20 %/√E
- Si+W → FCAL and/or CALICE

Q? Optimal sampling for $E_e \leq 17.5$ GeV ?

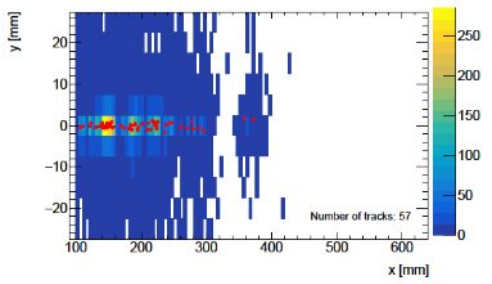
- ⊃ Hit counting, shower separations

Enough material for a full coverage ?

- PCB to be produced ; hard limit : ASIC < ~400
- Wafers : to be bought…



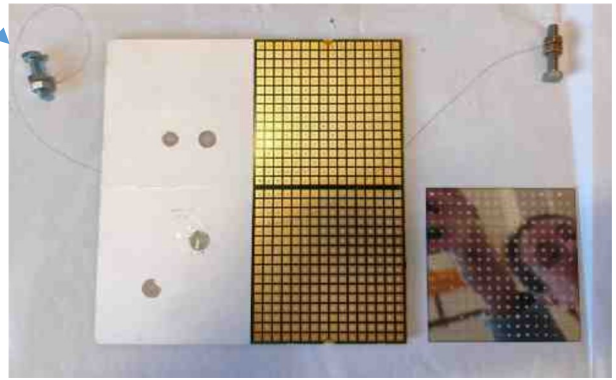
Overlap of showers
$E(x, z) \rightarrow$ small R_M

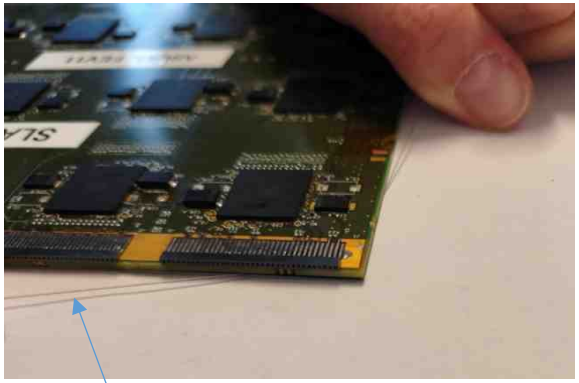


Sensor Recovery

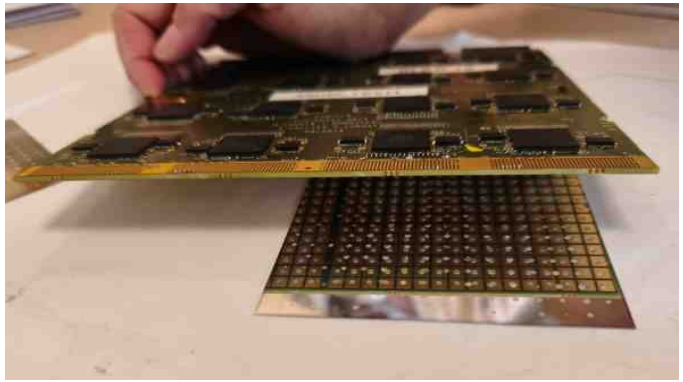
- Goal : To recover a many Sensors as possible
  - With a « magic » tool : Fishing line!
  - 44/48 Sensors recovered (price ~800€/pce)
    - Glue residue on sensor (white point)

Fishing line





Fishing line



+91% success rate !

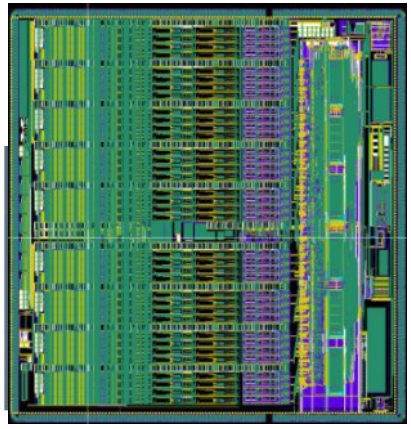


Leakage Current ✔

R&D for future experiments (FCC-ee & SHiP)

ASIC: CALOROC1C → GETROC

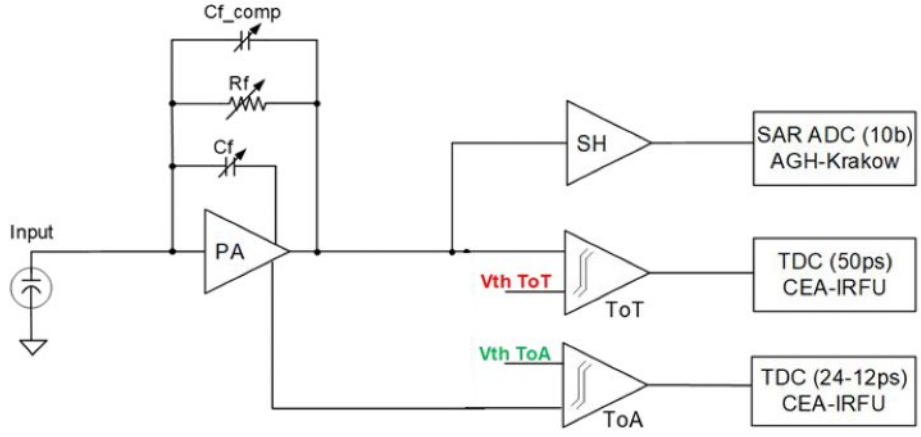
See **CALOROC/GETROC measurement results and plans**
... and the full electronics session



New ROC family from Omega based on TSMC 130nm technology:

- HGCROC
- HKROC
- CALOROC 1c
  - Dedicated to read Silicon signal
  - Radiation hardness
  - Analog: 36 channels
  - 10mW / chn
  - Streaming readout triggerless
  - 2 data link @1.28Gbps

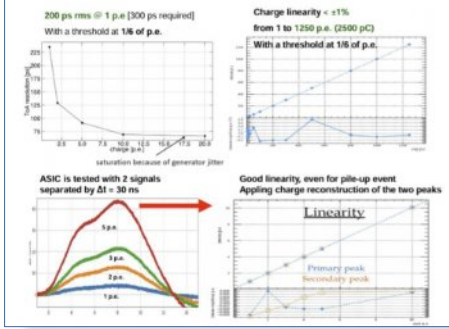
Silicon sensor (500µm-750µm):
1mip ~ 4-6pC
Our needs: dynamic 0,5 to 3000mip
→ 2pC to 18.000pC)



Preliminary studies for the integration of the CALOROC

HKROC test

Dedicated test bench
- XILINX KCU 105
- Test board with socket





Dedicated to read PM signal
Resolution 150ps for 1pe / 25 ps for 10pe
10mW / channel
Linearity < 1%
Charge measurement up to 1250 pe
Measurement with 2 events separated by 30 ns
→ **Interesting to study SNR and low energy measurement**

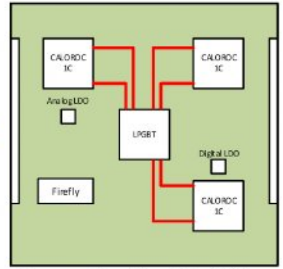
"Pin-to-Pin compatible"

→ Play and Learn

New front end boards for FCC

- Study new chips CALOROC
  - Adapt HKROC test board for Si sensors
- Study clock distribution system
- Study LPGBT to aggregate data
- Propose design with 3 CALOROC (108 chn)
  - I2c (slow control)
  - Clock distribution
  - LPGBT or similar
  - Power distribution
  - Measure power, noise, temperature, performances
  - Solution to chain boards
- Propose design for 512 channels
  - Equivalent to 5x miniFEB
  - Power estimation: 37mW/chn





Power estimation: 46mW/chn

Towards a Compact cooling system for the FCC-ee

"Boosted Standard Slab"

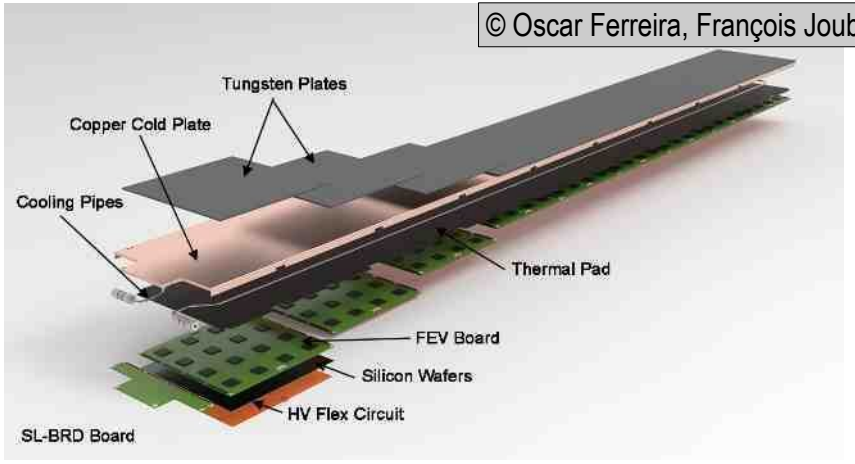
- → 210W (30W/ASU) : ASICs + Concentrators + PS…
  - (ILC like in CC ~ 130W)

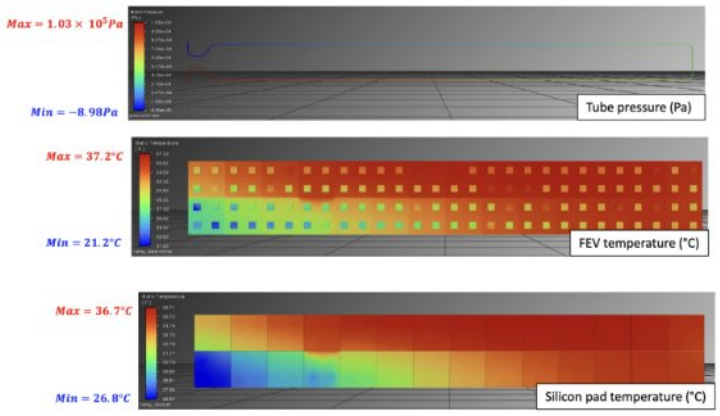
Active cooling:

- 4 mm Cu plate with 1/8'' Stainless Steel Tubing
- 0.2 ℓ/min of water @ 15°C

Simulations

Adiabatic, but for heat bridge at the end, $t = \infty$





Inlet flow rate : 0.25L/min

Results :

- Pressure drop : 1.03 bar
- **Silicon temperature gradient : 9.87°C**

- Preliminary results resumed in the following graphs.
- Operating point between **0.25 L/min** and **0.45 L/min** for allowable pressure drops.

Cold Plate Test bench

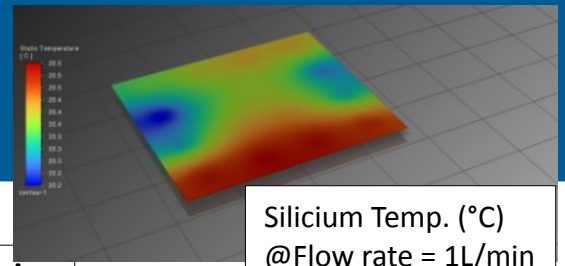
Prototype : 1 Fake FEV

- Cold plate in Copper with grooves for stainless steel pipe (1/8'')
- Curbing of pipes
- Soldering with tin (à la HGCAL…)
- Existing PCB with ASIC or Silicon → 3D fake ASIC + heating pads
- An Adiabatic box

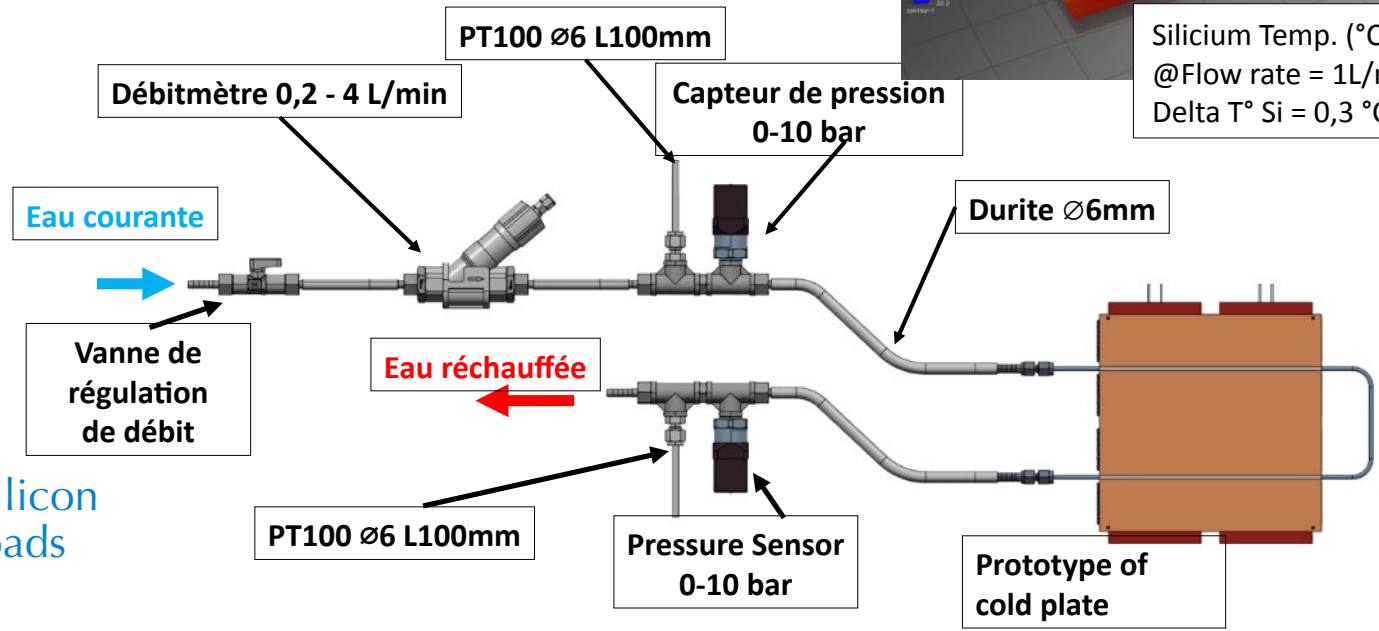
Instrumentation

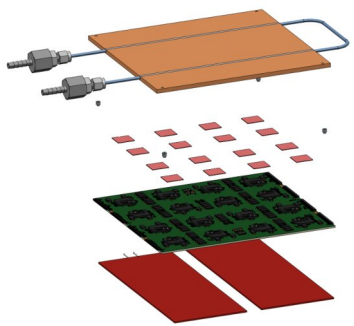
- Thermal, pressure, flow sensors + DAQ

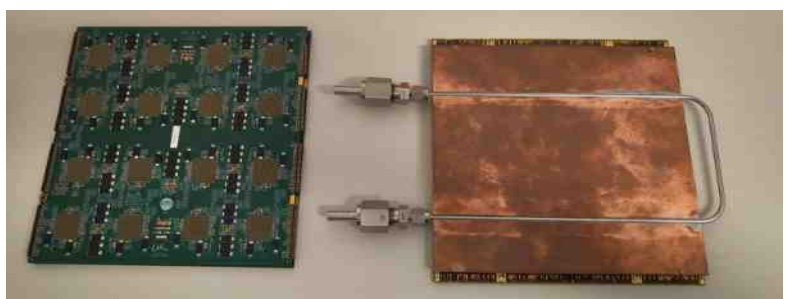
Being mounted… results by end 2028



Silicium Temp. (°C)
@Flow rate = 1L/min
Delta T° Si = 0,3 °C







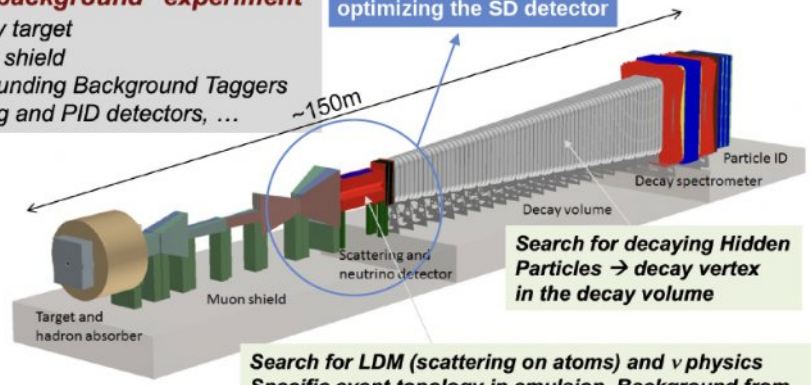
SHiP conception

The SHiP experiment

▸Search for **Hi**dden **P**articles (LDM, axions, etc.) & neutrino physics!

"Zero background" experiment
- *Heavy target*
- *Muon shield*
- *Surrounding Background Taggers*
- *Timing and PID detectors, …*

Our work goes here, optimizing the SD detector

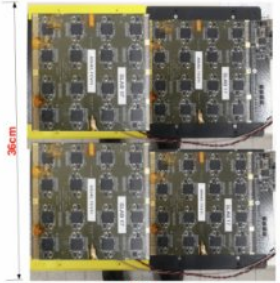


Search for decaying Hidden Particles → decay vertex in the decay volume

Search for LDM (scattering on atoms) and ν physics Specific event topology in emulsion. Background from neutrino interaction for LDM searches can be reduced to a manageable level

Andrei Golutvin
SHiP Spokesperson

A Silicon Pad (SiPad) Layer for SHiP



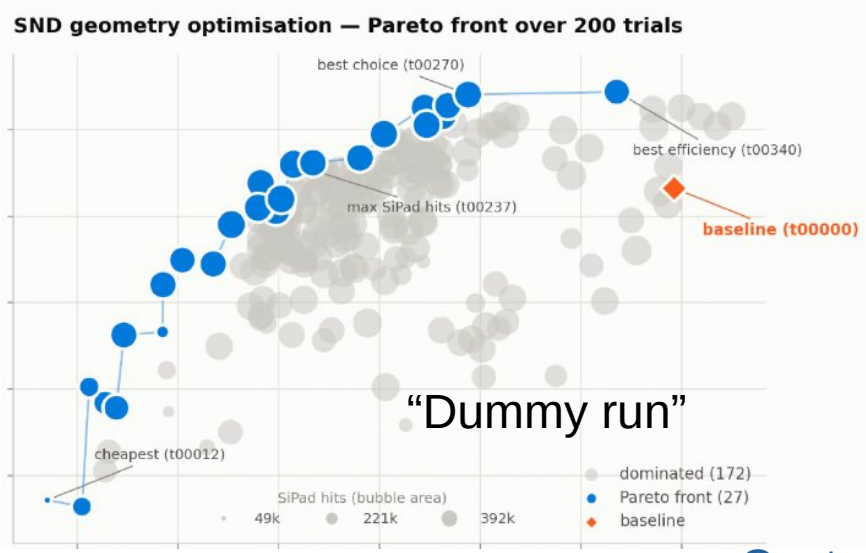
- Should be straightforward to arrange SiW ECAL ASUs
  - Modularity inherent to detector design
  - N.B.: 18x18 cm² is not a canonical number but many tools are or will be developed for this size
- 2 Chains of 2 ASUs/layer
- Engineering support at IJCLab!
  - Mechanics and Electronics Department

key4ship status

J. P. Márquez

▸The full stack is almost ready to go for optimization

Efficiency



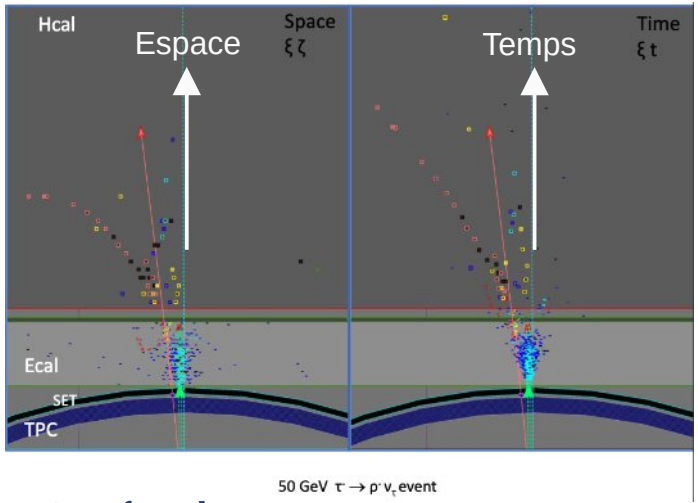
"Dummy run"

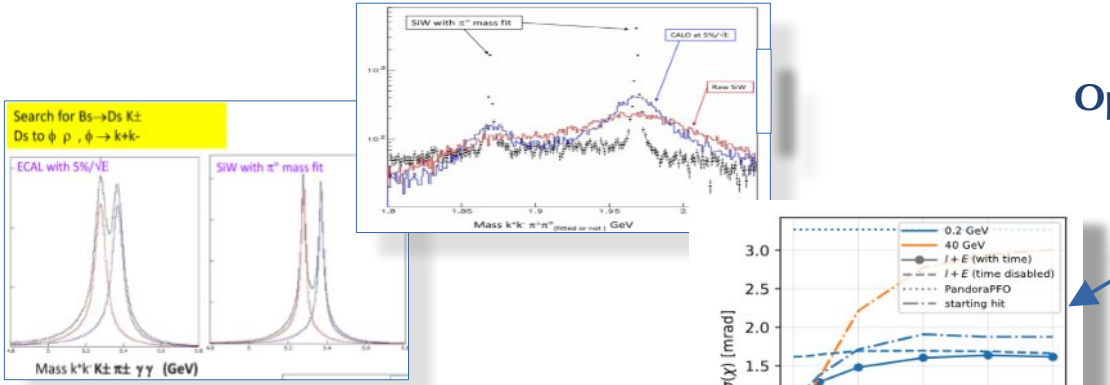
Cost

Re-optimisation of the SiW-ECAL for the FCC-ee

Exploration of the use of "centimetric timing" in the calorimeters (1cm~30ps)

- Easier Reconstruction & Showers in Particle Flow
- Better precision of photons in exclusive final states:
  - B^0's and τ's with π^{0}'s
    - High Granularity + Timing >> pure resolution in E
      (Eur.Phys.J.Plus 141 (2026) 6, 697, ArXiV 2605.23667)

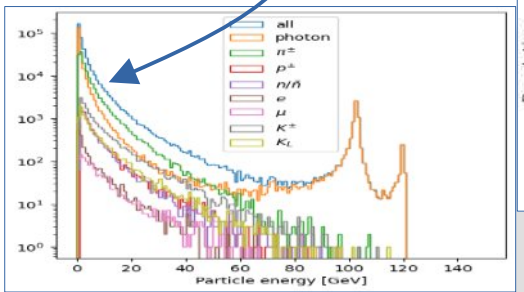




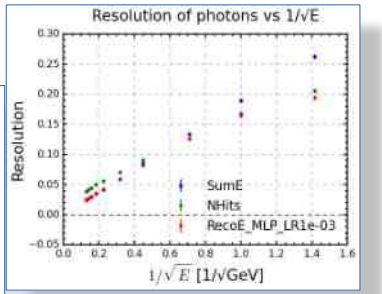
H. Liang

Optimisation of SiW-ECAL for photons

- $\sigma(E)/E$ at low E (for jets) : –20% using hit counting
- Precision in γ position vs $\sigma(t)$

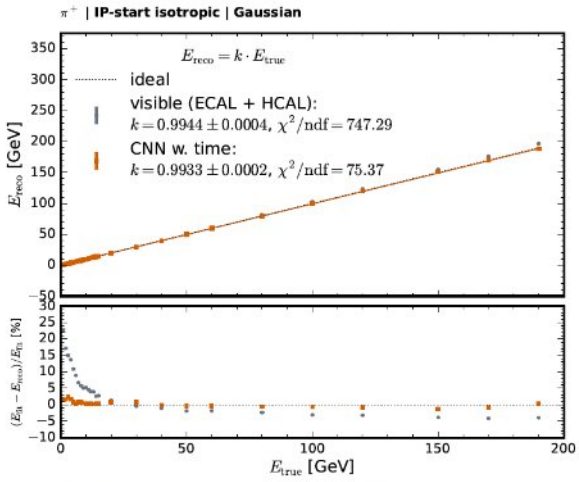


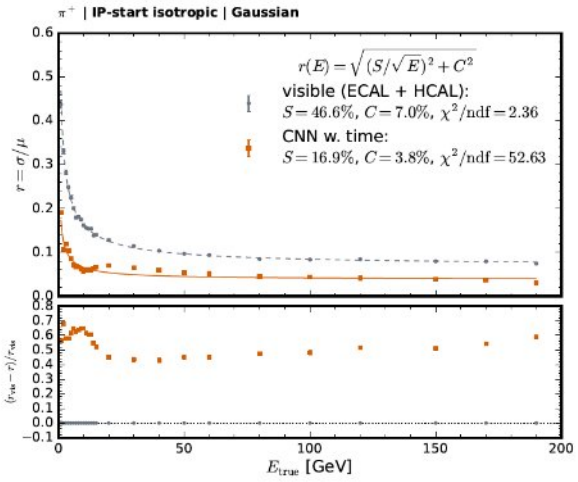
arXiv:2604.27853



Optimising the Calorimeter system : ECAL + HCAL

Isotropic sample: energy dependence





13 sampled energy points. Promising for both linearity and resolution. The stochastic-plus-constant fit does not describe the full energy dependence.

Next: At fixed direction, change the incident angle; check containment, tails and the energy fraction inside the input windows.

Preliminary isotropic study.



Xin Xia | ILD calorimeter reconstruction update

See **Update on CNN-Based Hadron Energy Regression at ILD**

Conclusion

Critical Milestone reached for the technological prototype with legacy electronics

- First Successful Beam Tests of a full working calorimetric stack
  - Analysis at full steam by a stack of highly motivated young physicists
  - Complementary studies:
    - Temperature dependence
    - Low-E at DESY ?

  → "Construction paper"
- Modernized Analysis SW with full chain in Key4HEP
- Applications: EBES@KEK started

Preparation of the follow-up

- New electronics : CALOROC1C & GETROC
  - Soon to be tested for integration
  - Updated characteristics?
- Active Cooling test bench being mounted
- Optimisation of designs:
  - Layout for low-E photons
  - Timing requirements
  - Calorimeters system
  - Optimisation chain being tested for SHiP requirements

Thank you for your attention