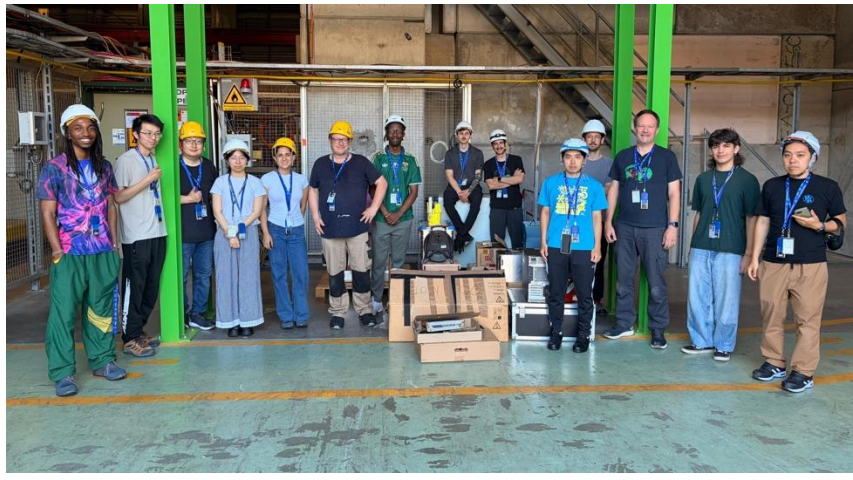


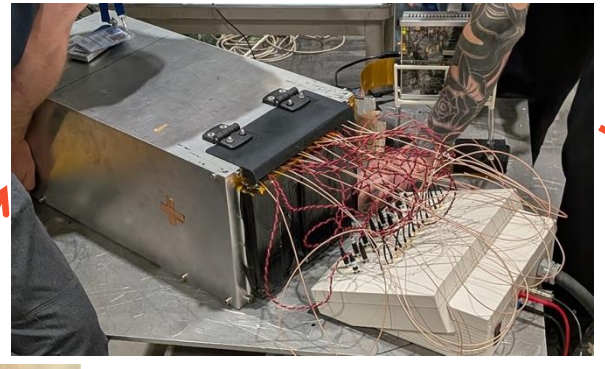
Performance Evaluation of the 15-Layer SiW-ECAL Technological Prototype with CERN SPS Beam Test Data

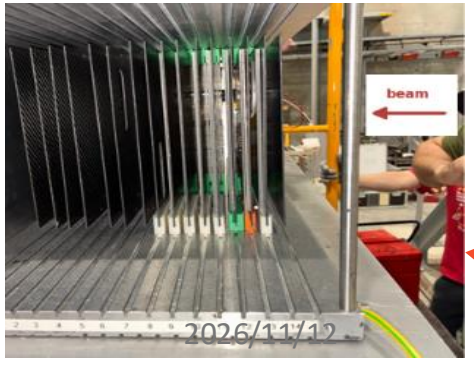
T. Kamiyama, V. Boudry, J. M. Hernandez, J. Nanni, D. Zerwas, J. Maalmi, D. Breton, A. Thiebault, J. Jeglot, A. Gonnin, H. Liang, Y. Shi, V. Pérez, T. J. Pule, O. A. Peinazo, T. Suehara, B. Gautier, M. Ruan, R. Poeschl, X. Xia, A. Irles, E. K. Nkadimeng, M. Almanza-Soto, C. Blanch, S. Huang, C. Orero

SiW-ECAL test beam at CERN in June 2026



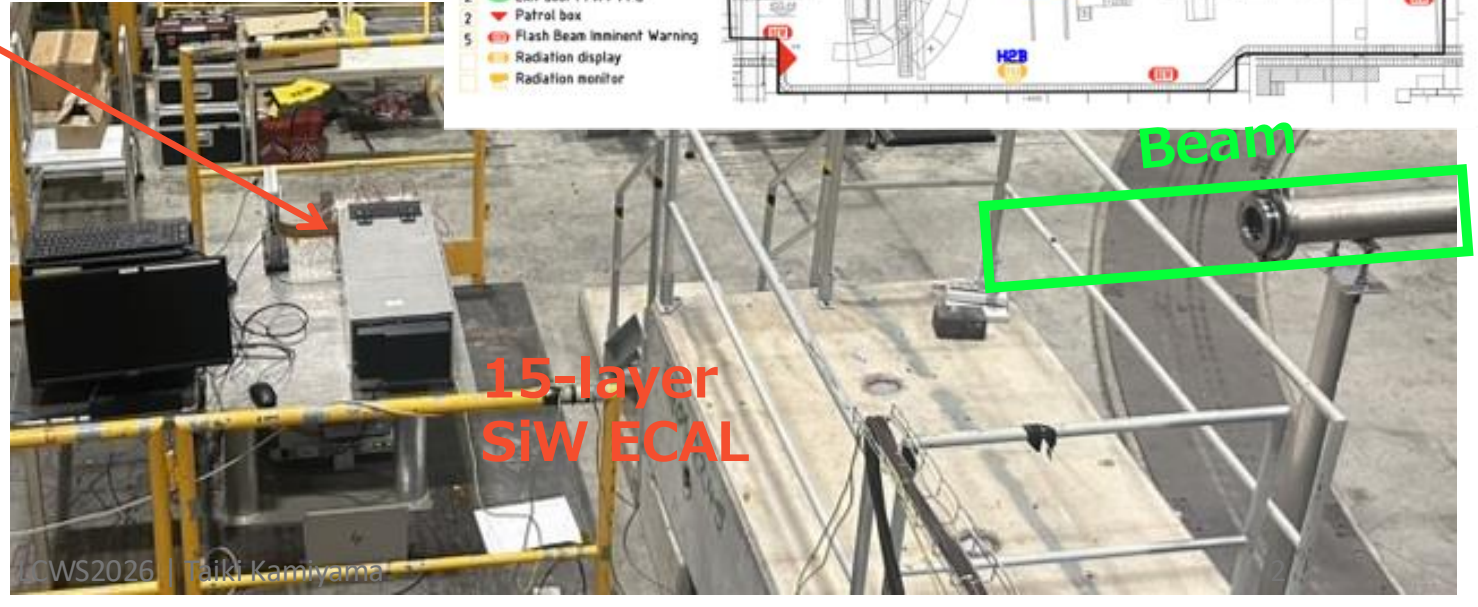
- Test beam at the CERN SPS H2 beam line, June 17th to 25th.
- One of the **most successful** SiW-ECAL TB ever.

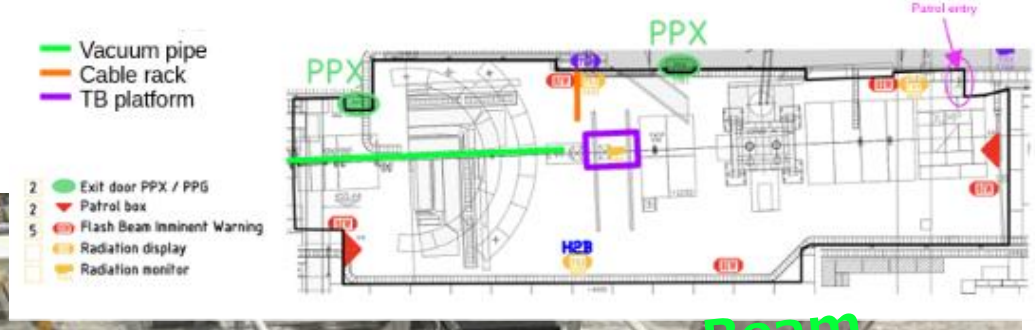




Active layer

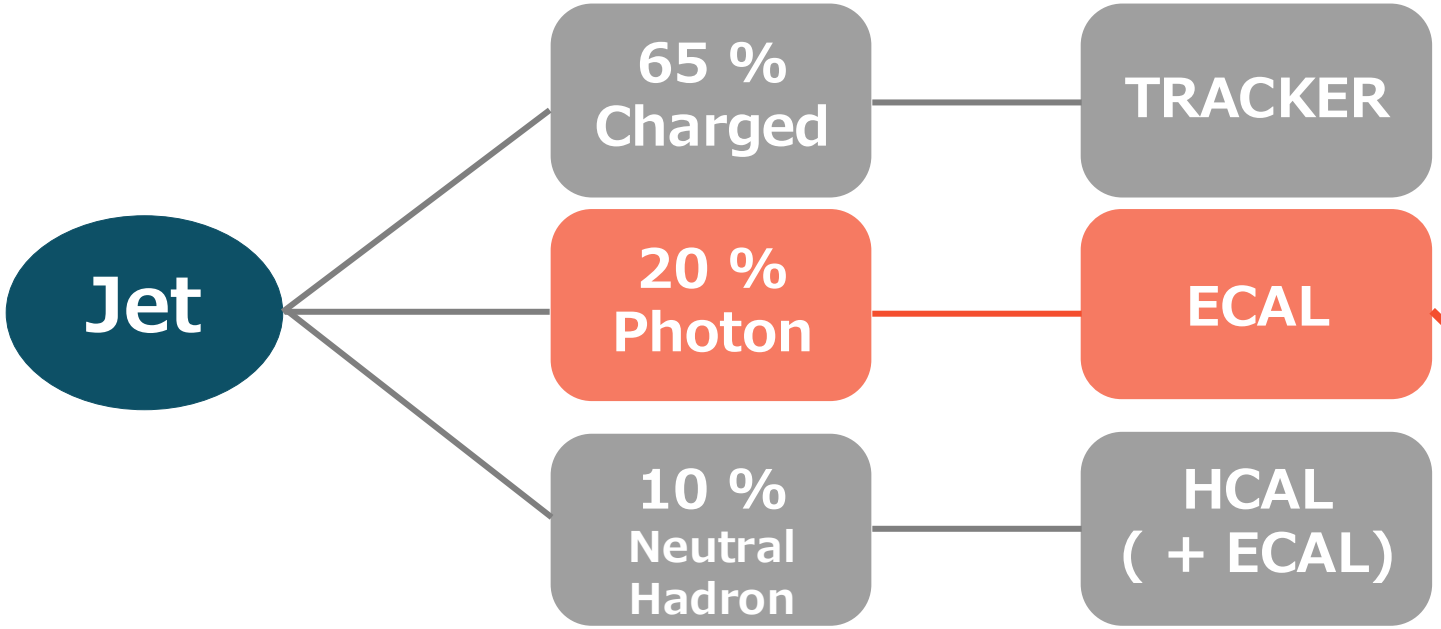




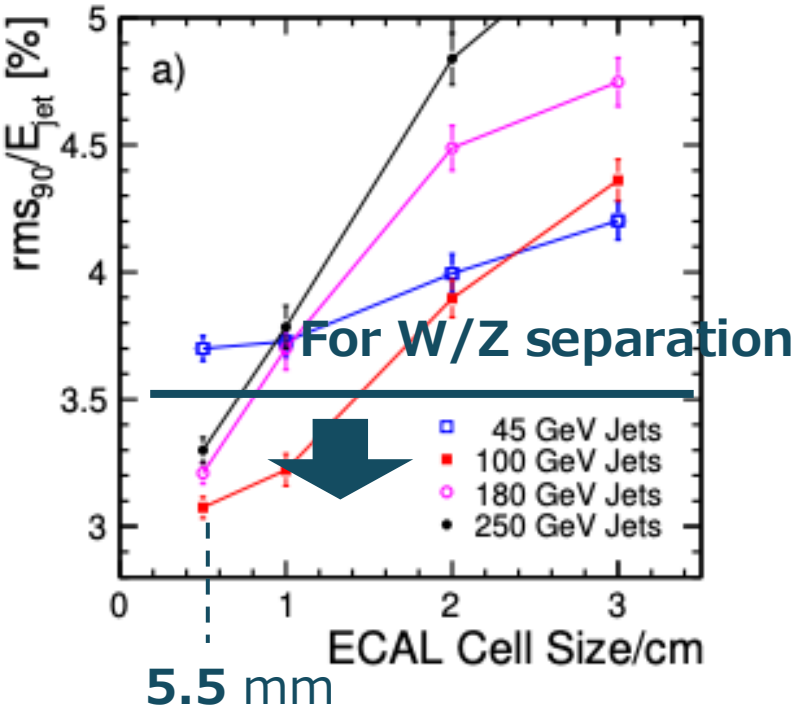


ECAL in Particle flow calorimeter system

Particle flow reconstruction



https://arxiv.org/pdf/0907.3577



Calorimeter requirement

High granularity to separate nearby showers

THIS STUDY

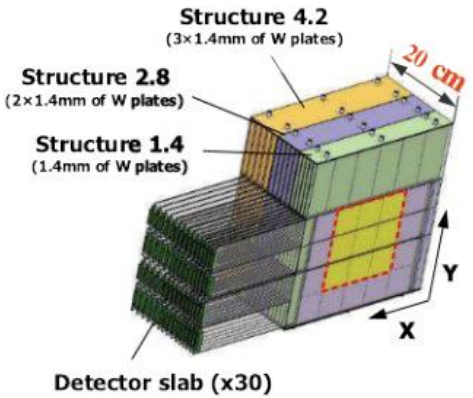
Highly granular SiW-ECAL

W absorber
→ **Compact showers**

Si pads
→ Fine shower imaging with
$\mathbf{5.5}\ \boldsymbol{mm}$ cell

SiW-ECAL development roadmap

Physics prototype
2005-2011
Proof of principle



- **External RO**.
- $1\times1\ \mathrm{cm}^2$ cells.
- 30 layers, 10 k channels.

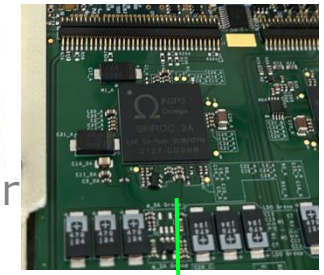
https://arxiv.org/pdf/0811.2354

We are HERE

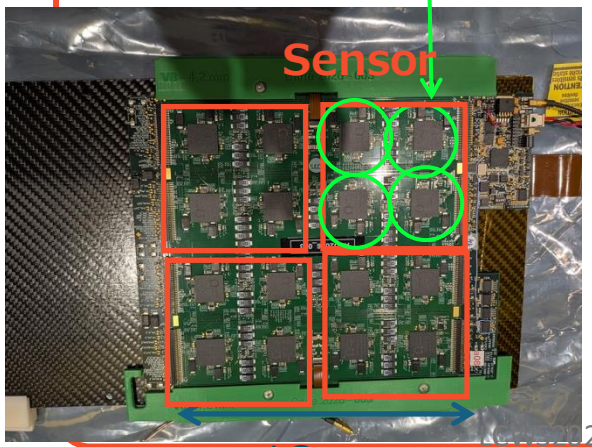
Technological prototype
Current stage
Integrated detector technology


Si sensor

SKIROC chip



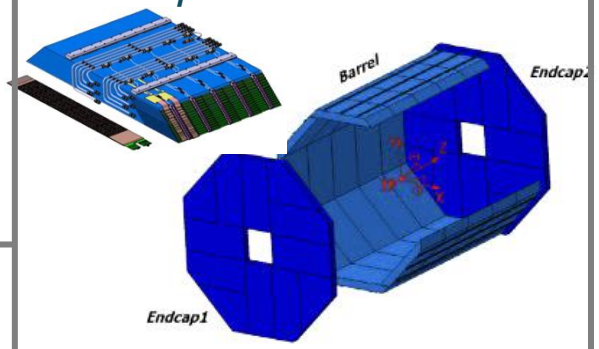
ASU



18 cm

- **Embedded electronics**:
  - **4** sensor per FEV PCB.
  - **4 SKIROC2a ASICs** per each sensor.
- **Self-triggered**.
- **64**-channel per ASIC → 1024 ch per FEV
- 15 memories per ch (SCA).
- $\mathbf{5.5\ mm^2}$ cells.
- Sensor thickness: 500 or $650\ \mu\mathrm{m}$.

Pilot → full detector
Next stage
Scale-up and production

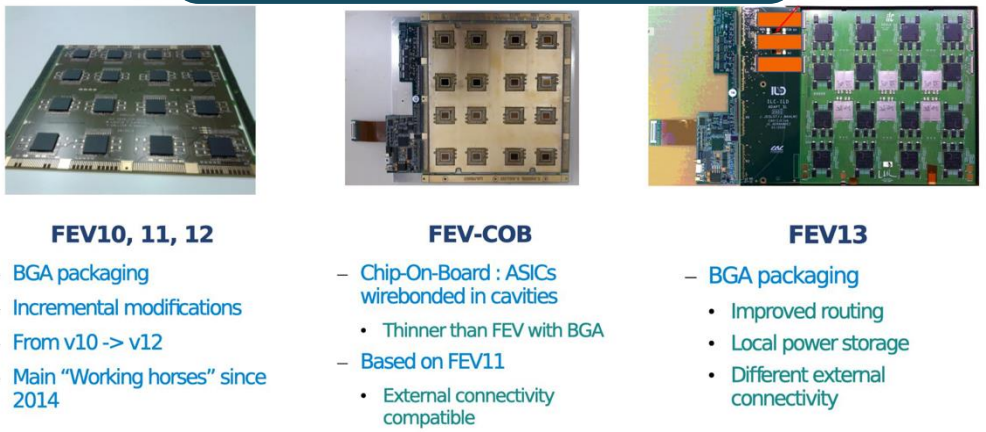


- Approximately 1M → 70M channels
- Cooling, power and DAQ integration
- **30 layers, $\sim 24\ X_0$.**

Reliable FEV2.1 production

https://arxiv.org/pdf/2211.07457

TB2021 & 2022
@ DESY & CERN



FEV10, 11, 12
- BGA packaging
- Incremental modifications
- From v10 -> v12
- Main "Working horses" since 2014

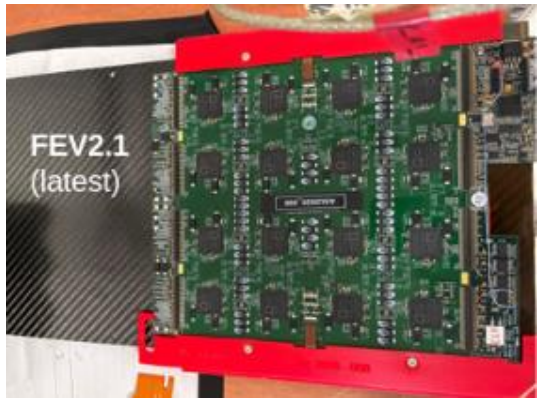
FEV-COB
- Chip-On-Board : ASICs wirebonded in cavities
  - Thinner than FEV with BGA
- Based on FEV11
  - External connectivity compatible

FEV13
- BGA packaging
  - Improved routing
  - Local power storage
  - Different external connectivity

- Multi-layer stack with three types of FEV designs.
- Inactive cells, wafer/PCB delamination, noise etc.

▶ FEV redesign

TB2025
@ DESY

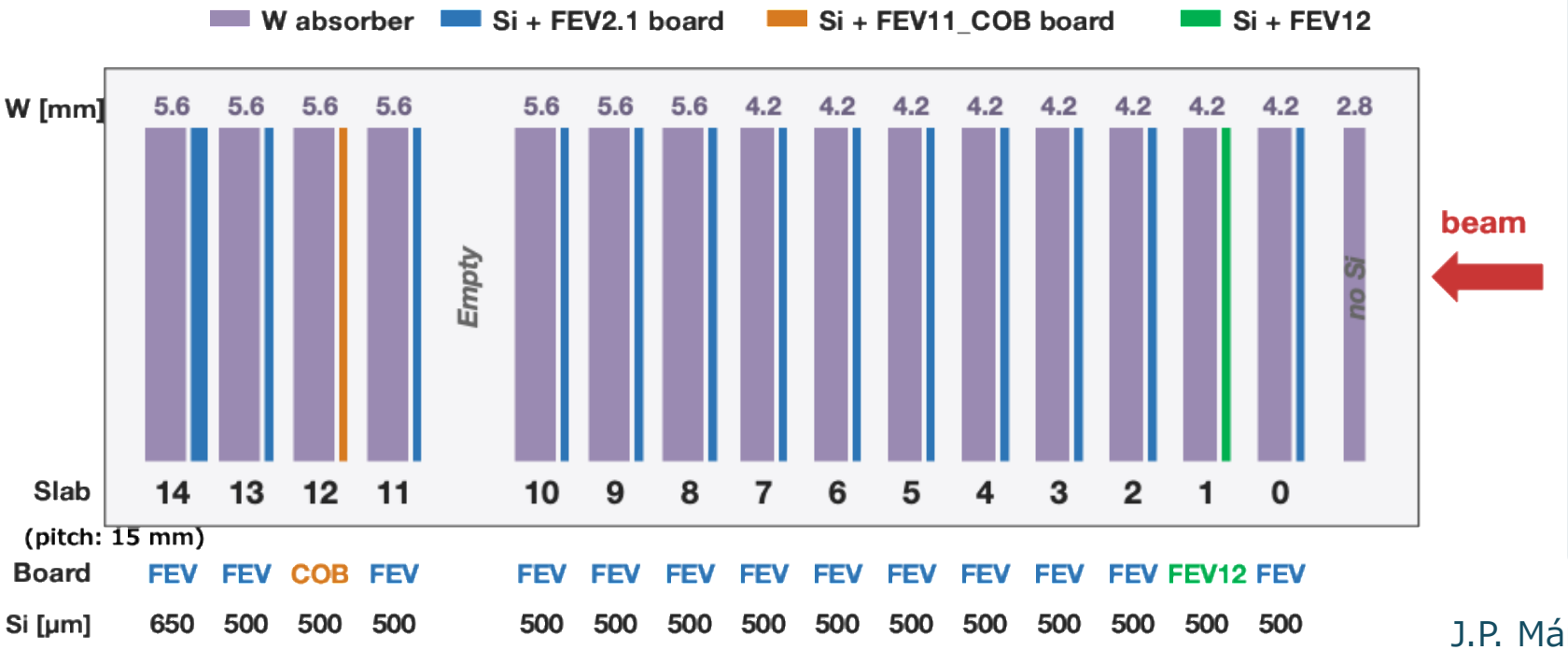


- Tested two new FEV 2.1 boards.
- Both boards operated successfully.

https://indico.in2p3.fr/event/36116/contributions/163076/attachments/97129/149385/SiWECAL_Beamtest.pdf

▶ Production of additional 13 boards

2026 test beam configuration & goals



Nearly uniform

15 layers with FEV2.1

$\approx 20\ X_0$

96.5 % Active cells

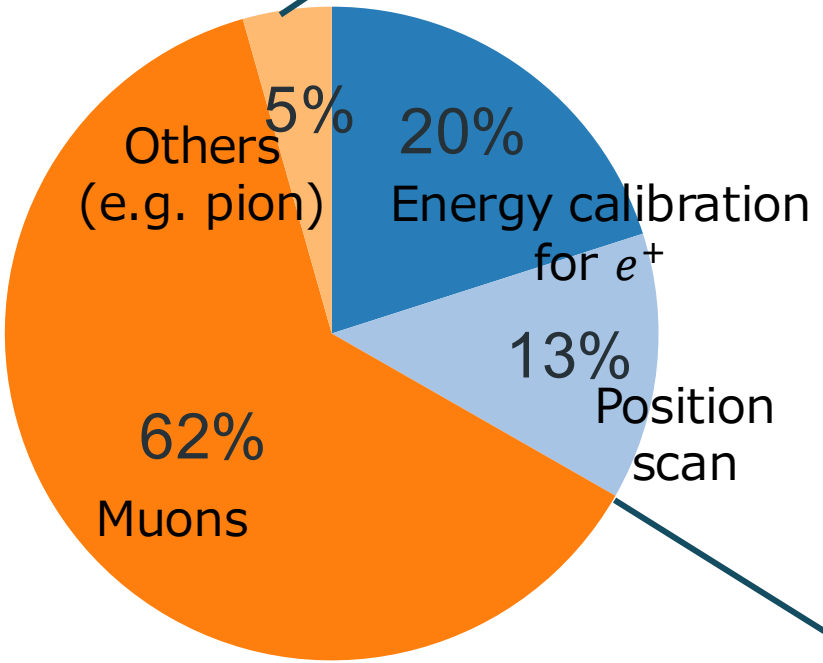
J.P. Márquez

Goal Electromagnetic performance over the full range energy, low-energy pion response and reference data for GEANT4.

Data collected

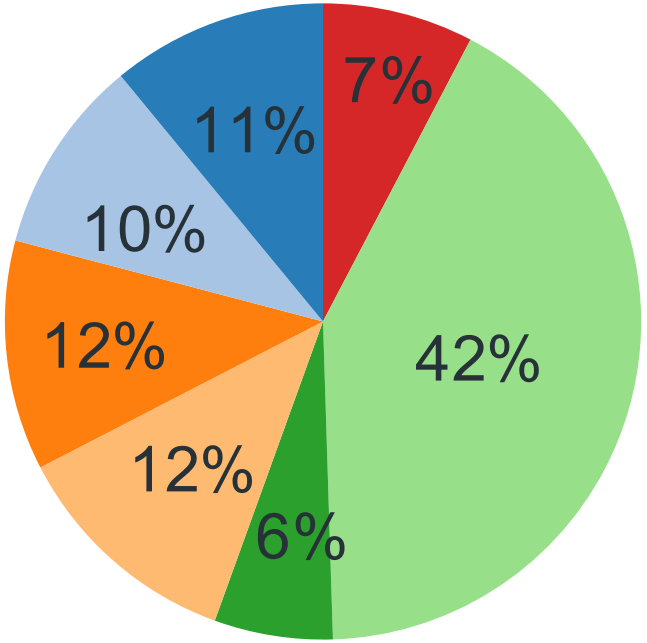
Campaign overview

27.8 M
events recorded



J.P. Márquez & V. Pérez

e^+ run



10.4 M events

- 7.5 GeV
- 10 GeV
- 20 GeV
- 34 GeV
- 52 GeV
- 74 GeV
- 99 GeV

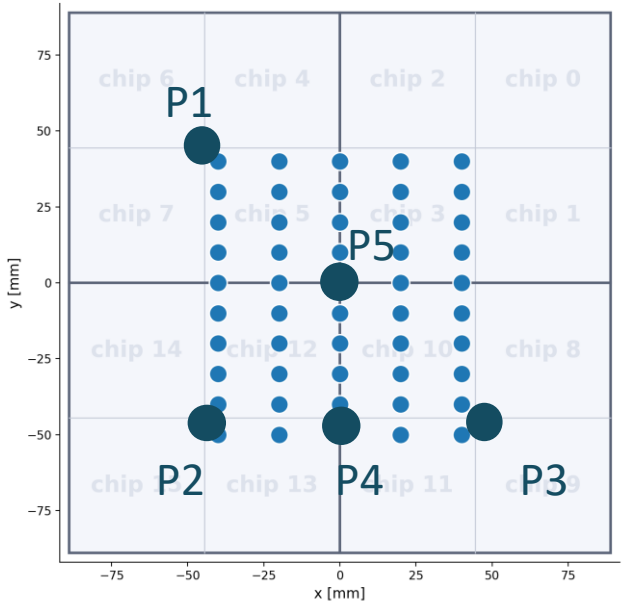
Scan positions:

- Energy scans
- Position scans

Angle scans:

$5\,°, 10\,°, 30\,° \,\&\, 45\,°$

Layer cross-section (x–y)



Software & ongoing analysis

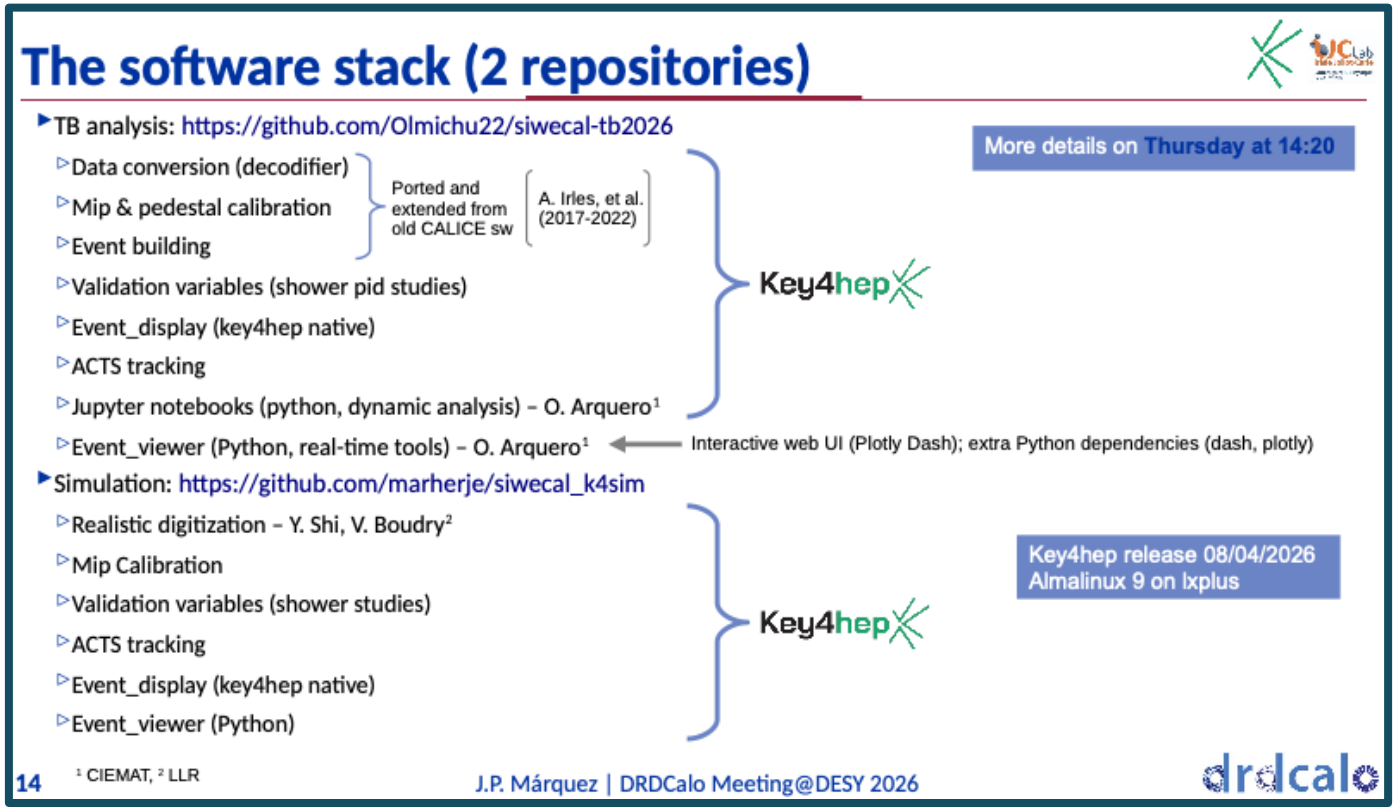
Software foundation

J.P. Márquez[A]

- Established the framework and initiated the analysis effort.

Ongoing analysis

- O. Arquero[B]:
  - ML-based event selection
- **T. Kamiyama[C]** & T. J. Pule[D]:
  - Linearity & resolution studies
- V. Pérez[E]:
  - Uniformity scan analysis & documentation
- B. Gautier[E]:
  - Angle and position reconstruction



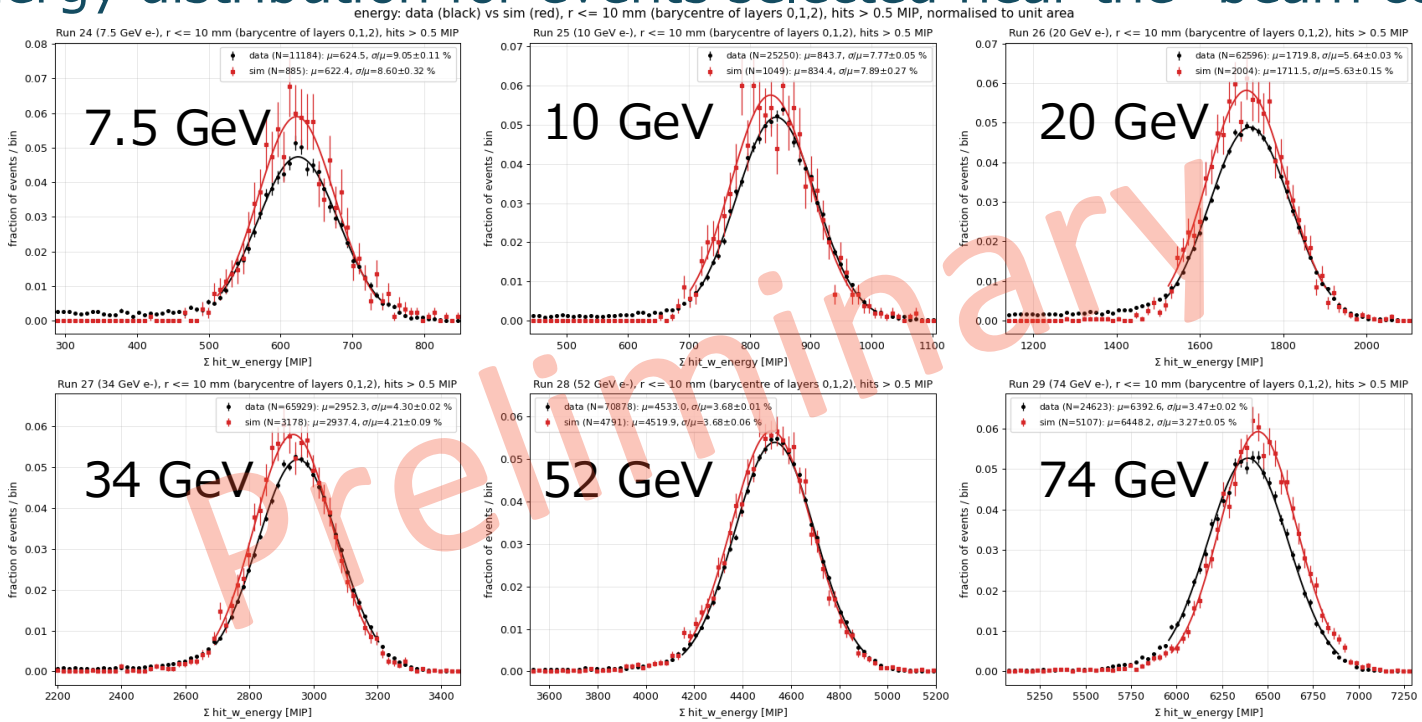
Note: This is not a complete list of contributors.

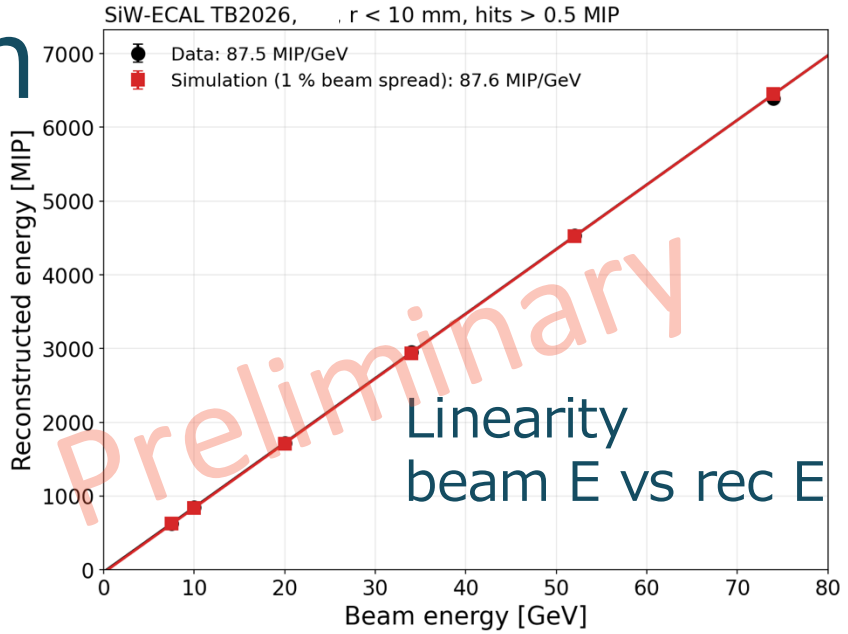
[A]IJCLab, [B]CIEMAT, [C]UTokyo, [D]U. Witwatersrand, [E]LLR

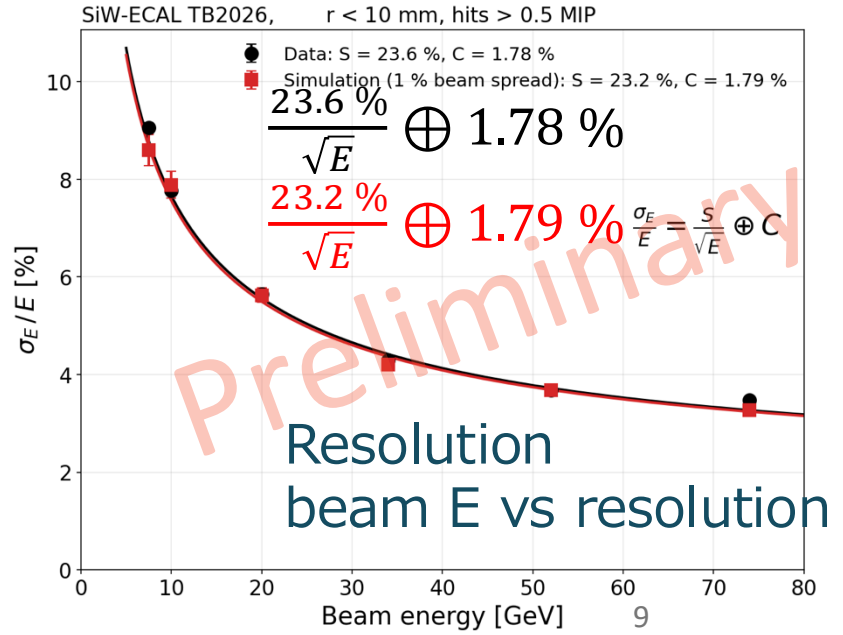
EM response: data-simulation comparison at pos. 2

Black: data, Red: simulation

Energy distribution for events selected near the “beam center”





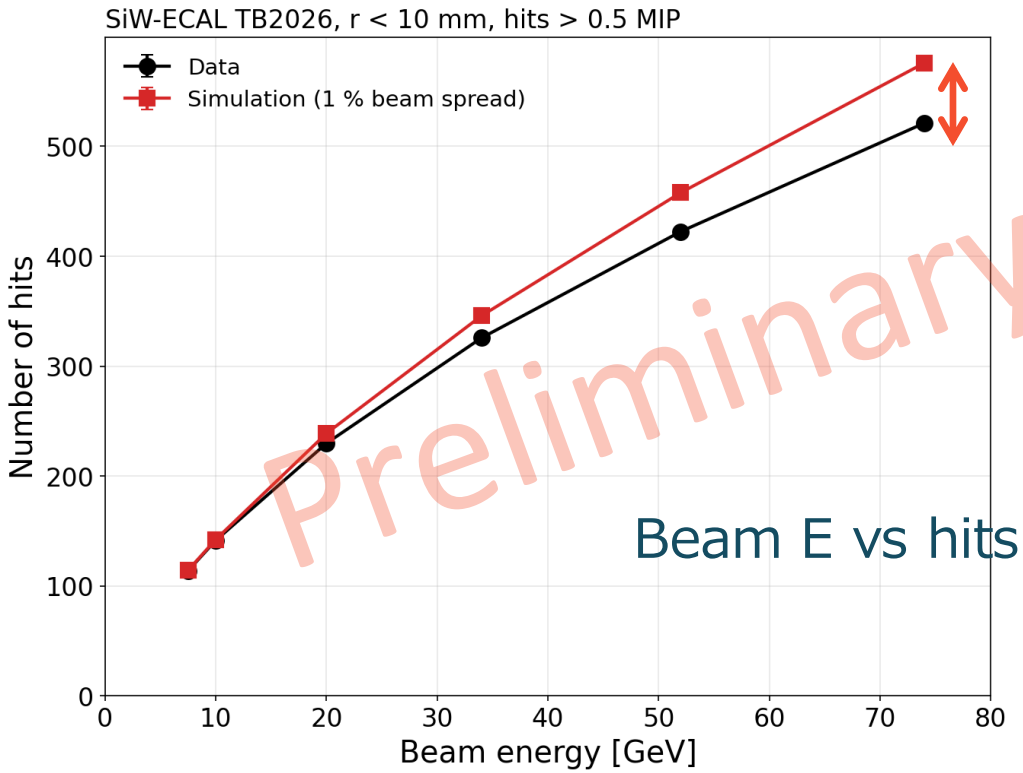


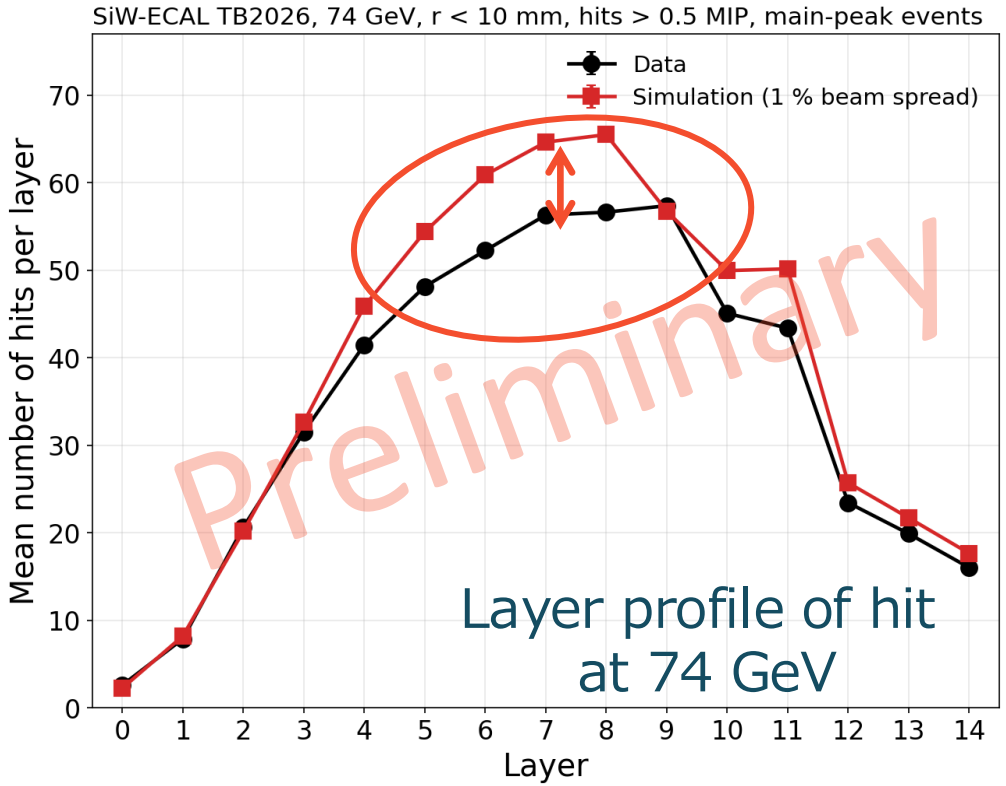
Broad agreement between data and simulation

A quantitative comparison requires corrections for hit loss and the position-dependent response discussed later.

Fewer low-energy hits at high beam energy

Data
Simulation





- The number of **low-energy hits decreases near the shower maximum** at high beam energies.
- Recent studies indicate that **high hit occupancy within a readout chip causes a pedestal shift**, suppressing low-energy hits (See backup slides).

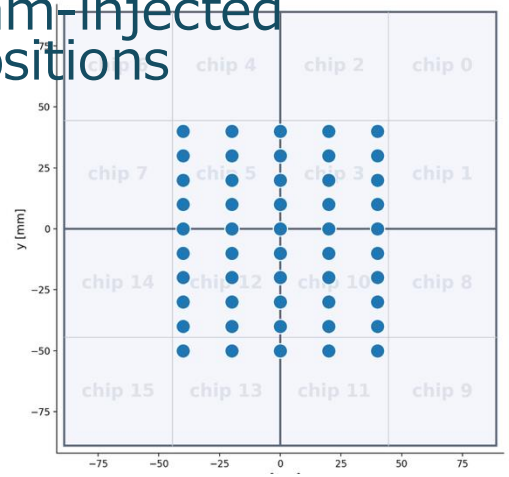
Position-dependent response

Beam position dependent detector response

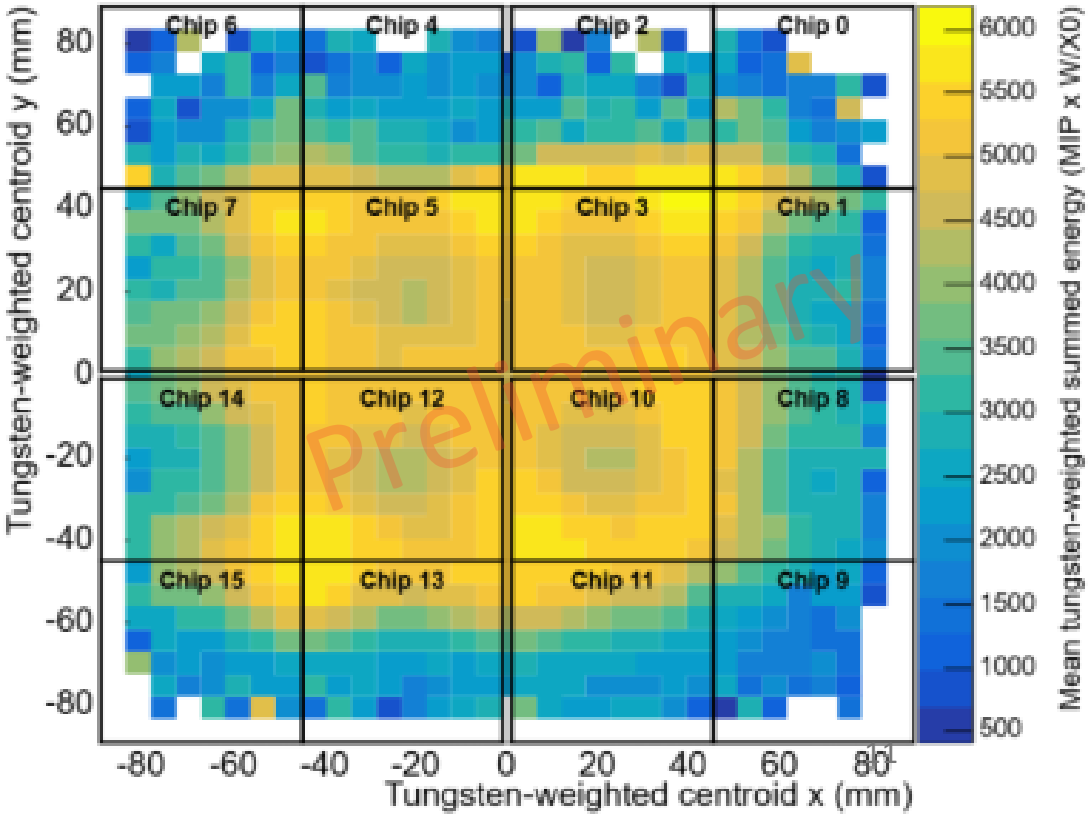
- Scanned 50 beam positions to map the detector response.
- The rec E depends on the beam-injected position.

  In particular, the rec E is lower when the beam hits the chip center.

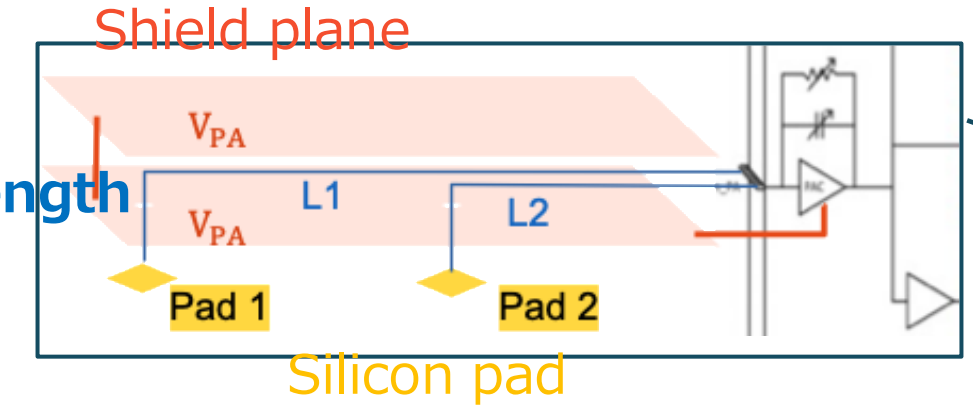
50 beam-injected positions

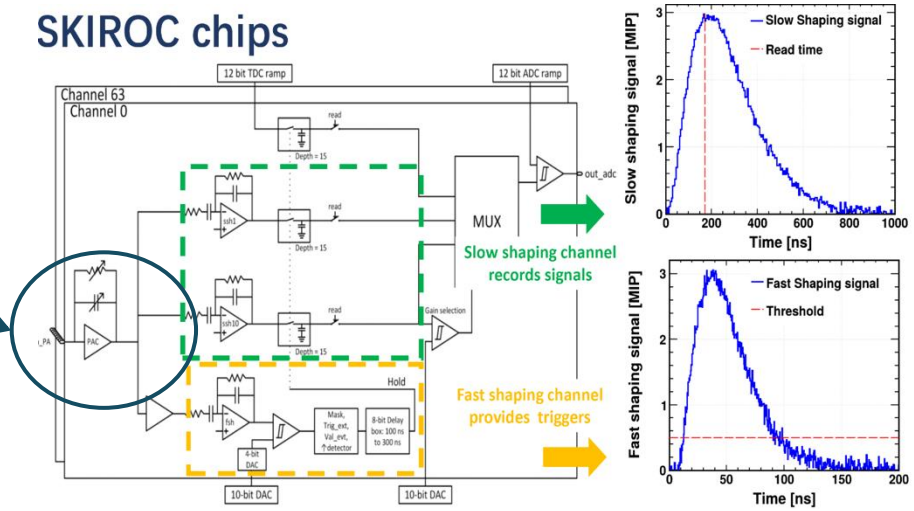


Reconstructed-energy map vs. beam position



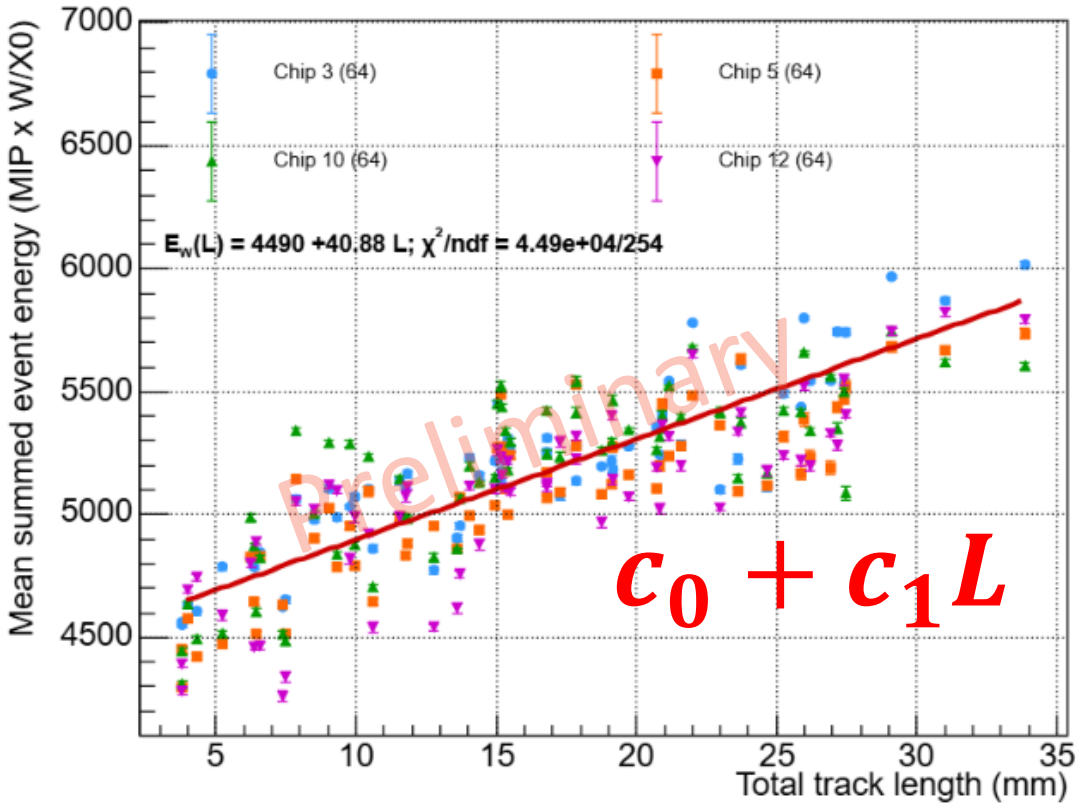
Correlation with PCB trace length





- Correlation between detector response & PCB trace length.
- Fitted with a linear function between total hit channel trace length & rec E.

Total channel PCB trace length vs rec E



Empirical correction

- Recovered rec E uniformity by $E_{\mathrm{corrected}} = \frac{E_{\mathrm{before}}}{c_0 + c_1 L}$
- Resolution improvement after correction.
- Correction strength "c_1/c_0" depends on beam energy.

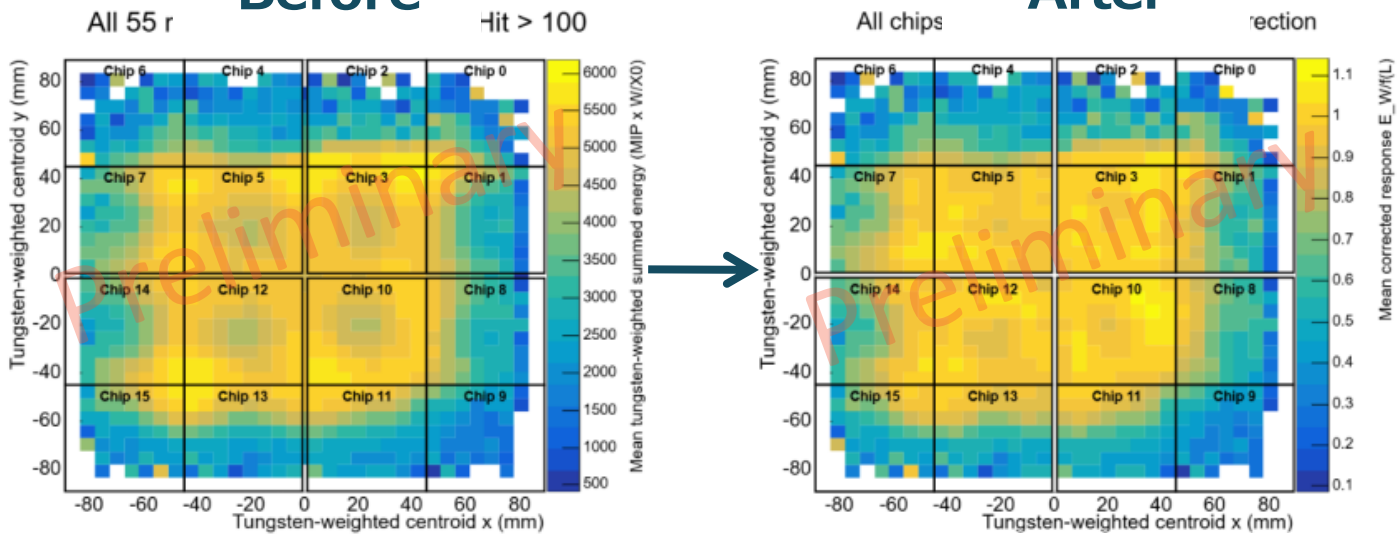
This would be a hint …

- Mechanism is under investigation.

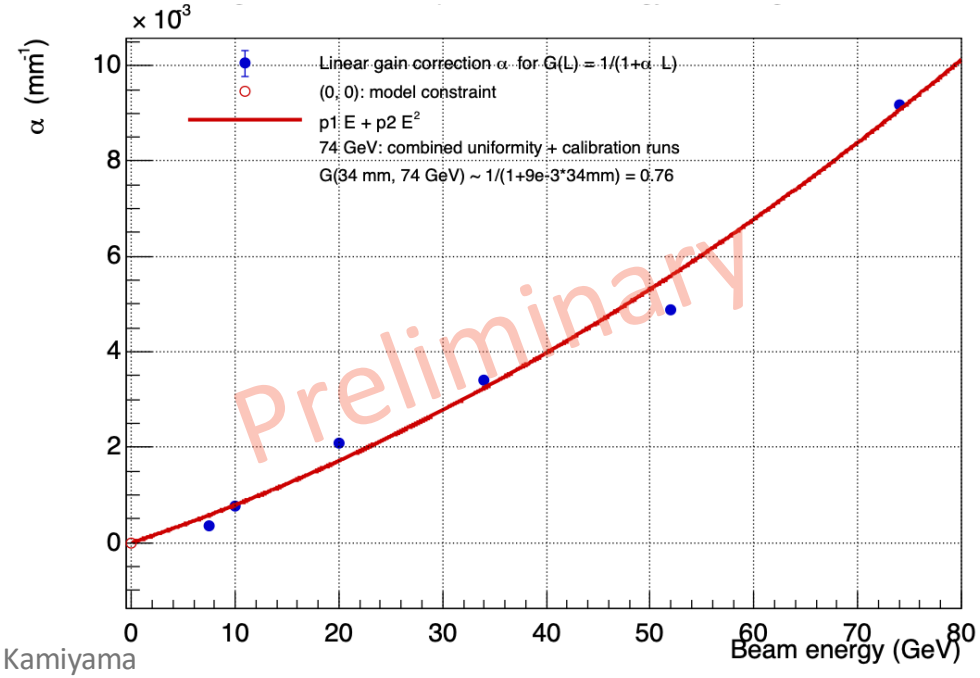
Energy (GeV)	Relative width reduction (%)
7.5	4.17
10	8.34
20	14.77
34	34.96
52	17.83
74	33.16

Preliminary

Before **After**



Beam energy vs c_1/c_0



ML-based EM event selection

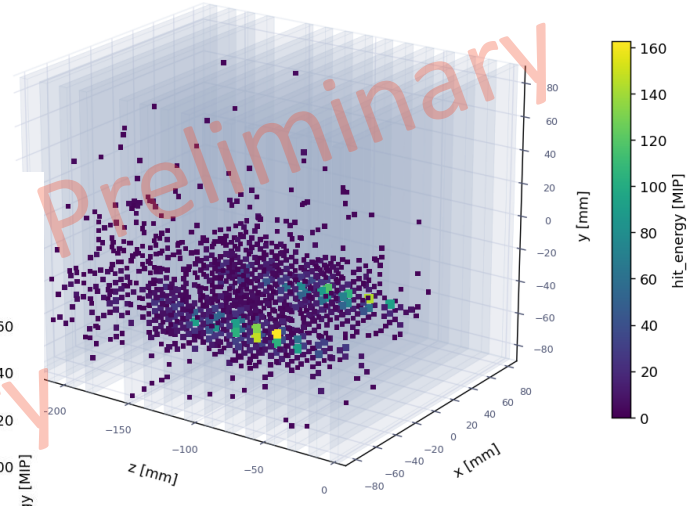
Motivation

- Real data contain muons, pions, multiple particles, and noise.
- Simple selections may leave residual background.

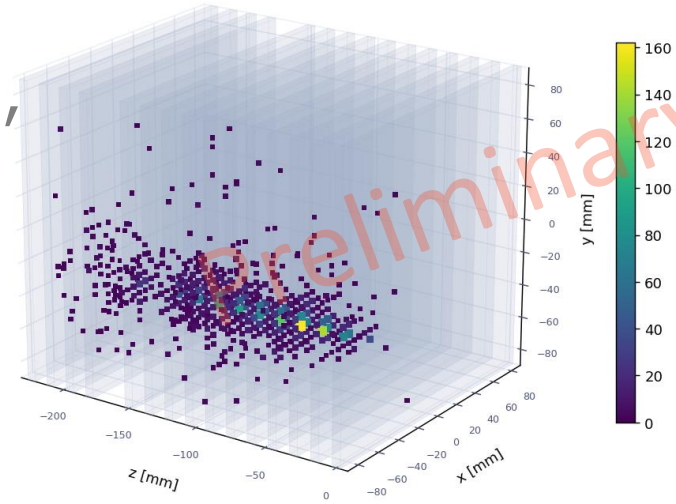
Approach

- A one-class autoencoder, **trained only on simulated EM events,** learns the characteristics of EM showers.
- Calculate “EM-likeness” with data.

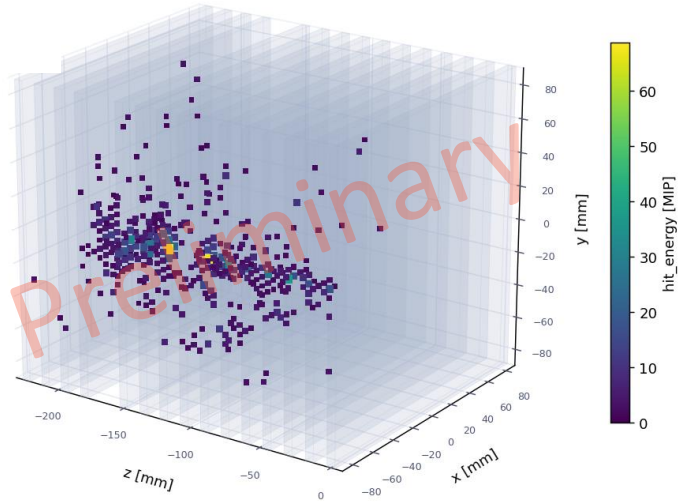
2 positrons?



Positron?



Pion?

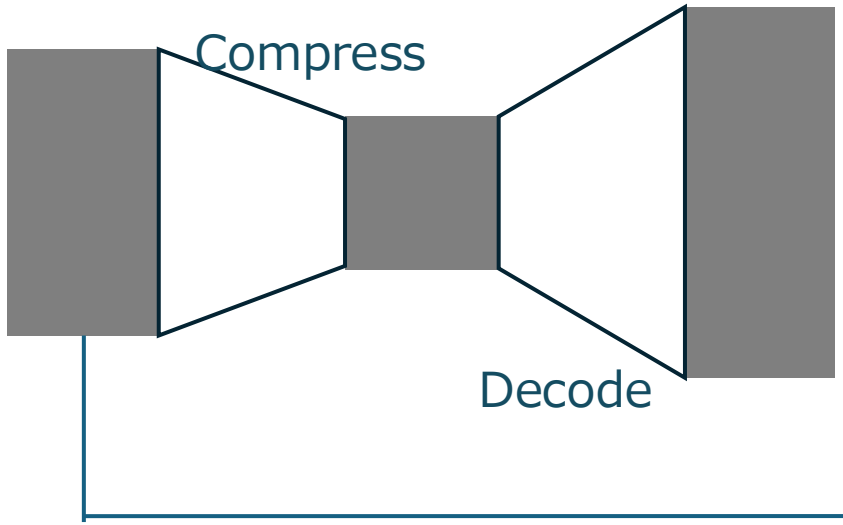


Architecture of the autoencoder

Attention-based model

Input:

- Hit x, y, layer
- Hit E



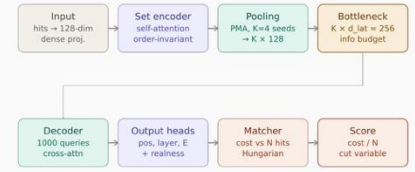
Predicted

- Hit x, y, layer
- Hit E

Check difference between input & reconstructed input

The neural network: a one-class set autoencoder (set-to-set, attention-based)

- **One-class set autoencoder**: trained only on simulated electrons, no labelled background classes
- **Set-to-set, permutation-invariant**: hits have no natural order, so no positional encoding is used.
- **Encoder (Set Transformer–style)**: 6 self-attention layers, 8 heads, over per-hit features (x, y, layer, energy).
- **Attention pooling (PMA, K=4 seeds)** compresses the variable-size hit set into a fixed latent: K × d_lat = 256 numbers (bottleneck dim).
- **Decoder (DETR-style)**: 1000 learned queries, cross-attention to the latent, four heads: position, layer, energy, realness.
- Hungarian matcher aligns predicted queries to real hits; the matched cost, normalized by N, is the anomaly score. Permutation-invariant.



Loss function:
Cost of matching:

$$C_{ij} = \underbrace{\|\hat{p}_i - p_j\|_1}_{\text{where}} + \underbrace{(-\log \hat{P}_i(c_j))}_{\text{at what layer}} + \underbrace{|\hat{e}_i - e_j|}_{\text{how much energy}} - \underbrace{\sigma(r_i)}_{\text{a confident query comes out cheaper}}$$

The score is that cost, solved and normalized:

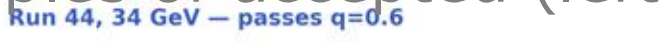
$$\text{score} = \frac{1}{N}\Big[\underbrace{\sum_{\text{matched}} C_{\pi^*(j),j}}_{\text{what it cost to explain the event}} + \underbrace{\sum_{\text{leftover}} \sigma(r_i)}_{\text{what the model over-predicted}}\Big]$$

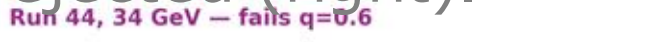
Model architecture inspired by S. Van Stroud, hepattn: Attention for High Energy Physics, v0.2.0, doi:10.5281/zenodo.16880940

1. The model calculate how closely each data event resembles a simulated EM shower.
2. Set threshold to separate EM events and backgrounds.
3. Events below the threshold are accepted as EM events.

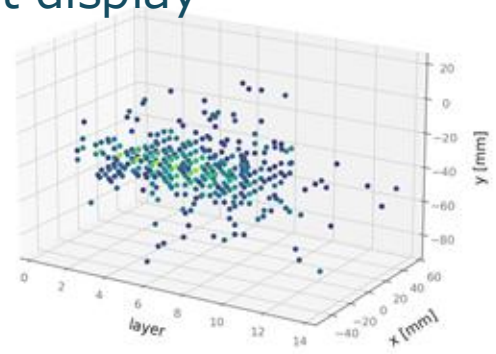
First selection result

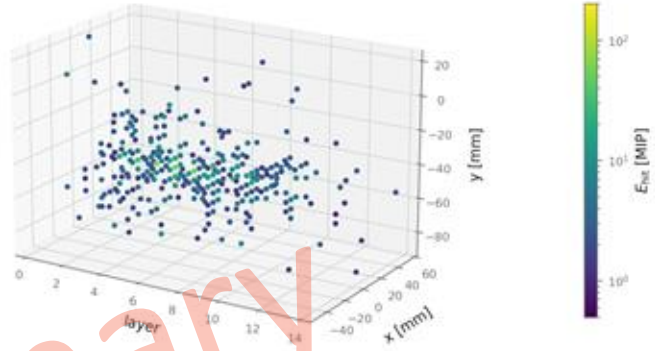
Examples of accepted (left) & rejected (right).



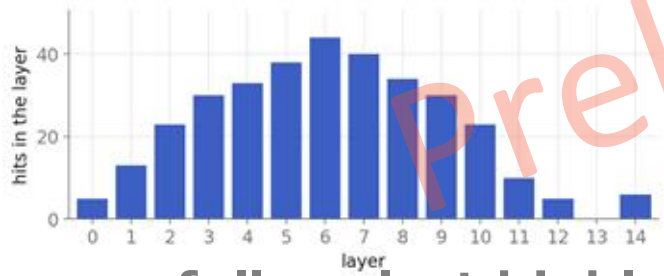


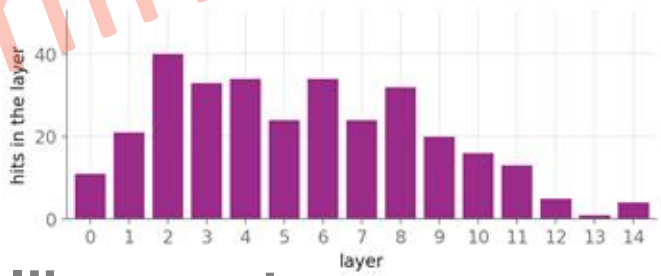
Event display





Layer profile of hits





Preliminary

- **Successfully select highly EM–like events**.
- Currently favors “clean” electron events, and the selection can still be tuned to reduce this bias.
- Background-separation model is also under study.

Summary & outlook

- **Test-beam campaign**
  - The 15-layer SiW-ECAL technological prototype operated successfully at CERN SPS.
  - The campaign recorded 27.8 million events over energy, position, and angle scans, including muon and pion samples.



- **Preliminary analysis results**
  - Reconstructed-energy distributions show broad agreement between data and simulation.
  - Two detector-response effects were identified: low-energy hit loss at high hit occupancy within a chip and a position dependence correlated with PCB trace length.
  - ML-based event selection is being evaluated for efficiency and selection bias.

- **Outlook**

  Understand and correct these response effects, then re-evaluate the energy response and resolution.

Backup

TB2006 summary

https://arxiv.org/pdf/0811.2354

- TB2006 at CERN, H6 beam line
- External RO
- 30 layers (1.4 mm - 10 layers, 2.8 mm - 10 layers, 4.2 mm - 10 layers, 24 X0 in total)
- E: 6 – 45 GeV
- Si sensor: $525\ \mu m$
- Ch in total: 6480 with 1 cm cell
- Reso: $\frac{\sigma_E}{E} = \frac{(16.6 \pm 0.1)\%}{\sqrt{E\,[\mathrm{GeV}]}} \oplus (1.1 \pm 0.1)\%$

TB2021 & TB2022 summary

https://arxiv.org/pdf/2211.07457

- November 2021 @ T21 area, DESY:
  - 15 layers (2.1 mm – 11 layers, 4.2 mm – 4 layers, in total 10.2 X0)
  - E : 1–6 GeV
  - FEV10/11 + SKIROC2 + 320 μm S – 11 layers, FEV12 + SKIROC2a + 500 μm Si – 4 layers
  - Aim
    - Commissioning of common 15-layer DAQ
    - Arrangement of threshold, hold value, gain
    - pedestal・MIP calibration
    - Evaluation of self-trigger & noise
    - Record of low E EM

- March 2022 @ T21 area, DESY:
  - 15 layers in total 15.2 X0
  - E : 1–6 GeV
  - Aim
    - Record shower with deeper calorimeter
    - Compare FEV13 and COB with other versions
    - Evaluation of S/N, effective threshold and cell response
    - Validation for simulation/digitization

# Layer	FEV	ASIC	Si sensor	W
2	FEV13	SKIROC2a	650 μm	2.8
2	COB	SKIROC2a	500 μm	2.8
4	FEV12	SKIROC2a	500 μm	2.8, 2.8,2.8,4.2
7	FEV10/11	SKIROC2	320 μm	4.2

- June 2022 @SPS, H2, CERN:
  - 15 layers in total 20.8 X0)
  - electron : 10, 20, 40, 60, 80, 100, 150 GeV
  - muon : 50, 150 GeV
  - pion : 10, 20, 70, 100, 150, 200 GeV
  - Change SKIROC preamplifierのfeedback capacitanceを1.2 pFから6 pFに変更し、gainを約1/4.7
  - Aim
    - Usage of common DAQ of EUDAQ2
    - Evaluation of ECAL

Layer	FEV	Si sensor	W
0–3	FEV13	650 μm	4.2 mm
4–5	FEV13	500 μm	4.2 mm
6	COB	500 μm	4.2 mm
7	FEV12	500 μm	4.2 mm
8	COB	500 μm	5.6 mm
9	FEV12	500 μm	5.6 mm
10–11	FEV11	320 μm	5.6 mm
12	FEV10	320 μm	5.6 mm
13	FEV13	320 μm	5.6 mm
14	FEV11	320 μm	5.6 mm

TB2025 summary

- March 2025 @ DESY:
  - 3 layers 2.1 -> COB -> 2.1
  - No absorber
  - E : 3 GeV
  - Aim

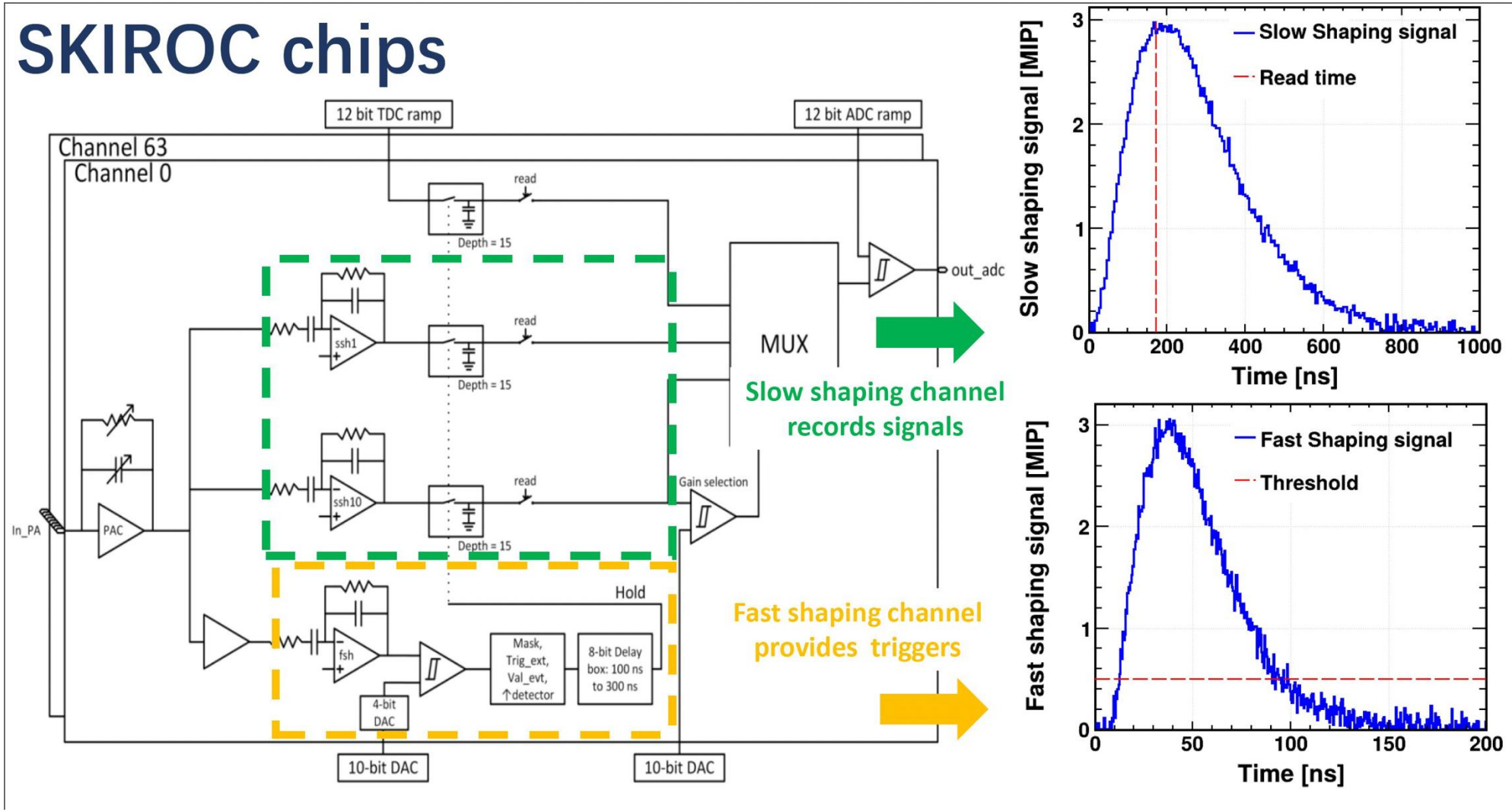
    Measure FEV2.1 response

How to upgrade FEV board

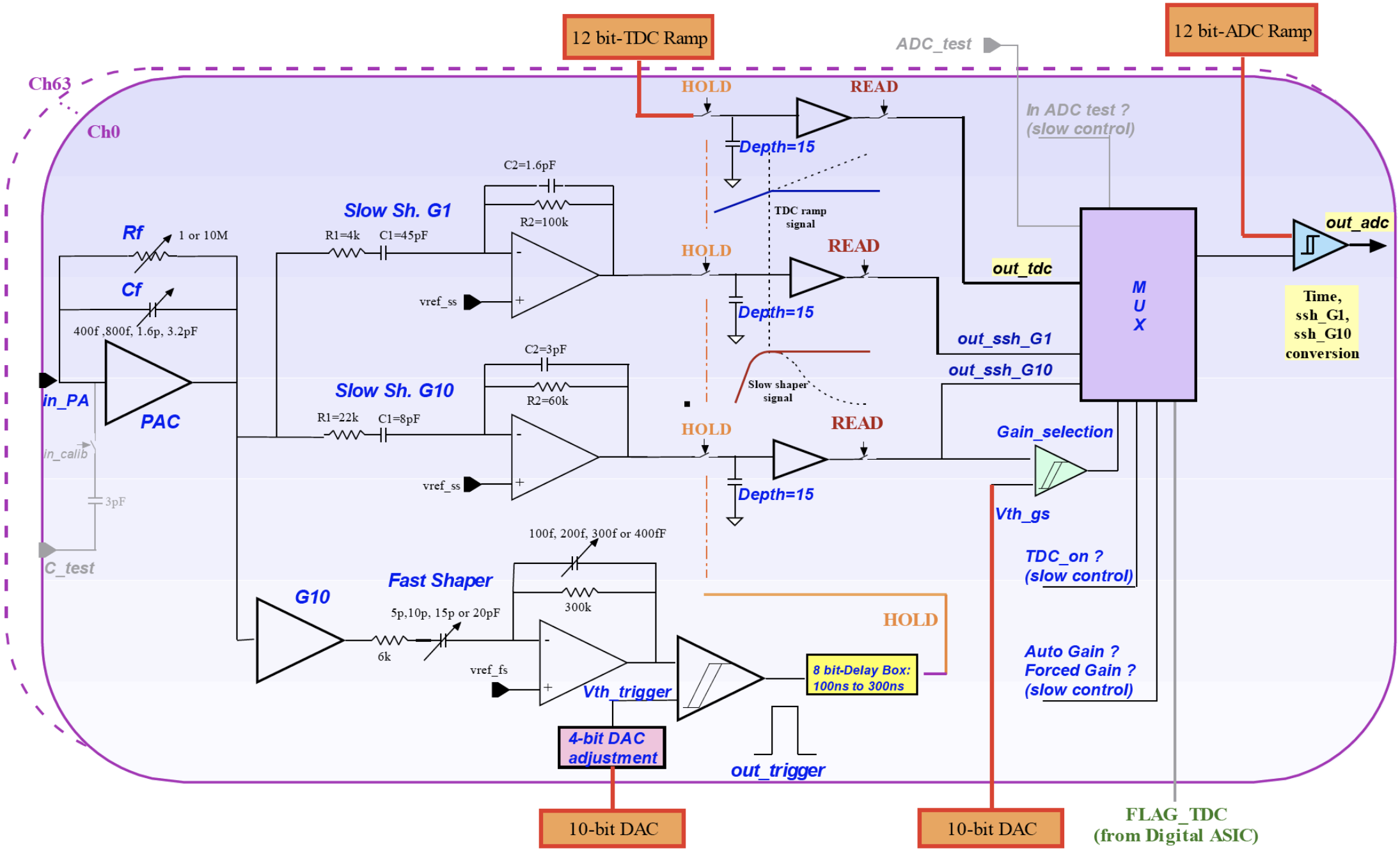
https://indico.in2p3.fr/event/36116/contributions/163076/attachments/97129/149385/SiWECAL_Beamtest.pdf

Problem in the previous boards	FEV2.1 update	Why it helps
Power-supply noise could affect the ASIC response.	Local low-voltage regulators (LDOs)	They provide cleaner and more stable power close to the ASICs.
Noise or voltage variations could enter through the sensor-bias line.	Local high-voltage filtering and distribution	They stabilize the bias voltage applied to the silicon sensors.
Dense PCB traces could cause noise and crosstalk between channels.	Simplified signal routing and improved ASIC shielding	They reduce electrical interference between channels.
Control and data signals could become unstable while travelling across the board.	Redesigned buffering and data paths	They improve the reliability of signal and data transmission.
A bad channel or a poor sensor connection was difficult to diagnose before a beam test.	Analogue-probe line, temperature monitoring, and board ID	They allow each module and channel connection to be checked on a test bench.
Testing a single board required much of the full detector system.	Flexible stand-alone HV distribution	It makes individual-module testing and commissioning easier.
Sensor-to-PCB connection failures were found in older modules.	Improved assembly procedure and analogue-probe checks	They improve the connection and allow defective glue contacts to be detected.

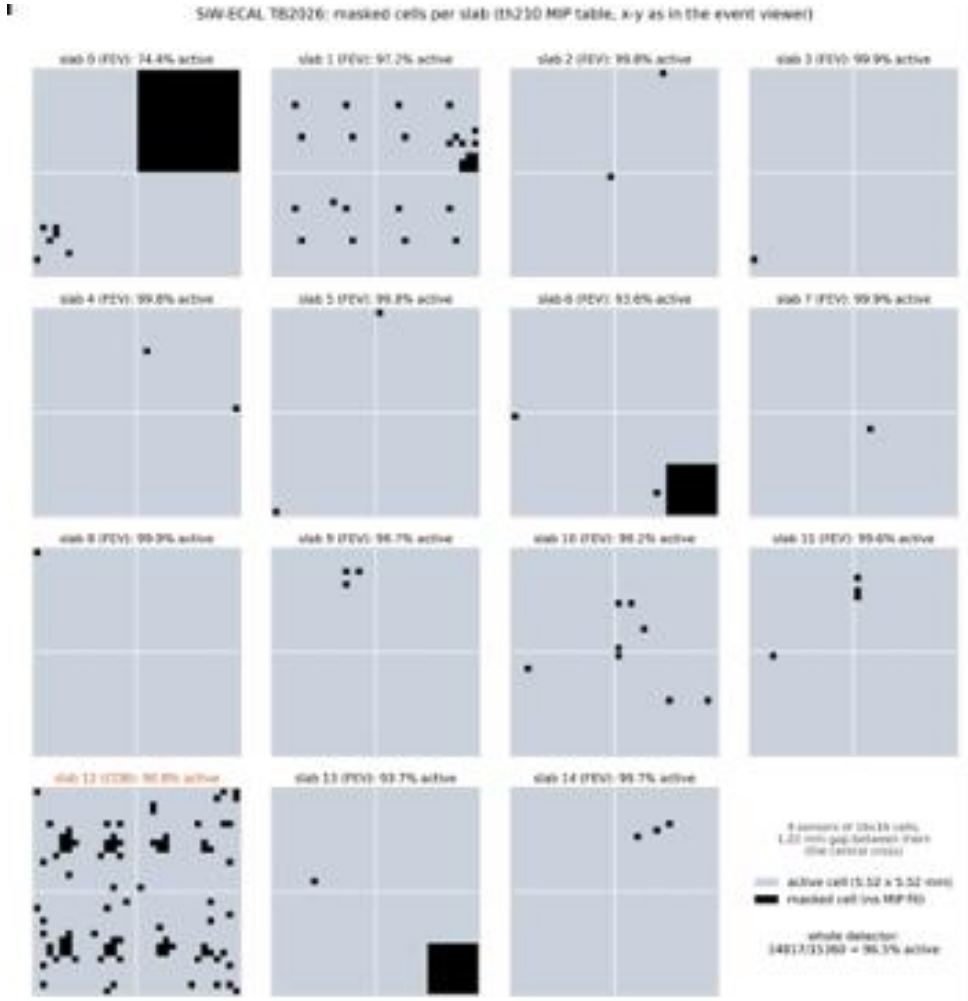
SKIROC chip


SKIROC chips
12 bit TDC ramp
12 bit ADC ramp
Channel 63
Channel 0
read
Depth = 15
out_adc
ssh1
MUX
Slow shaping channel
records signals
ssh10
Gain selection
In_PA
PAC
Hold
fsh
Mask,
Trig_ext,
Val_evt,
↑detector
8-bit Delay
box: 100 ns
to 300 ns
4-bit
DAC
Fast shaping channel
provides triggers
10-bit DAC
10-bit DAC
Slow shaping signal [MIP]
Slow Shaping signal
Read time
Time [ns]
Fast shaping signal [MIP]
Fast Shaping signal
Threshold
Time [ns]

TB


12 bit-TDC Ramp
ADC_test
12 bit-ADC Ramp
Ch63
Ch0
HOLD
READ
In ADC test ?
(slow control)
Depth=15
C2=1.6pF
Slow Sh. G1
R2=100k
TDC ramp
signal
Rf
1 or 10M
R1=4k
C1=45pF
HOLD
READ
out_adc
Cf
vref_ss
out_tdc
MUX
Depth=15
400f ,800f, 1.6p, 3.2pF
C2=3pF
out_ssh_G1
Time,
ssh_G1,
ssh_G10
conversion
Slow Sh. G10
out_ssh_G10
Slow shaper
signal
R2=60k
in_PA
PAC
R1=22k
C1=8pF
HOLD
READ
Gain_selection
in_calib
vref_ss
Depth=15
3pF
Vth_gs
100f, 200f, 300f or 400fF
C_test
Fast Shaper
TDC_on ?
(slow control)
G10
300k
HOLD
5p,10p, 15p or 20pF
Auto Gain ?
Forced Gain ?
(slow control)
6k
vref_fs
8 bit-Delay Box:
100ns to 300ns
Vth_trigger
4-bit DAC
adjustment
out_trigger
10-bit DAC
10-bit DAC
FLAG_TDC
(from Digital ASIC)

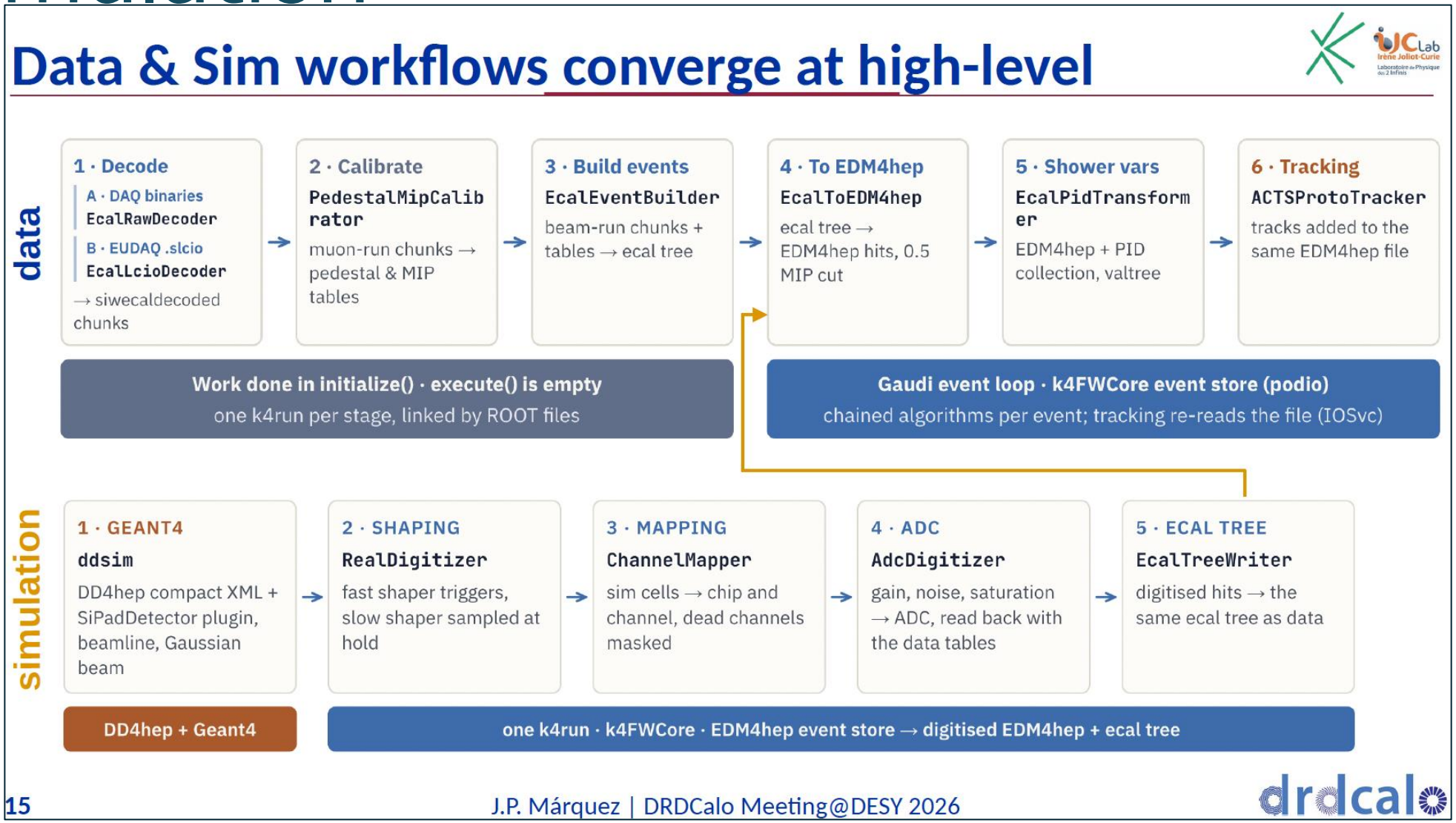
Detailed mask channels



Layer	Active cells (%)
0	74.4
1	97.2
2	99.8
3	99.9
4	99.8
5	99.8
6	93.6
7	99.9
8	99.9
9	99.7
10	99.2
11	99.6
12 (COB)	90.8
13	93.7
14	99.7
All	96.5

Simulation

QGSP_BERT_EMZ



“Beam center” estimation

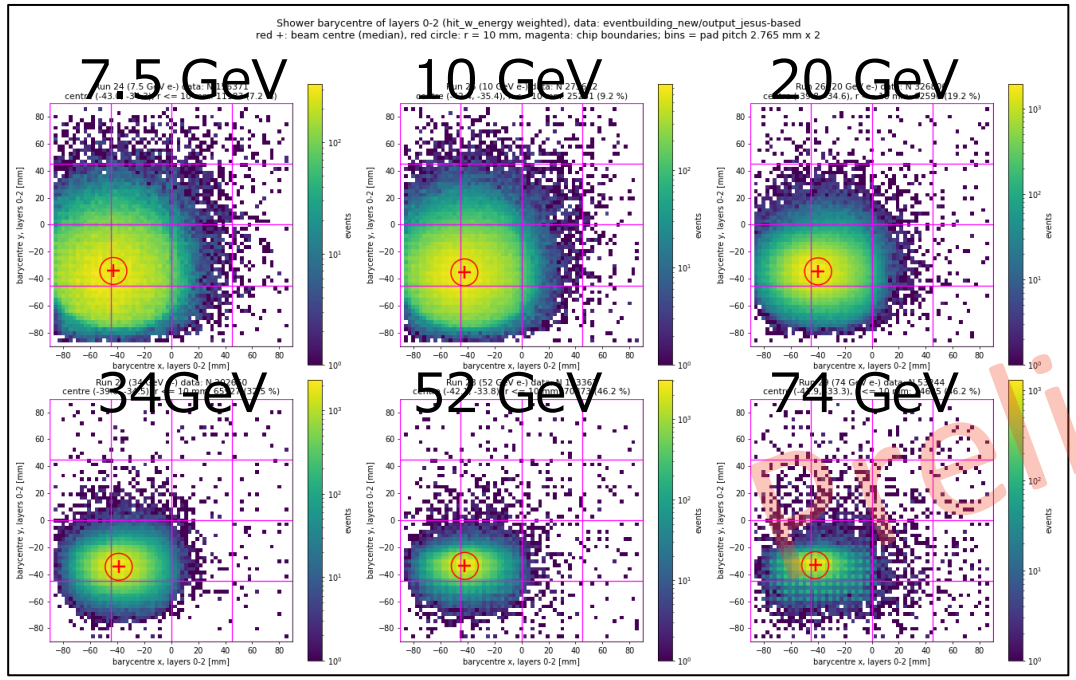
- “Beam-position” estimated by
  $\boldsymbol{x}_{center} = \frac{\sum(w_i \cdot \boldsymbol{x}_i)}{\sum(w_i)}$ (w_i: hit_w_energy, $\boldsymbol{x}_i$: hit position(x, y)) at layer 0-2,

with all events.

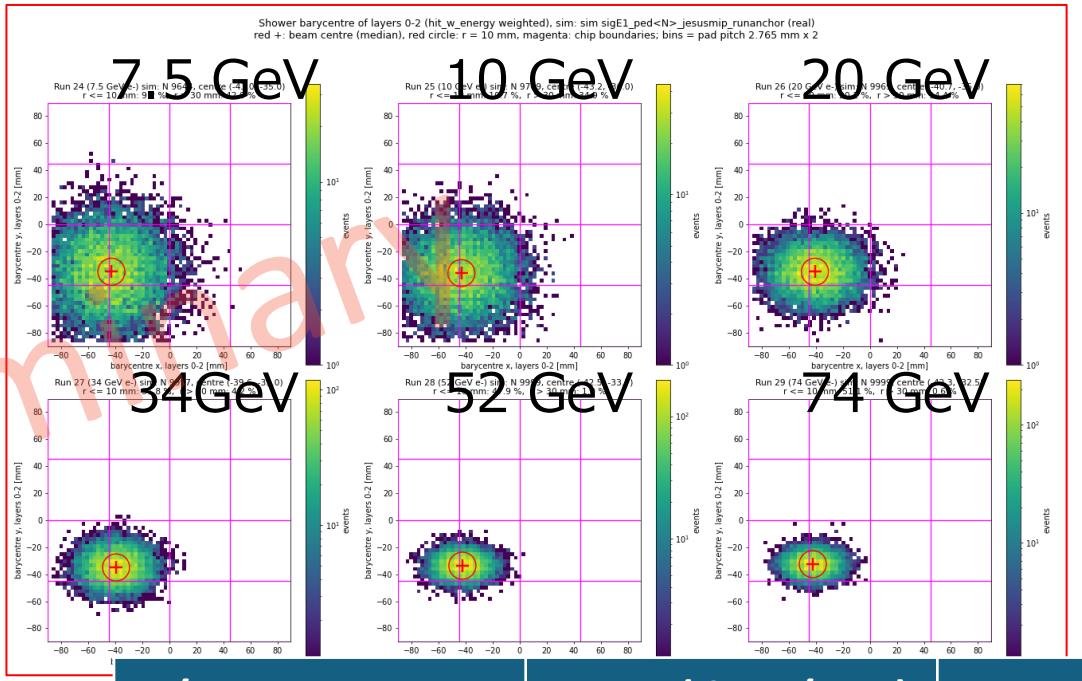
- Only selected events with **r < 10 mm** from the mean of “beam position” for both. (Near “beam-center” events)

- Comparison between heat map of “beam center”:

Data



Sim 10000 events



- Event fraction
  - R <10 -> almost same
  - **R >30 -> Data >> Sim**

E / GeV	R < 10 (data / sim)	R > 30 (data / sim)
7.5	7.2 / 9.2	48.8 / 42.0
10	9.2 / 10.7	40.1 / 34.9
20	19.2 / 20.1	17.5 / 14.4
34	32.5 / 31.8	6.4 / 4.2
52	46.2 / 47.9	3.9 / 1.0
74	46.2 / 51.1	**8.1 / 0.6**

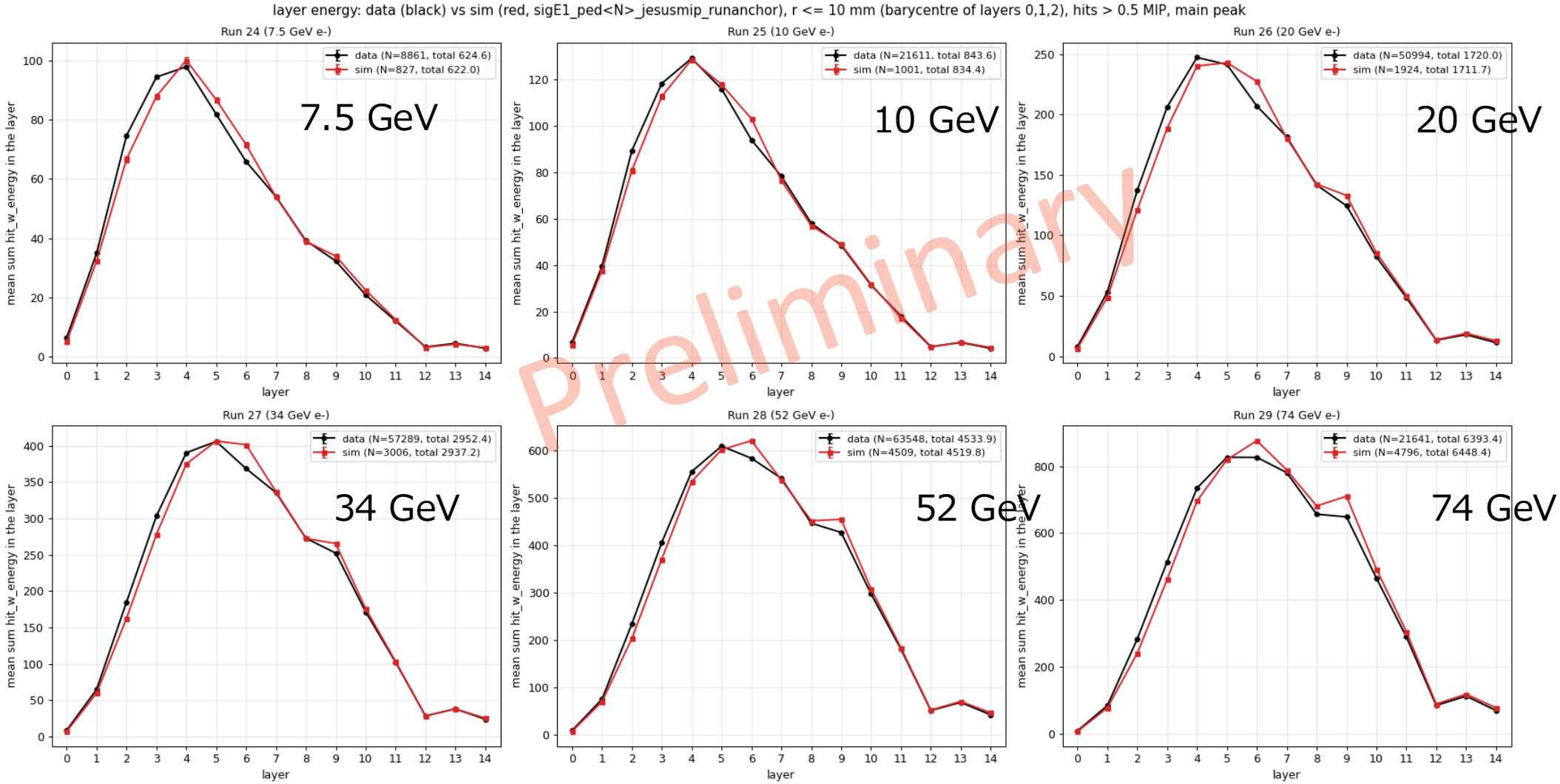
Preliminary

Simulation vs Data

Data

Simulation

- Layer E, 0.5 mip cut, R<10



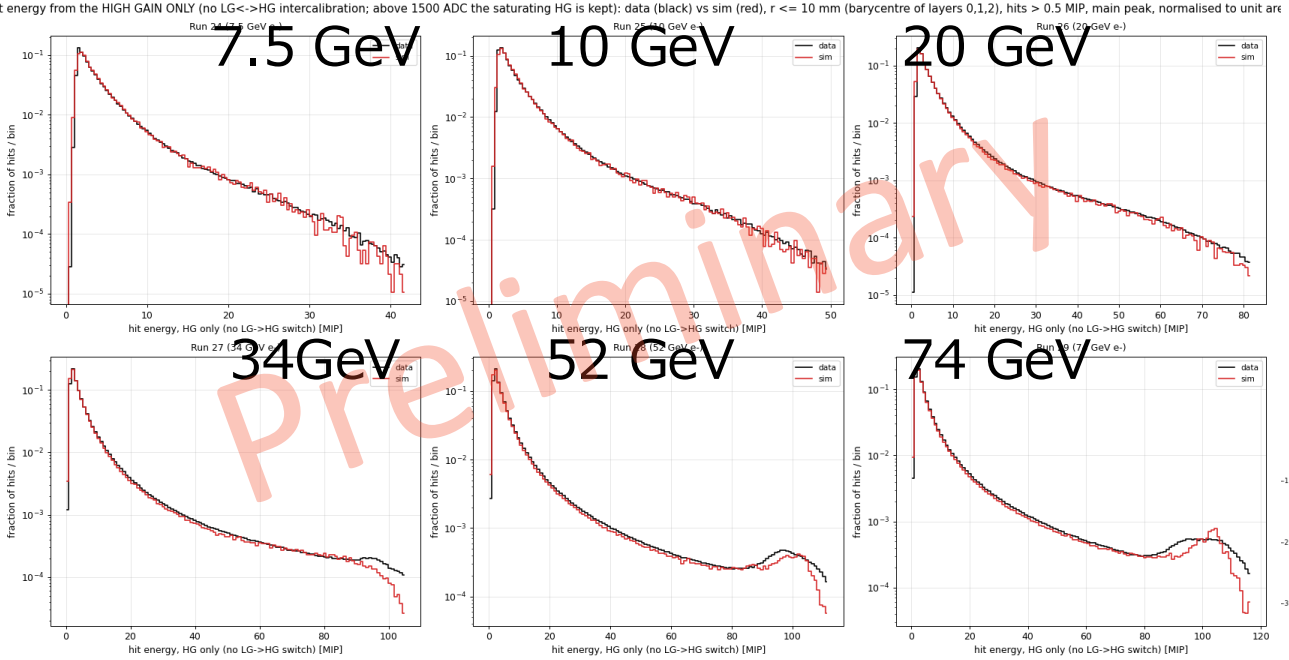
Analysis for EM response

- Hit E, 0.5 mip cut, R<10

No inter calibration (HG only)

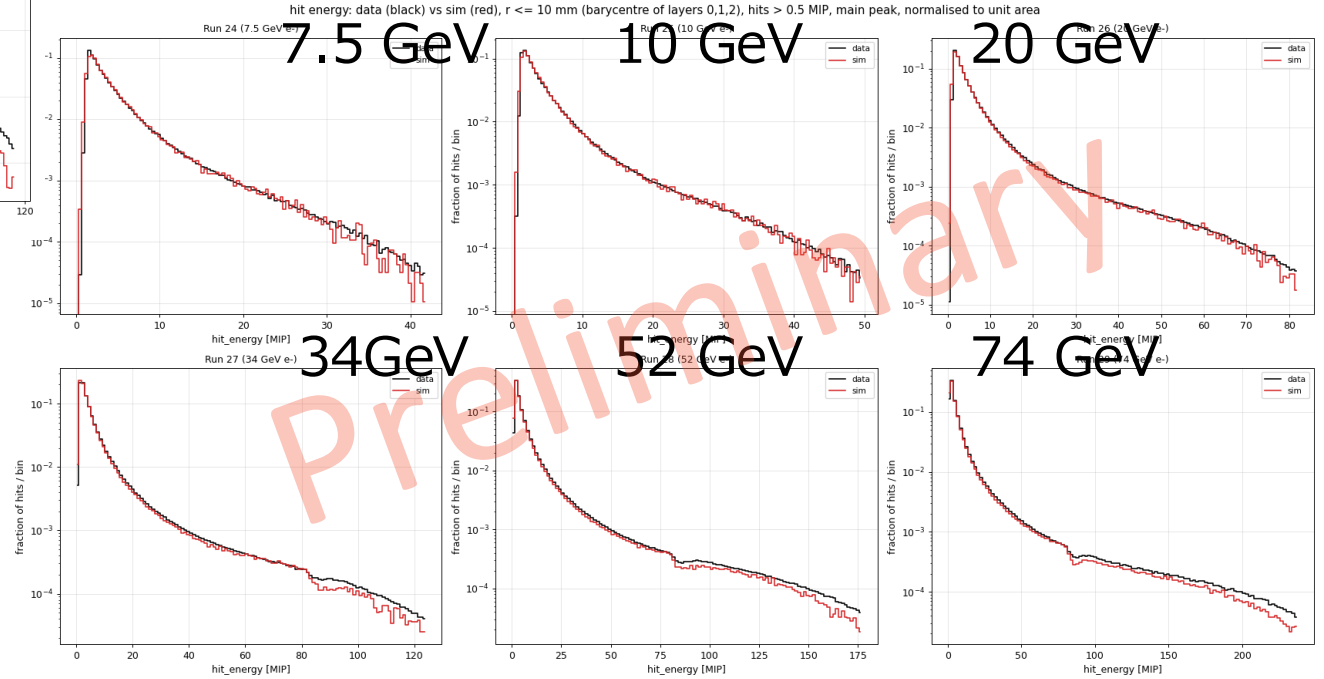
Data

Simulation



Preliminary

After inter calibration



Preliminary

Analysis for EM response

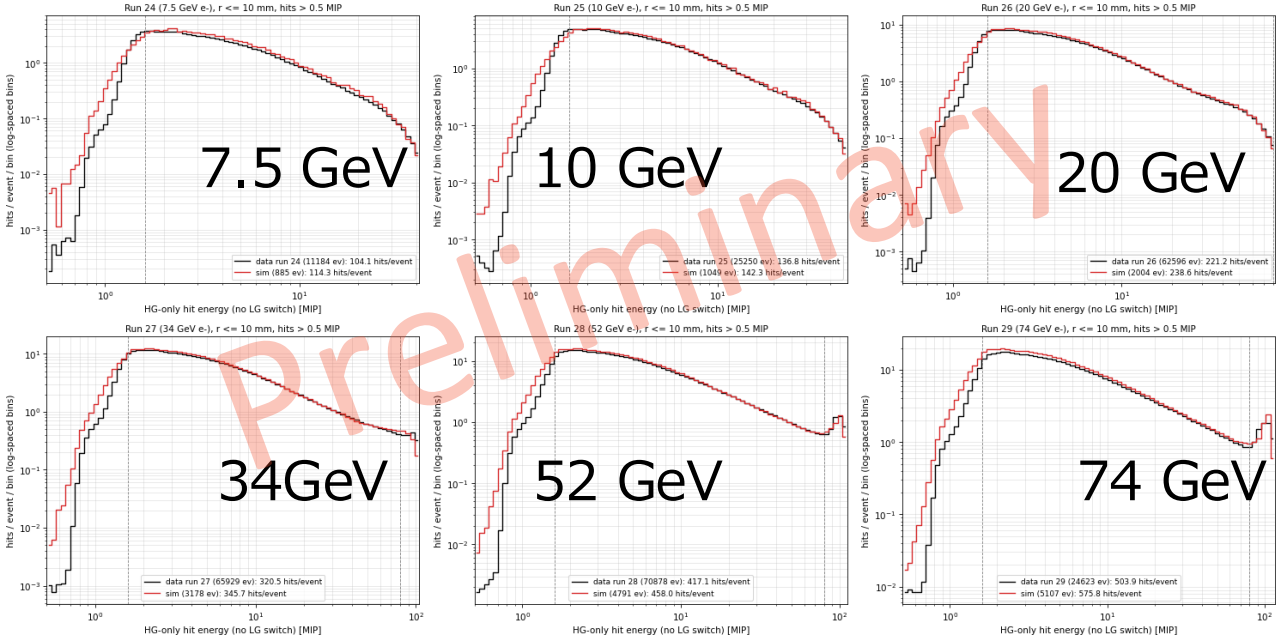
Log scale

Data

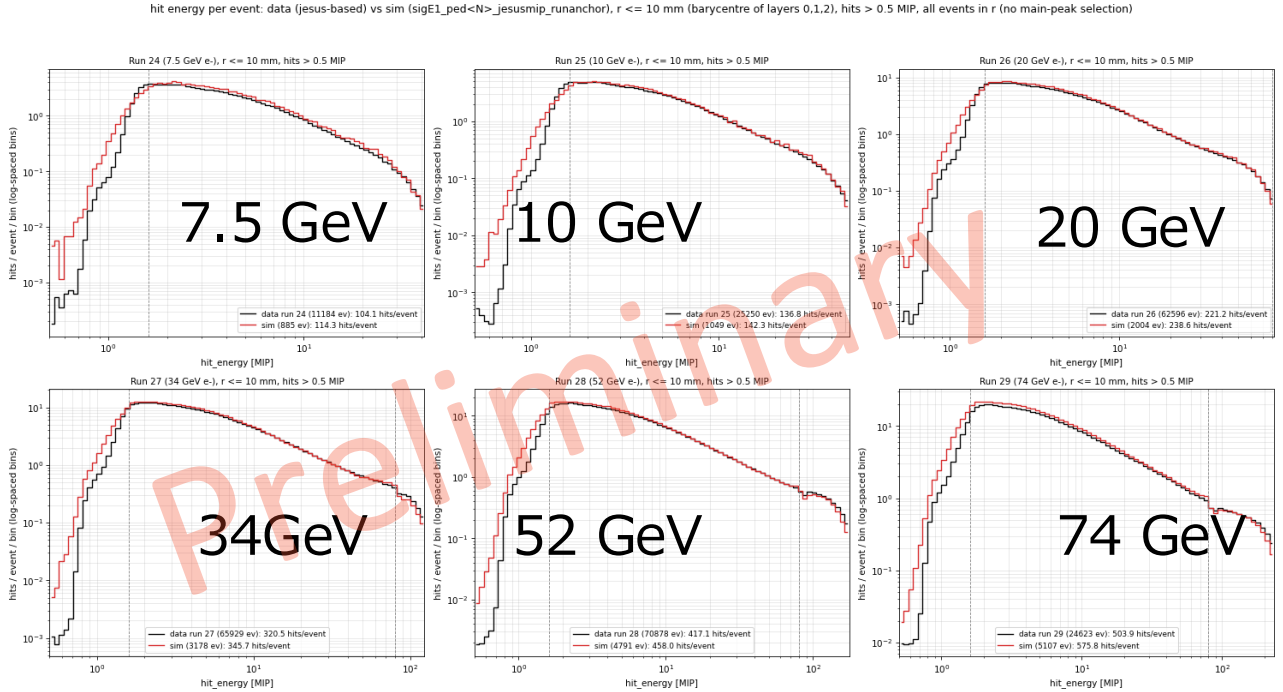
Simulation

No inter calibration (HG only)





After inter calibration



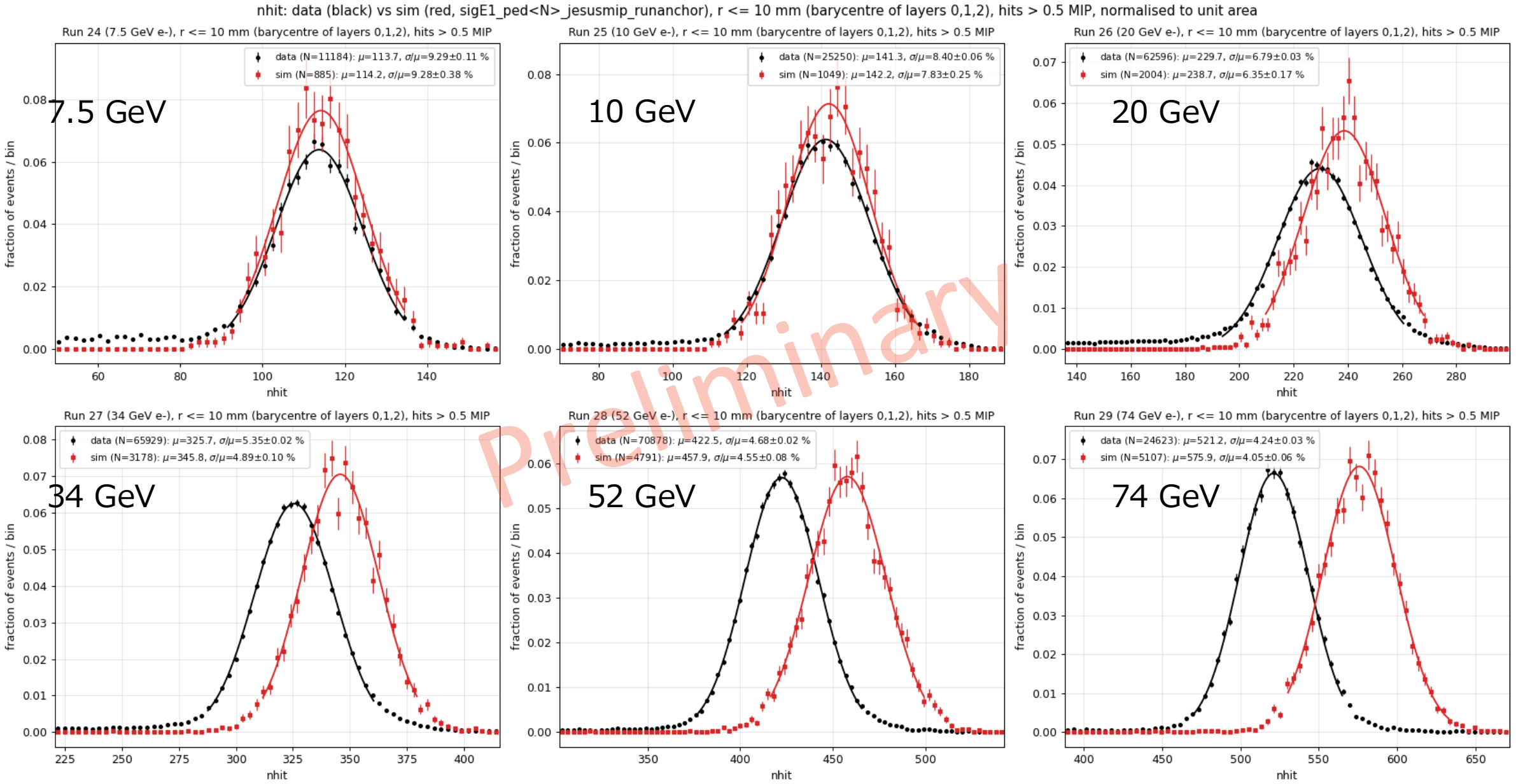
Preliminary
Preliminary

Analysis for EM response

- Nhits, 0.5 mip cut, R<10

Data

Simulation



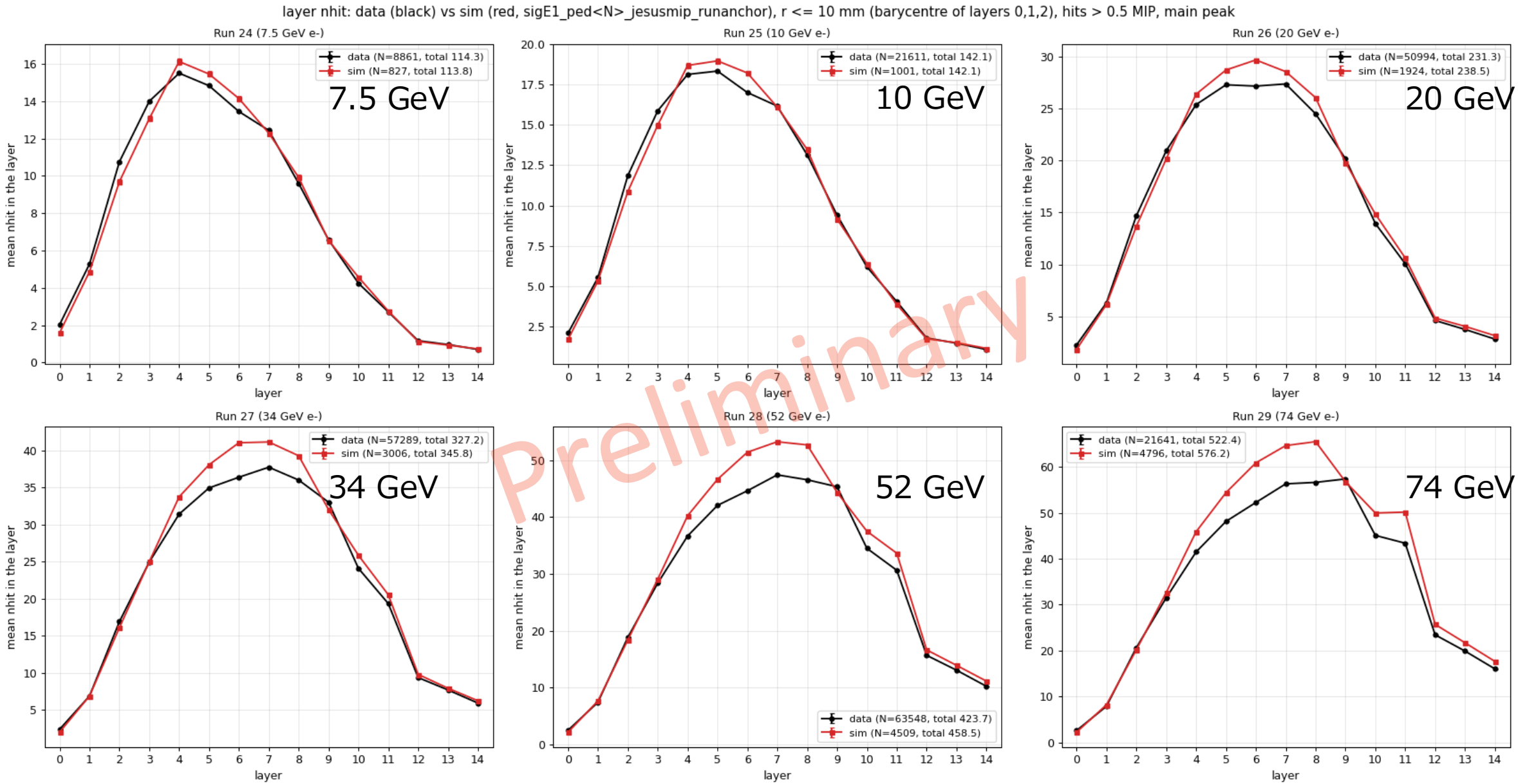
Preliminary

Analysis for EM response

- Layer hits, 0.5 mip cut R<10

Data

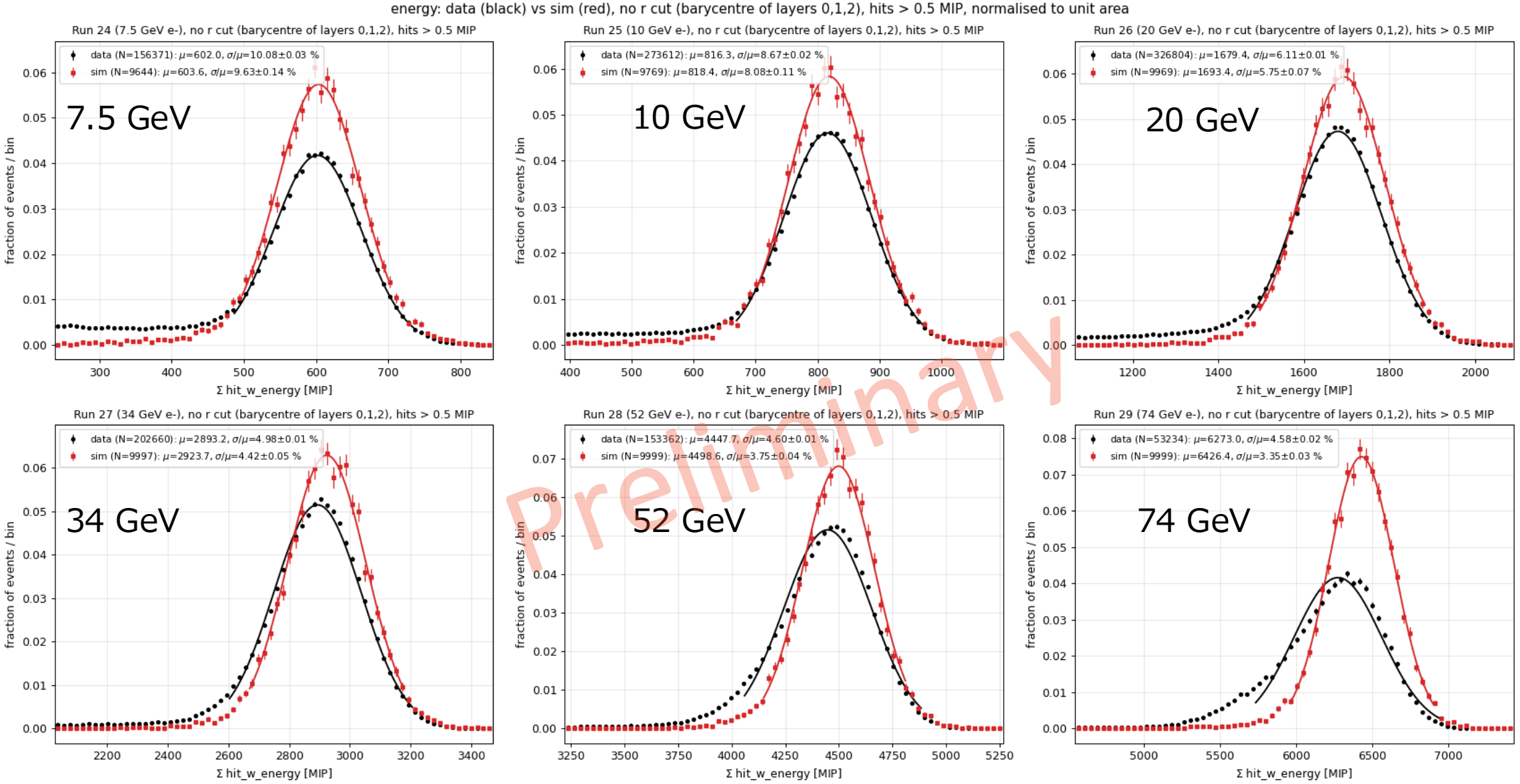
Simulation



- Energy, 0.5 mip cut, No event selection

Data

Simulation

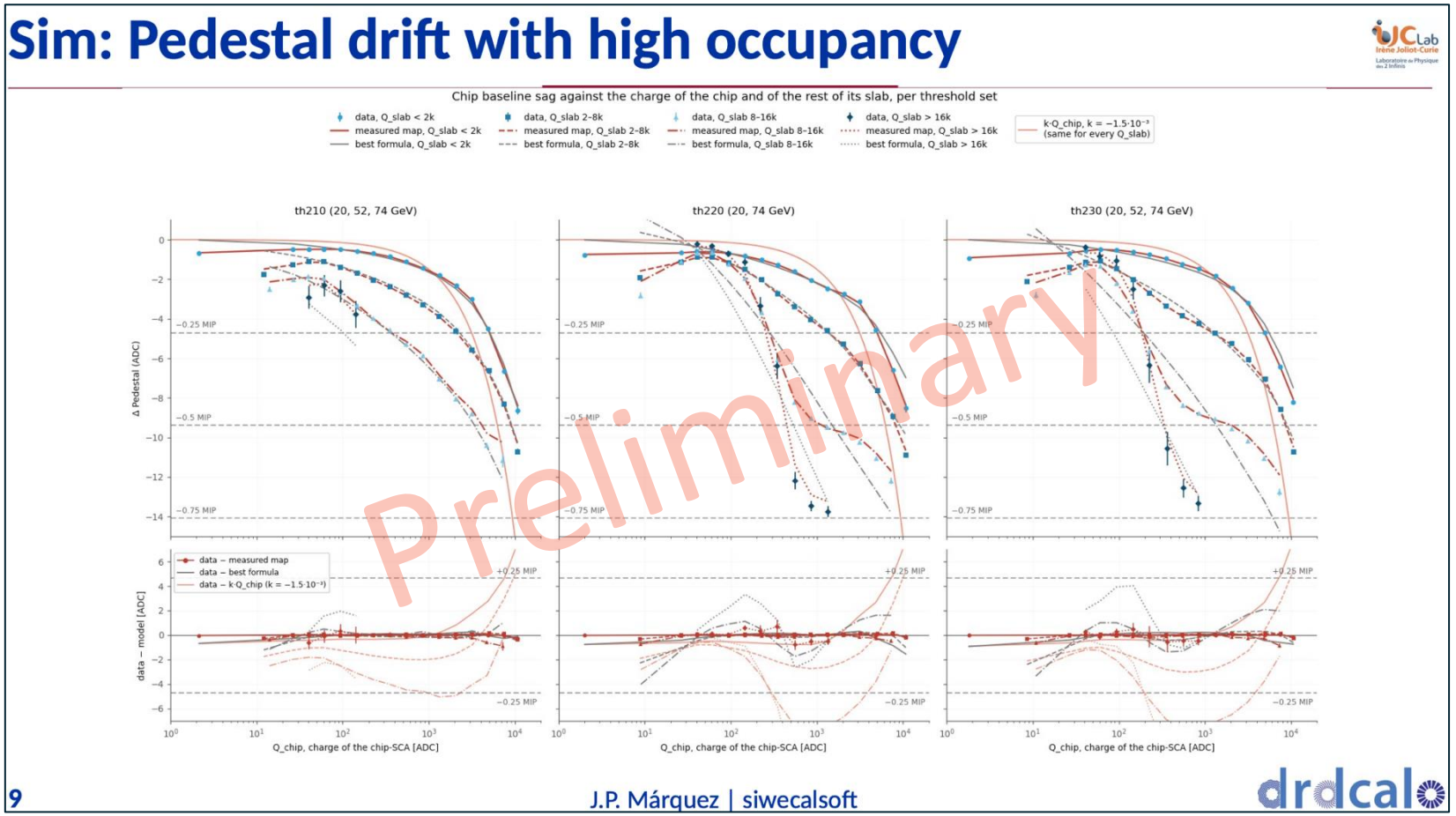


Preliminary

Pedestal shift at high occupancy chip

J.P. Márquez

- When a chip collects a large charge, the pedestal of the other channels in the chip drops, by up to about half a MIP or more.
- Effectively this raises the threshold, so small hits are lost, mostly near the shower maximum.
- The physical origin, for example the HV recovery or the front-end baseline, is still under investigation.



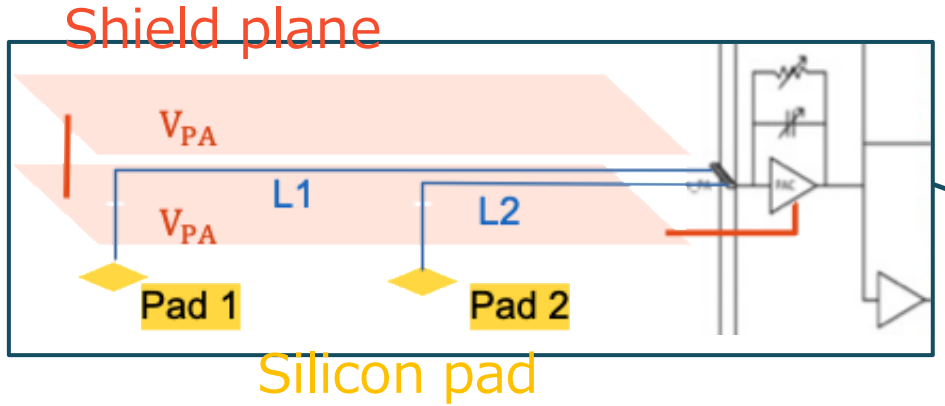
“Beam position” estimation

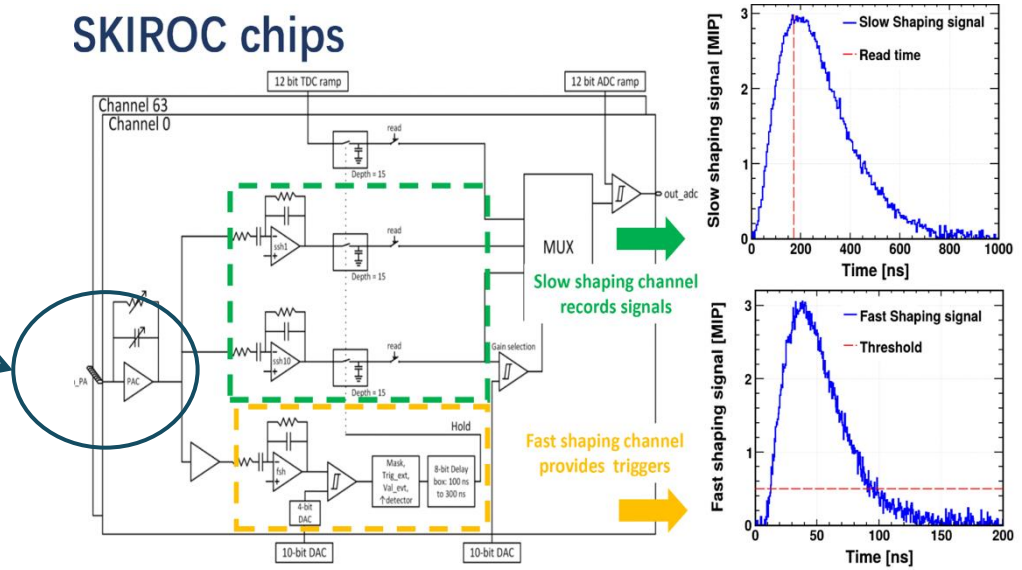
“Beam-position” estimated by
$\boldsymbol{x}_{center} = \frac{\sum(w_i \cdot \boldsymbol{x}_i)}{\sum(w_i)}$ (w_i: hit_w_energy, $\boldsymbol{x}_i$: hit position(x, y)) at layer 0-14,witout layer 1 & 14

with all events.

Candidate mechanism on non-uniformity response

- Trace-length-dependent cross-talk





  - ΔV_{pa} due to large charge from silicon pads, which is proportional to total charge Q_{tot}.
  - Effective capacitance between wire and shield plane gives $\Delta Q_i \propto \Delta V_{\mathrm{pa}} \cdot L_i$.
  - Cross-talk in each channel $\propto Q_{\mathrm{tot}} \cdot L_i$

- Chip-occupancy-dependent response loss

