FCC-SEED vertex detector project

A short overview

FCC-SEED
VERTEX DETECTOR FOR FCC-ee

Expression Of Interest for a Vertex Detector at FCCee :

FCC Snail-shape vErtEx Detector (FCC-SEED)

Involved laboratories : IPHC[1], CPPM[2], IP2I[3], LPNHE[4], APC[5], LAPP[6],
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FCCee requirements

- Vertex requirements
  - ✓ Data flux
    - Continuous beam ⇒ Data flux significantly higher than ILC,
    - Higher radiations doses as well, for both ionizing radiation and fluence.
  - ✓ Beam pipe
    - Cooling mandatory as well as shielding,
    - Compensated by small inner radius ~12 mm
  - ✓ Challenges:
    - How to reach the targeted resolution with an adapted read-out architecture while fulfilling all the other requirements ?
    - How to propose a robust but ambitious VTX concept ? ⇒ Integration

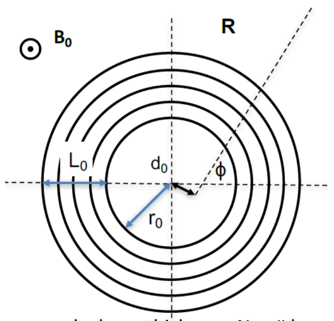
FCCee
$$\sigma_{d_0} = a \oplus \frac{b}{p \sin^{3/2}\theta}$$
$a \simeq 5\,\mu m$; $b \simeq 15\,\mu m\,GeV$

$b \sim r_0 \sqrt{material}$

$a \sim \sqrt{r_0}$

$$\Delta d_0|_{res.} \approx \frac{3\sigma_{r\phi}}{\sqrt{N+5}} \sqrt{1 + \frac{8r_0}{L_0} + \frac{28r_0^2}{L_0^2} + \frac{40r_0^3}{L_0^3} + \frac{20r_0^4}{L_0^4}}$$

$$\Delta d_0|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{\beta p_T} r_0 \sqrt{\frac{d}{X_0 \sin\theta}} \sqrt{1 + \frac{1}{2}\left(\frac{r_0}{L_0}\right) + \frac{N}{4}\left(\frac{r_0}{L_0}\right)^2}$$



d = layer thickness, N = # layers

Drasal, Riegler, https://doi.org/10.1016/j.nima.2018.08.078

Spatial resolution per layer	$\simeq 3$	μm
Pixel pitch	14-20	μm [1]
read-out time	$\simeq 500$	ns [2]
Power dissipation	$\simeq 20 - 50$	mW/cm^2
Sensor thickness	$40 - 50$	μm [3]
Safety factor on particle rate	3	[4]
Maximum Hit rate	75 / 25	MHz/cm^2 [5]
Maximum Hit rate	22.5×10^{-3} / 7.5×10^{-3}	$hits/mm^2/BX$ [5]
Assumed cluster multiplicity	5	
Fired pixel rate	375 / 125	MHz/cm^2 [5]
Fired pixel rate	0.33 / 0.11	$fired\ pixels/mm^2/BX$ [5]
Occupancy/pixel/read-out	3.45×10^{-3} / 1.15×10^{-3}	$/pixel/readout$ [5]
Ionising radiation (1^{st} layer)	30 / 10	$MRad/year$ [5 6]
Corresponding Fluence	$\simeq 1.8 \times 10^{14}$ / 6×10^{13}	$n_{eq(1\ MeV)}/year$ [5 7]

[1] Depending on charge sharing/encoding
[2] Compromise between power dissipation and pile-up at $\sqrt{s} = 91\ GeV$
[3] To allow bending
[4] due to beam background uncertainties estimates
[5] With / without safety factor
[6] assuming beam running 180 days/year, and average incident angle of $\simeq 70^o$.
[7] assuming NIEL factor of 5×10^{-2}

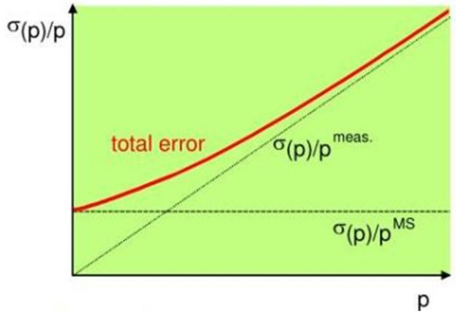
- Tracker requirements
  - ✓ Maximum precision with:
    - Good spatial resolution per plane
    - Low momentum
    - High level arm
    - High B field
    - High number of layers (N)
    - Minimize material budget ⇒vLow number of layers (N)
  - ✓ Typically σ_{sp} ~5-10 μm/layer ; material ~1-2% X_0/layer
  - ✓ Challenges
    - Large surfaces ⇒ Integration & Power management
    - How to include timing / PID ?

$$\frac{\sigma_{p_T}}{{p_T}^2} \sim 2 \times 10^{-5}\,GeV^{-1}$$

	thickness (mm)	Mat. Budget (X/X_0 %)
Beam pipe[1]		
Au	0.005	0.16%
AlBeMet162[2]	0.35	0.14%
Paraffin	1.0	0.18%
AlBeMet162[2]	0.35	0.14%
Total beam pipe	1.705	0.61%
Single layer		
Silicon sensor	0.050	0.05%
Cables, flex and support		$\simeq$ 0.10%
Material per layer		$\simeq$ 0.15%

[1] described in [6]
[2] 62% Be and 38% Al alloy

$$\frac{\Delta p_T}{p_T}\Big|_{m.s.} \approx \frac{0.0136\,\mathrm{GeV/c}}{0.3\beta\, B_0 L_0} \sqrt{\frac{d_{tot}}{X_0 \sin\theta}} \qquad \frac{\Delta p_T}{p_T}\Big|_{res.} \approx \frac{12\,\sigma_{r\phi}\, p_T}{0.3\, B_0 L_0^2} \sqrt{\frac{5}{N+5}}$$



for N equidistant measurements
(R.L. Gluckstern, NIM 24 (1963) 381)

[6] A. Novokhatski et al. Estimated heat load and proposed cooling system in the FCC-ee Interaction region beam pipe. In Proc. IPAC'23, number 14 in International Particle Accelerator Conference, pages 260–263. JACoW Publishing, Geneva, Switzerland, 2023.

SEED: a vertex detector for FCCee

- À la CLD/ILD: 3 double ladders + discs
  - Robust but not optimized for material budget
- À la ALICE ITS-3 (IDEA) : 3/4 layers with stitched half cylinders
  - Fill factor not 100% per layer
  - Stitching mandatory
    - Pitch ? Power ? Yield ? Fill factor ? Bent radius ?
  - Very competitive for mat. budget but limitations
  - (acceptance, resolution, radius ?)

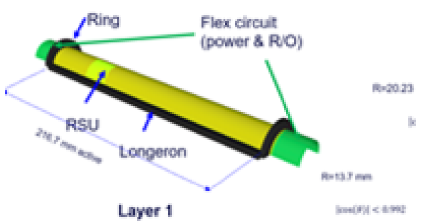


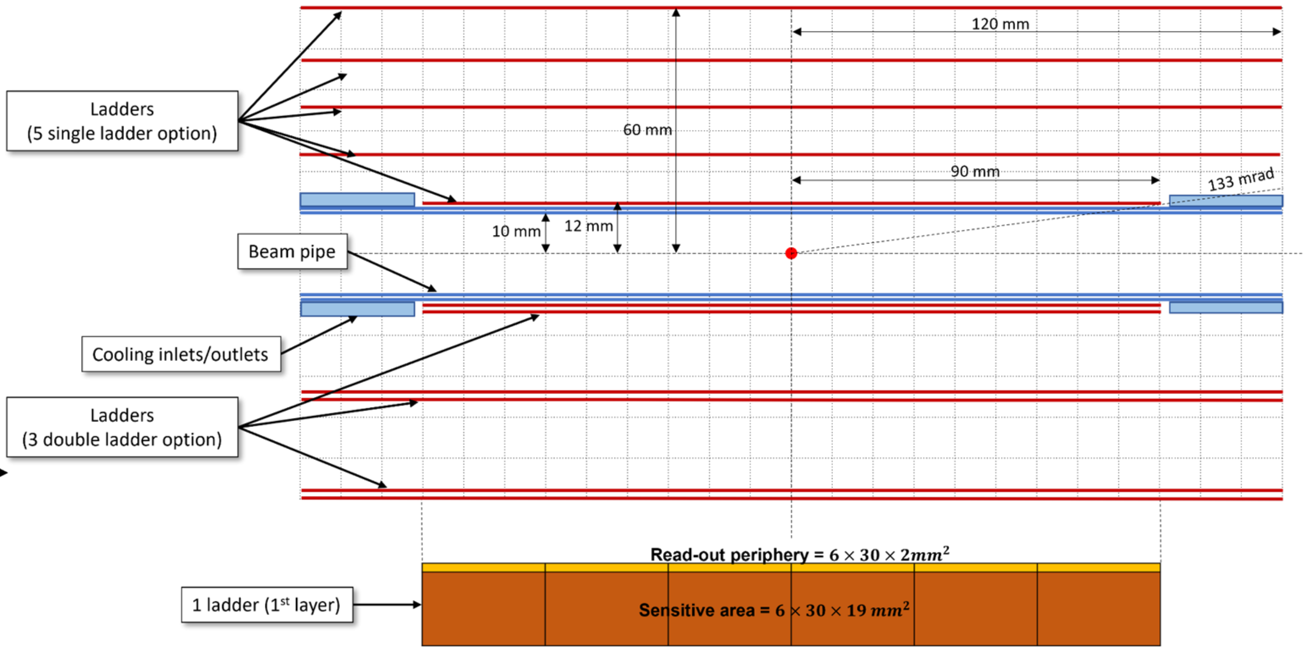
Table 3: Barrel dimensions (single and double sided option)

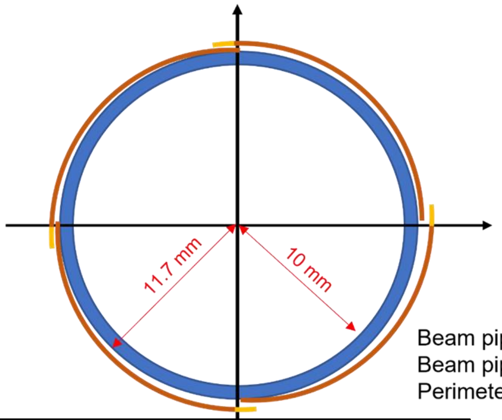
Layer	1	2	3	4	5
Radius (mm)	12-13	24	36	48	60
Zmax (mm)	90	120	120	120	120
Perimeter (mm)	75	151	226	302	377
# Chips per ladder	6	8	8	8	8
# ladders	4	8	12	16	20

Layer	1-2	3-4	5-6
Radius (mm)	12-13	35-36	59-60
Zmax (mm)	90	120	120
Max perimeter (mm)	82	226	377
# Chips per ladder	6	8	8
# ladders	4	12	20

Single chip dimension	$30 \times 22.2\ mm^2$
Sensitive area chip dimension	$30 \times 19.2\ mm^2$

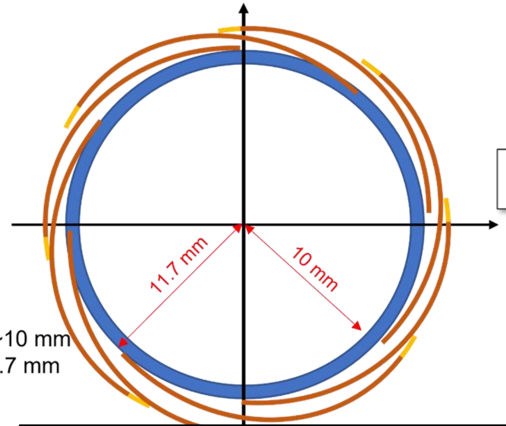
- Alternative Proposal: SEED concept = bent ladders + slight overlap
  - Stitching not mandatory
  - Inner radius minimized and approaching constant value
  - Full acceptance in φ
  - Option: double sided can be considered.
  - Number of layers = free parameter ⇒ redundancy
  - Competitive for mat. Budget. AND full azimuthal acceptance





Beam pipe inner radius ~10 mm
Beam pipe thickness ~ 1.7 mm
Perimeter ~73.5 mm

Option 1 : single layers



Option 2 : double layers

Pilars for the VTX R&D

Goals: establish a robust vertex concept for FCCee in the coming ~5 years.

CMOS Sensor R&D

- R&D trough DRD3/7
- OCTOPUS project dedicated to VTX (targets 3 μm spatial resolution)
- MANTA Project (outer tracker & timing R&D)
- CASSIA: Blue sky R&D (in pixel preamplification)
- Fast timing R&D

Simulations

- Beam background
- Full simulation of the VTX
  - IP resolution
  - Tracking performances
  - Realistic Digitizer – Clustering
- Vertex finder
- Flavour tagging
- Physics benchmark studies

Bent sensors & Integration

- Master curved sensor fabrication and testing
- Explore mechanical options, type of material, stress and cooling, etc…
- Design a full mechanical geometry, to be tested in full simulation
- Cooling

Iterative process (feedback loop)

Coherent developments of sensors, mechanic, integration and simulation.

Bent sensor and integration

ALICE ITS-3 TDR

- https://cds.cern.ch/record/2890181/files/ALICE-TDR-021.pdf

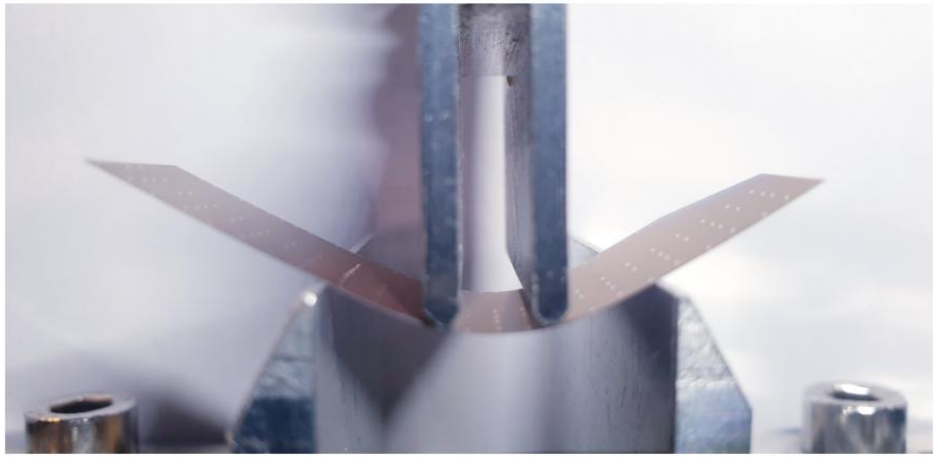
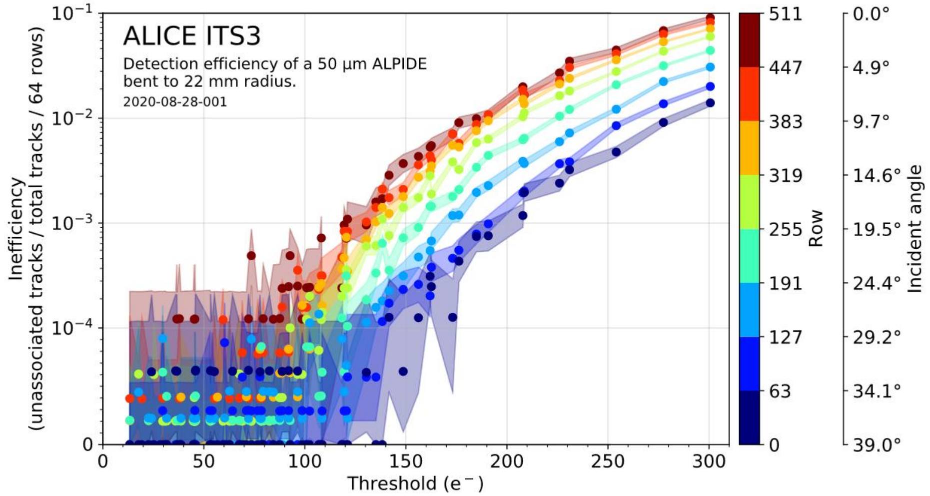
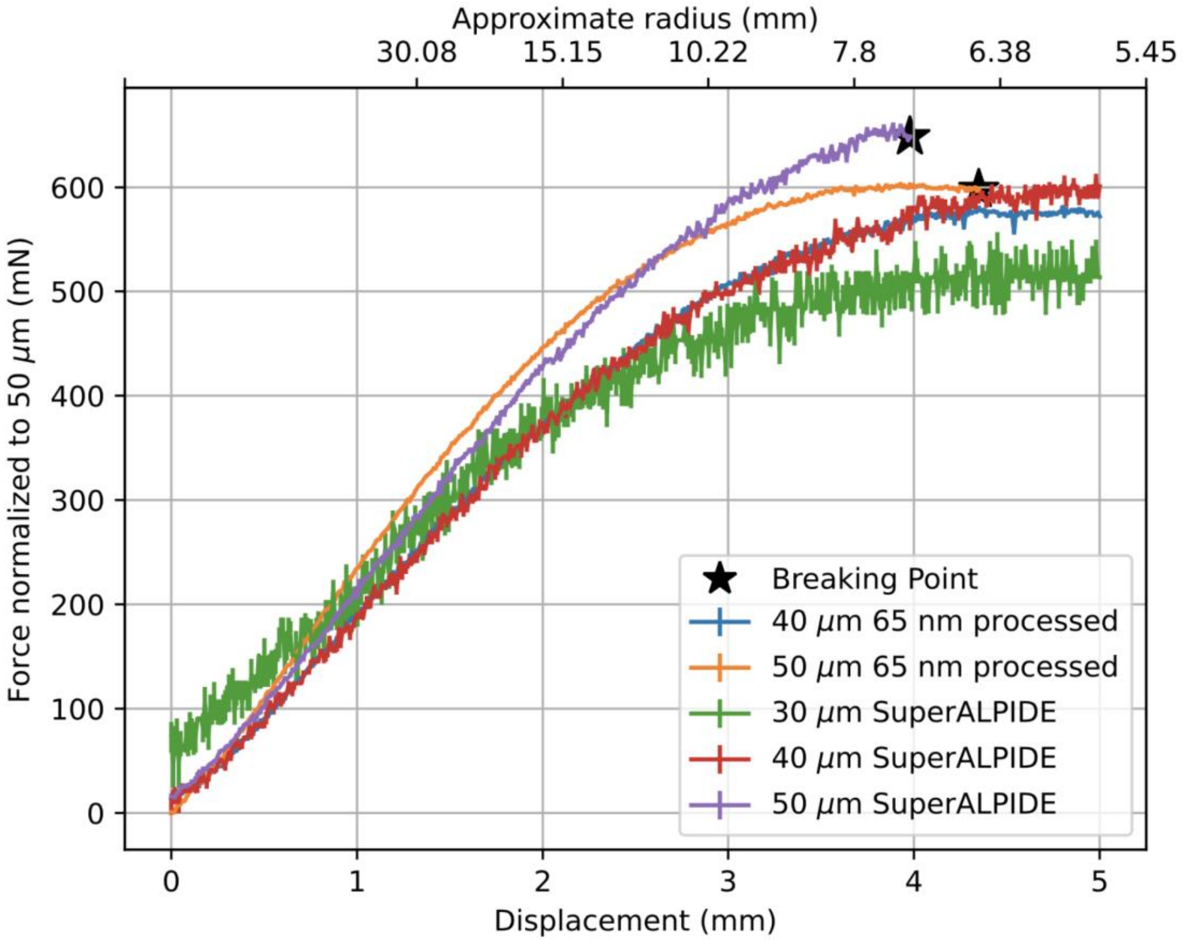


Figure 4.41: Setup for the bending strength measurements.





- Bent sensors pioneered by Alice ITS-3
- Idea: Develop a dedicated program for FCCee by bending sensor with MIMOSIS
  - ➢ e.g. functional tests @ R = 12 mm

Tower 180nm: MIMOSIS for CBM-MVD

Supported by
Bundesministerium für Bildung und Forschung
(05P19RFFC1)
This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

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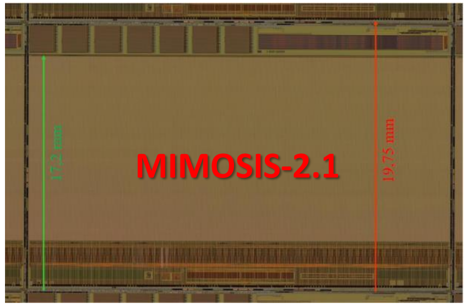
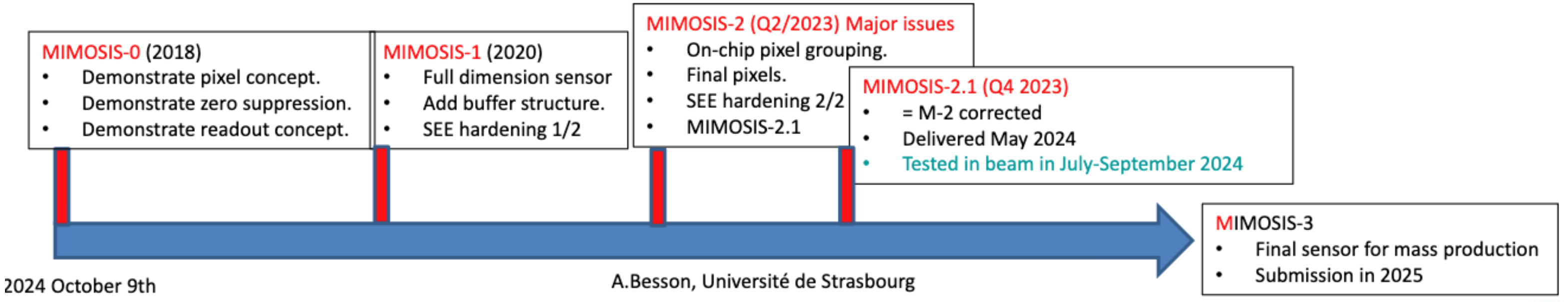
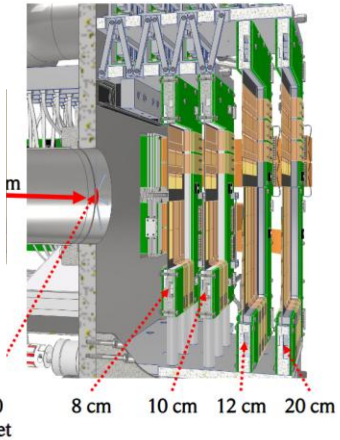
- Specifications (4 cm^2)
  - ✓ Based on ALPIDE architecture
  - ✓ Will equip the MVD of CBM@ FAIR
  - ✓ « 5µm - 5µs » + comparable flux to FCCee
  - ✓ Higgs factory demonstrator (closest sensor to specifications)
  - ✓ other applications considered (e.g. exp. FOOT, Integration tests)
- Timeline
  - ✓ 2023-24: Tests of Mimosis-2.1
    - Performances beyond requirements
  - ✓ Submission MIMOSIS-3 (final sensor): 2025/26
  - ✓ Will be used for bent sensor studies

Parameter	Value
Technology	TowerJazz 180 nm
Epi layer	~ 25 µm
Epi layer resistivity	$> 1k\Omega cm$
Sensor thickness	60 µm
Pixel size	26.88 µm × 30.24 µm
Matrix size	1024 × 504 (516096 pix)
Matrix area	≈ 4.2 cm^2
Matrix readout time	5 µs (event driven)
Power consumption	40-70 mW/cm^2

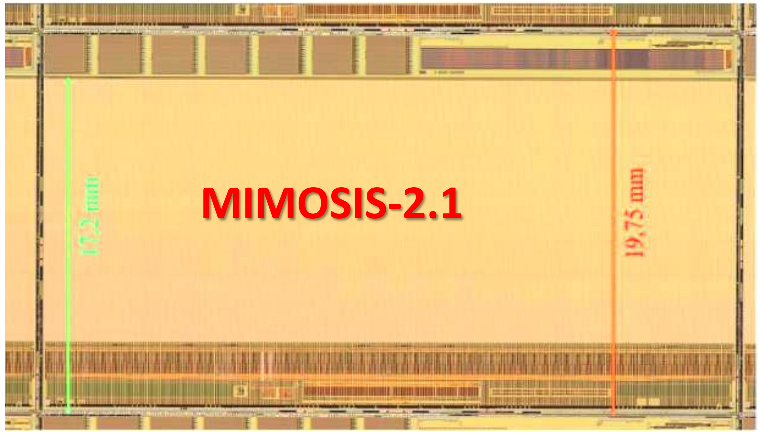


Physics parameter	Requirements
Spatial resolution	~ 5 um
Time resolution	~ 5 us
Material budget	0.05% X_0
Power consumption	< 100 – 200 mW/cm^2
Operation temperature	- 40 °C to 30 °C
Temp gradient on sensor	< 5K
Radiation tol* (non-ion)	~ 7 x 10^{13} n_{eq}/cm^2
Radiation tol* (ionizing)	~ 5 MRad
Data flow (peak hit rate)	@ 7 x 10^5 / (mm^{2}s) > 2 Gbit/s





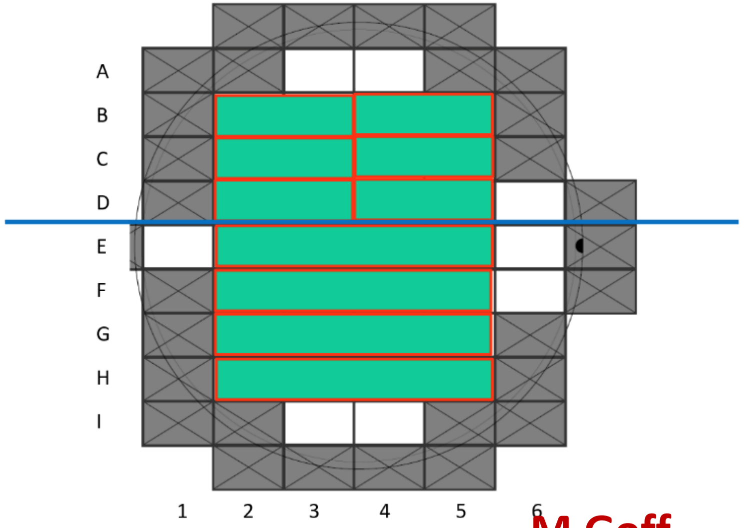
Toward curved Mimosis ladder



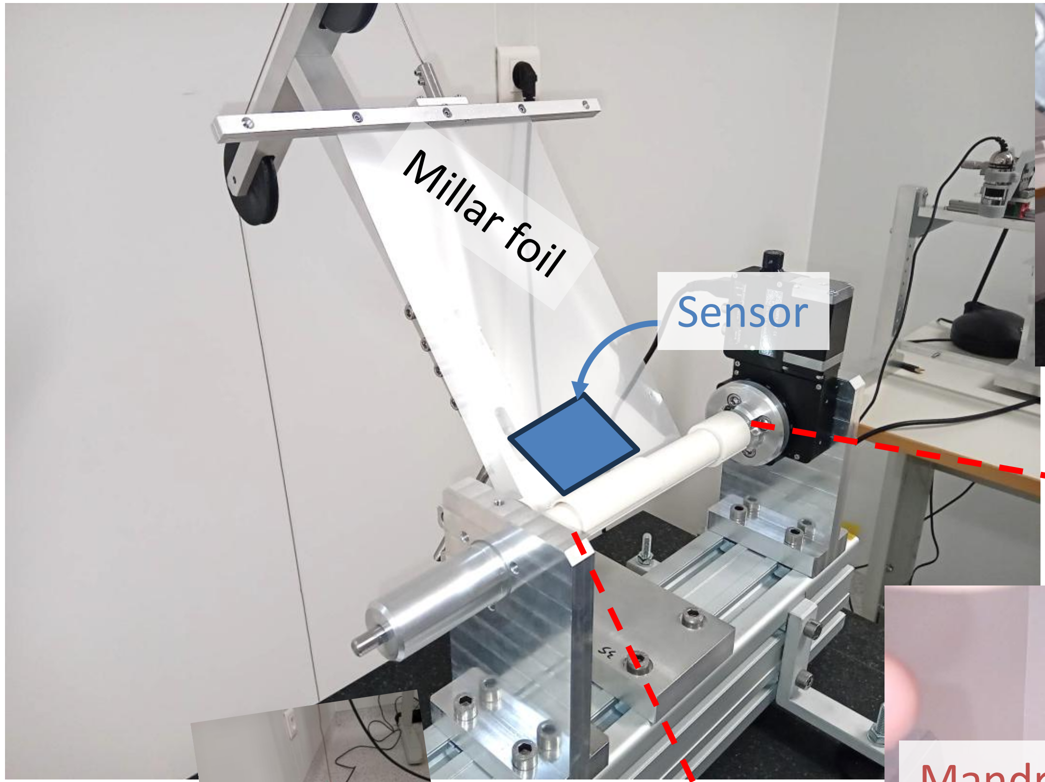
- Designs of FCC-SEED requires a gain of expertise in curved sensors. Many aspects to investigate, questions to answer.
  - ✓ To what minimal inner radius can we bend sensors ?
  - ✓ And for what sensors thickness ?
  - ✓ Does the bending change the chip performances ? Silicon properties ?
  - ✓ How to curve the sensors, and maintain the curvature ?
  - ✓ How to glue sensors on mechanical structure ?
  - ✓ How to make the bonding with curved sensors?
  - ✓ Etc… etc…

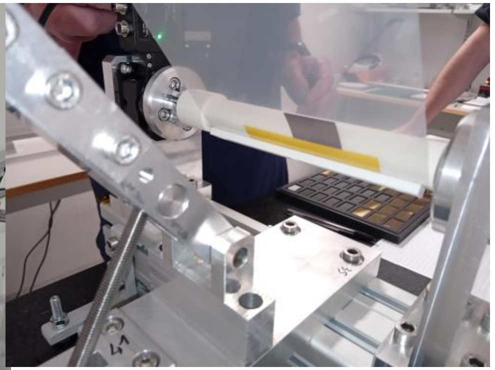
- Strategy/working plan.
  - ✓ Use existing and available chips : **Mimosis prototype versions**,
  1. Setup and practice sensors bending (different radii and different thicknesses), using sacrificial sensors,
  2. Bend single functional Mimosis, and tests them (lab, source, beam). Required flex and running DAQ,
  3. Bend a Mimosis ladder, integrated on simplified mechanical structure, tests,
  4. Design and realise a demonstrator/mock-up for the first FCC-SEED layer.

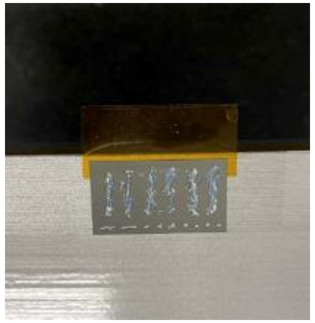
Cutting of Mimosis wafer

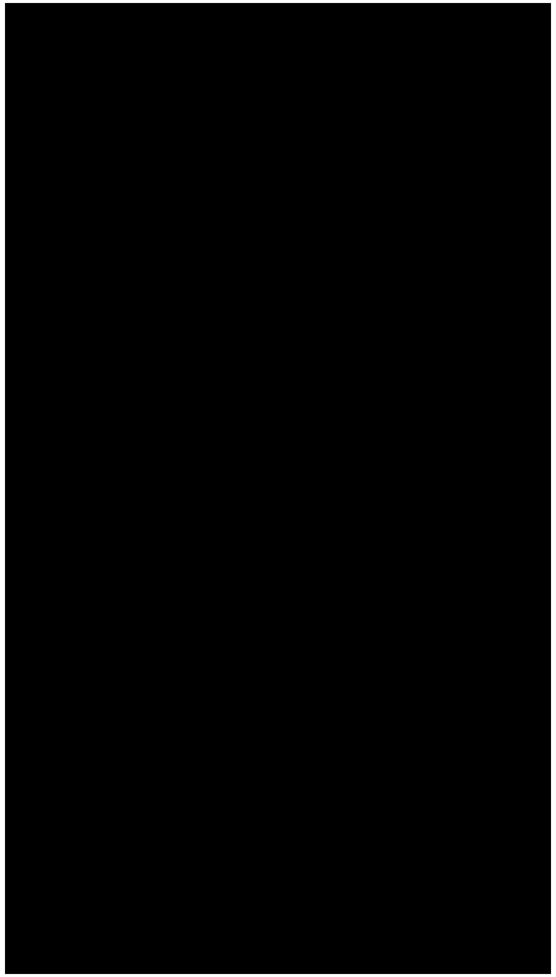


Sensor Bending

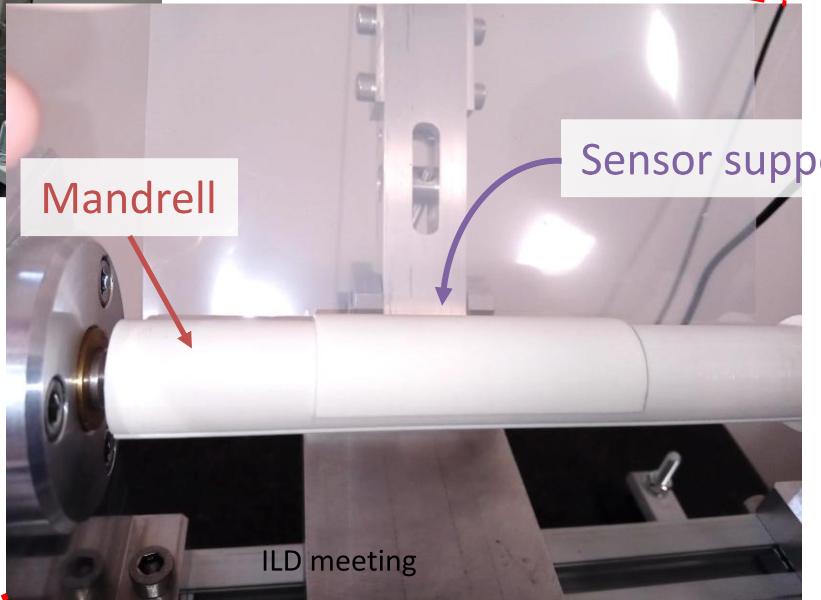








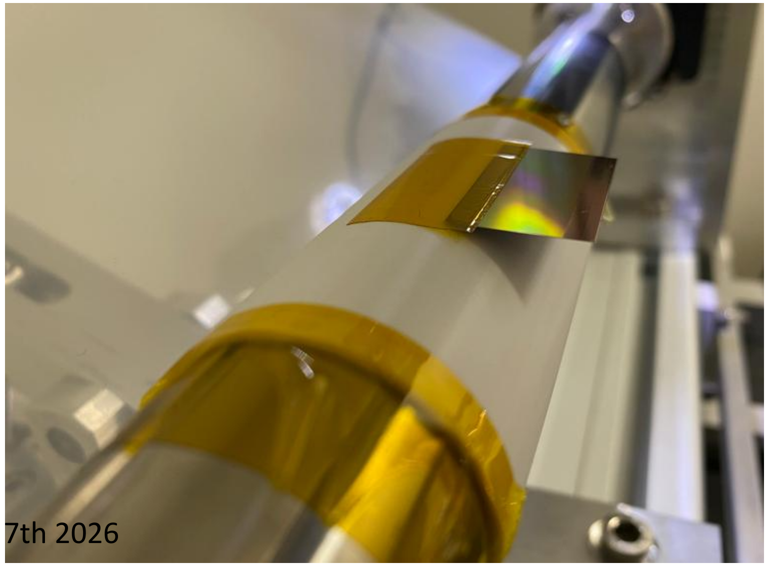
counterweight



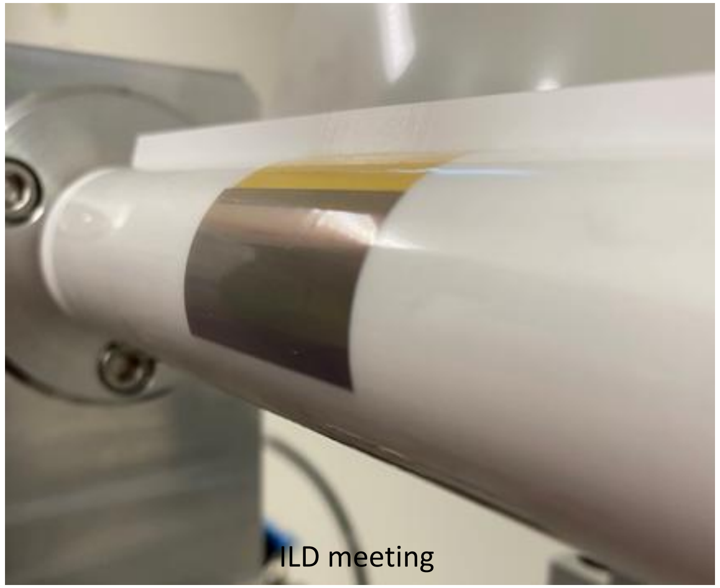
Toward functional bent Mimosis

- Several tests were performed, with different glue viscosities and glue doses.
- Methodology for bending and connecting sensors are defined and tested.
- Ready to glue and wire-bond a functional Mimosis for lab and beam tests (CYRCé then DESY).

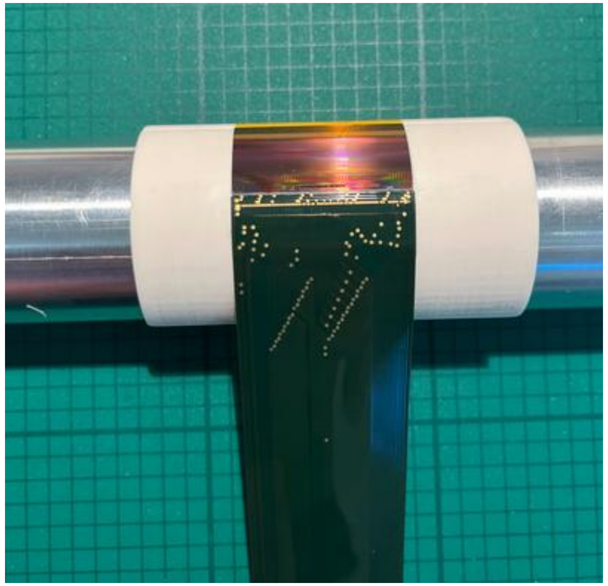
Sensor taping on the mandrel



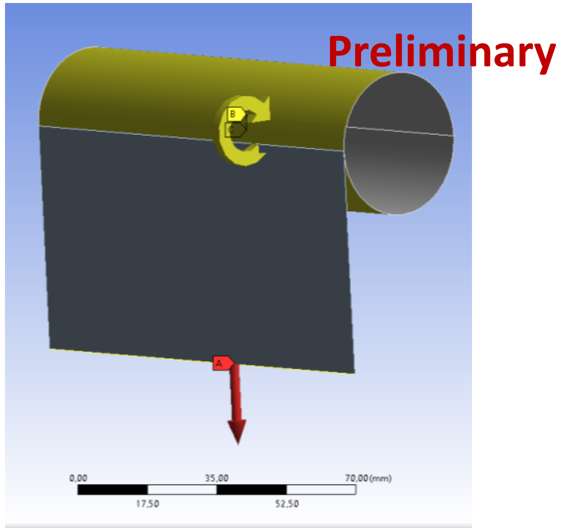
Sensor covered with Kapton foil, after rolling the Millar foil

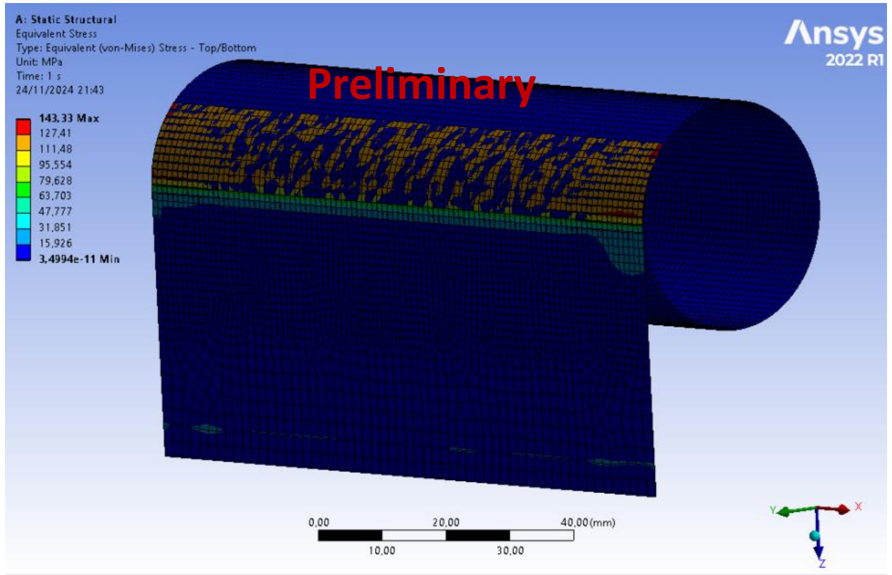


Curved sensor glued on it support, ready for bonding



Mecanical simulations





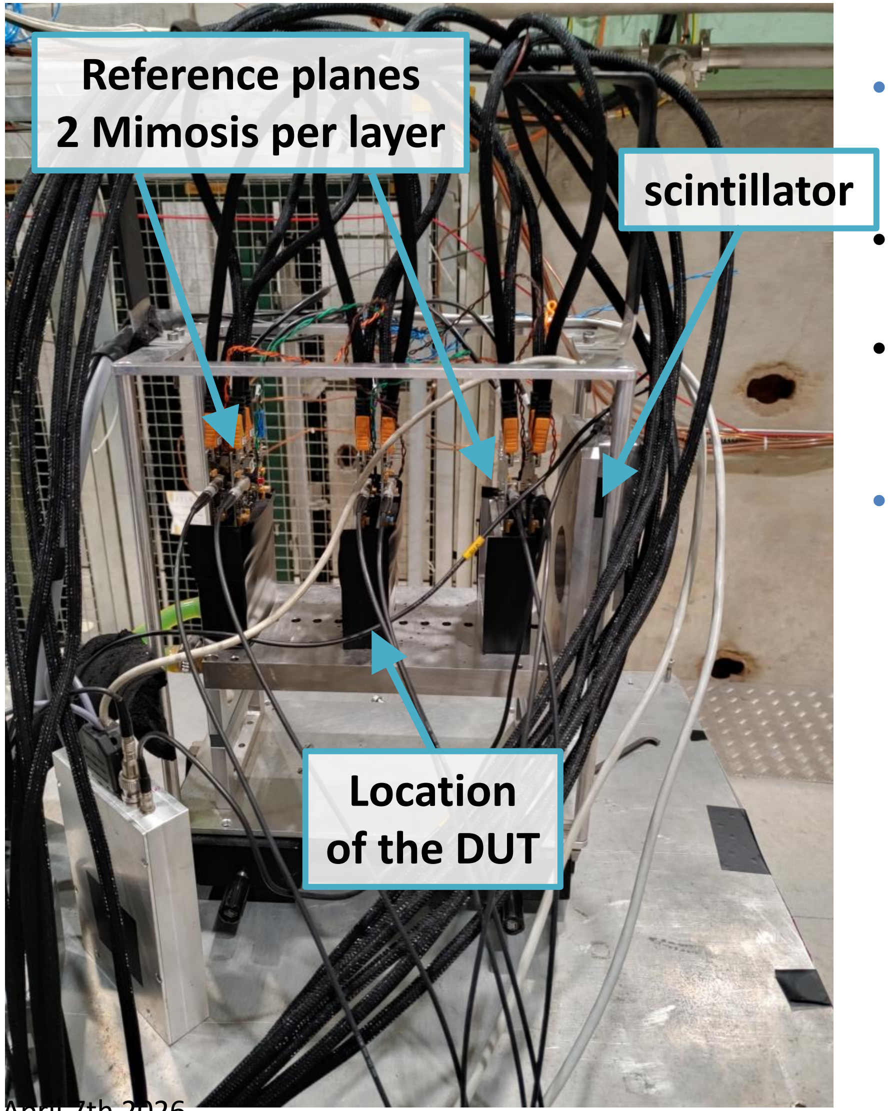
- Goal : simulate the bending of a silicon sensor, to determine the breaking points vs thickness and inner radius.

- Start with the modelling of a simple leaf of silicon, but mechanical characteristics of chips might be different :
  - ✓ Simulation of a complete chips might be difficult,
  - ✓ Considering measuring the mechanical characteristic of Mimosis and feed the simulation with the results.

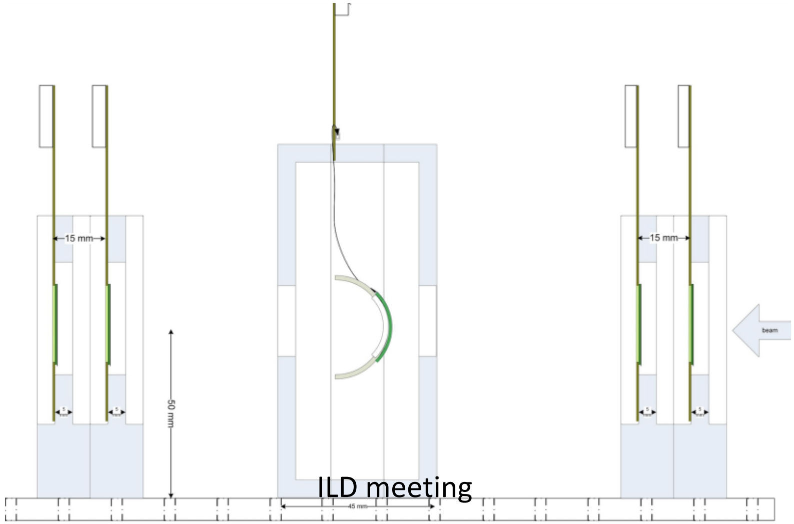
- Preliminary studies with ANSYS being performed, but much more work is needed.

- More simulations (thermo-fluidic) related to thermal aspects are also required.

Beam test preparation



- Testing with beams to be performed with a Mimosis-based telescope.
- Two layers with two Mimosis sensors each, sandwiching the Detector Under Test (DUT).
- Synchronisation "for free", uses same DAQ and software.
- Prior to test at DESY, testing of the sensors and telescope at the local IPHC cyclotron.
- Curved Mimosis supports and test box designed and fabricated.



MIMOSIS-2.1 features	
Spatial resolution	~5 µm
Time resolution	< 5 µs
Sensor thickness	~50 µm
Power dissipation	< 100 - 200 mW/cm²
Rate (average/50 µs peak)	20/80 MHz/cm²

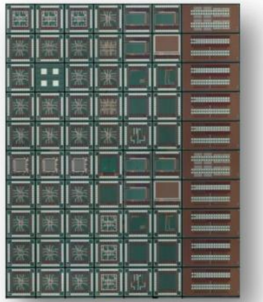
CMOS-MAPS R&D

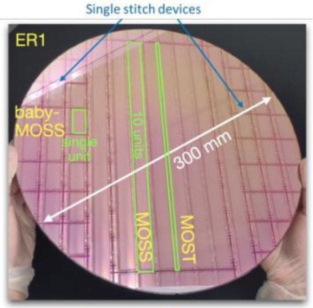
TPSCo 65nm in DRD3/DRD7 and ALICE

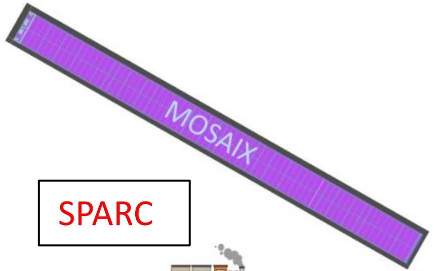
Timeline

W. Snoeys at DRD7 Week

EP R&D







SPARC

(OCTOPUS/MANTA)

MPR2 (2027)

Shared engineering run

WP 1.2 “rail”

ALICE “rail”

MLR1 (Multy-Layer Reticle, Dec 2020):

Learn about the technology, characterize pixels, transistors and building blocks

1.5 x 1.5 mm^2 test chips

>50 chiplets from: DESY, IPHC, RAL, NIKHEF, CPPM, Yonsei, CERN

ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

MOSS (1.4 x 25.9 cm)

MOST (0.25 x 25.9 cm)

Hybrid-To-Monolithic (H2M)

51 chiplets from: DESY, IPHC, RAL, NIKHEF, SLAC, INFN, CERN

ER2 (August 2025):

Full-scale stitched sensor prototype for ALICE ITS3

MOSAIX (1.9 x 26.6 cm)

~30 chiplets from: IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN

Submitted, approved for mask making, masks ordered, wafers not yet in the line.

ER3 (2026):

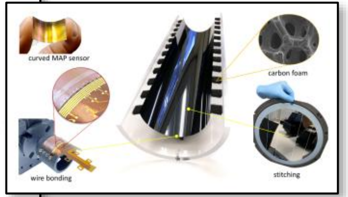
Stitched sensor production for ITS3 (ALICE-specific)

- OCTOPUS
  - ✓ Vertex for e+e-
- MANTA
  - ✓ Outer trackers

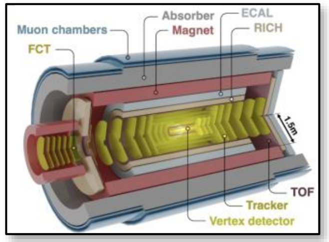
(OCTOPUS/MANTA) v2

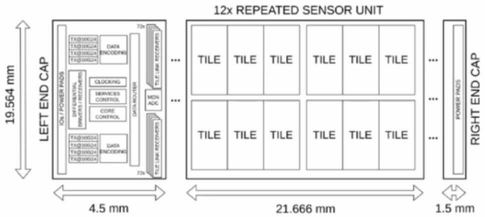
MPR3 (~2028-29)

ALICE ITS-3



ALICE-3





- Tape-out : 2025-07-14
- Delivery : 2026-01/02
- Pad Wafers : ≈2025-11-26

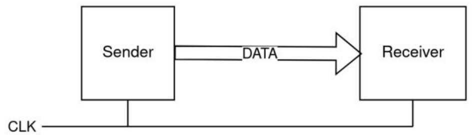
(i.e. MOSAIX, babyMOSAIX + chiplets)

SPARC sensor (IPHC, IRFU)

- SPARC 1st prototype for asynchronous readout
  - ✓ Asynchronous Priority Arbiters (APA)

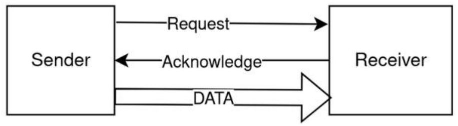
Synchronous

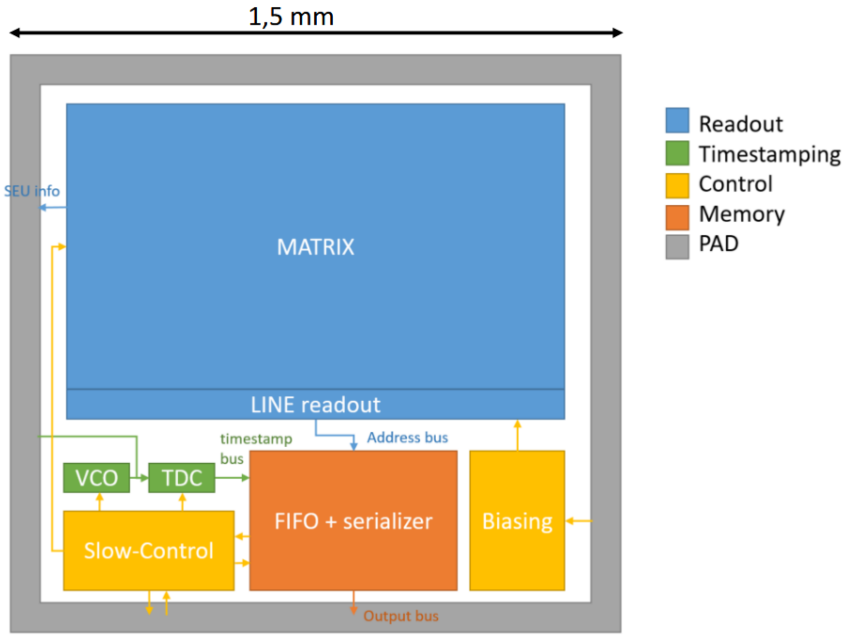
Data are read at regular intervals, synchronized to a common clock running at a specific frequency



Asynchronous

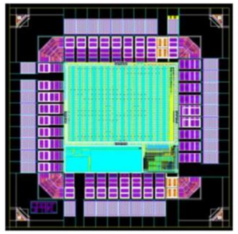
Data are read immediately when they become available through a handshake protocol



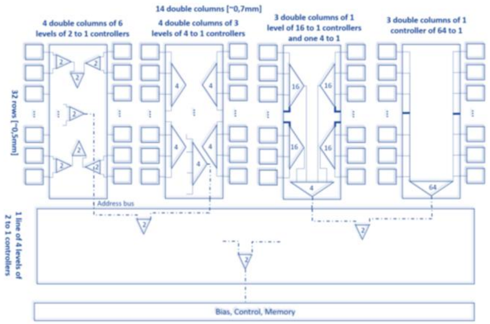


readout

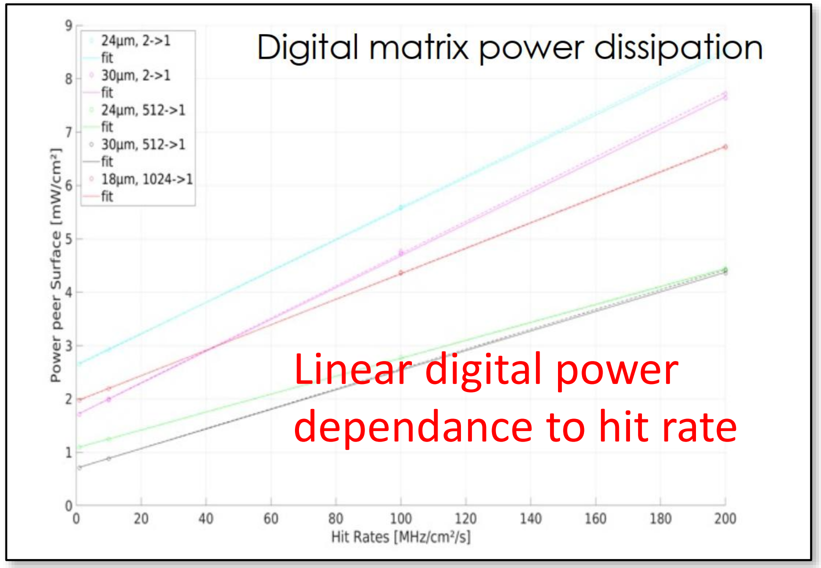
- Pixel matrix: 32 × 28
- Pixel pitch: 24 × 16 μm²
- Pixel front-end: DPTS-like (CERN)
- FPA tree types: 2:1, 4:1, 16:1, 64:1
- Power dissipation: 5 mW/cm²
- Mean readout time: 6.3 ns
- Designed by: IPHC, IRFU
- Submission: summer 2025 (ER2)
- Test system in preparation for 2026



1.5×1.5 mm²



S. Senyukov (CNRS-IN2P3-IPHC) Second FCC Italy & France workshop (5 Nov 2024) 10



Back from foundry end 2025 ⇒ to be tested in 2026 by group of partners (Belle-2, OCTOPUS, etc.)

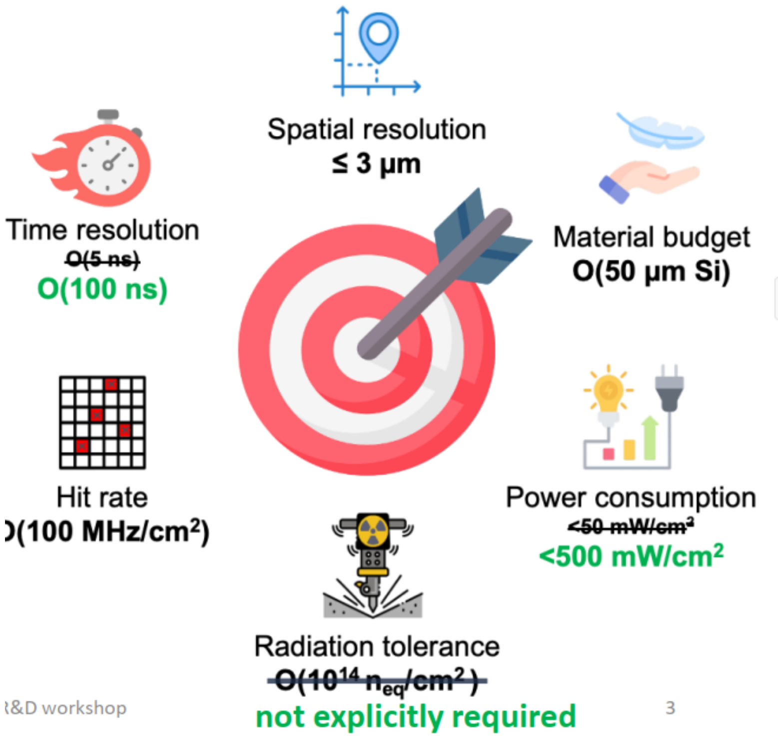
https://octopus.web.cern.ch/

DRD3: Octopus project

Coordinators: S. Spannagel *(DESY)*, D. Dannheim *(CERN)*

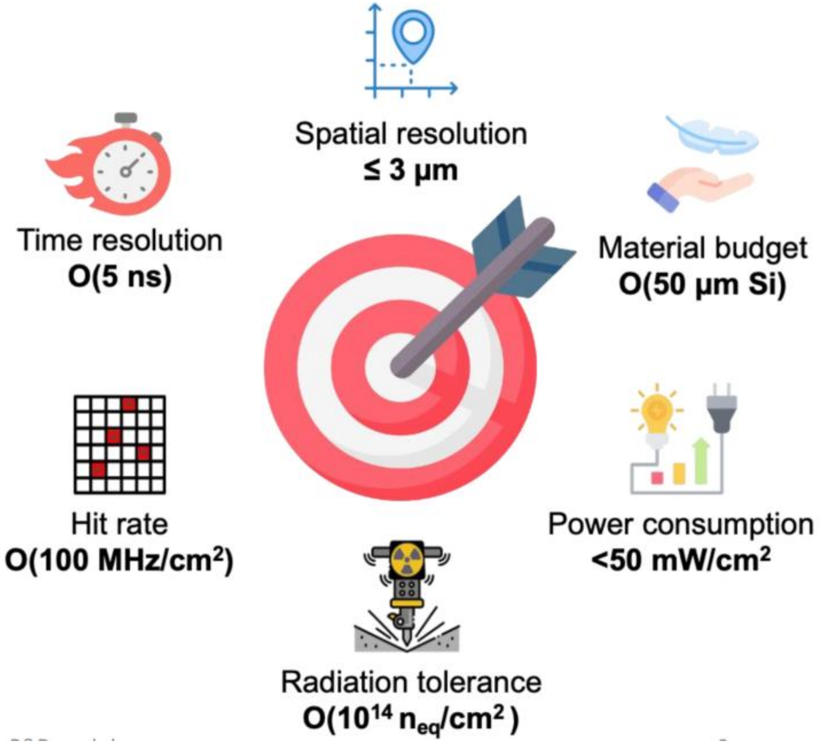
contact email: drd3.octopus@cern.ch

WP1: Simulations	WP2: ASIC design	WP3: Data Acquisition	WP4: Testing and characterization
A. Ilg, A. Velyka	F. Guezzi, L. Huth, S. Senyukov	Y. Otarid	F. King, M. Franks



Intermediate goal
(beam telescopes)

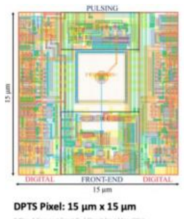
Institute	Main areas of contribution
APC Paris	Simulations, testing
University of Bonn	ASIC design, testing
CPPM Marseille	ASIC design
NIKHEF	Testing, DAQ
CERN	Testing, DAQ, ASIC design support
DESY	ASIC design, testing, DAQ, simulations
ETH Zurich	ASIC design, testing
CTU Prague	ASIC design, DAQ, testing
GSI Darmstadt	Simulations, testing
MBI Vienna	DAQ, testing, ASIC design
IPHC Strasbourg	ASIC design, testing
University of Oxford	Powering, integration, testing
University of Zurich	Testing, DAQ, simulations

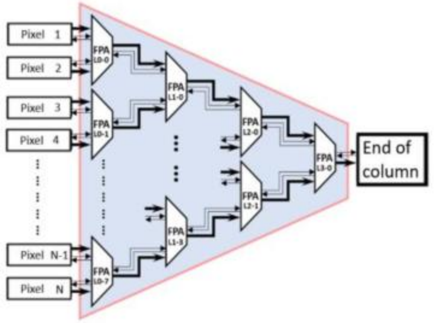


Final goals

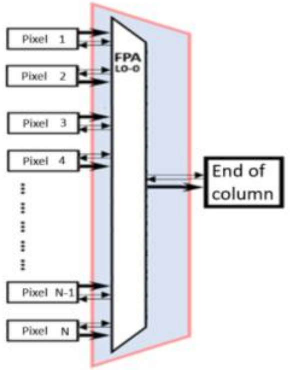
OCTOPUS Asynchronous read-out

- Front-end from DPTS/MOSS (ALICE-ITS3)
  - ✓ Compact footprint
- Asynchronous Priority Arbiter from SPARC
  - ✓ Architecture shared with MANTA
  - ✓ Pixel pitch optimization
- Readout
  - ✓ Various options of column merging under study
  - ✓ In chip lpGBT logic
  - ✓ Expected data rate 10 Gb/s/cm^2
- Time stamp
  - ✓ Rising / falling edge
  - ✓ Time stamping via TDC end of column (ToA + ToT)
  - ✓ Time walk correction
  - ✓ ToT used for charged measurement ⇒ spatial resolution

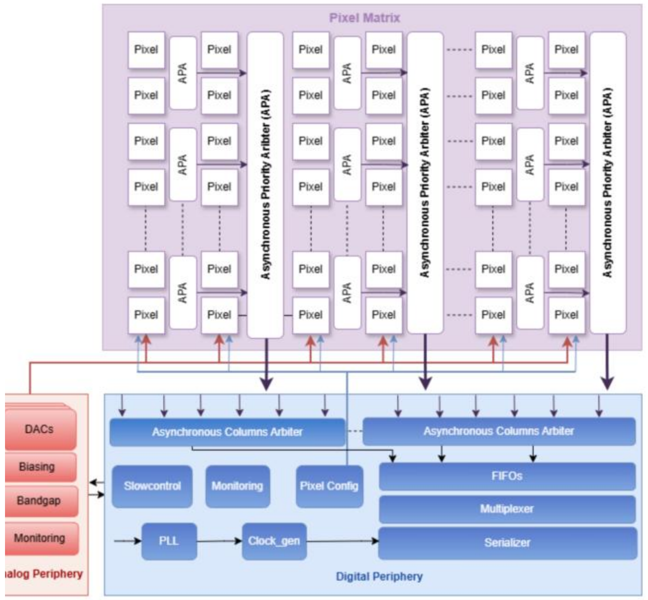


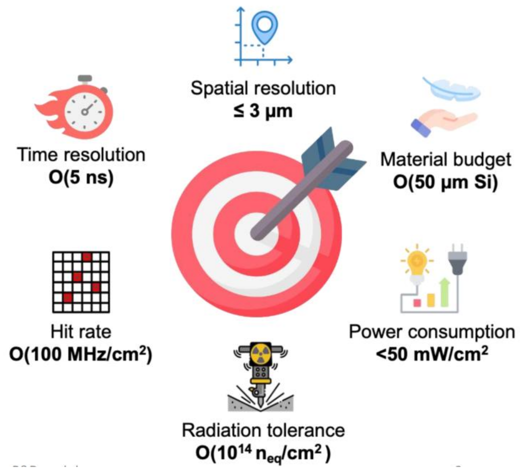


Bandwidth ↑
Footprint ↓



Bandwidth ↓
Footprint ↑





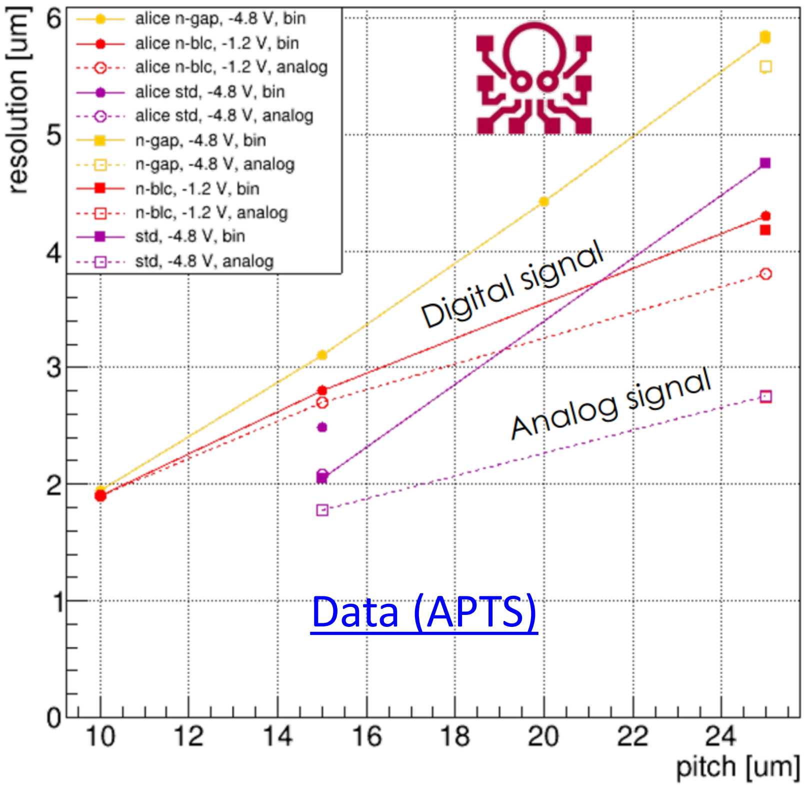
OCTOPUS: coherent and staged program to reach VTX requirements

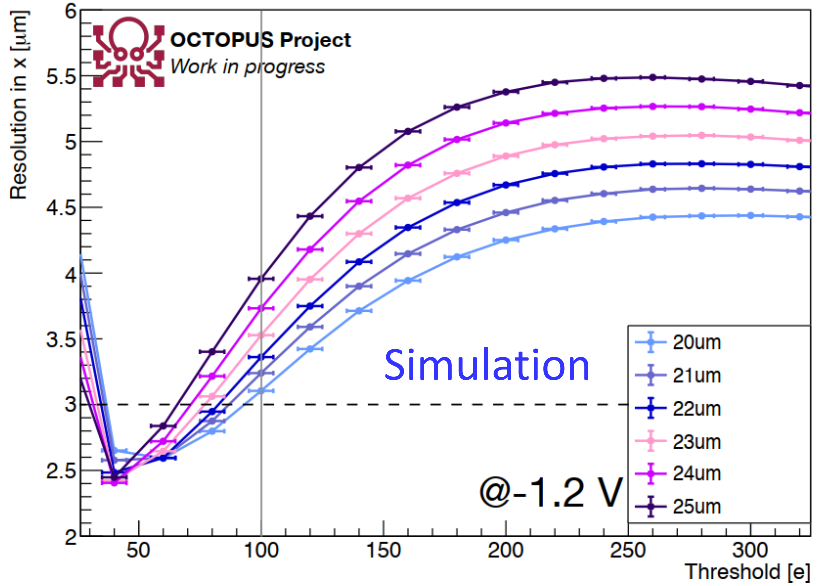
Simulations

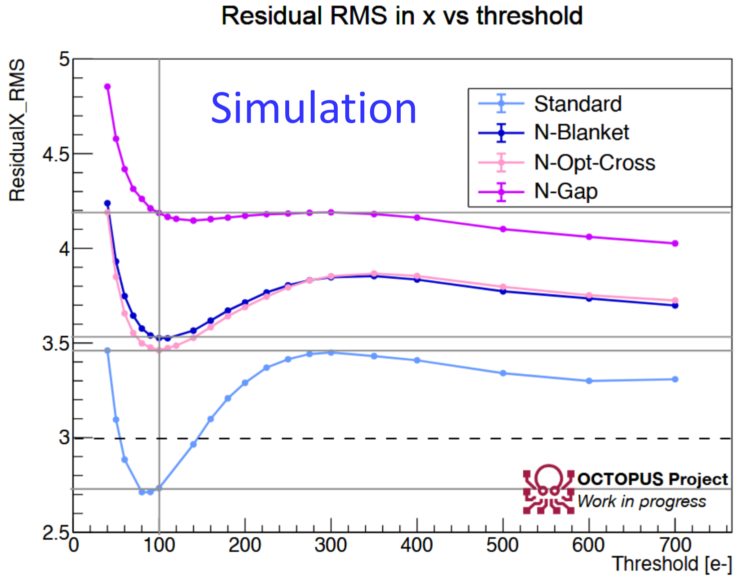
Octopus: the spatial resolution challenge

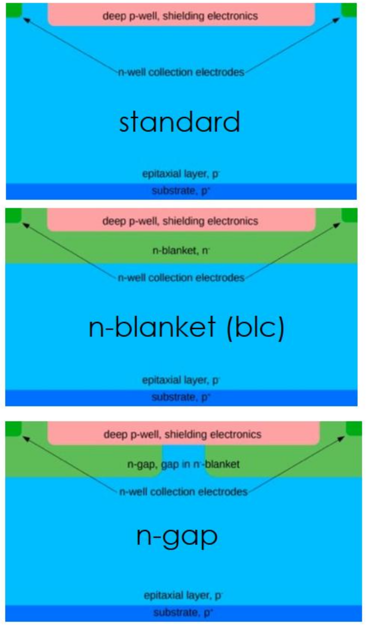
Taken from Russo et al. More details here (DRD3 week)

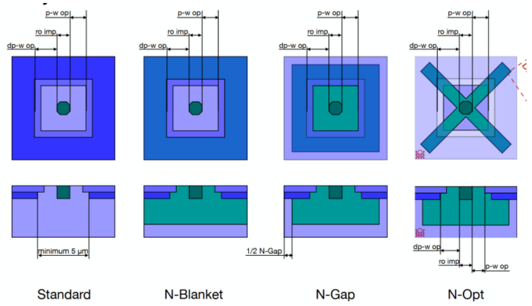
Geo	Process	Pitch(um)	HV(V)	Sp. Res.(um) (telescope resolution subtracted)
SQ	GAP	22.5	10	~5.1
SQ	GAP	18	10	~4.1
SQ	GAP	15	10	~3.2
SQ	STD	22.5	10	~2.4
SQ	STD	18	10	~1.8
SQ	STD	15	10	~1.3







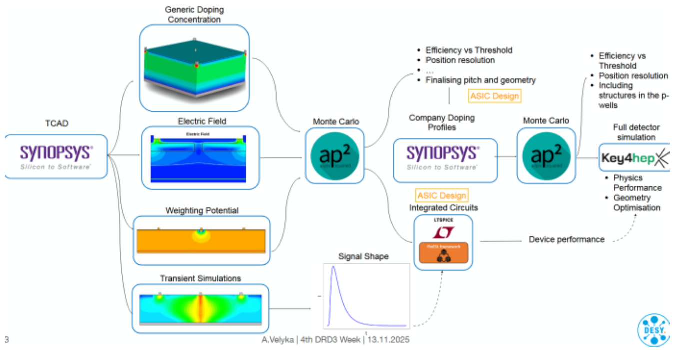


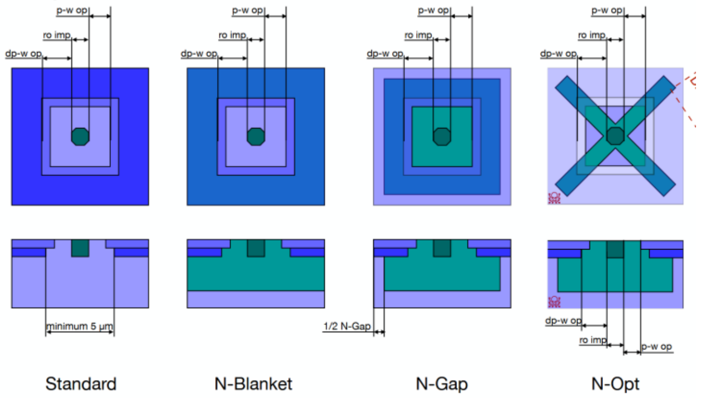


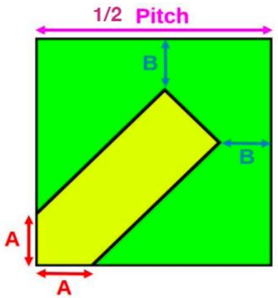
Goal :
optimize the design to guarantee 3 μm spatial resolution
vs efficiency and pitch

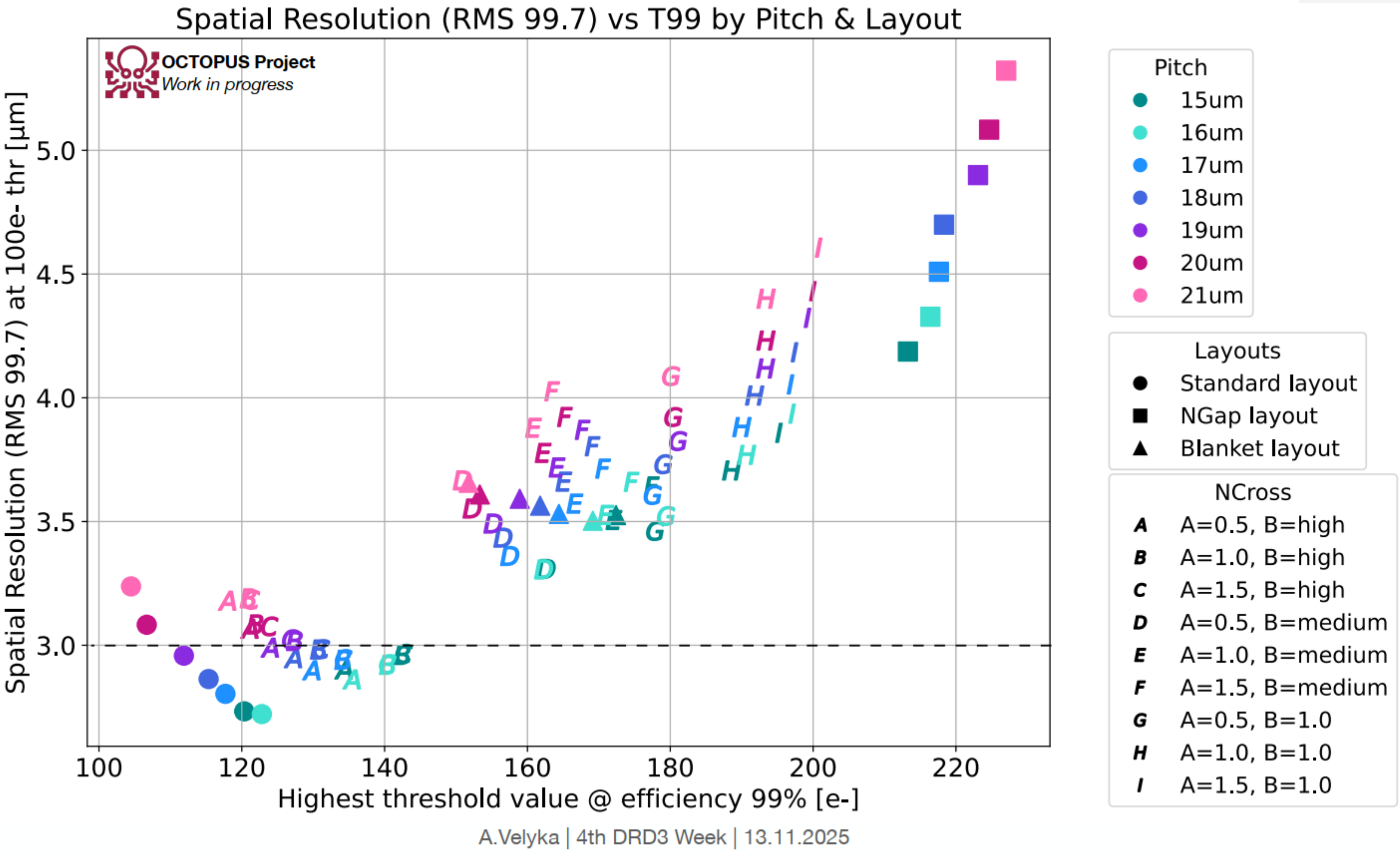
OCTOPUS: Spatial resolution optimization

- [See Velyka (DRD3)](#)

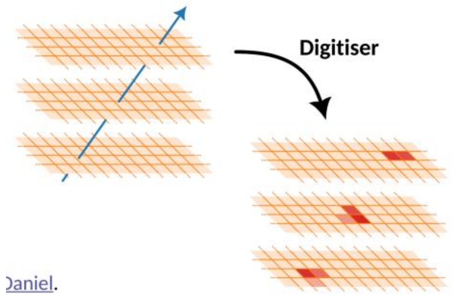








Idea: improve the homogeneity of the response



LUT for a digitizer and Beam background studies

Jona Dilg[1], Ono Feyens[2], Armin Ilg[1], Simon Spannagel[2] and Anastasiia Velyka[2]
[1]University of Zurich, [2]DESY. Contact: jona.dilg@cern.ch

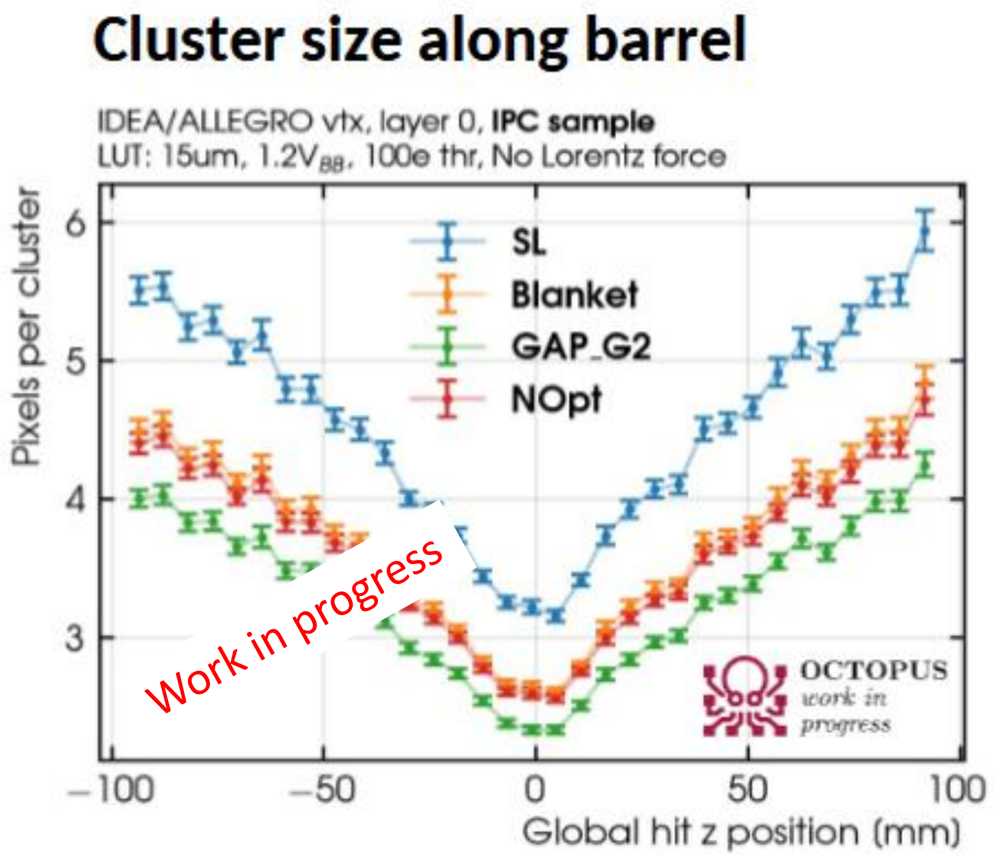
Universität Zürich[UZH]

More details here

- Builds upon work in Allpix2 done in ALICE and by C. Lemoine (CERN & IPHC Strasbourg)

- Digitizers:
  - ✓ Smearing with gaussian
  - ✓ Technology-agnostic approach (G. Boudoul, J. Daniel)
  - ✓ Lookp Up Table inspired from ATLAS & CMS
- Caveat:
  - ✓ Timing information not easy
- Caveat on BX frequency
  - ✓ 25 ns down to 5-10 ns ? See here

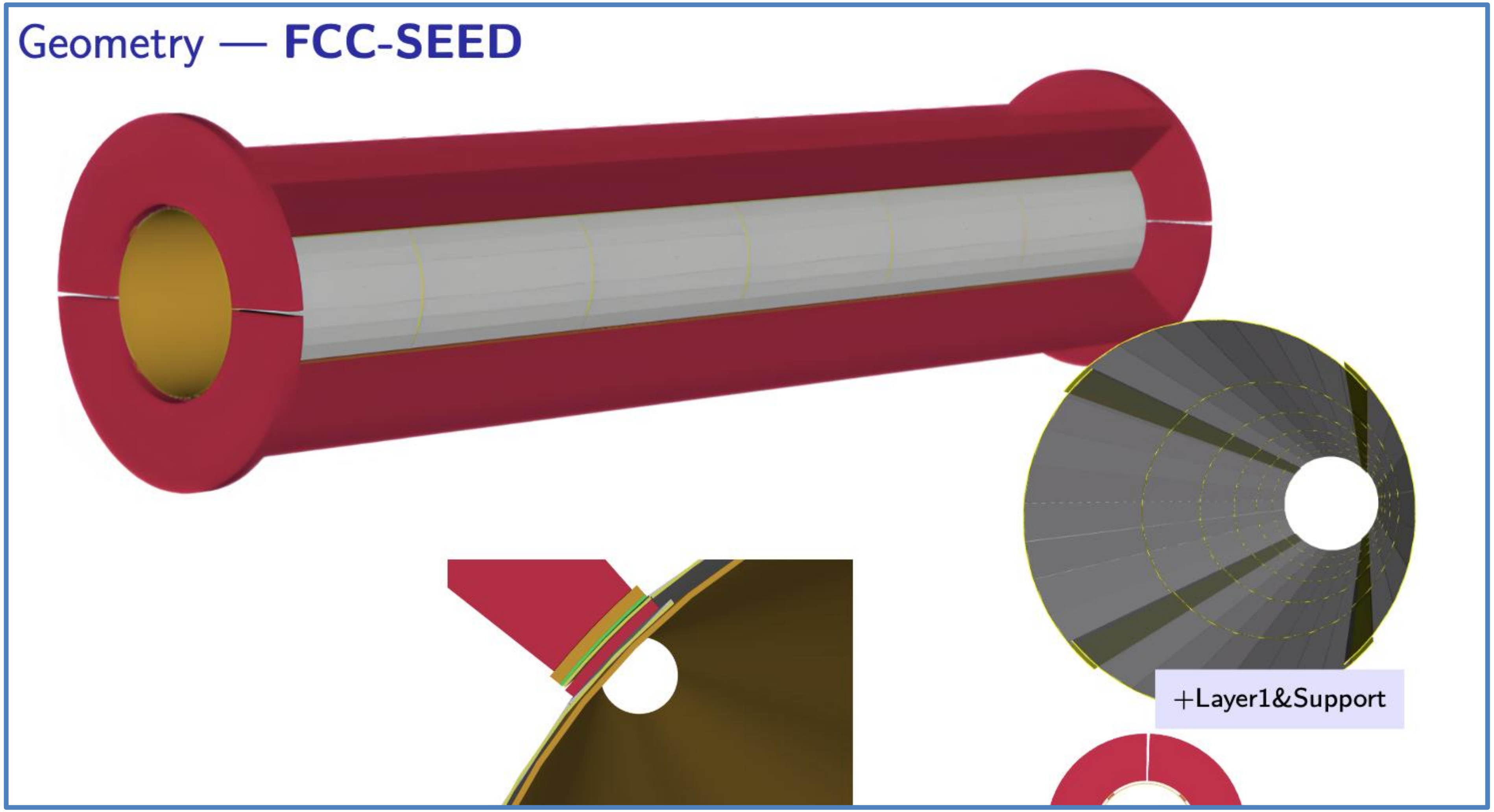
SYNOPSYS ⇩ ap² allpix squared ⇩ Key4hep



Key message: Assuming 5 pixels per cluster seems conservative enough

Full simulation: Implementation of the FCC-SEED barrel geometry

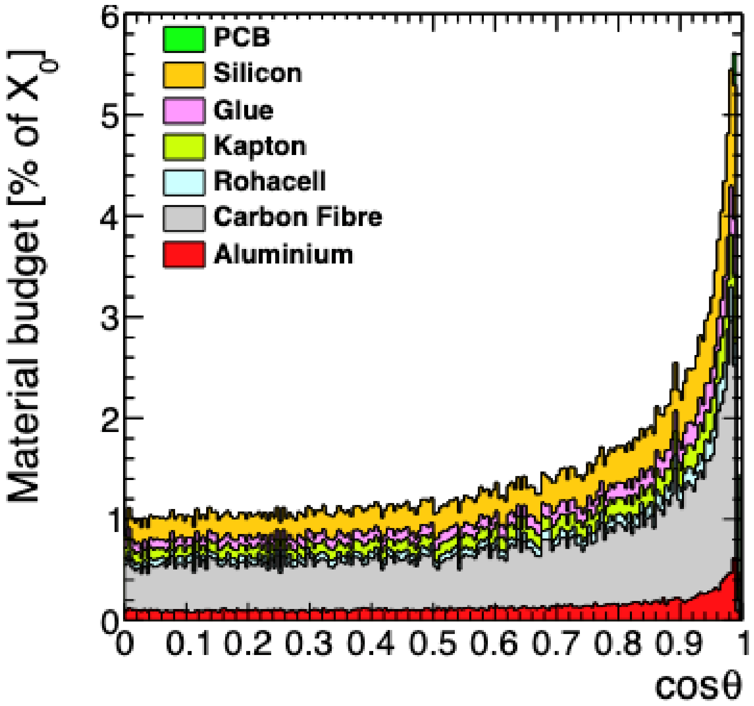
Slide taken from Armin Ilg, Mohamed Ahmed link



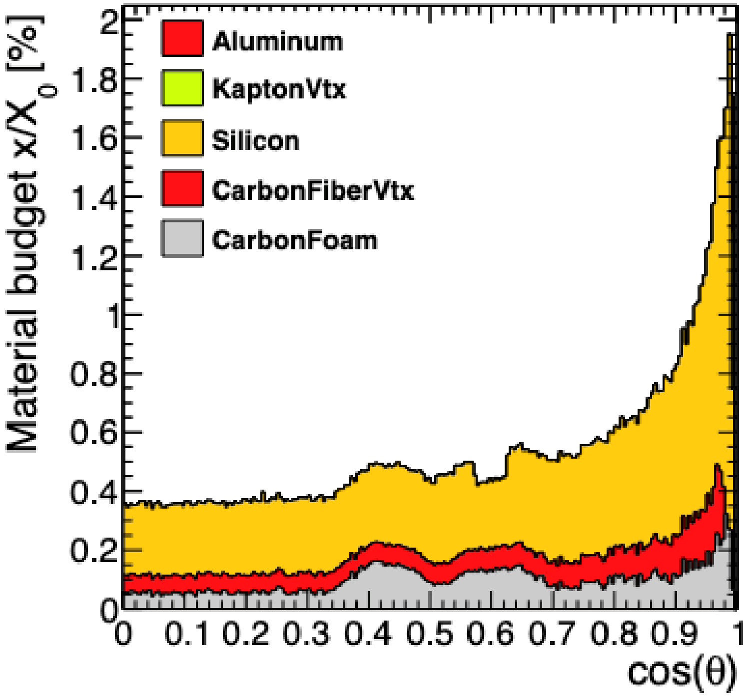
- Mechanical studies ongoing to
    - Design lighter mechanical supports,
    - Study assembly and integration,
    - Design the overall interface with MDI,
    - Design the cooling system (with air),
    - Test different material for the supports,
    - Etc…
- Very significant design work, but **requires mechanical realisations : prototyping !**

Full simulation: comparisons of material budgets

Armin Ilg, Mohamed Ahmed @ Detector Concept meeting: link

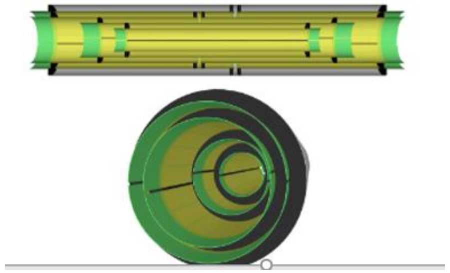


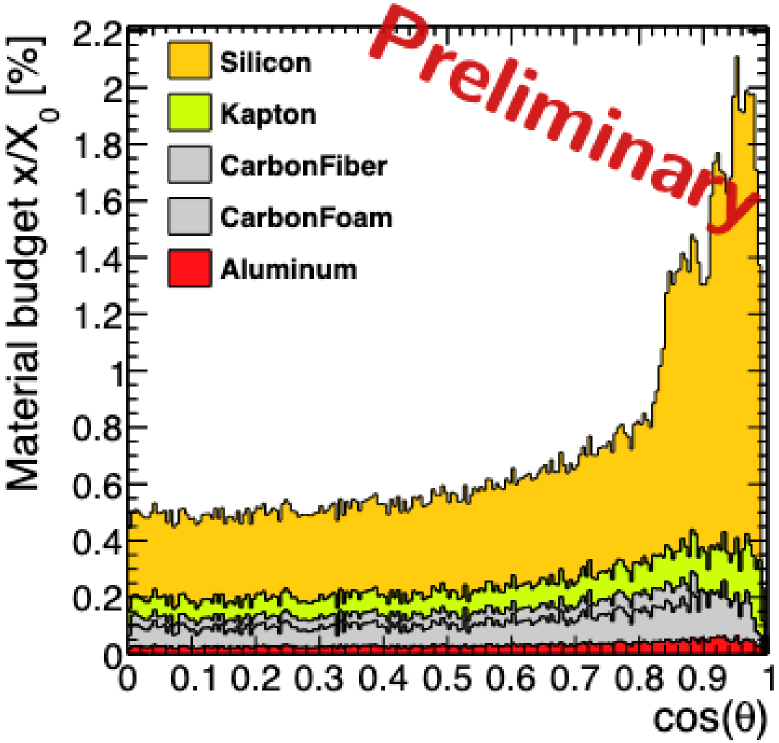
Classic



Ultralight

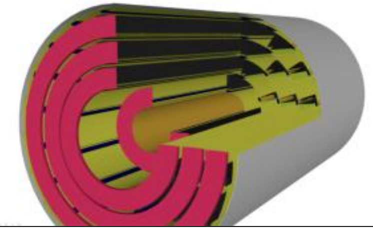
(ITS3 like adapted to IDEA)





FCC-SEED

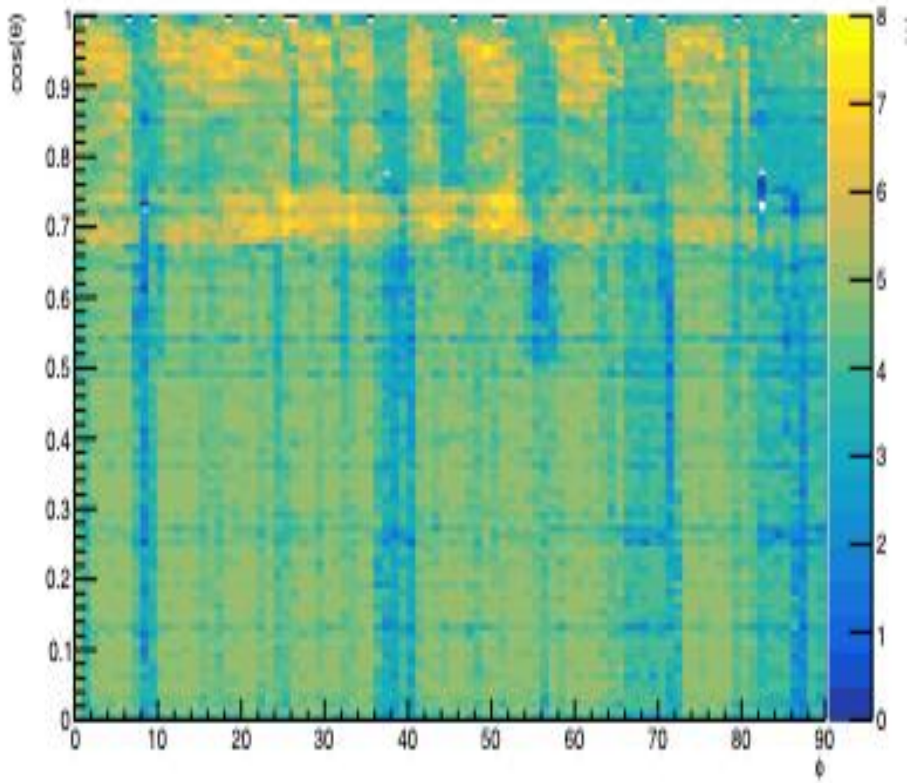
(readout & support material implemented)



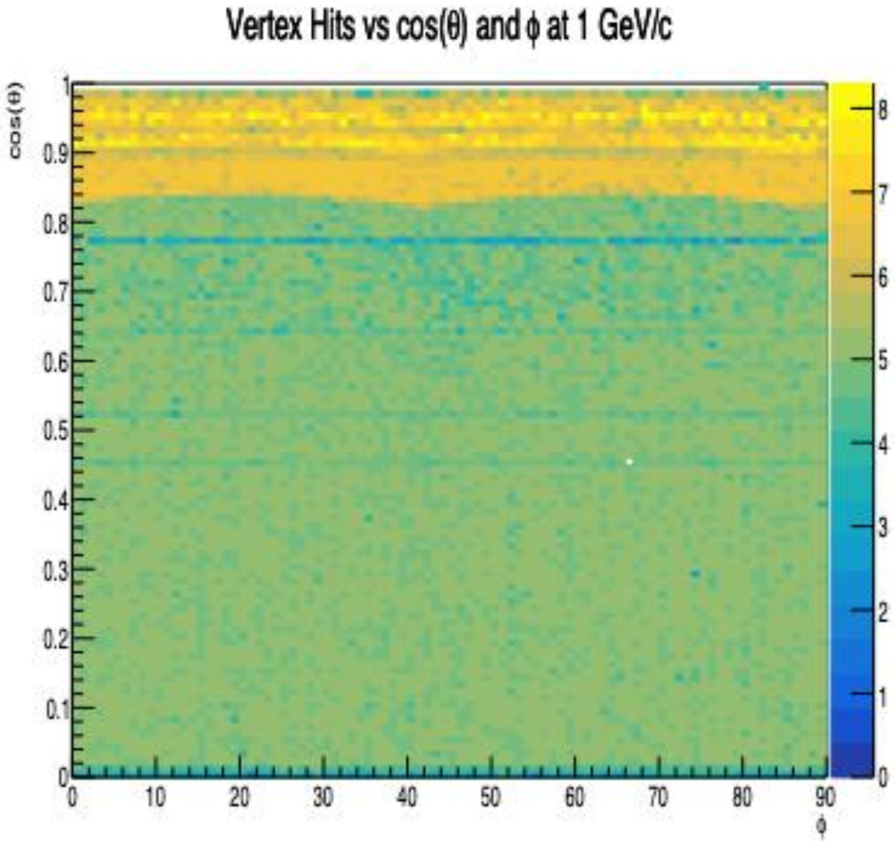
Only the FCC-SEED Barrel is new, endcaps from CLD detector !

Full simulation: Hit distribution and acceptance coverage

Armin Ilg, Mohamed Ahmed link



Ultralight

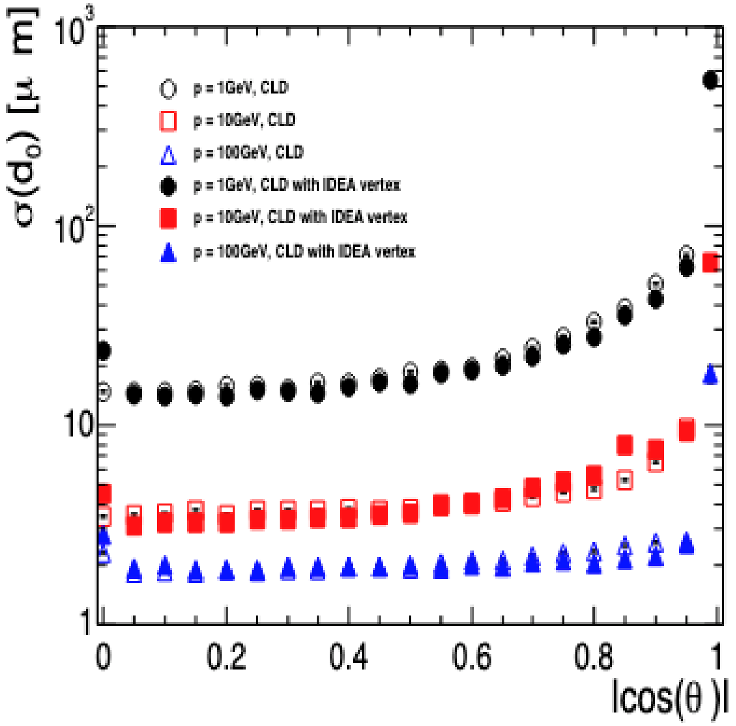


$1\ GeV/c$ FCC-SEED

FCC-SEED shows an hit acceptance, with a large majority of tracks having 5 hits in the Vertex detector

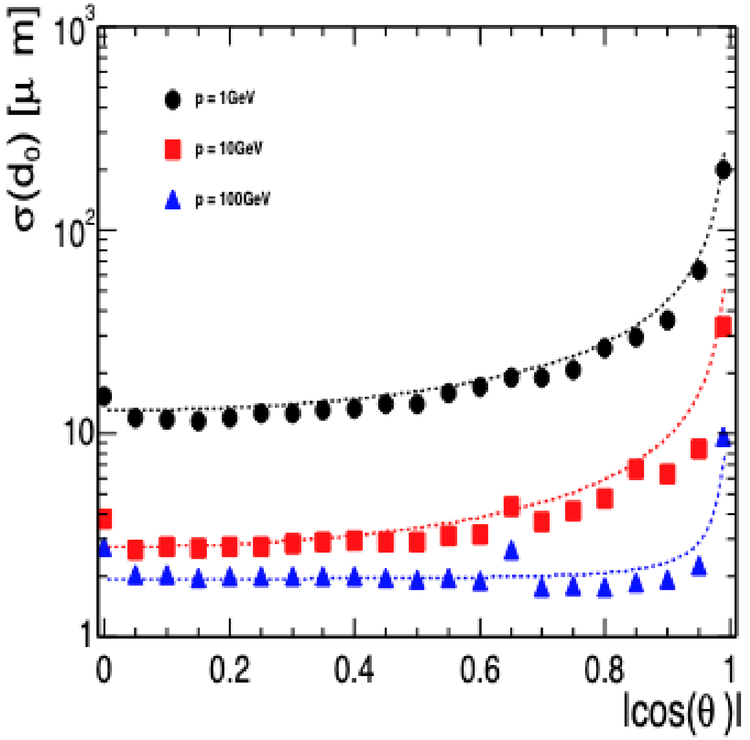
Full simulation: Impact parameter resolution (σ_{d0} resolution)

Armin Ilg, Mohamed Ahmed link



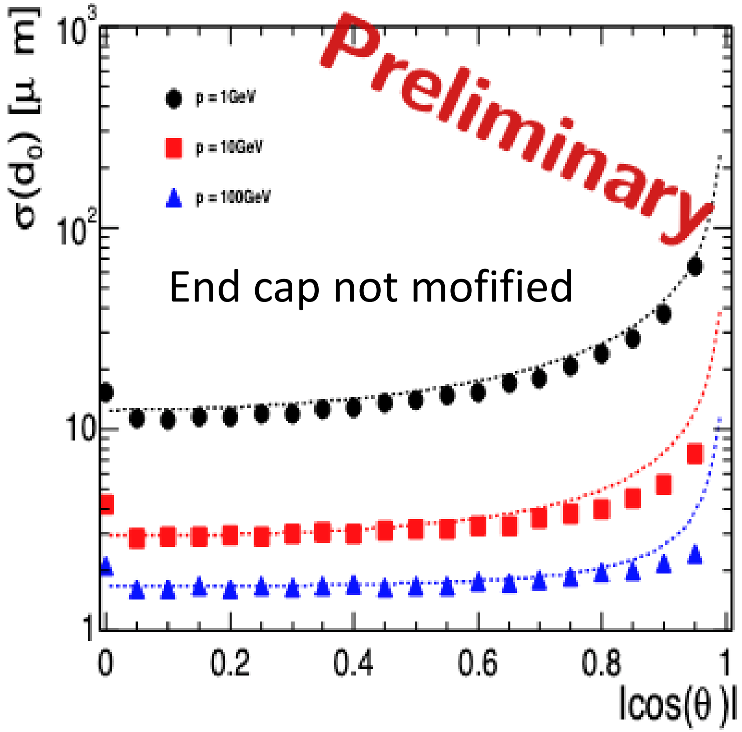
Classic

- 1 GeV: $\sim 14.6\ \mu m$
- 10 GeV: $\sim 3.5\ \mu m$



Ultralight

- 1 GeV: $\sim 11.8\ \mu m$
- 10 GeV: $\sim 2.9\ \mu m$



FCC-SEED

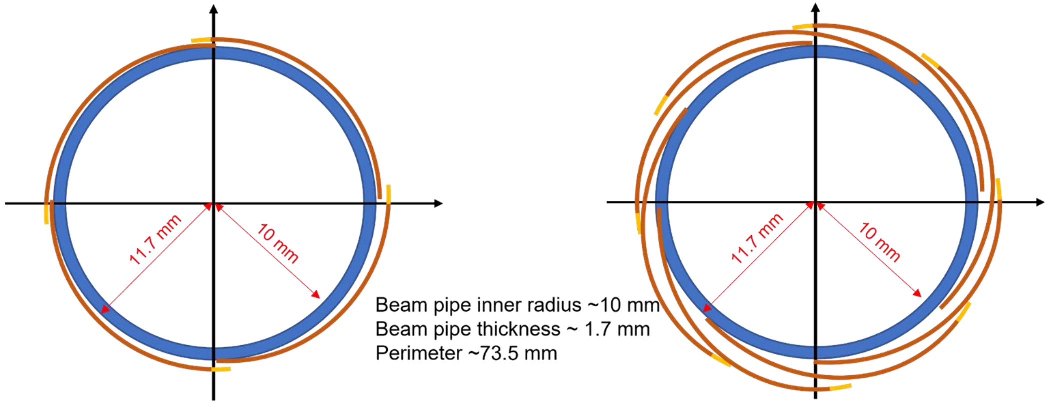
- 1 GeV: $\sim 11.1\ \mu m$
- 10 GeV: $\sim 2.9\ \mu m$

Despite slightly higher material budget, best performance observed for FCC-Seed => almost always 5 hits per tracks.

Summary

FCC-SEED
VERTEX DETECTOR FOR FCC-ee

- FCC-SEED is a vertex detector concept for FCCee
  - ✓ Based on bent sensors to optimize inner radius & material budget
    - keeping robustness, flexibility & redundancy
  - ✓ Based on CMOS sensor R&D
    - via DRD3/7 (OCTOPUS, MANTA, CASSIA)
  - ✓ Connected to simulation studies (Full simulation, beam background, digitizer, etc.)
  - ⇒ Coherent devpt to progress in parallel on every aspects

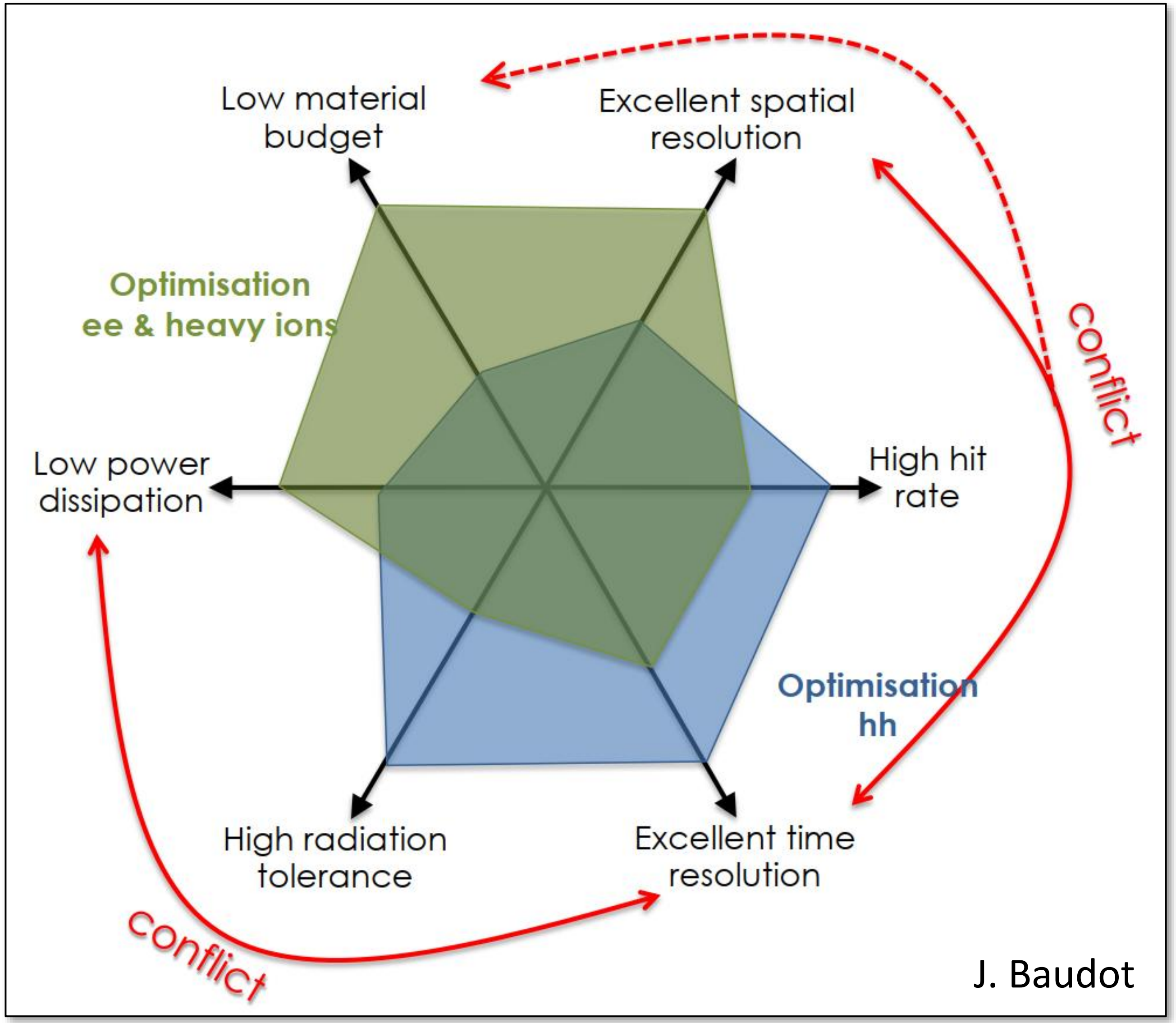


- Agnostic approach w.r.t the detector concept
  - Outer radius & discs not frozen.

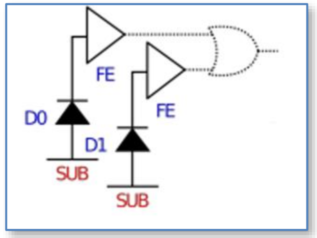
- People willing to join are welcome
  - ✓ (contact: Jeremy Andrea)

Back up

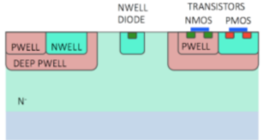
Conflicting parameters

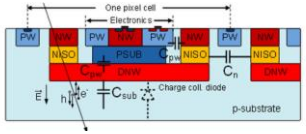


Main axis of R&D

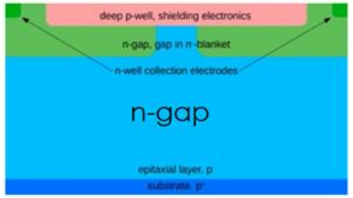


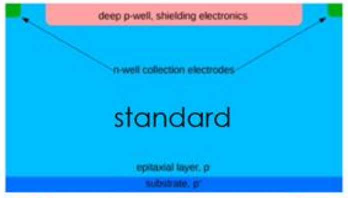
- Smaller features sizes
- Small diodes / large diodes

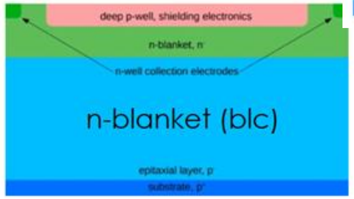


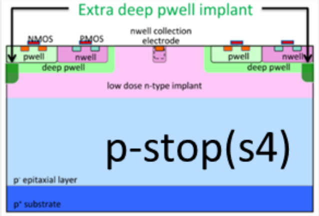


- Sensitive volume



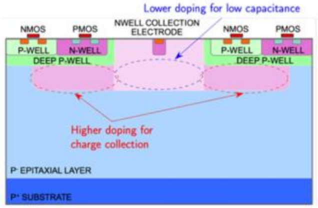


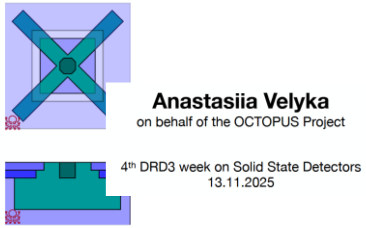




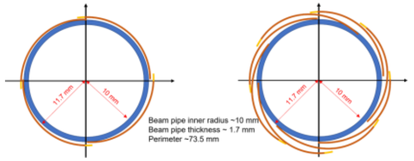
- C.Lemoine (PhD CERN-IPHC) JINST 19 (2024) 02, C02033

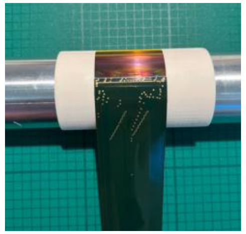
=> Heterogeneous n-implant dose



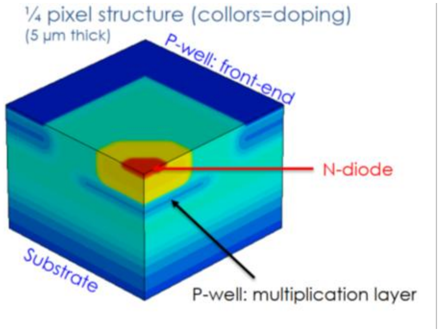


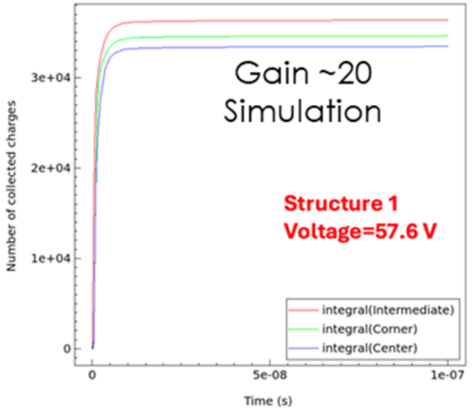
- Integration and mat. Budget optimization
  - ✓ Stitching
  - ✓ Bent sensors
    - FCC-Seed concept and DRD8





- In pixel and in matrix circuits
  - ✓ Amplification, digitization
  - ✓ Read-out architecture
    - Asynchronous read-out (SPARC ⇒ OCTOPUS/MANTA)
    - Pixel grouping (MANTA)
- Peryphery circuit
  - ✓ powering, multiplexing, configuration, control, outputs
- Preamplification
  - ✓ ANR APICS (IPHC, CPPM, icube)
    - Proto tested in 2026
  - ✓ DRD3-CASSIA
  - ✓ CACTUS (IRFU)

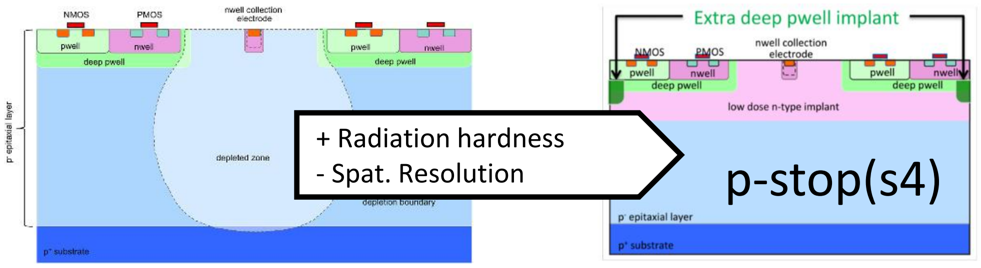




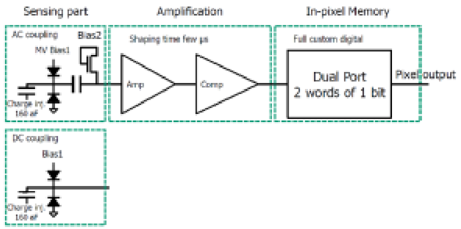
- Pitch reduction (spatial resolution) ⇒ OCTOPUS
  - ✓ Global effort on the footprint
- Power reduction, large surfaces
- Timing ⇒ CACTUS, MANTA

MIMOSIS-2.1 results to chose the final pixel in MIMOSIS-3

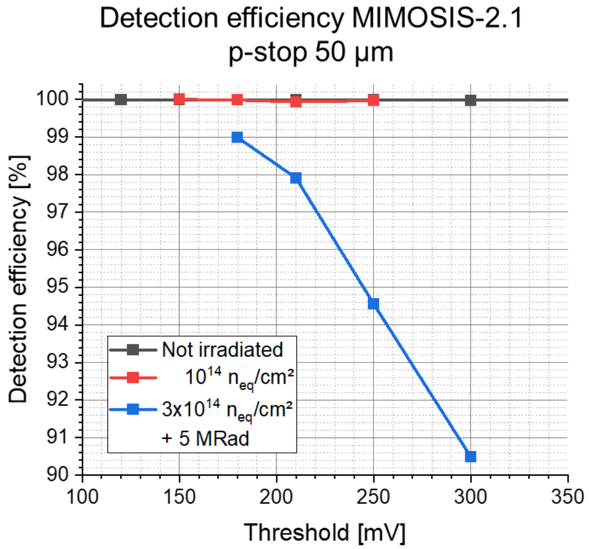
First proposed by W. Snoeys et al.
H. Pernegger et al., 2017 JINST 12 P06008

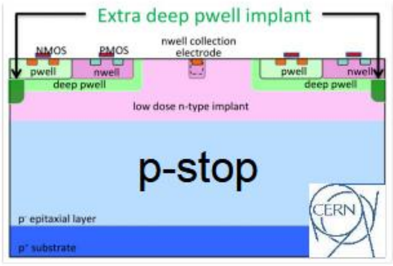


MIMOSIS-2.1: 25µm OR 50µm epitaxial layer

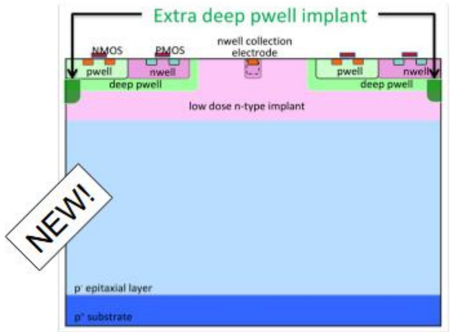


- DC pixel – limited rad. hardness.
- AC Pixel – more biasing lines.

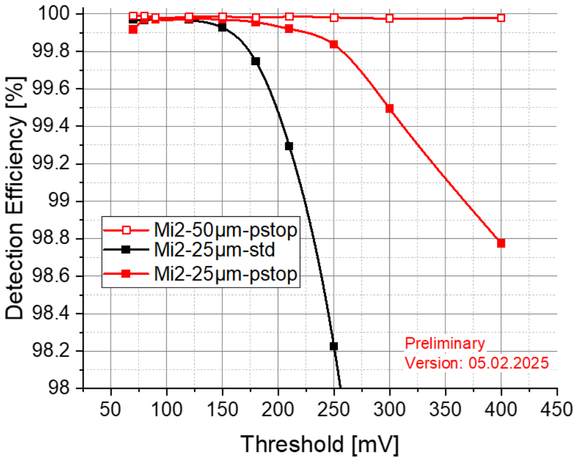




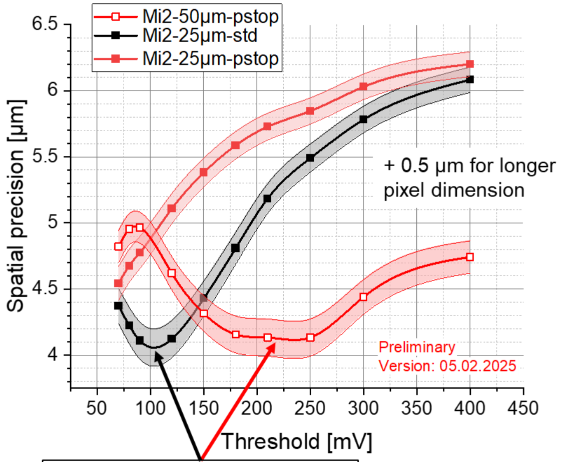
Rad. hard, candidate 1



25 µm & 50 µm epi thicknesses



Dark rate typically <10^{10}/pixel (2 Hz/cm²) driven by individual hot pixels.



Optimal number of fired pixels/particle (about 2.5)

Chosen baseline : p-stop; 50 µm epi; AC pixel; amincis à 70 µm