

Calorimetry at FCC-ee and ILD developments and plans

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Work from ScECAL, SiW-ECAL, T-SDHCAL and AHCAL, FCAL groups

A detector for the next CERN flagship project: ILD
Workshop CERN, 16/09/2026

Topics

Options for the calorimeters

- “Legacy HW”
 - SiW-ECAL + ScW-ECAL
 - AHCAL + SDHCAL (+ Muons)
 - FCAL/Luminosity
- Electronics:
 - CALOROC & KLAUS

Rates and Power at the FCC

- Estimations

Cooling on SiW-ECAL & AHCAL

Timing & Electronics

- Methods
- HW: T-SDHCAL

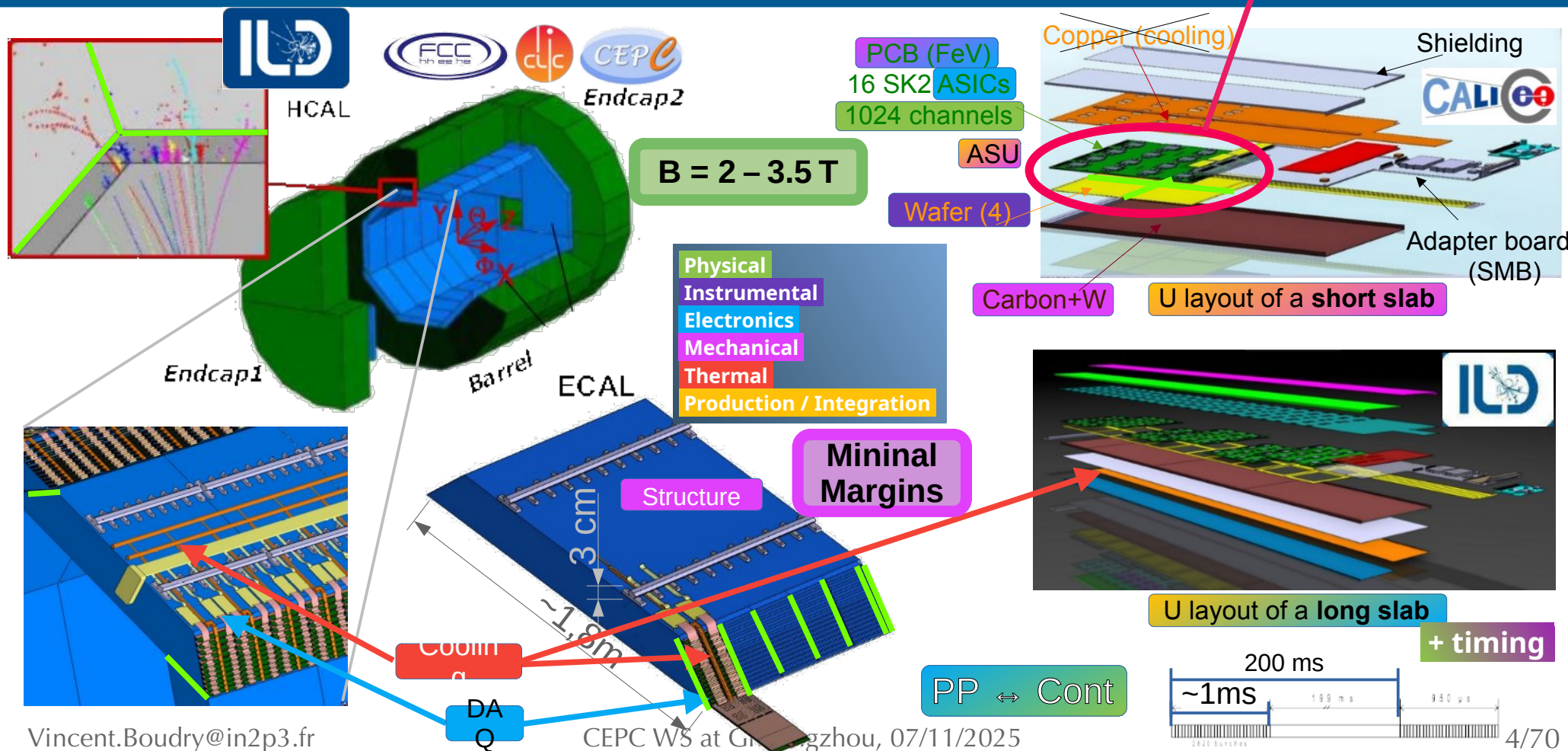
Discussions & To Do's

- Geometries : no changes

SiW-ECAL

SiW-ECAL Design Constraints LC vs CC

ASU = most critical element



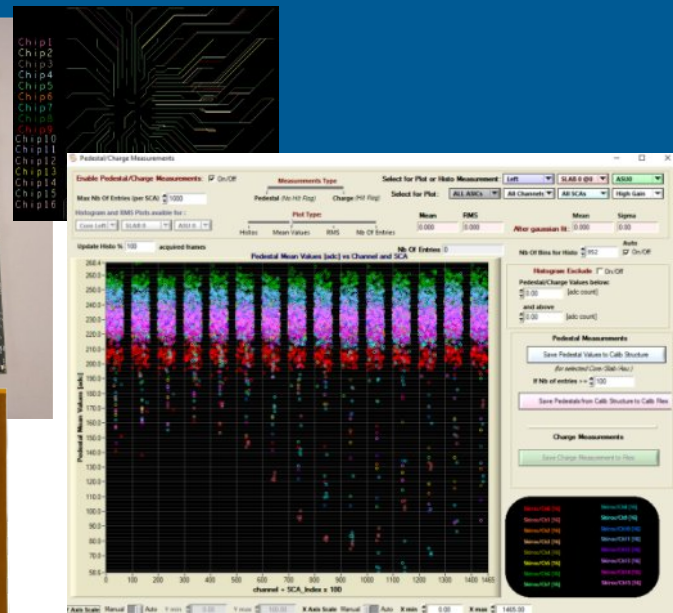
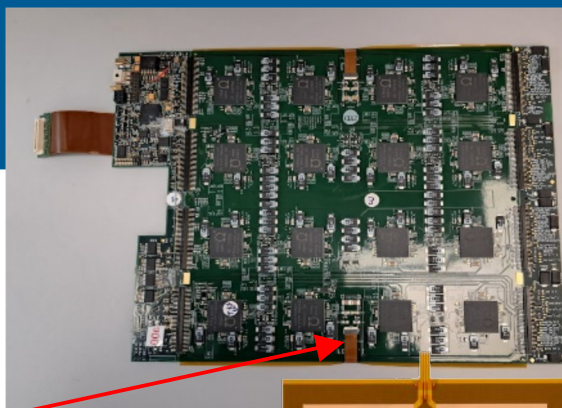
ASU2.1 (2023–...)

Improvements wrt FEV11/12/13

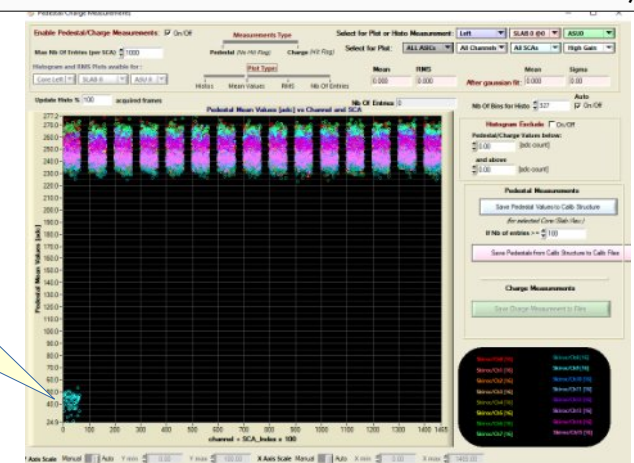
- Power distributions
 - Local LV power regulation: LDO's
 - Local HV filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing streamlined
- Stand-alone HV distribution → flexibility (testing, set-ups)

Status:

- Noise uniformity dramatically improved (ex: outliers in thr. / 20)
- version 2.1 produced
 - 15 cabled, 2nd metrology, 2 equipped with sensors (Fev'25)



Pedestal measurements vs. Ch# + Mem# × 100)



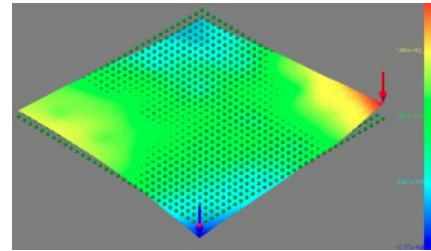
Hybridization studies (2024): How to assemble silicon sensors & PCB ?



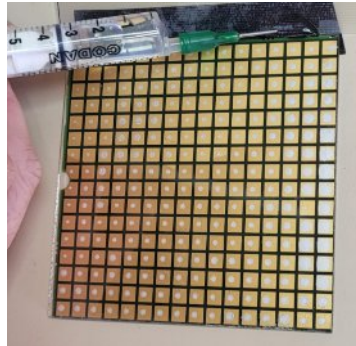
Revisiting gluing (IFIC, IJClab, DMLab)

- PCB metrology
- Bef. & After curing & soldering
- Glue formula & preparation
- Gluing methods
 - Robot
 - Stencil
- Reenforcement
 - Filling glue
 - Adhesive films

IJClab (méca)

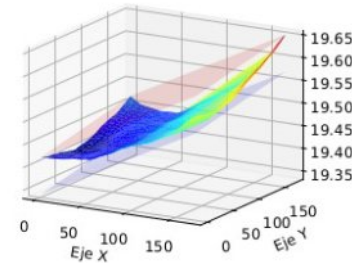


Conductive glue + filling
(~invisible) on a glass plate

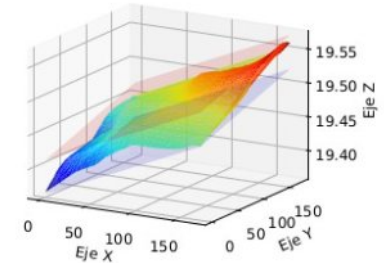


Flatness of PCB

ISOMETRIC VIEW



ISOMETRIC VIEW



Same PCB before / after 10-day dry storage



Measurements by C. Orero, IFIC



Puncturated
adhesive film (**DMLab**)
+
conductive glue dots

(Almost) Uniform Prototype:



A Stack of 15 uniform sensor layers, separated by W absorbers (non-uniform)

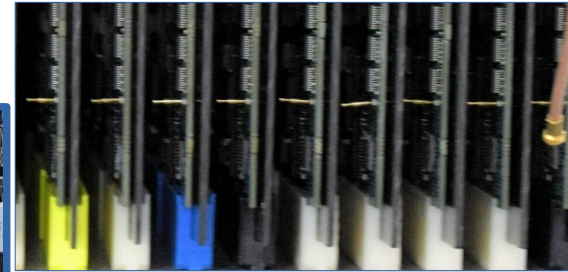
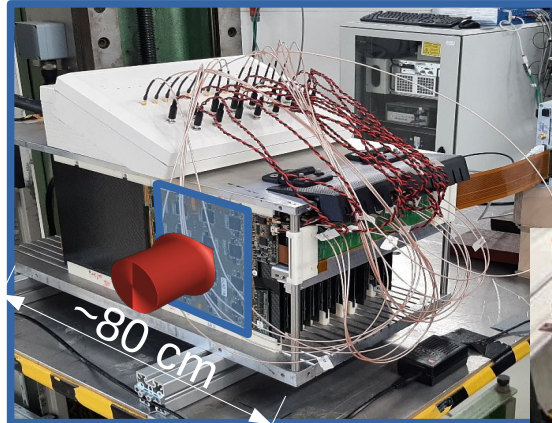
- 15 Sensor layer made of :
 - 4 wafers [$500\mu\text{m} \times (16 \times 5.5\text{mm})^2$ Si PIN Diodes] $\Rightarrow 18 \times 18\text{ cm}^2$
 - 1 PCB (FEv2.1)
 - 16 ASICs (SKIROC2a)
- Tungsten absorbers:
 - $8 \times 4.2\text{ mm}$ [$1.2 X_0$] + $7 \times 5.6\text{ mm}$ [$1.6 X_0$]
Total= 20.8 X_0

10 days in July 2026: very smooth running

- Muon position scans (0 & 45°)
- e^+ Energy & angular scans (10–99 GeV; 0– 45°)
- Low $E\pi$ samples
- Electronics modes $\supset$ TDC

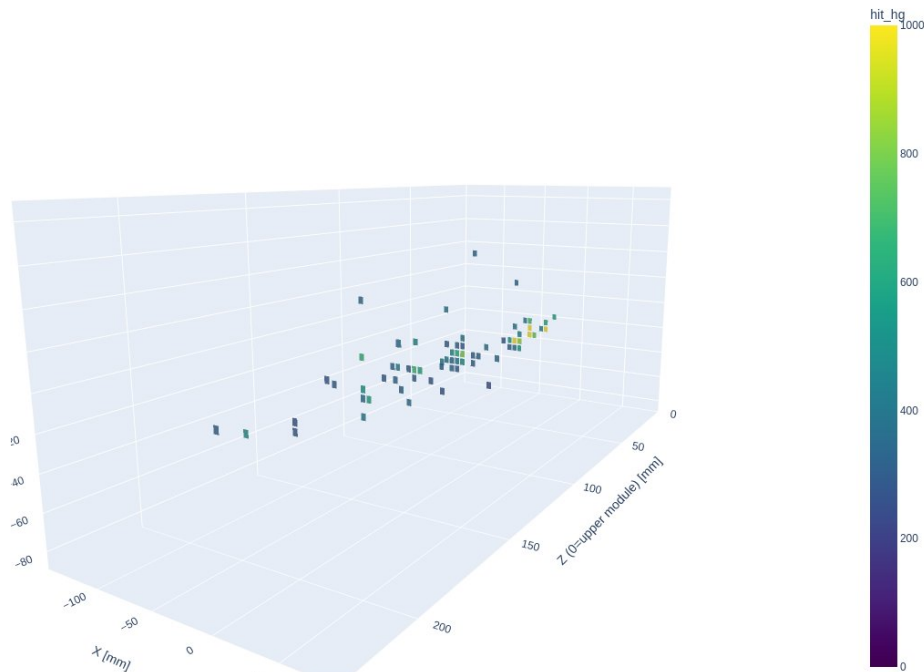
Data is being analysed

No results to be shown yet, but very good quality

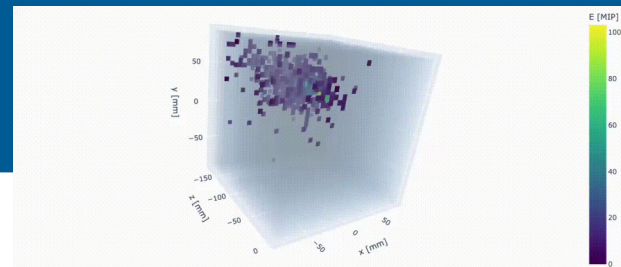
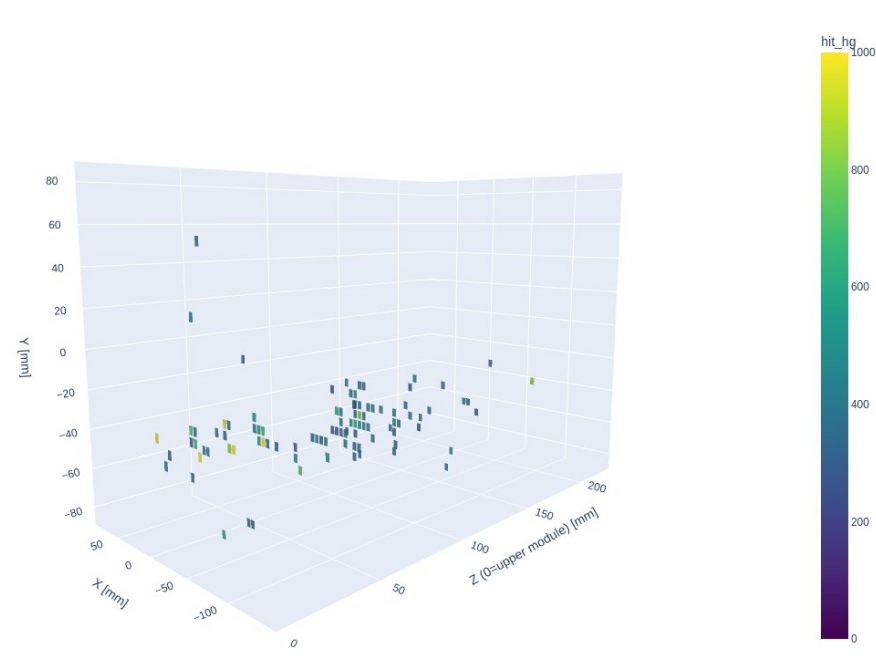


Event displays (Data ↔ MC)

Event display Run_name_0 #Hits=68 #Coincidences=15



Event display Run_name_3 #Hits=96 #Coincidences=14

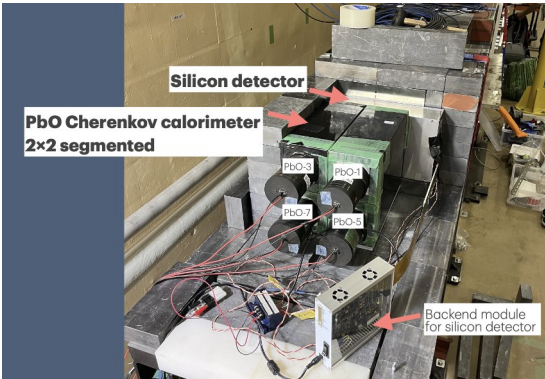
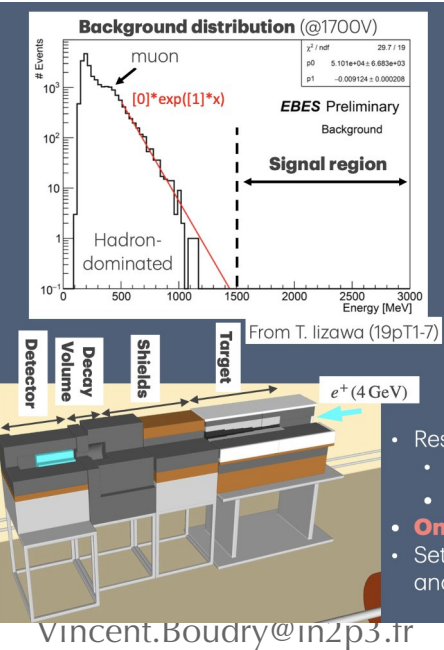


Applications: EBES, LUXE, SHiP, Lohengrin

EBES

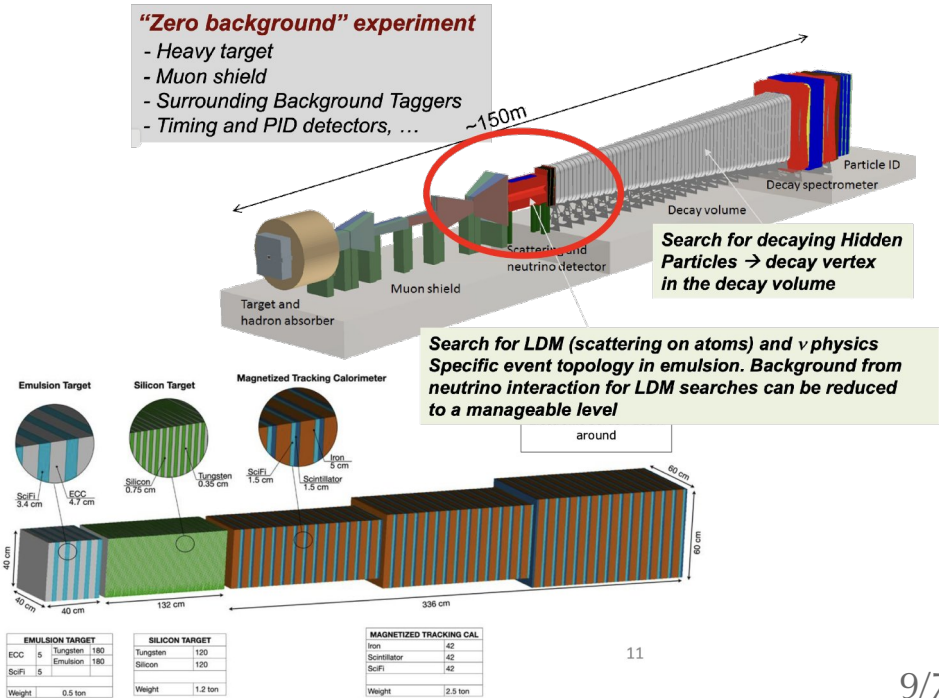
- Electron Beam dump Experiment at KEK Linac Switching Yard 3
- Searching Axion-like particles in MeV-GeV region using e^+/e^- beam and fixed-target
 - Signal: $\alpha \rightarrow 2\gamma$
- The first physics run is conducted in 2025

Diagram illustrating the EBES experiment setup. An electron beam ($e^\pm$) is directed at a beam dump, producing a particle a via the Primakoff effect. The particle a then decays into two photons (γ).



- ## SHiP

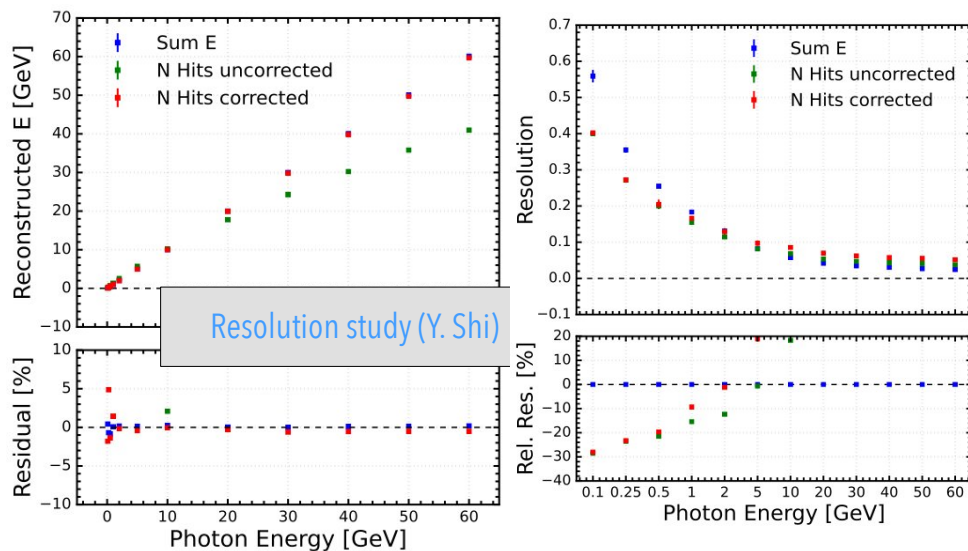
 - Scattering and Neutrino Detector (SND)
 - Perfect application for new electronics & experience building with intermediate size device



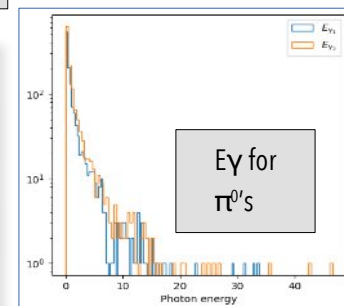
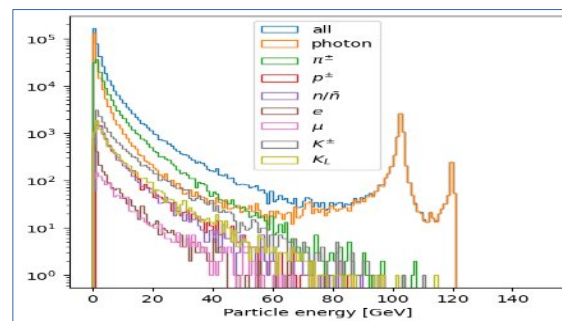
Resolution optimisation

Better $\sigma(E)/E$ for photons from hit-counting for $E_\gamma \leq \sim 2 \text{ GeV}$

- Seen in 2009 (M. Reinhard, PhD) but somehow never integrated in optimization



Event composition ($ee \rightarrow qq$ @ 240 GeV) [H. Liang]



Re-evaluation on flexible (uniform, 60 layers) toy model

- “Fast” MLP model for combining layers for “best energy resolution”, wrt:
 - Thresholds (0.1 – 1.5 MPV of a MIP)
 - Silicon thickness (150 – 750 μm)
 - Cell size (1 mm – 20 mm)
 - Sampling fraction (n layers with const. W thickness)
 - Total thickness (fixed Sampling fraction)
- To be cont'd with angular resolution, non-uniform sampling, timing, **LGAD timing layers** ?

JINST 21,(2026) P08028.

High-granularity ECAL for B/ τ physics by improved γ reconstruction

Work by JC. Briant (LLR)**

1. $B_s \rightarrow D_s \pi^\pm, D_s K^\pm$
2. $B^0 \rightarrow \pi^0 \pi^0$
3. Transition from quark $b \rightarrow s \gamma$
4. τ physics rare decays
5. τ polarisation and AFB measurement

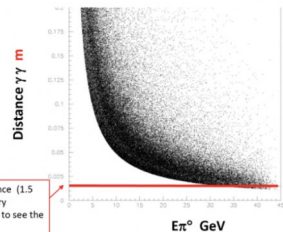
Based on fast simulation:
rare events = millions of events needed

$B^0 \rightarrow \pi^0 \pi^0$ and $B^0 \rightarrow K^* \gamma$

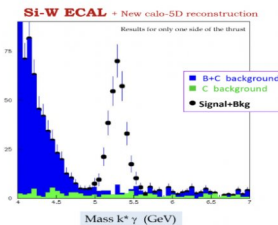
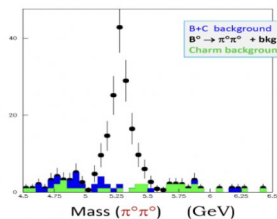
Selection on tracks + γ/π^0 identification: → “Background free” (90% purity) measures

- Detailed report from JC.Briant here:
Performances of ultra granular ECAL for flavor physics at ILC, LCWS25

The γ/π^0 identification

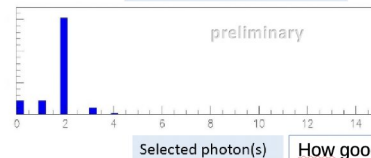
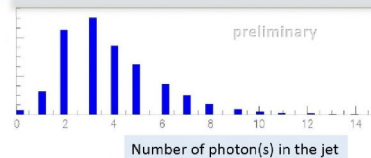


With the bulge mass method, we can probably go higher than 35 GeV

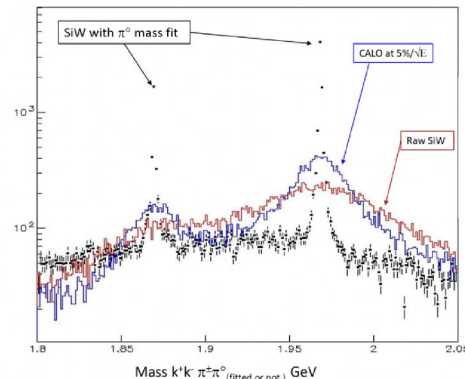


$B_s \rightarrow D_s \pi^\pm, D_s K^\pm$ with $D_s \rightarrow \varphi \rho \rightarrow K^+ K^- \pi^\pm \pi^0$

- The events are split in 2 hemisphere with the Thrust axis
- select a displaced vertex with $K^+ K^- \pi^\pm (K^\pm)$ in one hemisphere
- Select the ϕ mass region for $K^+ K^-$
- Define the jet direction as the direction of $K^+ K^- \pi^\pm (K^\pm)$
- Photon(s) in the cone such $\cos(\gamma/\text{jet}) > 0.75$

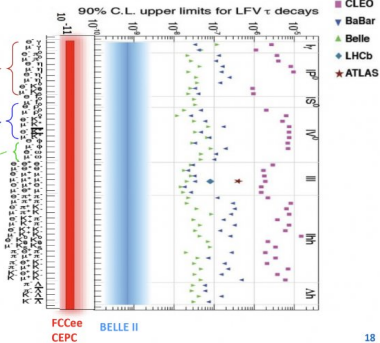


How good is the selection?



Many channels requiring a very good $\gamma/K_L/n$ and γ/π^0 ID

- BC mass, $\gamma/\pi^0, \eta$ and γ/K^* Identification
- Meson mass fit (π^0, η)



BC for Beam Constraint

18

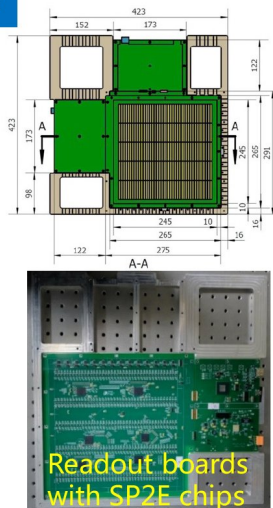
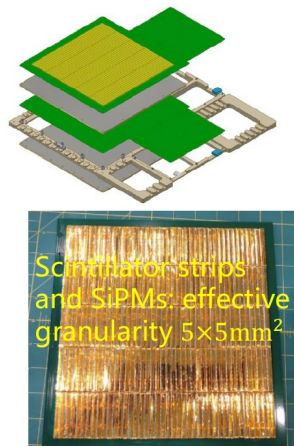
SciECAL

ScW-ECAL technological prototype

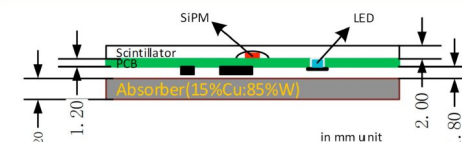
ScW-ECAL tech. prototype



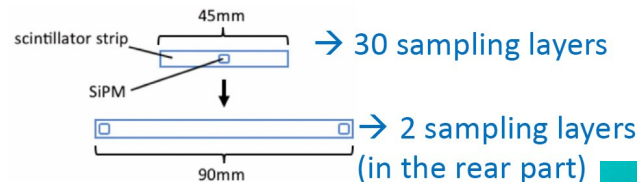
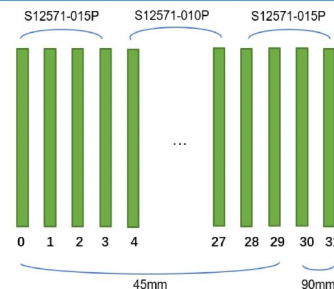
"Super-layer" design



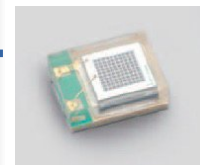
Scintillator-SiPM readout scheme



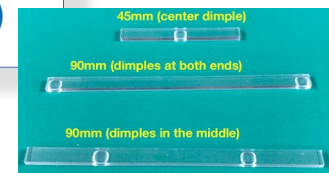
Sensitive layer arrangements



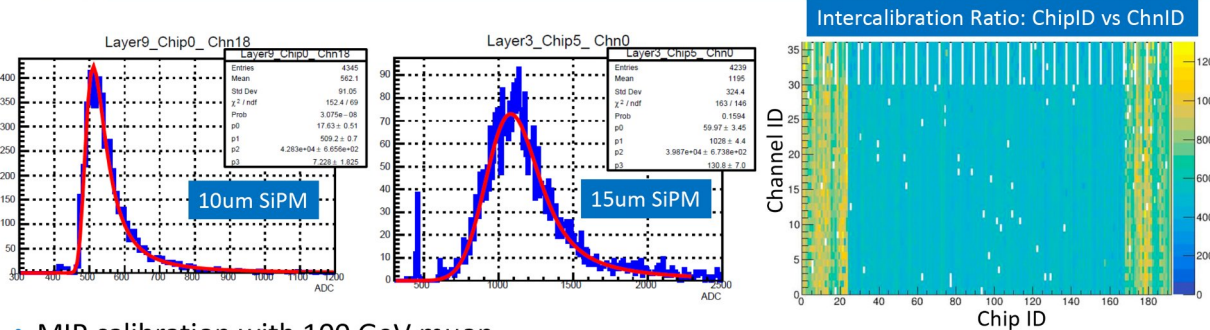
SiPM:
10k & 15 k



- ScW-ECAL prototype: developed in 2016-2020
 - Transverse area $22 \times 22 \text{ cm}^2$, 32 longitudinal layers
 - 6,720 channels based on SPIROC2E (192 chips)
 - Total weight $\sim 350 \text{ kg}$



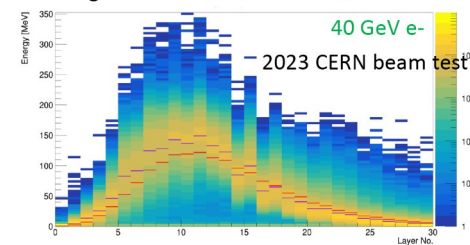
ScW-ECAL technological prototype: BT at CERN (2022–2023) (with CEPC-AHCAL)



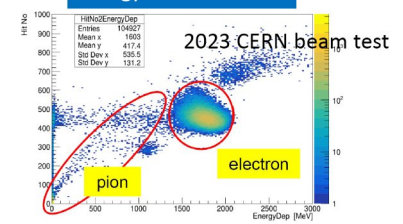
- MIP calibration with 100 GeV muon
 - Extracted MPV value from Landau distribution convoluted with Gaussian
 - Muon tracking algorithm applied to improve fitting quality
- Remaining issue: channels with 10 μm SiPMs
 - The MIP signal-to-noise ratio (SNR) is low and the trigger threshold was relatively high in MIP spectra

- Goals for new MIP calibration runs
 - To re-do especially for channels with 10 μm SiPMs (low signal-to-noise ratio)
 - Better temperature control than at CERN: lower temperature and better uniformity
 - To optimise trigger threshold in order not to cut into MIP spectrum
- EM performance studies with low-energy electrons (< 6 GeV)
 - Better electron beam purity than at CERN

Longitudinal Shower Profile: MC vs Data



Energy vs Hit Number



2025: BT at KEK

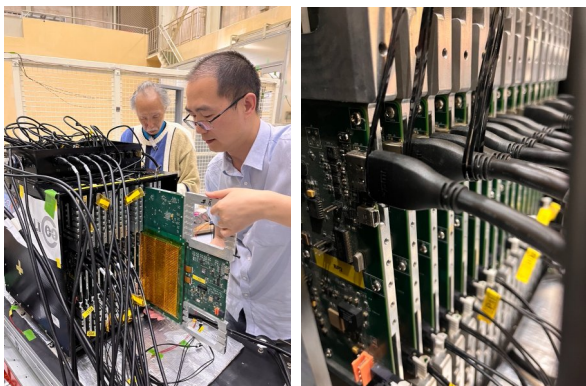
From Yong Liu @ 2025 DRD-Calo Collaboration Meeting at Ancona

Beam test period: May 26 – June 10 (schedule)

- 5 GeV electrons: MIP calibration of EBU layers
- Electron beam energy scans: 0.5 – 5.8 GeV

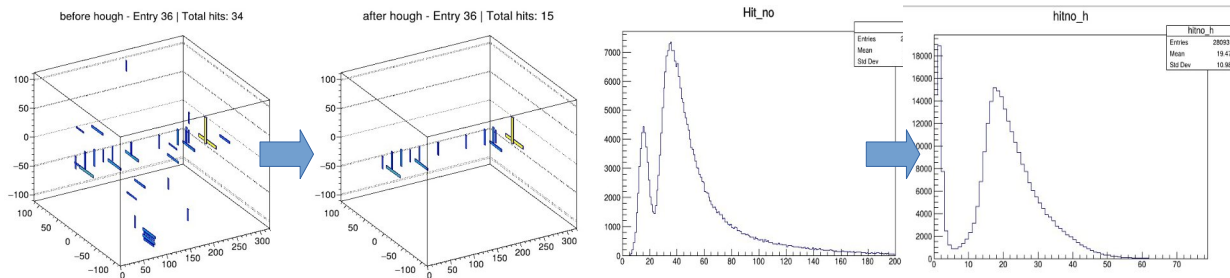
Detector:

- 8 EBU layers with 15 μm SiPMs
- 24 EBU layers with 10 μm SiPMs
- With and without CuW Absorbers



On-going Analysis:

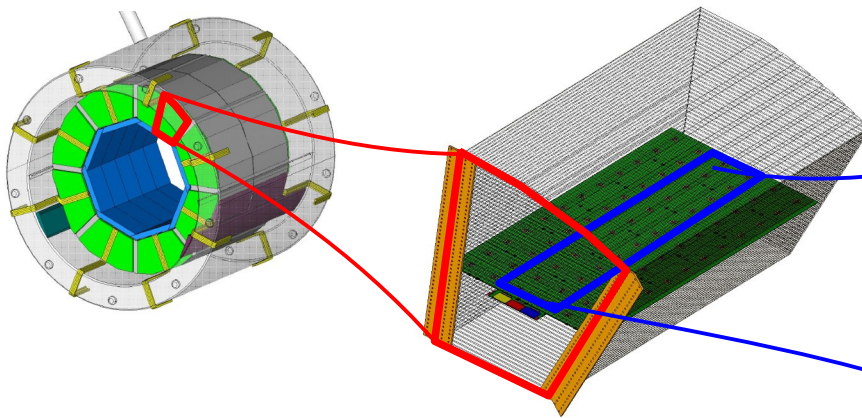
- Pedestal studies: “many” “bad” channel
 - larger pedestal sigma
 - near the edge, or due to Chip 2 in odd layers
 - Even EBU layers > than odd layers
- Single photon calibration
- MIP calibration & track finding (strip-splitting + Hough transform): noise cleaning



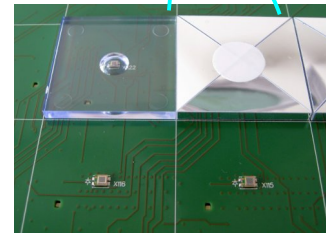
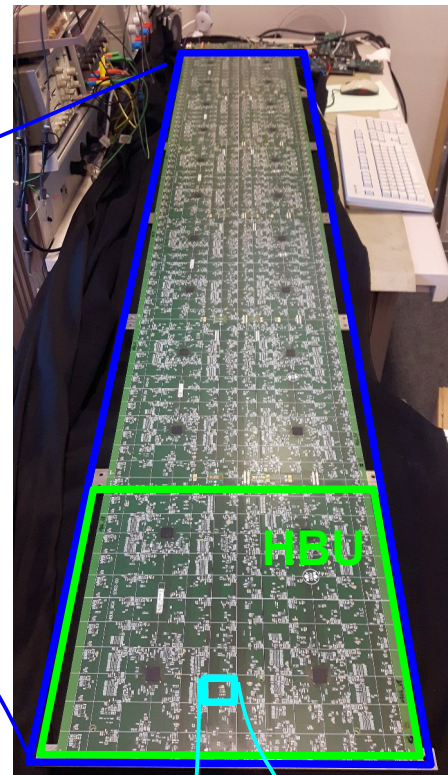
Some HW failures ($\supset$ cooling, PS) : new BT at KEK planned

AHCAL

AHCAL Technological Prototype

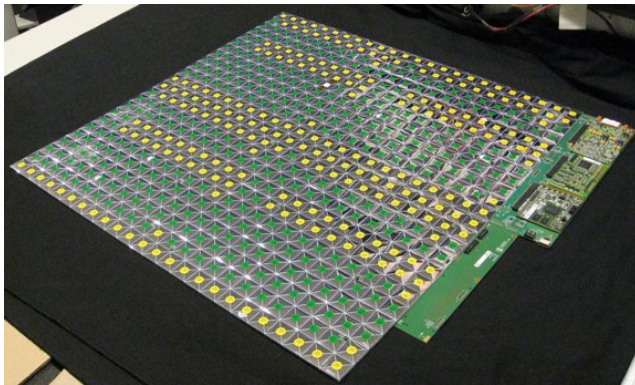


- highly granular scintillator SiPM-on-tile hadron calorimeter, $3 \times 3 \text{ cm}^2$ scintillator tiles optimised for uniformity
- **fully integrated design**
 - front-end electronics, readout
 - voltage supply, LED system for calibration
 - no cooling within active layers → **power pulsing**
- **scalable** to full detector (~8 million channels)
- geometry inspired by ILD, similar to SiD and CLICdp
- HCAL Base Unit: $36 \times 36 \text{ cm}^2$, 144 tiles, 4 SPIROC2E ASICs
 - slabs of 6 HBUs, up to 3 slabs per layer



AHCAL Technological Testbeam Prototype

- Large enough to contain hadron showers
 - 38 active layers of $72 \times 72 \text{ cm}^2$
 - 4 HBUs per module
 - in total: 608 SPIROC2E ASICs, ~22000 channels
 - SiPMs: Hamamatsu S13360-1325PE
- All modules interchangeable
- Built with scalable production techniques in ~2 years
- Operated in beam tests with muons, electrons and pions at **CERN SPS in 2018** (2022 with SiW-ECAL)
 - 3 weeks of beam time
 - Collected $O(100)$ mio events
 - Very stable running
 - Nearly noise free
 - < 1 per mille dead channels

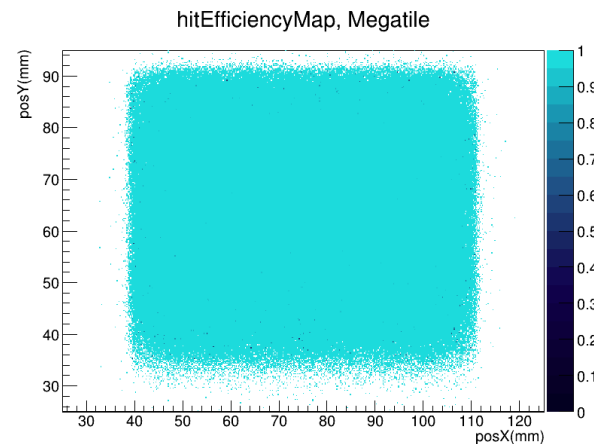
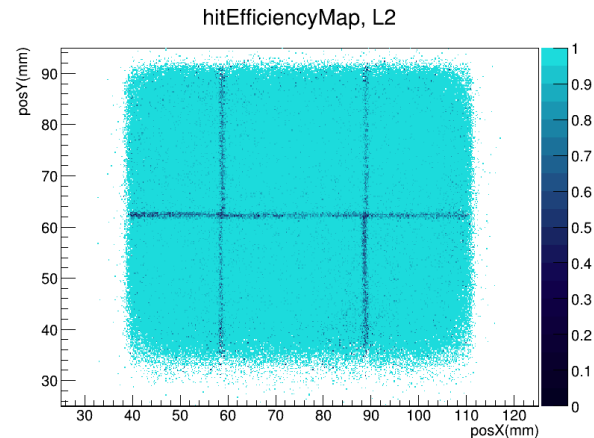
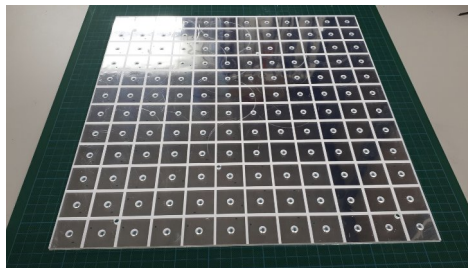
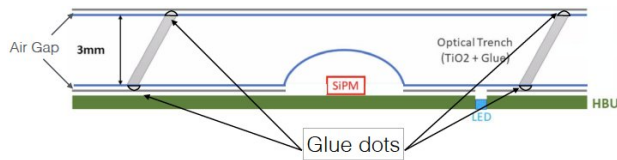
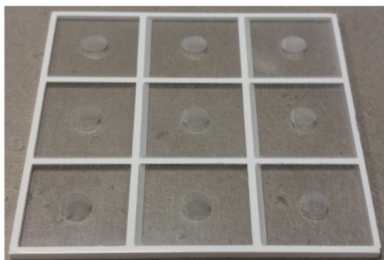


AHCAL Plans: Hardware Developments

Alternative scintillator geometry

- ILD will require two orders of magnitude more tiles than AHCAL prototype, one order more than CMS HGCal
- Megatiles would allow larger units for mechanical assembly
- Challenge: reach good uniformity while keeping the cell-to-cell light cross talk small
- Status:
 - Several generations of Megatiles produced
 - Last one shows reasonable uniformity and light yield, working on optimization of edge cells
 - One Megatile HBU included in 2022 testbeam setup
 - Plan to build a 2×2 HBU layer to study also Megatile-Megatile transition region

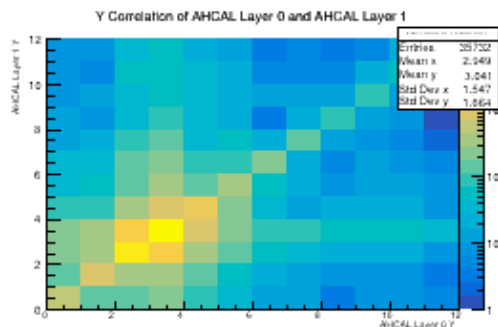
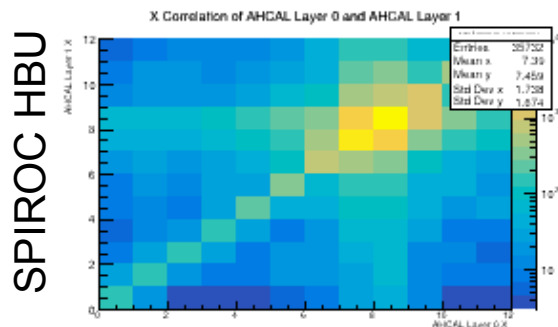
Recent:
3D printed “mini-megatile”



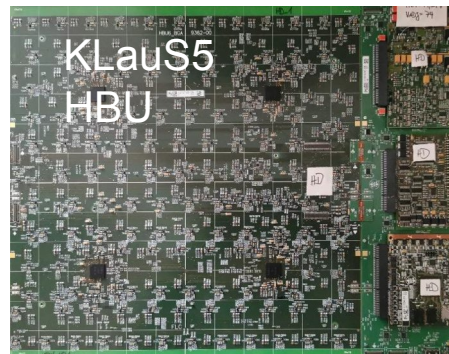
AHCAL Plans: Hardware Developments

Readout ASIC (KLauS)

- Wide range of applications
- Possible application at circular Higgs factories
- Optimised for SiPMs with small pixels ($10\mu\text{m}$) → possible application in scintillator ECAL
- Status:
 - First HBU with KLauS5 operated within AHCAL DAQ
 - KLauS6 with full functionality available

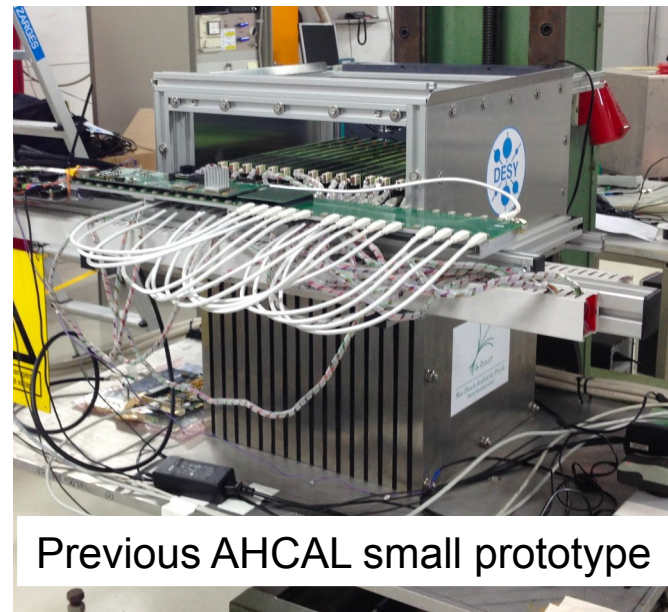


KLauS HBU



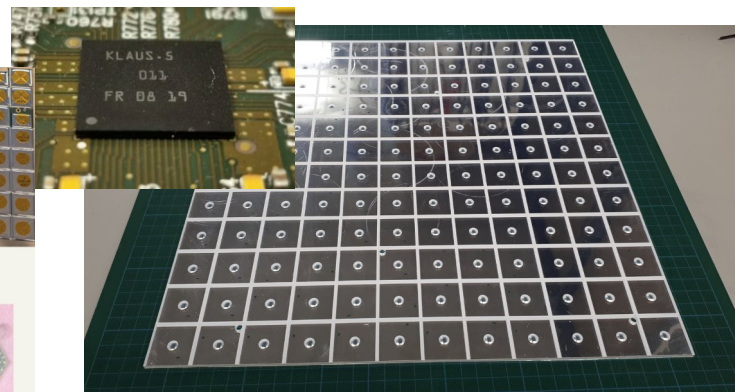
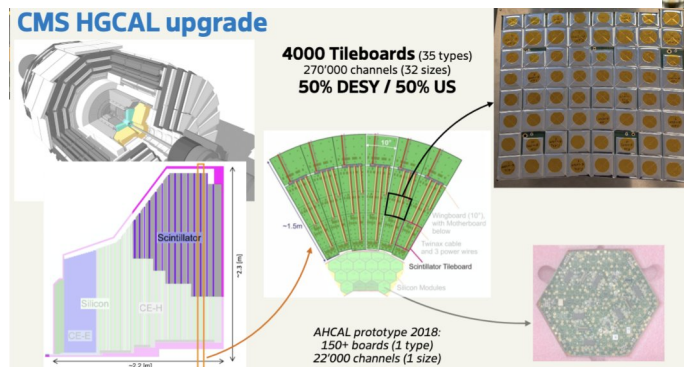
DRD plans for AHCAL

- Build a small AHCAL prototype with continuous readout with hit timing capability
- Task sharing between institutes working on AHCAL
 - Front-End ASIC (HD)
 - Back-End / DAQ (KIT, Mainz)
 - Megatiles (Mainz)
 - Mechanics & Cooling (Mainz, HD, DESY)
 - Common tasks: software, testbeams, analysis, ...



Previous AHCAL small prototype

Practical implementation in
HGCAL
(HGCROC ~ → CALOROC)



T-SDHCAL

SDHCAL for ILC

G. Grenier, CEPC 2026 European Workshop, April 7-10, Lisboa

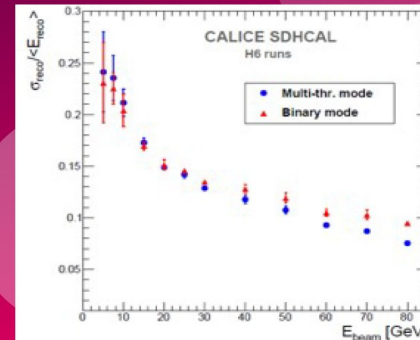
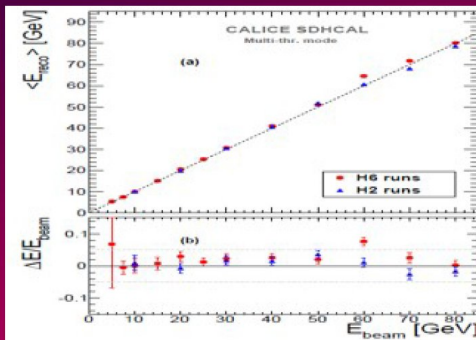
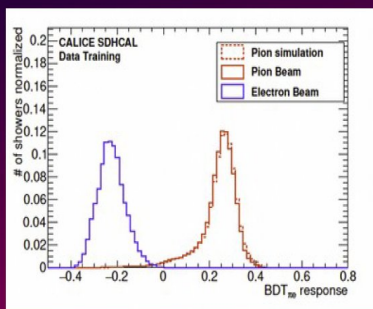
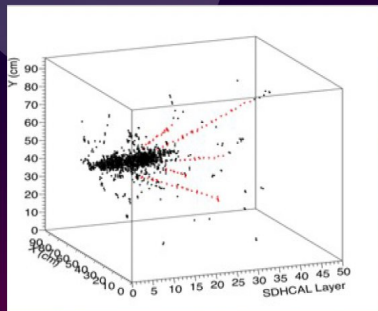
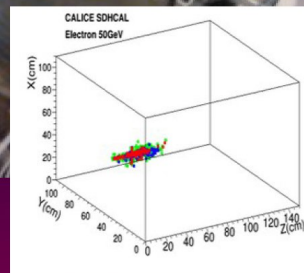
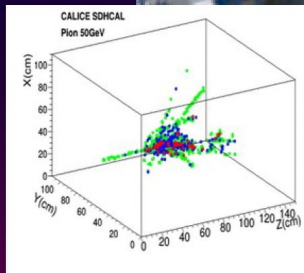
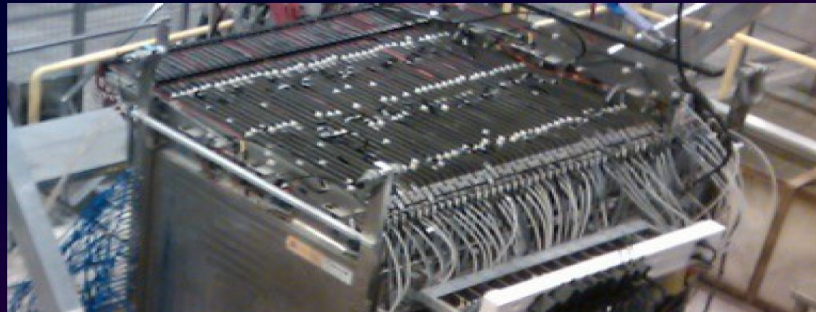
SDHCAL- ILC

48 layers of 2 cm stainless steel interleaved with planes made of Glass RPC and their embedded readout 2-bit electronics allowing a lateral segmentation of 1 cm²

A technological prototype of 48 layers fulfilling all the ILD-ILC requirements :

- Compactness
- Self-supporting mechanical structure.
- triggerless mode
- Power-pulsing mode

was built and extensively and successfully tested



Hough transform tracks to control the detectors in situ

Pion/electron separation in SDHCAL

$$E_{\text{rec}} = \alpha (N_{\text{tot}}) N_1 + \beta (N_{\text{tot}}) N_2 + \gamma (N_{\text{tot}}) N_3$$

SDHCAL → T-SDHCAL for FCC-ee

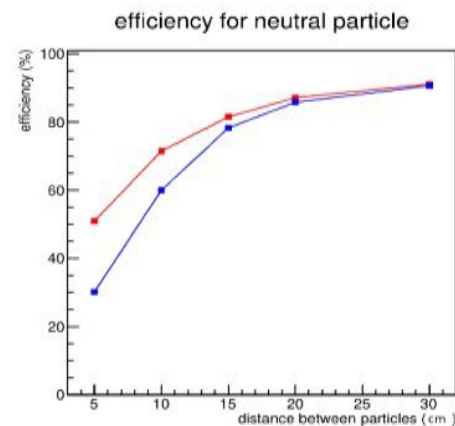
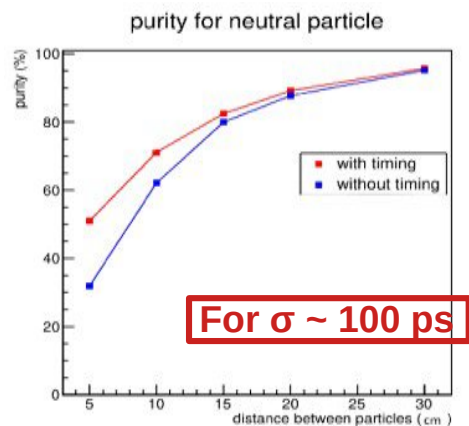
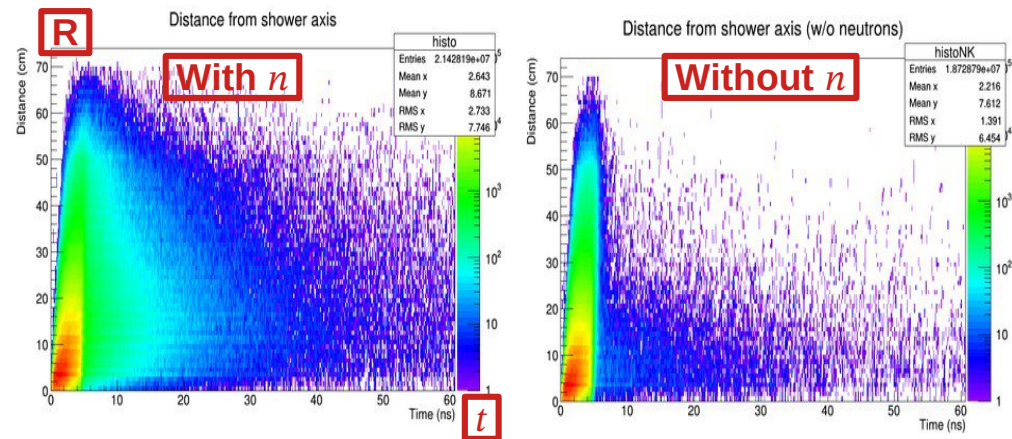
Circular Colliders:

- Continuous readout, cooling
- Higher rate

RPC → Multi-Gap RPC (MRPC)

Timing

- Timing with GNN was shown to improve energy reconstruction (N. Akchurin et al.)
- recent studies show time information could improve significantly hadronic showers separation at lower distances.



SDHCAL → T-SDHCAL

TSDHCAL Goal : technological proposal for FCC/CEPC HCAL

Within 3 to 4 years

A 4D/5D sampling hadronic calorimeter with high granularity and precision timing.

Multigap RPC

- Known since decades that $<100\text{ps}$ resolution achievable.
- Timing response uniformity never tested on large area.
- RPC and MRPC simulations (electronic avalanche) do exist but are :
 - Complex
 - Not fully reliable
 - Very long to compute

Timing electronics

- Collaboration with Omega.
- Needs a physical detector to define electronics input.

Calorimeter simulation

- Geant4 calorimeter simulation
- Model MRPC+electronics response from physics principles and data from physical detector (digitisation)
- Getting data from hadronic showers needs a Hadronic Calorimeter : reuse SDHCAL prototype

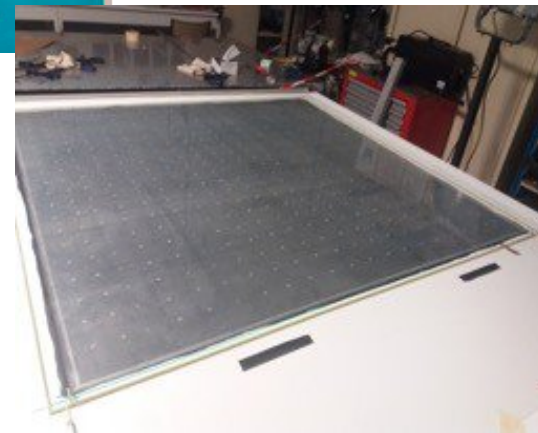
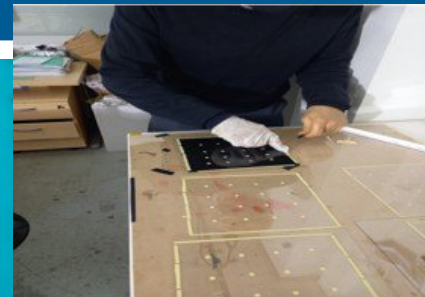
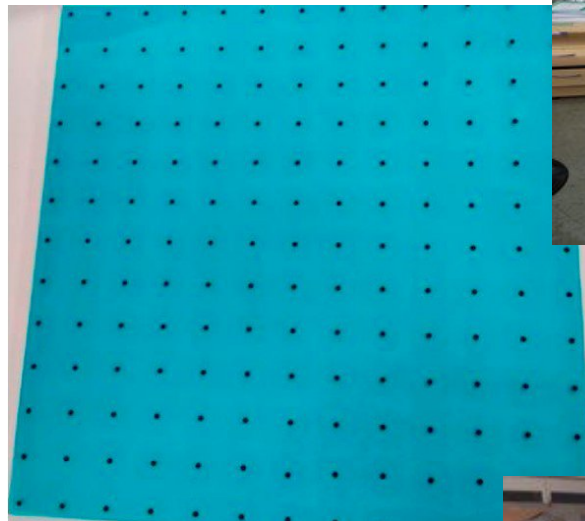
Building of MRPCs

Recents news from Imad:

- Construction of MRPG with 3,4 & 5 gaps started
 - Measure the time resolution
 - Fix the gap number for 100 ps
 - Results by the end of 2028

New way of producing MRPC was developped in Lyon

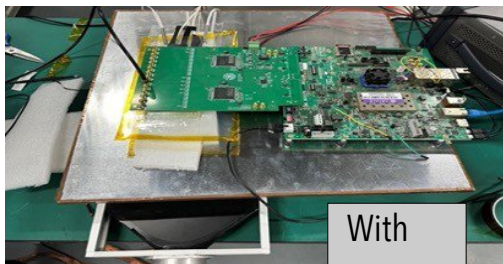
- Replace fishing lines by spacers (~SDHCAL)
- Spacer and gas contour = industry product
- Easy production, cheap detector



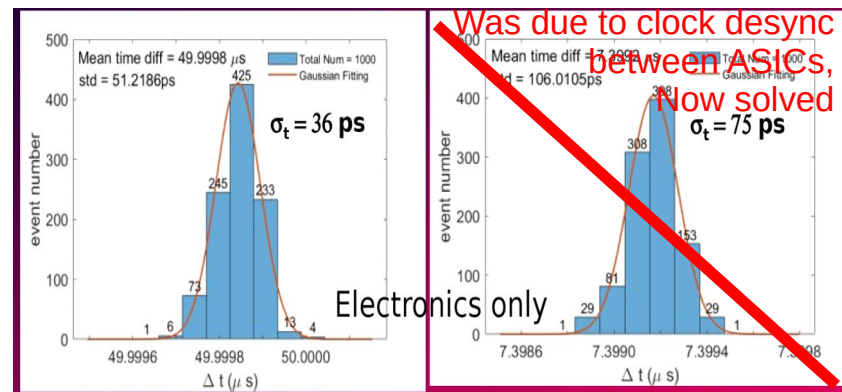
MRPCs timing performances

Recent news from Imad:

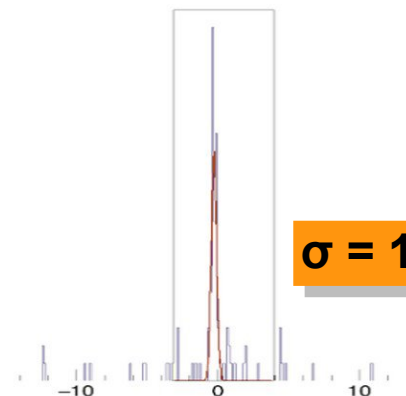
- 100× 50 cm² ASU built
- PETITROC ASIC (TDC) for test



With
SJTU



Timing Histogram



$\sigma = 133$ ps

FCC-ee readout

- PETITROC deadtime ~ 12,5μs
- CALOROC*D with Ωmega (discussion)

T-SDHCAL: Rates

High-rate capability

RPC is low-rate capability detector due to the resistive nature of the electrodes.

Low-resistivity glass developed by Tsinghua U., but problem with the glass thickness and dimensions

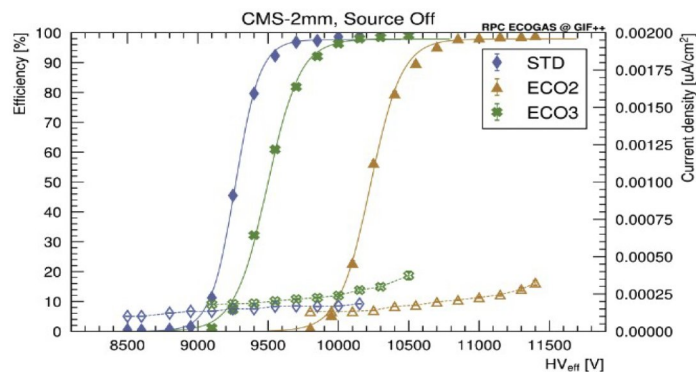
PVdF and **PEEK** are very stable and chemically inert **thermoplastics**, doped to reduce bulk resistivity (BR)

- New kind of PVdF developed by IP2I with the help of PolyOne (Germany). Achieved BR of $10^{11-12} \Omega \cdot \text{cm}$
- New charged PEEK developed with the help of Krefine (Japan). Achieved BR of $10^{8-9} \Omega \cdot \text{cm}$.

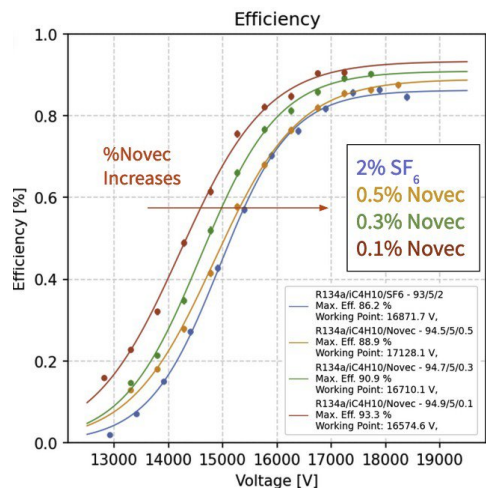


Eco-friendly gas mixtures

Mixture	$C_2H_2F_4$ [%]	HFO [%]	CO_2 [%]	iC_4H_{10} [%]	SF_6 [%]	tCO_2e	M. Verzeroli ↓ Impact ~ 1/4.5
STD	95.2	0	0	4.5	0.3	3384	
ECO3	0	25	69	5	1	762	
ECO2	0	35	60	4	1	763	



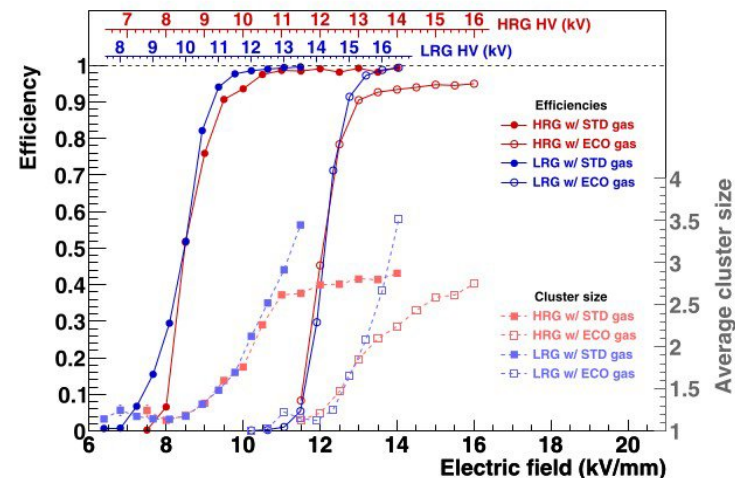
HFO+NOVEC+CO2 to be tested
in near future



Caveats:

- Eco-gas require higher voltages
- Low Resistivity electrodes (high rate) might require SF6-like quencher

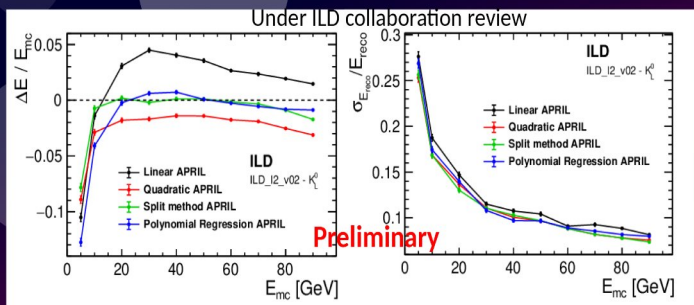
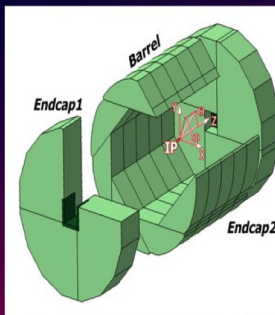
MRPC with pure HFO: NIMA 1061 (2024) 169104



Reconstruction Efforts

SDHCAL in ILD

- Developing APRIL PFA.
- Calibration for ILD with SDHCAL and Videau geometry.
- Exploration of new ways to reconstruct hadronic energy.



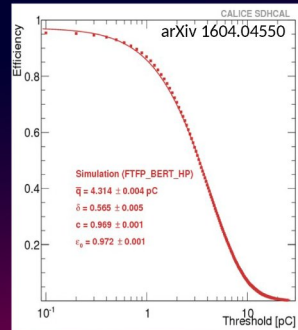
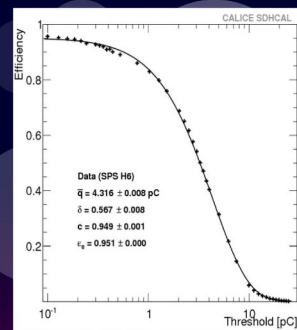
R. Eté PhD thesis
L. BO (LIO postdoc)
T. Pasquier PhD thesis

Collaborations and PhD's in

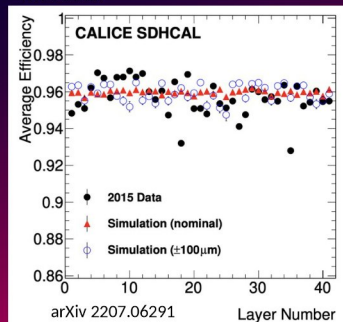
- Timing for PFA (T-Calo)
- MRPC

RPC Digitisation

Modelling RPC response based on physics principle and test beam data



Modelling RPC response based on full MC simulation of avalanches and comparison with data.



- Modelling MRPC response based on physics principle and data (started).
- RPC Digitiser from LCIO to LCIO+EDM4HEP.

A Steen, PhD thesis
G. Garillot, PhD thesis
V. François PhD thesis (LPC)
W Vaginay PhD thesis (multigap)

Muons

(the little that was not covered
by Riccardo Farinelli)

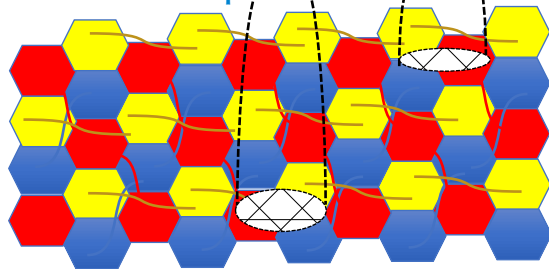
New Readout Scheme (by Imad)

Pixels with multiplexed readout woven strips

- Two neighbouring pixels are connected to two different strips of different directions (by induction)
- Each strip is connected to one electronic channel

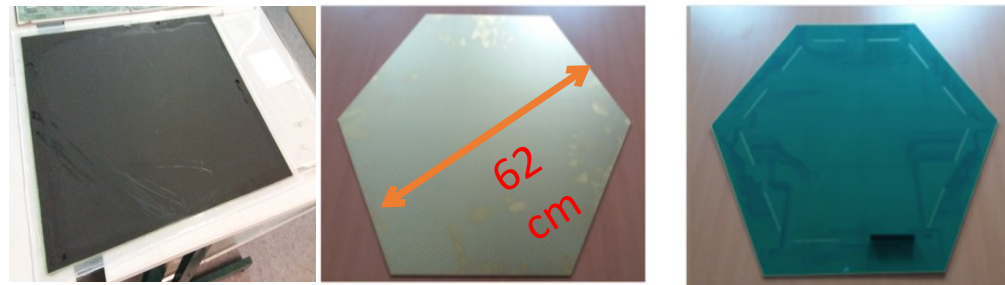
Share the charge among a few ones

- Cross the fired strip to determine the position



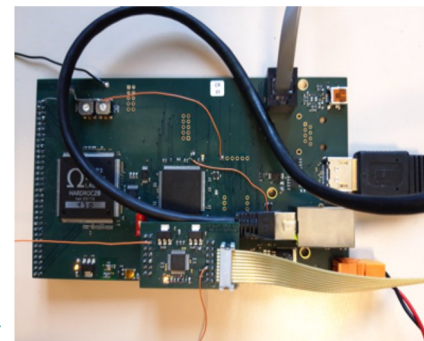
- $N \times N \rightarrow 3N$: Reduction of electronic channels, power consumption and occupancy

RPC Prototype (IP2I, Lyon)



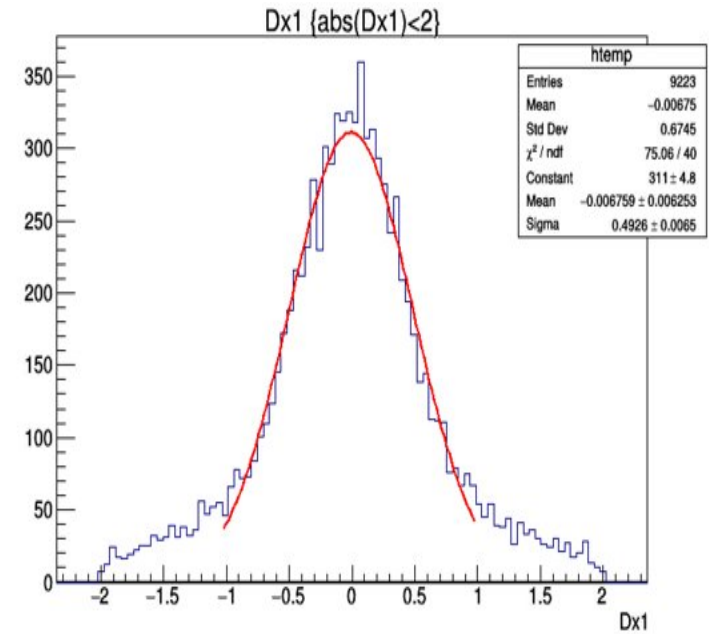
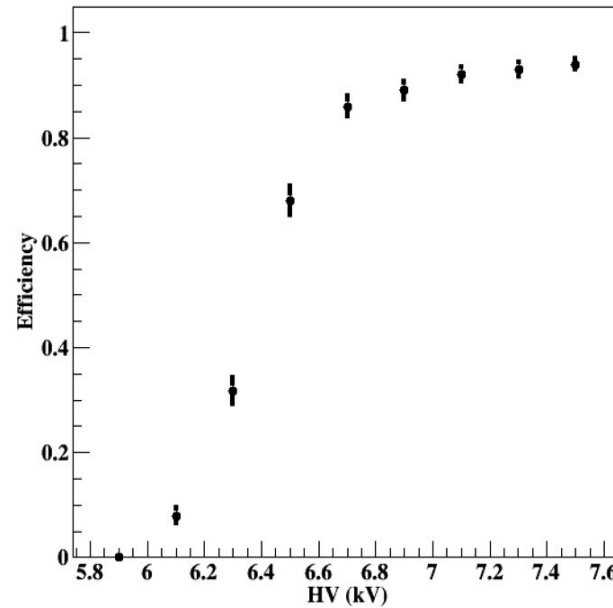
- Readout board hosting

- One Hardroc ASIC
- One Microcontroller
- Plugged directly on the back of the PCB, on the edge to readout 64 woven strips.

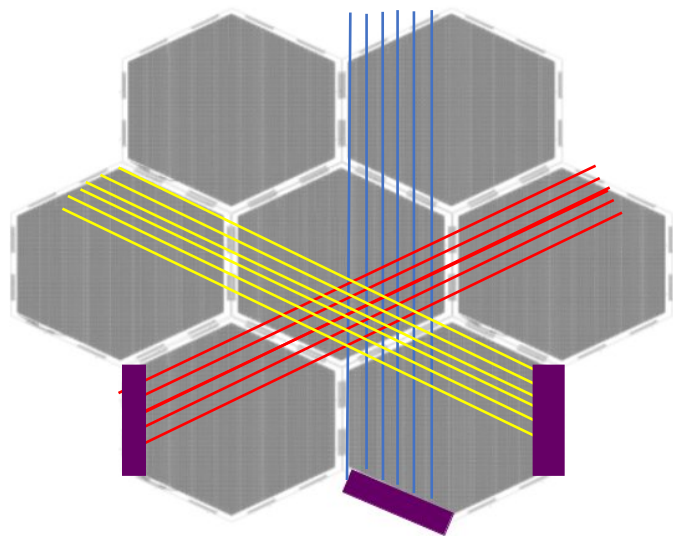


Spatial Resolution

$\sim 1 \text{ cm} / \sqrt{12}$

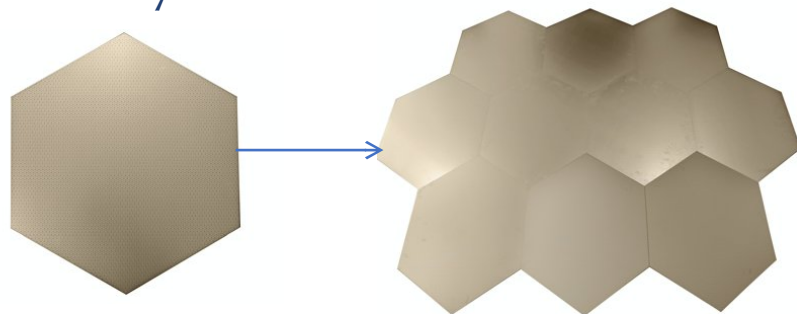


Large Systems

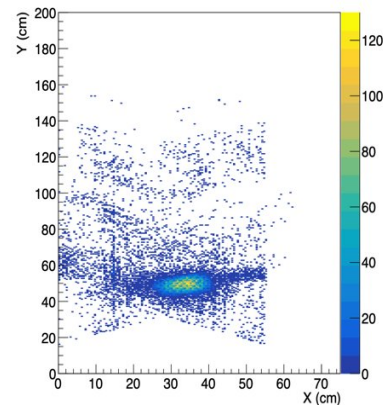


“Well matched impedance will help to keep the signal in good shape for long distances”

Assembly of many PCB



- being tested: $2 \times 1 \text{ m}^2$ GRPC with several PCBs
- Reconstruction efficiency (1 direction efficiency is not included) is around 90%.

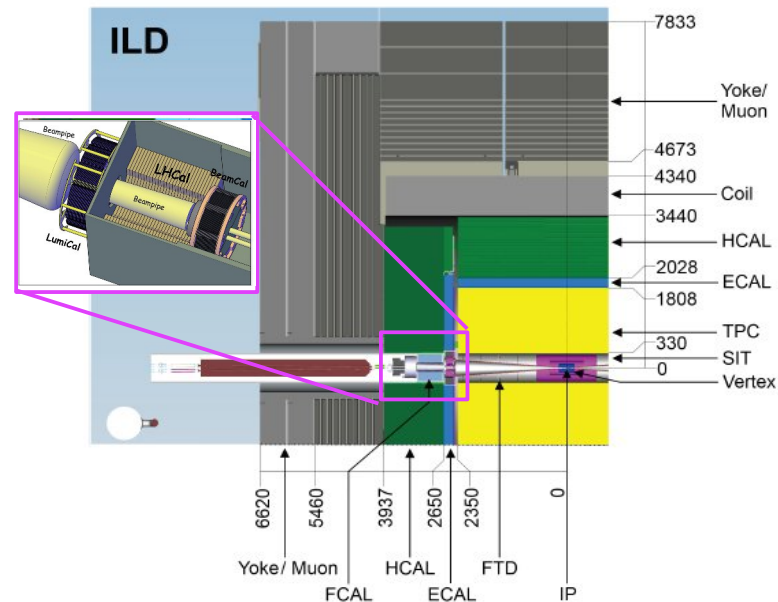
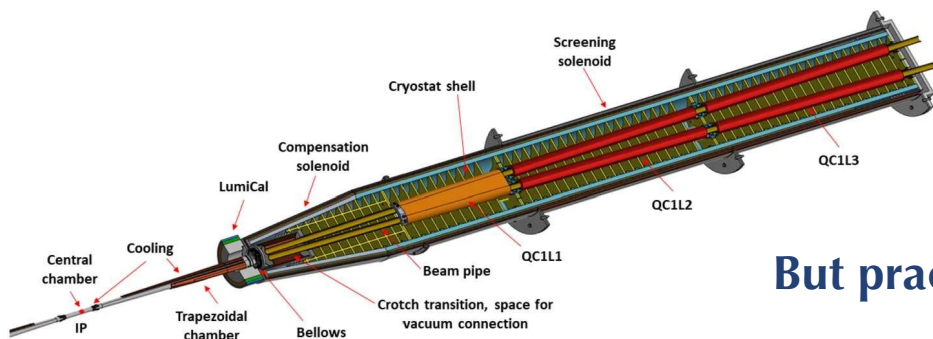


FCAL

FCAL collaboration

Legacy contributors to the Forward calorimetry at ILC:

- LumiCal (W + Si or GaAs) + LHCAL
- No update in years
- Study needs to be redone completely
 - See Yan's summary on FCC-ee Luminosity WS



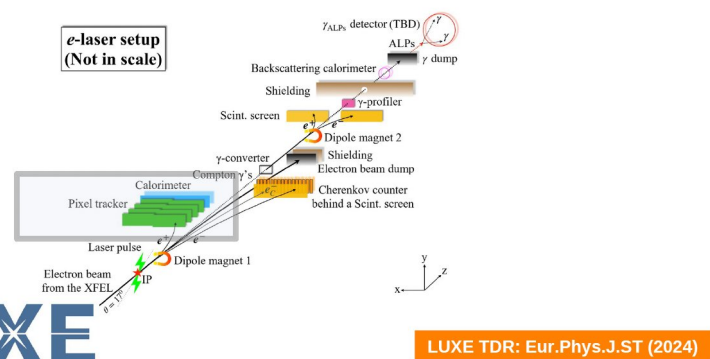
But practical application of FCAL technology → LUXE

- Continuation of work on very compact calorimeters

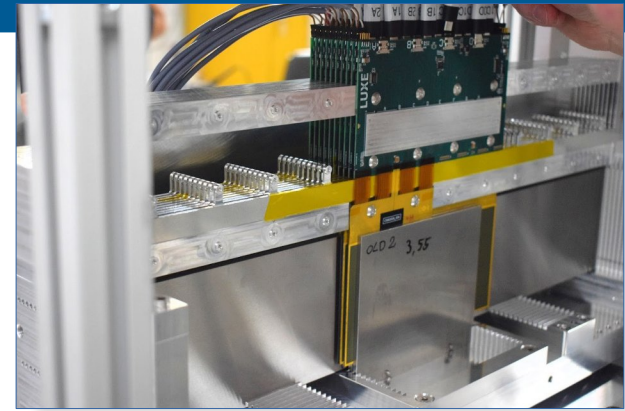
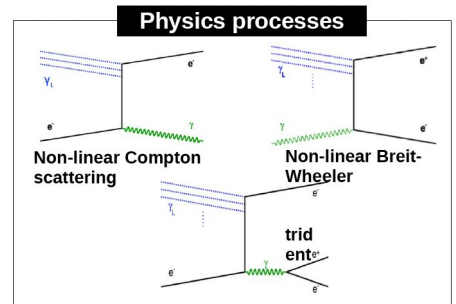
LUXE experiment

Positron ECAL for LUXE

- ▷ LUXE: Experiment based at **DESY-XFEL**
- ▷ **Strong EM field:** 30-350TW **laser** & 16.5 GeV **e⁻ beam**
- ▷ e⁻ / laser interaction mode and γ / laser interaction mode
- ▷ Vast range of multiplicities per beam bunch depending on the mode of operation
 - up to 10^6 e⁺e⁻ pairs per BX
 - Physics-driven detector technologies at each location

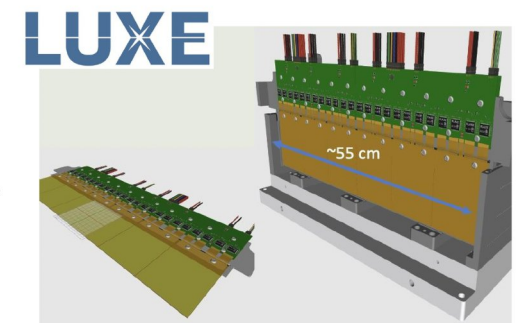


A. Irles



ECALp design

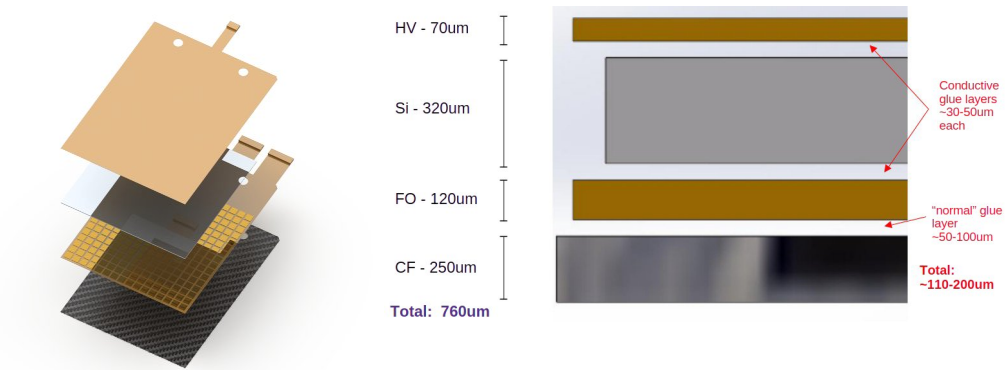
- ▷ Highly **compact and modular calorimeter** to **minimize** the **Molière radius**. Design based on the concept considered by the FCAL collaboration for compact calorimeters for luminosity measurement at future Higgs factories. Based on thin silicon sensors developed previously for CALICE (16×16 pads 5.5×5.5 mm²).
- ▷ Silicon – tungsten planes
- ▷ Six sensors per plane (~55cm)
- ▷ 20 active planes (21 W plates)
- ▷ Distance between tungsten plates : 1mm
- ▷ Front End Boards above the sensors : readout and HV
- ▷ Dedicated electronics (FLAXE) developed for LUXE
- ▷ **Test beam with single sensors (Si, GaAs) in 2022**
 - Eur.Phys.J.C 85 (2025) 6, 684
- ▷ **Test beam with 20 sensors in June 2025**



LUXE experiment

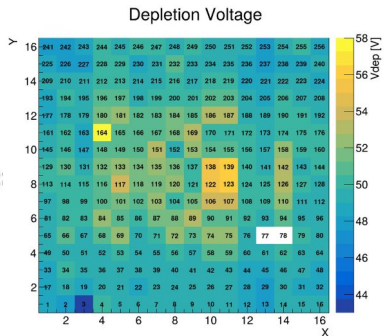
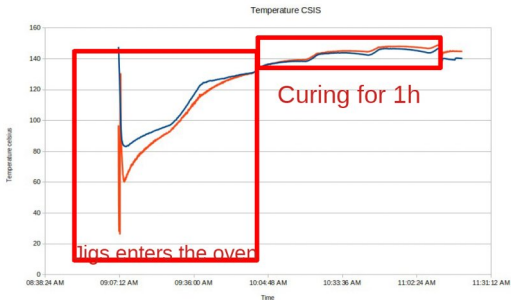
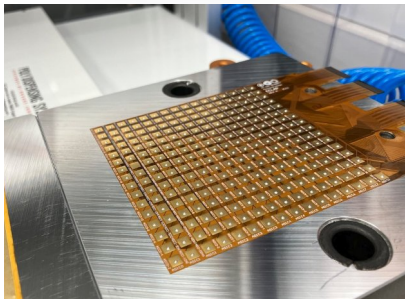
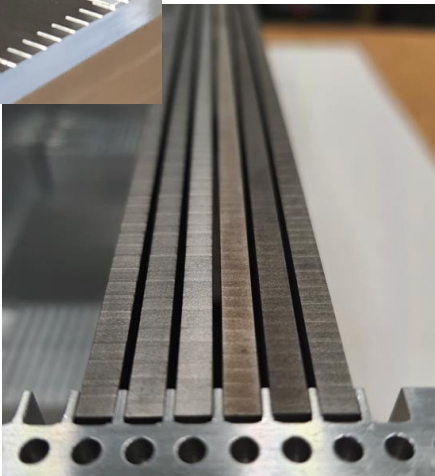
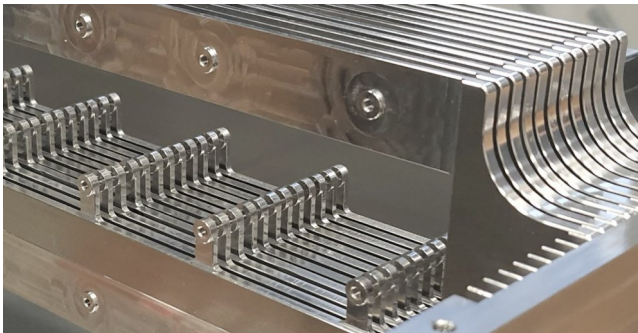
SiW 'CALICE' Sensors (320μm) + Kaptons

- 90 units, all tested (TAU) ↔ IFIC / CERN



Highly Compact Tungsten structure

- Precision



Electronics & some selected results

ECALp readout : FLAXE-FLAME

▷ Based on previous developments FLAME ASIC: developed for the luminosity detector at future e+e- accelerators.

- **FLAME has been extensively tested → including in the last beam test in 2025**

▷ Main features

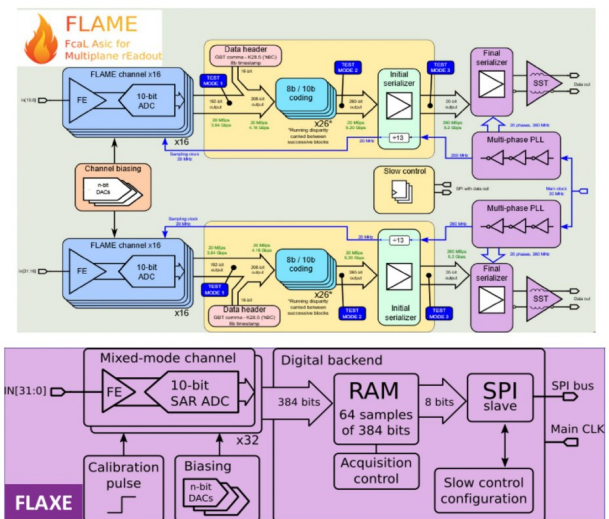
- 32 channels
- 10 bit ADC at 20 MHz **in each channel**
- Analog front end in each channel. CR-RC shaper of 50 ns
- High speed serialize

- ▷ FLAXE is similar but w/o the high speed serializer

- Acquisition at LUXE frequency (10 Hz)

▷ Production failure in 2024.

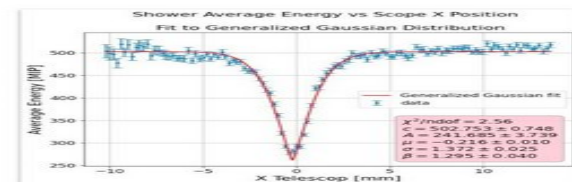
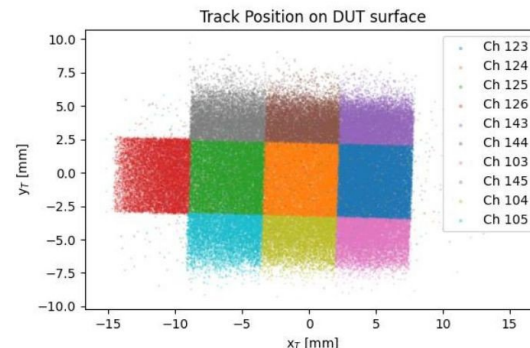
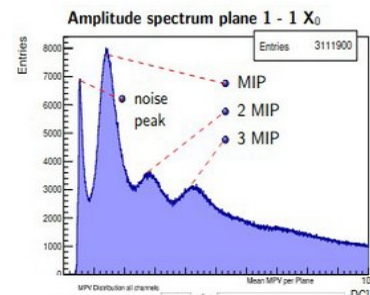
- New production in 2025-2026 (MORE INFO in the backup)



<https://iopscience.iop.org/article/10.1088/1748-0221/20/01/C01026/pdf>

Developments from AGH Krakow

Beam test, DESY 2025



1511-1512

Many more results!!! Shower profiles, Energy response, etc.

- Cf A.F. Zarnecki presentation at ILD Monthly meeting, May 2026

Vincent.Boudry@in2p3.fr

Calorimeters for ILD at FCC-ee | 15/09/2026, CER.

Adaptations

How to adapt calorimeters to FCC-ee conditions

CALICE calorimeters:

- Embedded readout:
compact design & DAQ
- Minimal consumption by power pulsing
 - 1–2ms readout , 198–199 ms off.
 - Passive cooling → no dead materials

1) Rates and cross-sections

- Z-peak out-of-scale wrt all the other configurations
 - One detector fits all ? “optimal” granularity ?
- DAQ Scheme ? Continuous readout ?

2) Continuous running

- Electronics base consumption $\times$ 100–200 wrt ILC

3) New opportunities: timing in calorimeters

- Adds consumption
- Large potential but at what cost ? What precision ?

Linear → Circular Collider's Conditions (old)

Linear (ILC, HL-ILC...)

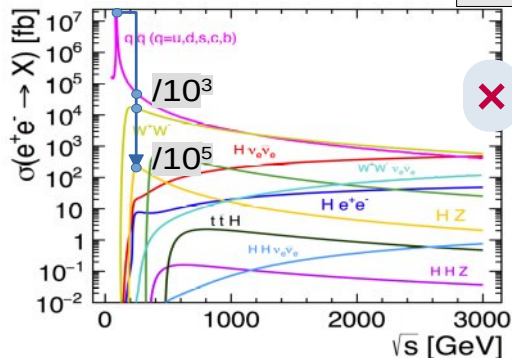
- 250 GeV (ZH), 365 GeV (tt), 500 GeV (ZHH) + [1000 GeV], $\mathcal{L} \sim \text{cst.}$
- Power pulsing : 5 [10–15]Hz $\times$ 1 [2] ms Power $\sim \mathcal{L}$.

More diverse et stringent conditions:

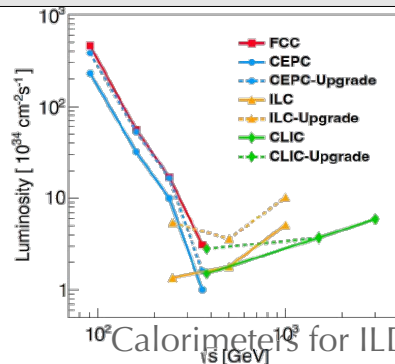
- 90GeV $\times$ $10^7 \text{ fb} \times 5 \cdot 10^{36} \text{ cm}^{-2} \text{ s}^{-1}$ (qq $\times$ 20,000 ILC @ 250)
- 150 GeV (WW) + 250 GeV (ZH) + 365 GeV (tt)
 $\sim 10^4 \text{ fb} \times 5 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (qq $\times$ 5–10 ILC @ 250)

From Pulsed to Continuous operation

- Power = **cst** + conversion+RO $\times$ local rates ($P_{\text{Conv}} + P_{\text{RO}} \sim 40\% P_{\text{ACQ}}$)
- ASIC, Power/Cooling, DAQ, Granularity, Precisions (E, t), New ideas...



Status of the CEPC, October 2022 J. Guimarães da Costa



Calorimeters for ILD at FCC-ee | 15,

HL-ILC:

- $\mathcal{L} \times 4$ (6)
- $N_{\text{bunches}} \times 2 : \tau_{\text{Train}} : 1 \rightarrow 2 \text{ ms}$
- $f_{\text{rep}} \times 2$ (3): $5 \rightarrow 15 \text{ Hz}$

Dominated by ACQ time:

$$P(\sim 25 \mu\text{W}/\text{ch}) \times 6$$

HL-CLIC:

- $\mathcal{L} \times 2$
- $N_{\text{bunches}} \rightarrow : \tau_{\text{Train}} : 176 \text{ ns}$
- $f_{\text{rep}} \times 2 : 50 \rightarrow 100 \text{ Hz}$

Dominated by Set-up &

Conversion time: $P(\sim 82 \mu\text{W}/\text{ch}) \times 2$

FCC-ee parameters		Z	W ⁺ W ⁻	ZH	ttbar
$\sqrt{s}$	GeV	91.2	160	240	350-365
Luminosity / IP	$10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	230	28	8.5	1.7
Bunch spacing	ns	19.6	163	994	3000
"Physics" cross section	pb	35,000	10	0.2	0.5
Total cross section (Z)	pb	40,000	30	10	8
Event rate	Hz	92,000	8.4	1	0.1
"Pile up" parameter [μ]		10^{-6}	1,800	1	1

Experimentally, Z pole most challenging

- Extremely large statistics
- Physics event rates up to 100 kHz
- Bunch spacing at 20 ns
 - "Continuous" beams, no bunch trains, no power pulsing
- No pileup, no underlying event ...
 - ...well, pileup of 2×10^{-3} at Z pole

<https://indico.cern.ch/event/1064327/contributions/4893208/>
 Mogens Dam @ FCC Week, 10/06/2022

Linear → Circular Collider's Conditions (current)

Linear (ILC, HL-ILC...)

- 250 GeV (ZH), 365 GeV (tt), 500 GeV (ZHH) + [1000 GeV], $\mathcal{L} \sim \text{cst.}$
- Power pulsing : 5 [10–15]Hz × 1 [2] ms Power $\sim \mathcal{L}$.

More diverse et stringent conditions:

- 90GeV × $10^7 \text{ fb} \times 5 \cdot 10^{36} \text{ cm}^{-2} \text{ s}^{-1}$ (qq × 20,000 ILC @ 250)
- 150 GeV (WW) + 250 GeV (ZH) + 365 GeV (tt)
 $\sim 10^4 \text{ fb} \times 5 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (qq × 5–10 ILC @ 250)

From Pulsed to Continuous operation

- Power = **cst** + conversion+RO × local rates ($P_{\text{Conv}} + P_{\text{RO}} \sim 40\% P_{\text{ACQ}}$)
- ASIC, Power/Cooling, DAQ, Granularity, Precisions (E, t), New ideas...

HL-ILC:

- $\mathcal{L} \times 4$ (6)
- $N_{\text{bunches}} \times 2 : \tau_{\text{Train}} : 1 \rightarrow 2 \text{ ms}$
- $f_{\text{rep}} \times 2$ (3): $5 \rightarrow 15 \text{ Hz}$

Dominated by ACQ time:

$$P(\sim 25 \mu\text{W}/\text{ch}) \times 6$$

HL-CLIC:

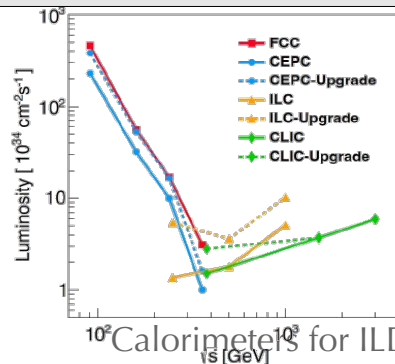
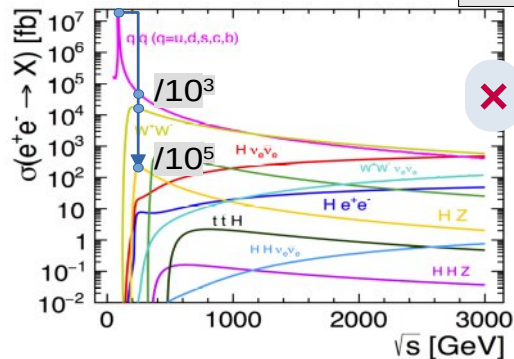
- $\mathcal{L} \times 2$
- $N_{\text{bunches}} \rightarrow : \tau_{\text{Train}} : 176 \text{ ns}$
- $f_{\text{rep}} \times 2 : 50 \rightarrow 100 \text{ Hz}$

Dominated by Set-up &

$$\text{Conversion time: } P(\sim 82 \mu\text{W}/\text{ch}) \times 2$$

FCC-ee parameters		Z	W ⁺ W ⁻	ZH	ttbar
$\sqrt{s}$	GeV	91.2	160	240	350-365
Luminosity / IP	$10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	140	20	7.5	1.5
Bunch spacing	ns	25	160	680	5000
"Physics" cross section	pb	35,000	10	0.2	0.5
Total cross section	pb	70,000	30	10	8
Event rate	Hz	100,000	6	0.5	0.1
"Pile up" parameter [μ]	10^{-6}	2,500	1	1	1

Status of the CEPC, October 2022 J. Guimarães da Costa



Experimentally, Z pole most challenging

- Extremely large statistics
- Physics event rates up to 100 kHz
- Bunch spacing at ~~20 ns~~ **25 ns**
 - "Continuous" beams, no bunch trains, no power pulsing
- No pileup, no underlying event ...
 - ...well, pileup of 2×10^{-3} at Z pole

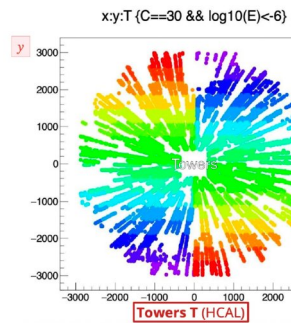
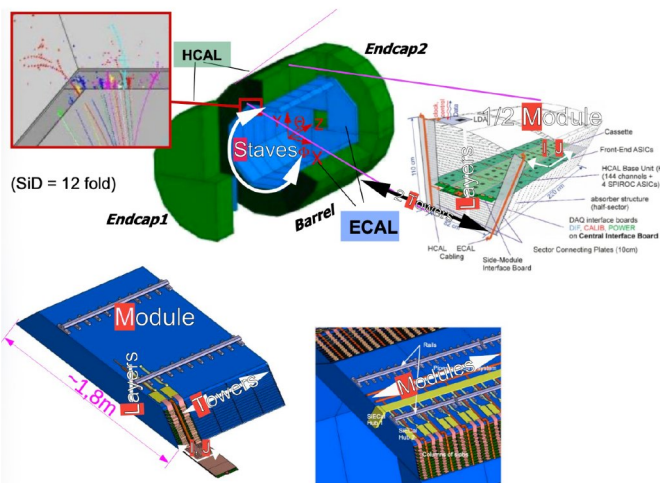
<https://indico.cern.ch/event/1064327/contributions/4893208/>
 Mogens Dam @ FCC Week, 10/06/2022

Power and Rates estimations using CaloFlux

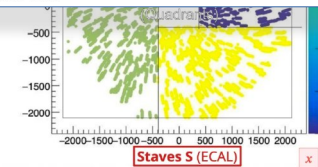
V. Boudry, K. Hassouna Work continued by
M. Akbiyik (KIT)

– (mixed sensor) simulations of

- Main processes $\times \mathcal{L}$
- Update on background $\times f_{\text{BX}}$ (100 BX $\rightarrow$ 4000BX)
- Use of ILD_FCCee_v01_detailed MDI



Towers & staves



Signal samples at 91.2 GeV & Geometry

Table 2. $\sqrt{s} = 91.2 \text{ GeV}$
($N = 10000$, $\mathcal{L} = 1.4 \times 10^{-3} \text{ fb}^{-1} \text{ s}^{-1}$).

Channels	σ (10^3 fb)	$\sigma \times \mathcal{L}/N$ (s^{-1})
$e^+e^- \rightarrow q\bar{q}$	344	4.82
$e^+e^- \rightarrow \ell\bar{\ell}$	34.6	0.484
$e^+e^- \rightarrow \ell\bar{\ell}$ ($M_{ee} < 30 \text{ GeV}$)	1.01	0.0141
$e^+e^- \rightarrow \ell\bar{\ell}$ ($M_{ee} > 30 \text{ GeV}$)	57.8	0.809

Systems	Staves	Modules per stave	Towers per module	Layers
ECAL-Barrel	8	5	5	30
ECAL-Endcap	4	2	9	30
ECAL-Ring	1	2	1	30
HCAL-Barrel	8	2	2	48
HCAL-Endcap	2	2	16	48
HCAL-Ring	4	2	1	7

ILD calorimeter geometry.

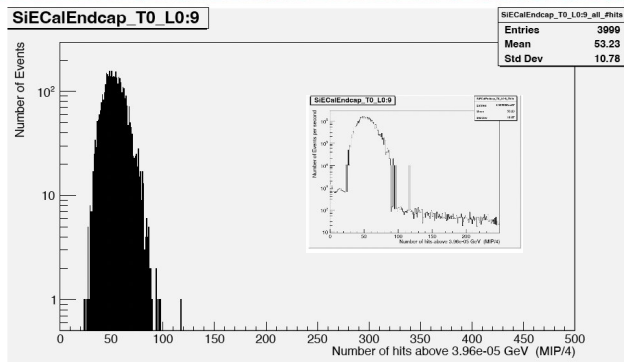
- qq90 (quark pairs): lots of hadronic activity $\rightarrow$ most hits
- ll90 (lepton pairs): cleaner events but still significant.
- $M_{ee} < 30 \text{ GeV}$ ($\sigma = 1.01 \times 10^3 \text{ fb}$): The region where the pair's invariant mass is much smaller than the 91.2 GeV beam energy, kinematically this is where the t-channel piece, unique to Bhabha scattering, the $<30 \text{ GeV}$ slice isolates the part of Bhabha scattering that has no analogue in $\mu\mu/\tau\tau$ (the residual t-channel piece).
- $M_{ee} > 30 \text{ GeV}$ ($\sigma = 57.8 \times 10^3 \text{ fb}$): here the pair is produced with invariant mass close to the full CM energy, meaning it's dominated by the s-channel Z resonance — the same diagram that produces $\mu\mu$ and $\tau\tau$, while the $>30 \text{ GeV}$ slice is the part that is physically the same s-channel process as the generic $\ell\bar{\ell}$ row above it.
- Here: https://github.com/LLR-ILD/CalorimeterFluxes/tree/main/Histograms/1D_histograms/GV91.2

September 2026

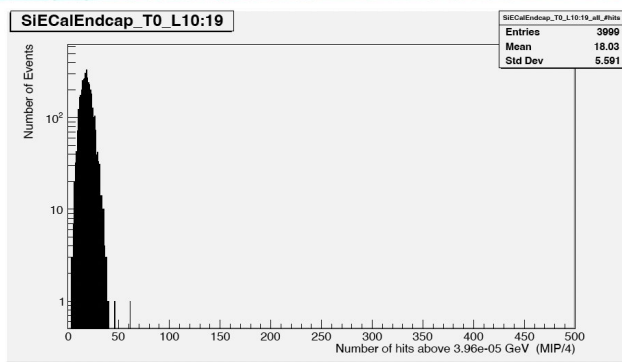
Melike Akbiyik (melike.akbiyik@kit.edu)

IPC background in SiW-ECAL EndCaps

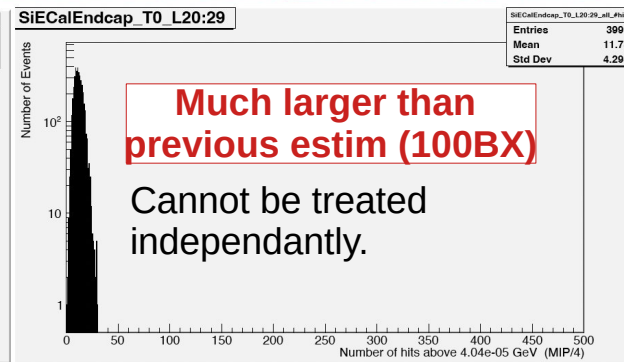
Comparison *All #Hits* : SiECALendcap T0 4k BX sample (2025) VS 100 BX (2023)



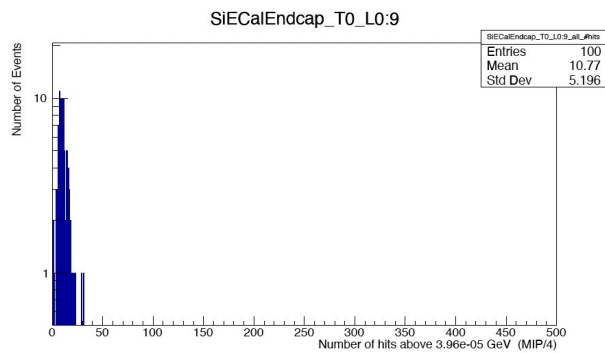
4k Bx



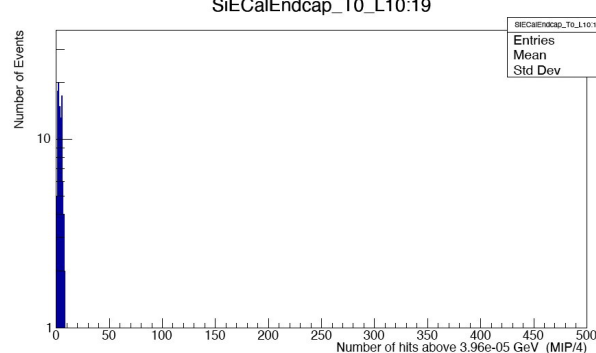
4k Bx



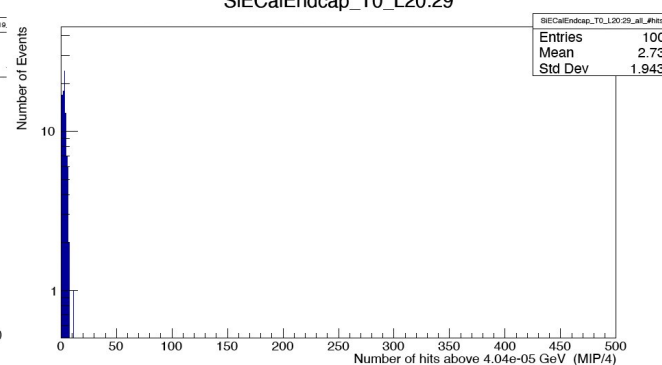
4k BX



100 Bx



100 Bx



100 Bx

Estimation of Power and Rates (no SR!!!)

SK2 in SiW-EndCaps

Metric	Layers 0–9	Layers 10–19	Layers 20–29
Average hit rate	2.13×10^9 hits/s	729×10^6 hits/s	475×10^6 hits/s
Noise hit rate	3×10^6 hits/s	3×10^6 hits/s	3×10^6 hits/s
Maximum hits per event	1,040	1,830	900
Data rate	14.94 GB/s	5.10 GB/s	3.32 GB/s
Number of cells	3,729,560	3,729,560	3,729,560
Occupancy per bunch crossing	1.1×10^{-5}	3.7×10^{-6}	2.4×10^{-6}
Base power	16.8 kW	16.8 kW	16.8 kW
Conversion power	1.921 kW	655.8 W	427.1 W
Total power	18.7 kW	17.4 kW	17.2 kW
Conversion share	10.27%	3.76%	2.48%

To be consolidated

cell size	5,5
Bytes/hit	7
powa (W/cell)	4,5 E-03
powb (J/hit)	8,7 E-10
Conv & RO E/hit/μJ	9,0 E-01
Δt/s	19 E-09

Calculation parameters:Bunch-crossing frequency: 5.263×10^7 Hz ·

Klaus6 in AHCAL

Metric	Layers 0–15	Layers 16–31	Layers 32–48
Average hit rate	847×10^6 hits/s	701×10^6 hits/s	677×10^6 hits/s
Noise hit rate	220.1×10^3 hits/s	220.1×10^3 hits/s	220.1×10^3 hits/s
Maximum hits per event	505	422	292
Data rate	5.08 GB/s	4.21 GB/s	4.06 GB/s
Number of cells	278,756	278,756	278,756
Occupancy per bunch crossing	5.8×10^{-5}	4.8×10^{-5}	4.6×10^{-5}
Base power	4.5 kW	4.5 kW	4.5 kW
Conversion power	317.5 W	262.8 W	254 W
Total power	4.8 kW	4.7 kW	4.7 kW
Conversion share	6.65%	5.57%	5.39%

Cooling

Towards a Compact cooling system

“Boosted Standard Slab”

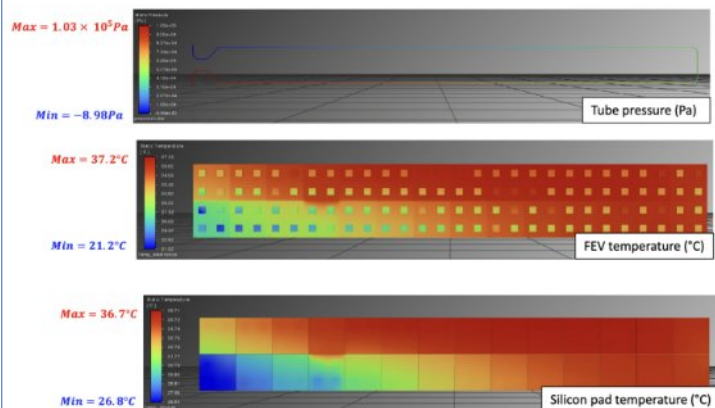
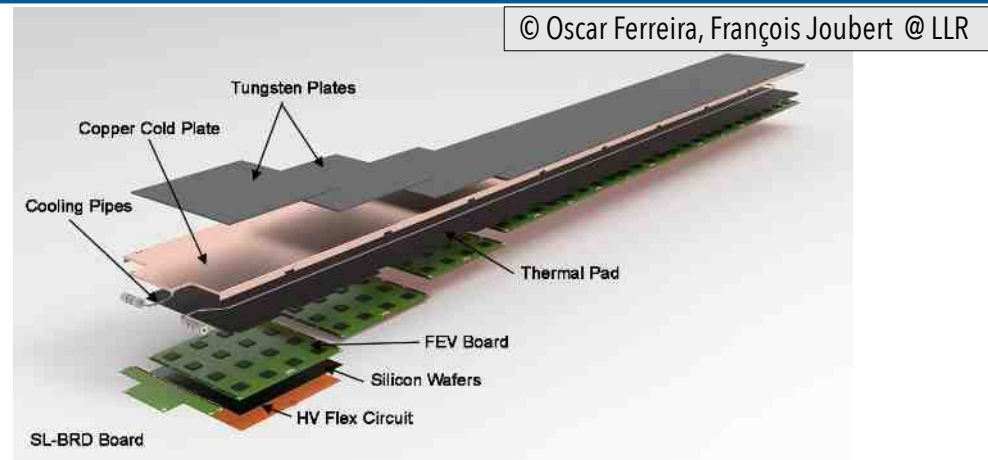
- 210W (30W/ASU) : ASICs + Concentrators + PS...
- (ILC like in CC ~ 130W)

Active cooling:

- 4 mm Cu plate with 1/8" Stainless Steel Tubing
- 0.2 ℓ /min of water @ 15°C

Simulations

Adiabatic, but for heat bridge at the end, $t = \infty$



Inlet flow rate : 0.25L/min

Results :

- Pressure drop : 1.03 bar
- Silicon temperature gradient : 9.87°C**

- Preliminary results resumed in the following graphs.
- Operating point between **0.25 L/min** and **0.45 L/min** for allowable pressure drops.

Active Cooling for ECAL

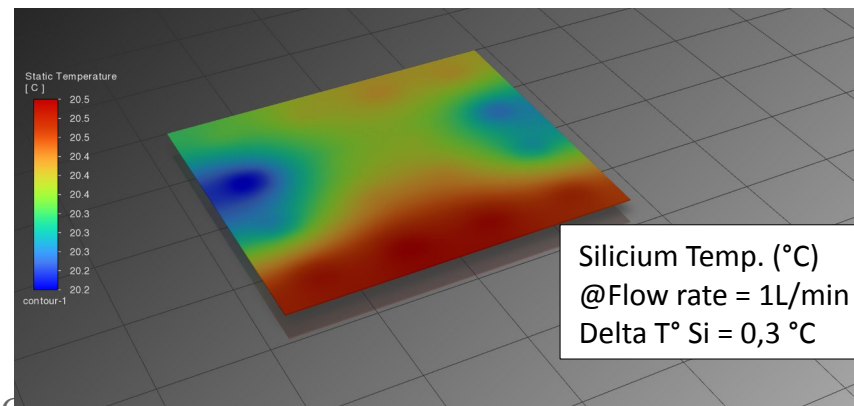
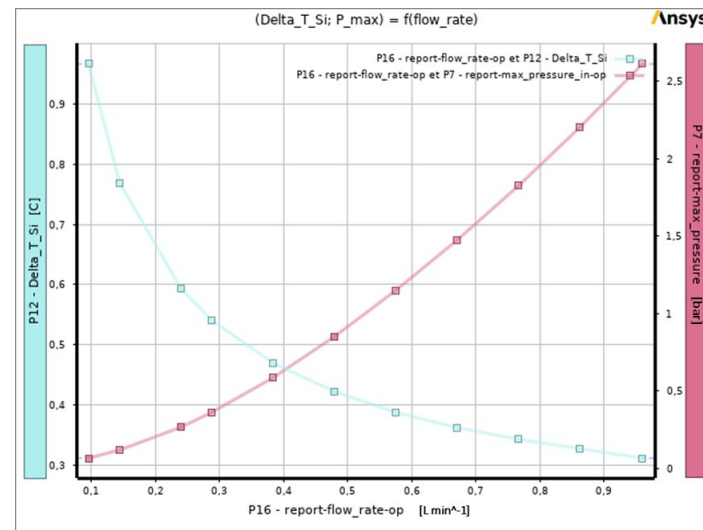
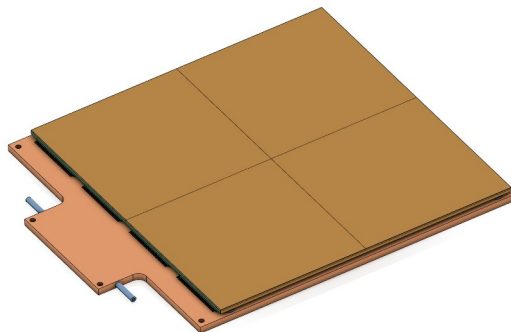
work from F. Joubert, O. Ferreira, J. Nanni (LLR)

Constraints:

- Water cooling of slab (8 FEV) from a single end
 - Thermal power : **~30W** (16 ASIC)
 - Cold point : 15°C
 - Water Flux ($0.1 < Q < 4\text{L/min}$)
 - Pressure: $0 < P < 5\text{ bar}$

Preliminary Simulation studies: 1 FEV

- ANSYS
- To be redone with updated design



Cold Plate Test bench

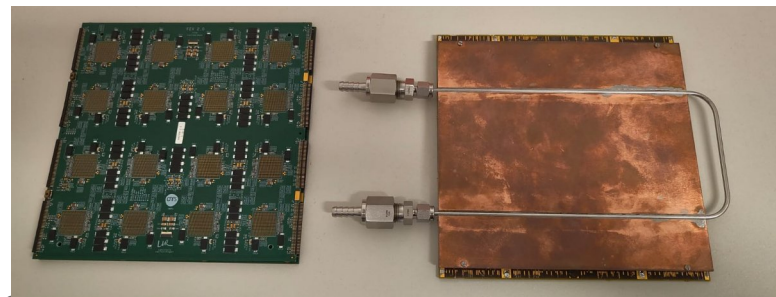
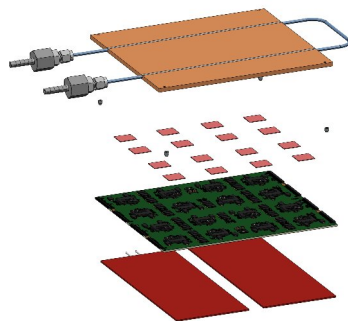
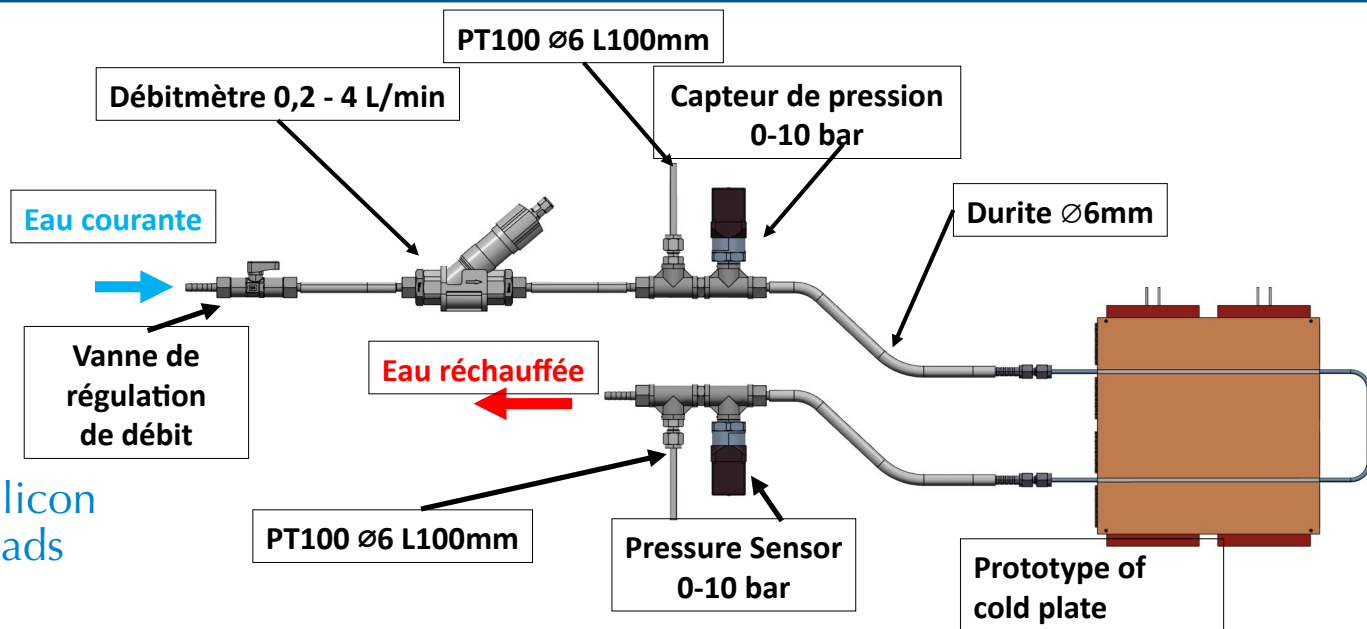
Prototype : 1 Fake FEV

- Cold plate in Copper with grooves for stainless steel pipe (1/8")
- Curbing of pipes
- Soldering with tin (à la HGCAL...)
- Existing PCB with ASIC or Silicon
→ 3D fake ASIC + heating pads
- An Adiabatic box

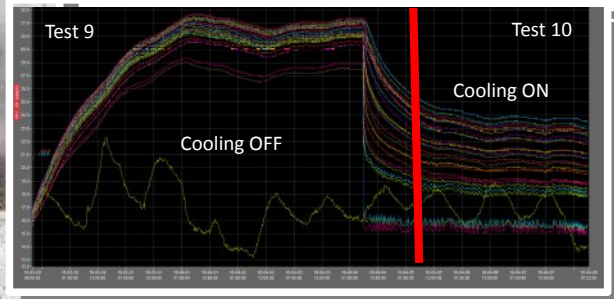
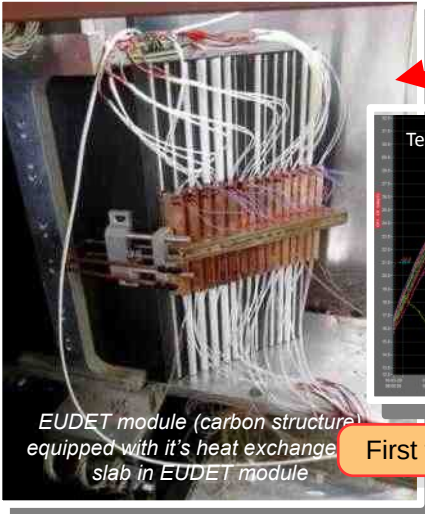
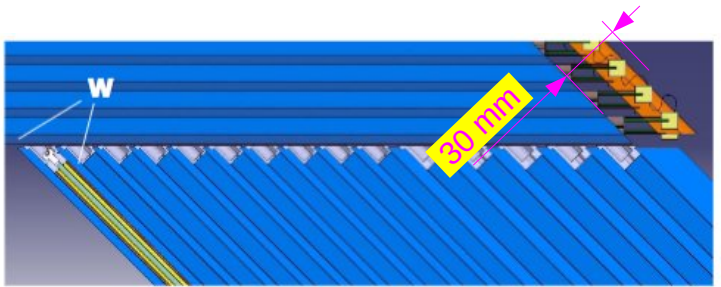
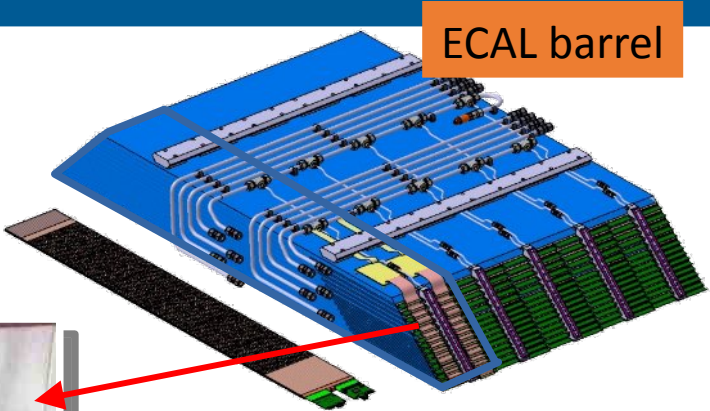
Instrumentation

- Thermal, pressure, flow sensors + DAQ

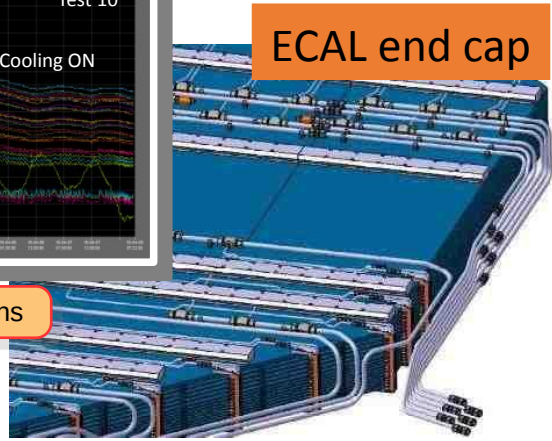
Being mounted... results by end 2028



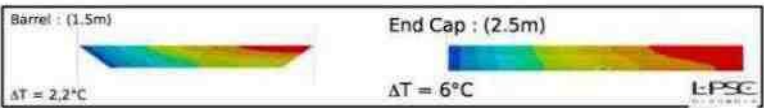
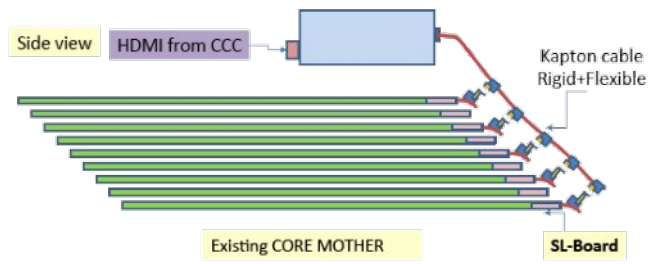
Cooling



First tests results in line with simulations



DAQ



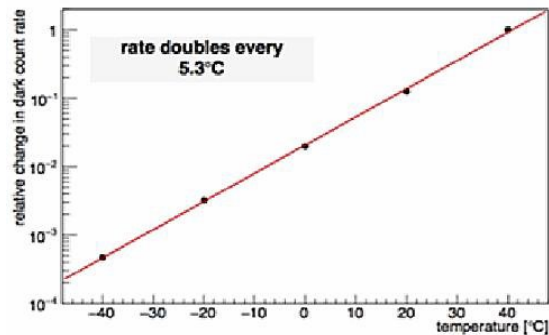
AHCAL cooling studies

Mostly work from A. Klotzbücher

3 month stay at LLR beg. 2026

Objectives:

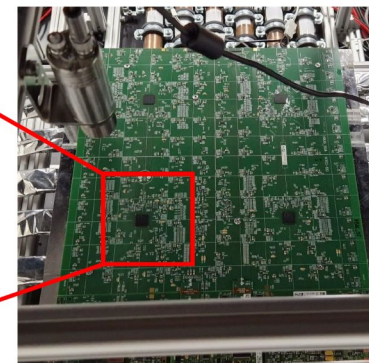
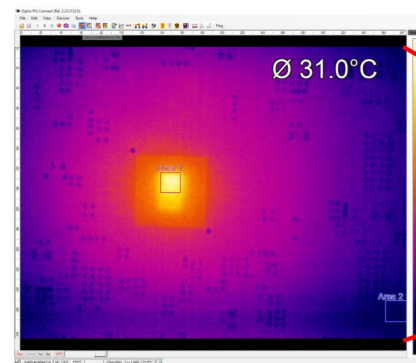
- Low maximum temperature (SiPM DCR, electronics)
- Minimal temperature gradient (uniform SiPM gain via overvoltage correction)



Picture taken from <https://hub.hamamatsu.com/us/en/technical-notes/mppc-sipms/what-are-the-effects-of-temperature-on-dark-count-rates-in-an-SiPM-MPPC.html>

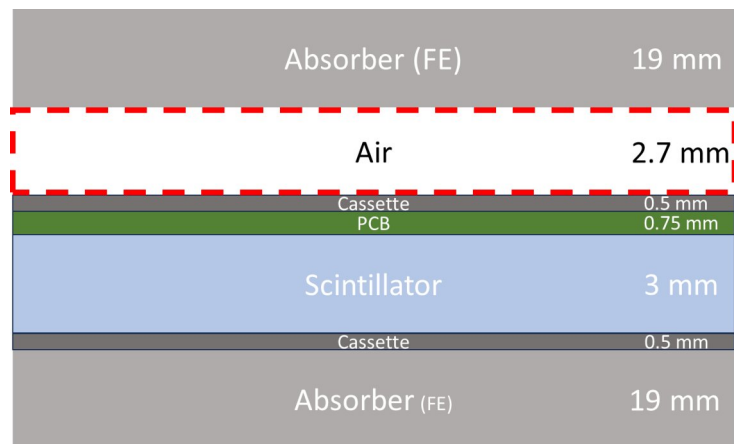
Temperature Distribution on the HBU

- Temperature measurements with thermal imaging camera
- ASICs power consumption in continuous mode: 3.34 mW/ch. → **120 mW per chip**



Cooling designs

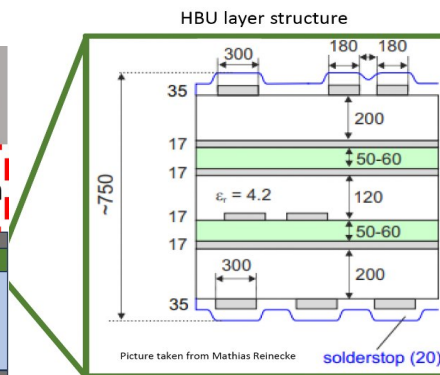
Simplified design (à la CLD):



Inspiration taken from "CLD - A Detector Concept for the FCC-ee" (<https://arxiv.org/pdf/1911.12230>)

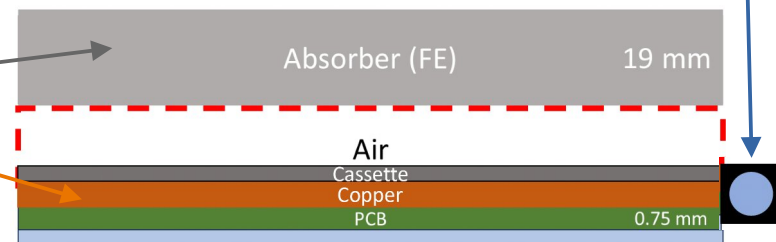
Test of Solutions

- Using ground planes in the PCB



Water based cooling
at as inle-end of the slab

- Just the Absorber
- A Copper plane
- A combination of Both



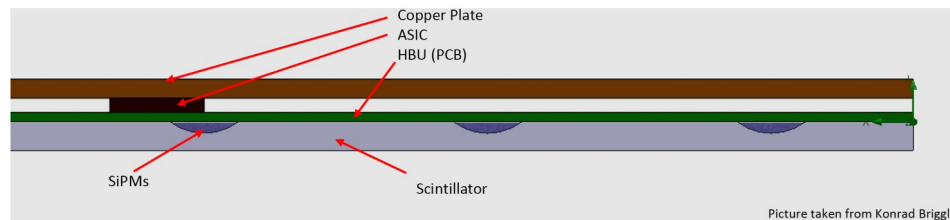
Thermal Simulation based on measurements

Simulations done with Heidelberg & LLR Groups

- Models the cooling system for the whole detector
- Needs calibration

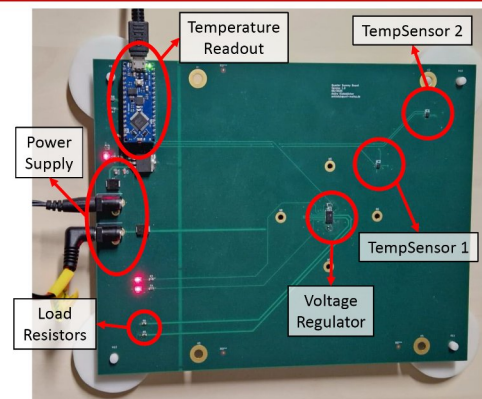
Lab measurements done in Mainz:

- Determines thermal conductivity of the PCB and to the heat spreader
- Contact pressure of the heat spreader



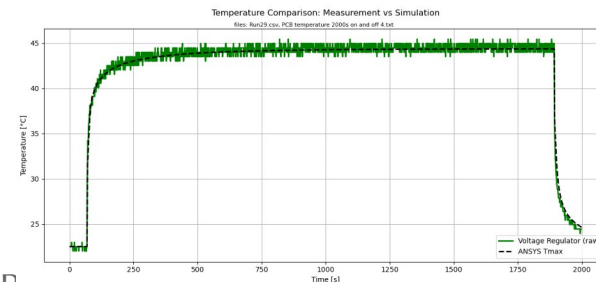
Dummy Board

- Dummy HBU to mimic ASIC heat production
- “Main part”:
 - 18 cm x 18 cm (1/4 of HBU)
 - Voltage regulator as heat source
 - Temperature sensors
- “Extension”:
 - 18 cm x 5 cm
 - Used for placement of power supply, sensors readout...



Measurements

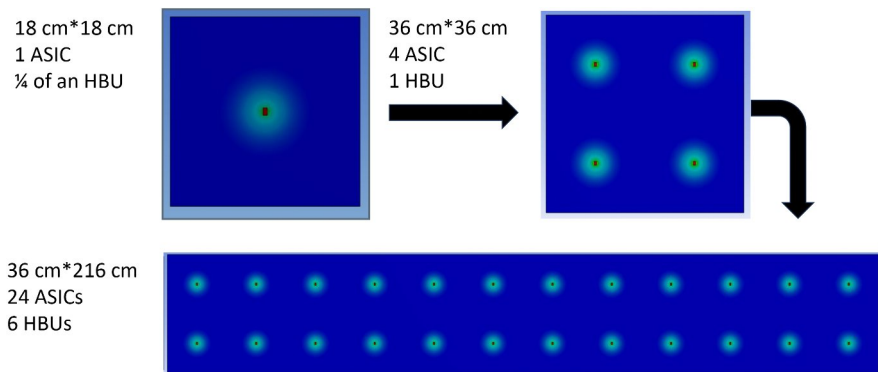
- with and without copper plate
- temperature sensors and thermal imaging camera
- ANSYS sim.



Scaling to a Full Slab and Module

Full Slab

- Power Input: 120 mW/ASIC $\rightarrow$ **2.88 W** for the slab
- Convections off; Cooling with 10 °C at one side of the slab
- Thermal coupling from measurements
- Important values:
 - Maximum Temperature
 - Temperature gradient at the bottom side of the Slab (Scint + SiPM)



Cooling Material	Thickness	T max (°C)	ΔT (°C)
Copper plane	35 μm	614.1	596.4
Copper plane	140 μm	165.9	152.7
Copper plate	1 mm	36.2	16.4
Copper plate	3 mm	22.5	5.6
Copper plate	5 mm	19.6	3.4
Stainless Steel Absorber	19 mm	44.6	22.6
Copper Plate + Stainless Steel	1 mm + 19 mm	27.7	9.8
Copper Plate + Stainless Steel	3 mm + 16 mm	21.3	4.7

Combination of absorber and copper plate:

- Maximum temperature sufficiently low
- Best trade off between less additional material and smaller temperature gradient
- Challenge: achieving good thermal coupling between all components

Impact on physics (Λ_i , X_0) ~ very small

- Simulating detector response using Key4HEP
- Key observables: λ , X_0 , energy leakage, backscattering fraction
- Comparison with the current CLD detector design

	Steel Absorber [mm]	Copper [mm]	Integrated X_0	Integrated λ	$\frac{\lambda}{X_0}$
Current Design	20.0	0.0	56.51	6.11	9.25
Variation 1	18.0	2.5	59.42	6.32	9.41
Variation 2	15.5	5.0	60.97	6.38	9.55

To select the right option: **Mechanical feasibility; Thermal coupling**

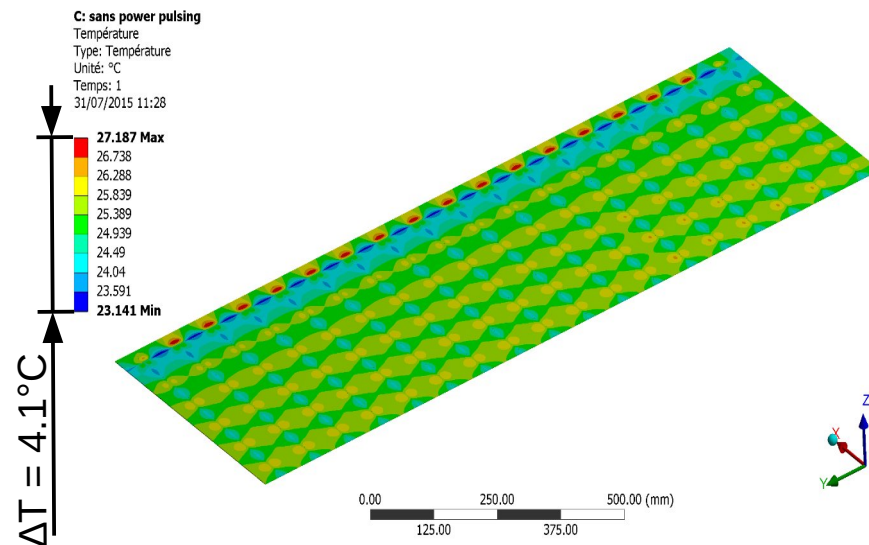
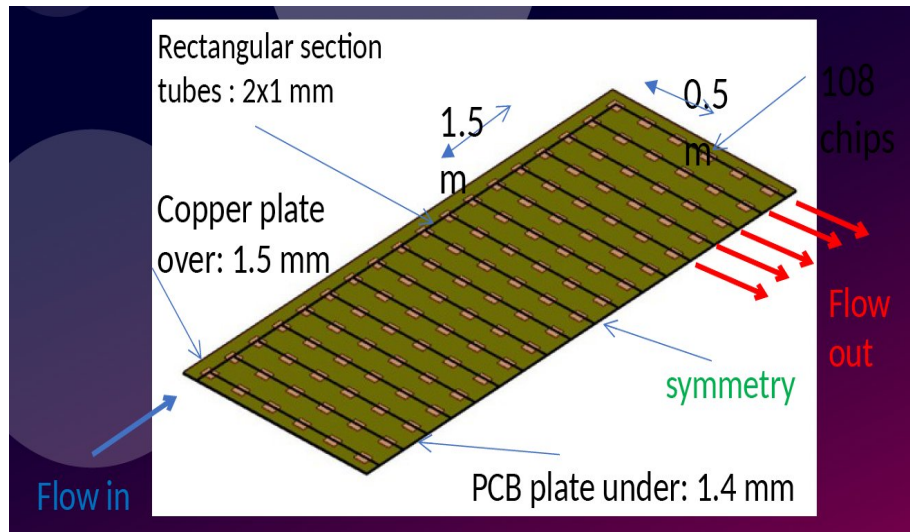
T-SDHCAL: cooling & rates

Cooling:

Previous studies were performed on Hardroc (full regime : 80 mW/ch)

Active cooling needed and worked on for SDHCAL (Lyon&Shanghai groups) using water circulating into copper pipes

Next studies and technical implementation will be done at CIEMAT.



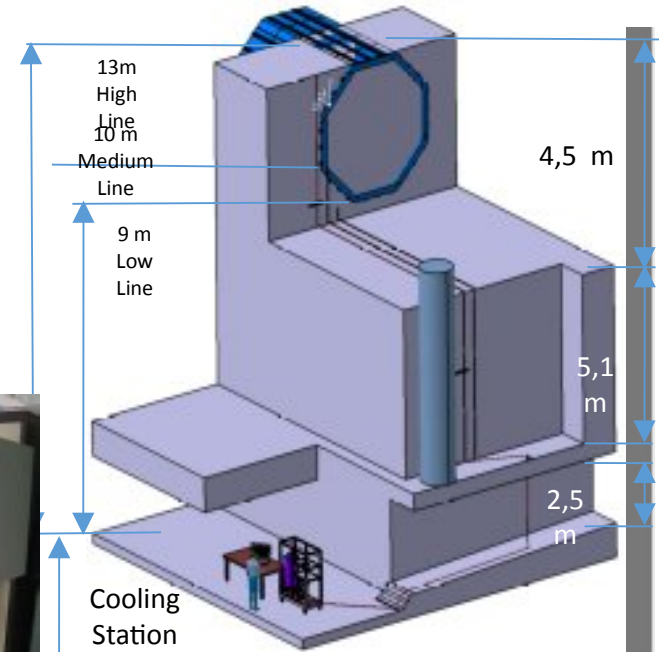
Leakless Water cooling system

Thermal Integration by LPSC (Grenoble)



Goals

- Heat evacuation at end of slabs
- Leakless (depression)
- Designed for ILC → needs full rescaling



LPSC cooling test area with a drop of 13 m

Electronics

❑ CALOROCs common features

- ❑ 36 channels $\sim 10\text{-}15$ mW/ch
- ❑ Auto-trigger and Streaming readout : 2 links @ 1.28 Gb/s
- ❑ Triplicated I2c configuration and fast commands inputs
- ❑ TSMC 130n technology
- ❑ BGA package : same pinout

❑ Conservative **CALOROC1A**: SiPM readout from H2GCROC

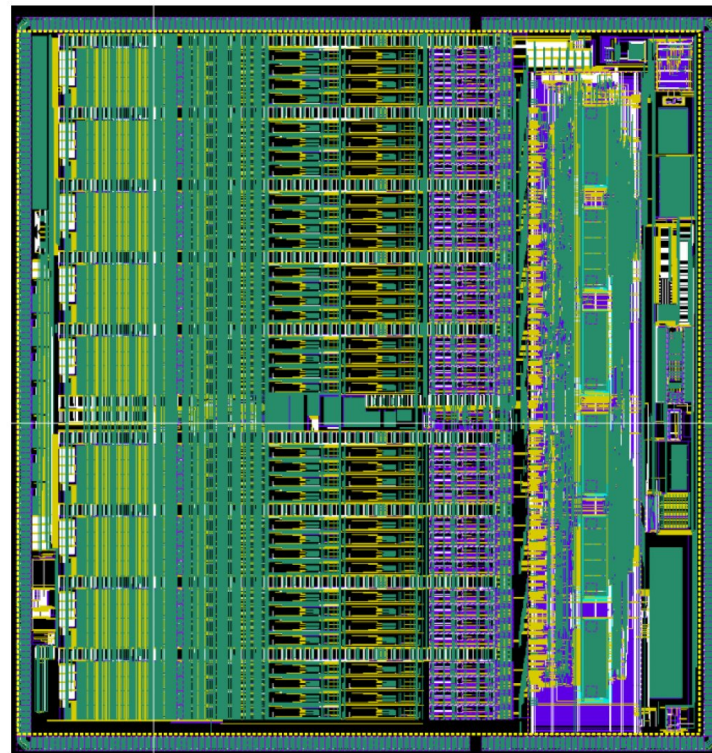
Reserved for EIC calo

❑ New **CALOROC1B**: SiPM readout with gain switching

- ❑ New analog front end : higher dynamic range and input capacitance
- ❑ Lower noise, better jitter

❑ **CALOROC1C** for Si/LAr detectors: Si readout from HGCROC

- ❑ Slower shaping
- ❑ Cryogenic temperature adjustment



Testing 1B

❑ CALOROC characterization motherboard under design at OMEGA:

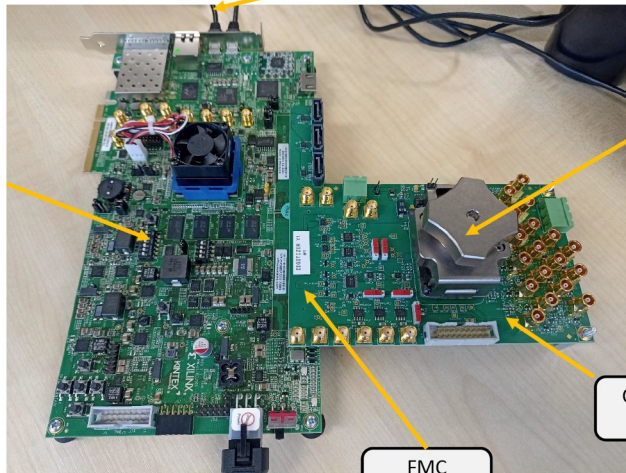
- ❑ Originally developed for HGCROC and the HKROC
- ❑ Well-known at OMEGA and LLR (firmware based only)
- ❑ Compatible with KRIA motherboard (CERN) but software + firmware needed

Python scripts

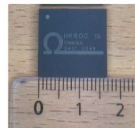


Monitor
Program
Test

Commercial
KCU105 board



CALOROC
BGA socket



Custom CALOROC
motherboard

FMC
connector

Custom motherboard
+ KRIA module

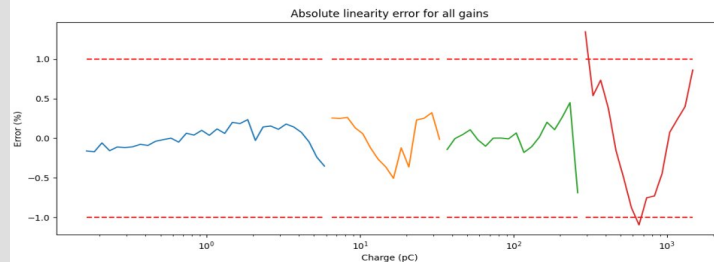
CdLT DRDCALO WP4 30 jun 2026

5

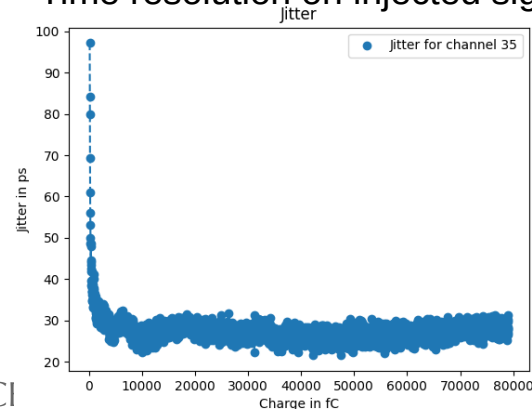
> May 2026

– Good results, e.g.

Non-linearity 1B < 1%



Time resolution on injected signal:



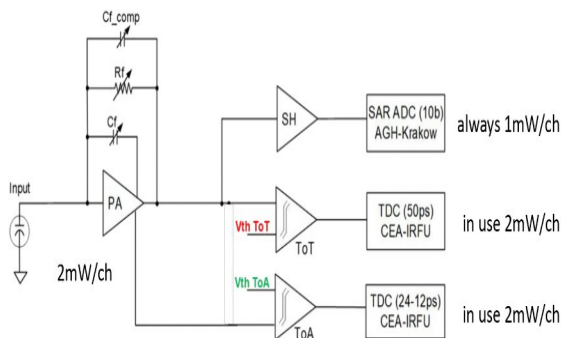
CALOROC 1C (ℓ Ar / Si)

CALOROC1C Requirements and Test Setup

	LAr (FCC)	Si
Function	Charge Measurement	Charge and Time Measurements
MIP	2.25fC (750keV)	4fC
Dynamic Range	0.2fC - 4.5pC (70keV - 1.5GeV)	0.4fC - 10pC
Temperature	87K	Ambient T
Cdet	50 - 220pF	20 - 50pF
Crosstalk	<1%	<1%

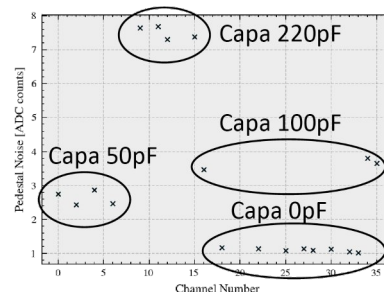
Low Power: solutions:

- Remove PLL and reduce ADC frequency
- Increase shaping time and lower the current
- Reduce the number of bits of the ADC/TDC
- Turn off the ADC when not in use
- Turn off TDC

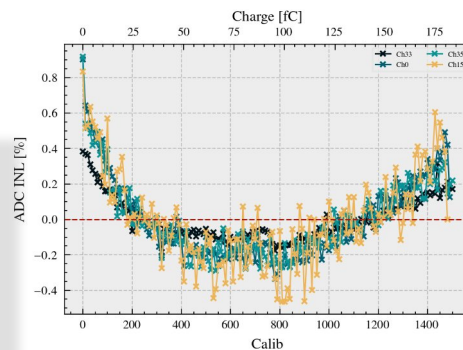


Noise for various Cdet

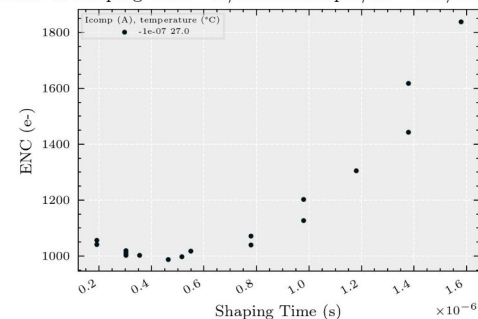
The expected range of detector capacitances is tested.



Non linearity < 1% ; ENC vs shaping times



ENC vs Shaping Time - Si/Perfect Shaper/Rf = 1M/Cdet = 50p



Caveats

Annoyances

- Producers & packagers captured by data centres
 - > 6 month delay in get 1st version of CALOROC

Major threat:

- In June, TSMC announced stopping 130 nm in September (for AI usage...)
 - Delayed by ~1 year
 - Tech prod (no more new items) to be transferred to a sub-company
- Shift to 65 nm ? $\Rightarrow$ cost $\times$ ~2
 - Long Term ?
 - Little advantages for analogue usage
 - dyn. Range $\searrow$ $\Rightarrow$ Multiple gains, complexity...

– Other technologies ?

- Historical founders bought by car companies
 - Avoid the shortage from the COVID / Trade war
- Will need 2–3 years of adaptation

$\rightarrow$ a industrial arrangement around CERN

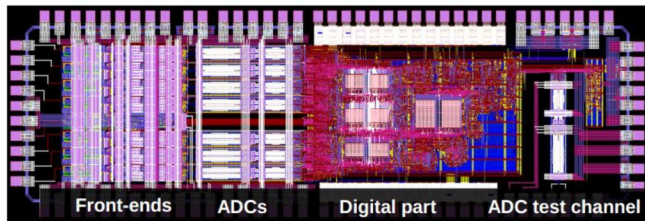
TSMC130	TSMC65	UMC110	XFAB130	VIC130
5M 1T 1U RDL C4	5M 2T 1U RDL C4	5M 1T 1U no C4?		As TSMC130
Radhard 200 Mrad	Radhard 200 Mrad	Bump @ 5 Mrad	N/A	Which fab ?
ER : 300 k\$	ER : 750 k\$	ER : 300 k\$?		
EIC	EIC, LHCb	EIC, LHCb, ALICE		
AGH, Lisbon, SLAC	FNAL, BNL, CERN	Torino		
Discontinued	Perenity ?	Low volume	6-9 months fab	Available when ?
	ADC			
DNW, HiR, CMIM	DNW, HiR, CMIM			

Status of the KLauSv7 ASIC developments

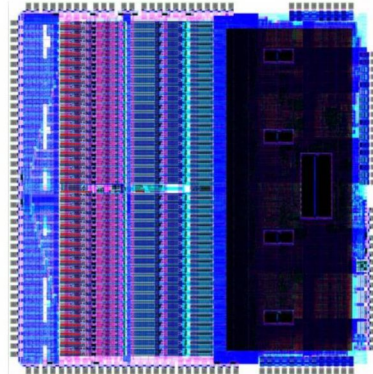
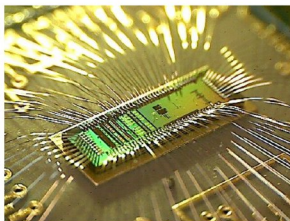
Willy Chang, DRD6 @ Ancone (Sept.2025)

KlauS ASIC R&D review

Klausv6

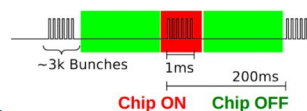


7-channel KLauS4 prototype (2016)



36-channel KLauS6 (2021 until now)

power pulsing scheme



- SiPM readout ASIC developed for CALICE AHCAL & ScECAL
- Target on low gain SiPMs (10/25 μ m pixel, 1x1/3x3 mm² area, charge range 15fC – 150pC)
- Process : UMC 180nm mixed-mode 1.8V/3.3V CMOS technology
- Power consumption : ~3 mW/channel (~26uW @ 0.5% duty cycle)
- Current version KLauS6 with 36 channels
- Analog front-end + ADC + TDC + Digital interfaces (I²C, SPI, LVDS)

Input stage:

CC-CG input + 4 distribute signal current mirrors, SiPM HV bias tuning range ~2V

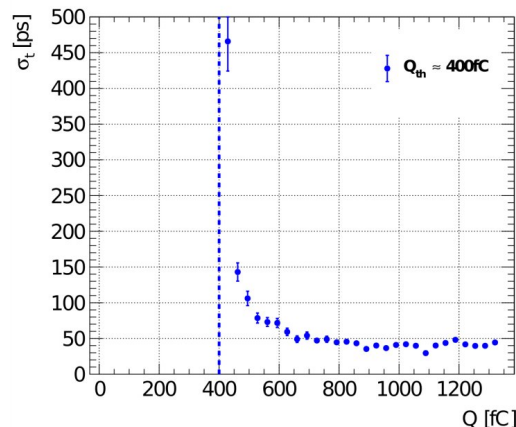
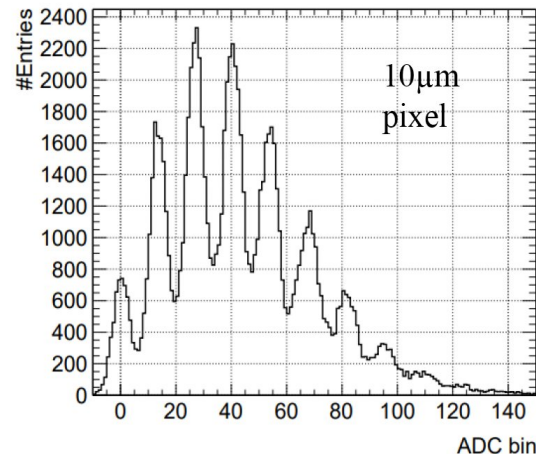
- 2 integration branches with different charge range (HG, LG)
- 2 comparator branches with timestamp hit logic + ADC start logic, HG/LG selection

SAR ADC:

- 10-bit mode - SiPM spectra for 25 μ m pixels and above
- 12-bit mode - Single pixel spectra for small gain SiPMs (pipelined mode)

TDC for time stamp recording:

- Since KLauS6: ~195ps bins, ~3.3ms dynamic range (@nominal 40MHz clock)



KlauS7: Slow + Fast Command/Readout Interface

Same A2D block as Klausv6

Moving forward to IpGBT eLink

- Reduce the number of IO pads.
- Lower design complexity of redundant bus interfaces.
- Standardize interface with IpGBT.

I²C interface:

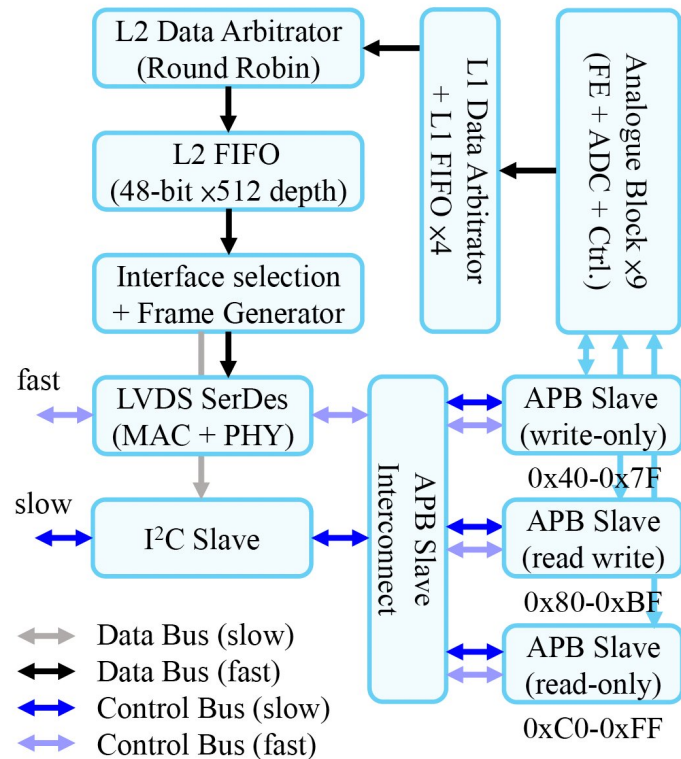
- Slow data readout, read-write status/control registers
- 1Mbit/s data rate (limited by PCB routing)

LVDS interface:

- 8B10B decoded/encoded (160Mbit/s, 320Mbit/s) for high data rate applications (Frame-based link)

On-chip interconnect specification:

- I²C-to-APB bridge + LVDS-to-APB bridge
- Status/control registers refer to byte addressing



KlauS7 Digital Interface Architecture

ASIC testing and readout

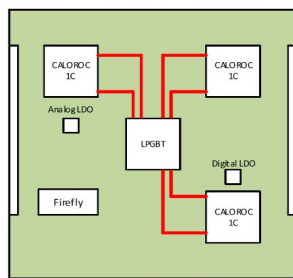
New interface with lpGBT (Concentration)

→ Dedicated cards

- LLR: CALOROC
- DESY : Klaus ?

New front end boards for FCC

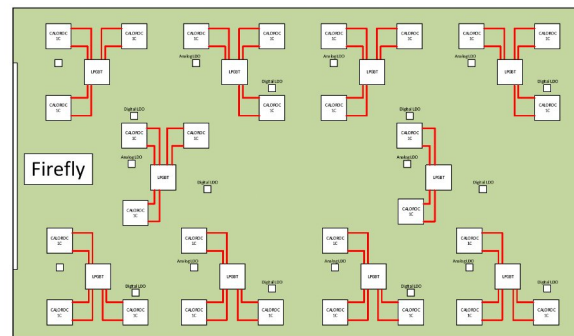
- Study new chips CALOROC
 - Adapt HKROC test board for Si sensors
- Study clock distribution system
- Study LPGBT to aggregate data
- Propose design with 3 CALOROC (108 chn)
 - I2c (slow control)
 - Clock distribution
 - LPGBT or similar
 - Power distribution
 - Measure power, noise, temperature, performances
 - Solution to chain boards
- Propose design for 512 channels
 - Equivalent to 5x miniFEB
 - Power estimation: 37mW/chn



Power estimation: 46mW/chn

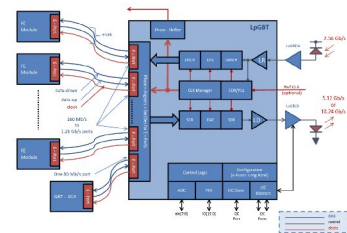
Grenoble:

- Possible: dev't: LPGBT in FPGA
 - LAr + Si
- Optimisation of number of links / ASICs.
- Single fibre for output



LPGBT:

- Radiation tolerant
- Up to 7 in link @1.28Gbps
- 1 out link up to 10Gbps
- Pre-emphasis



- 29 CALOROC (1044 chn)
 - 29 i2C load possible ?
- 10 LPGBT
 - Too many signals to drive for 1 board and 10 chained boards
- 38mW/chn

Need more channel, data link optimisations in new ROC chip, reduce power consumption

Need new solution to aggregate more data links

Wait for new technology ?

Reduce power costing → passive or active cooling

Conclusions

Many developments

(too many to be sanely summarized)

Main messages:

- Technologies are more or less mature
... with the “old electronics”
Applications (HGCAL, LUXE, SHiP, EBES, ...) are time consuming
but extremely important for funding, experience building, motivation
- Practical work has started on the new electronics
 - ASIC (⚠ if we can produce them ⚠)
 - Pre³-prototypes of Very Front-end
- Revival of groups for FCC-ee : Lumi, Muons

Skipped but to be considered from DRDCalo and DRD1 activities

- MPGD (for muon colliders) for forward regions ?
- Hybrid RPCs (ADRIANO)
- DECAL / MAPS / LGAD ...

Extras

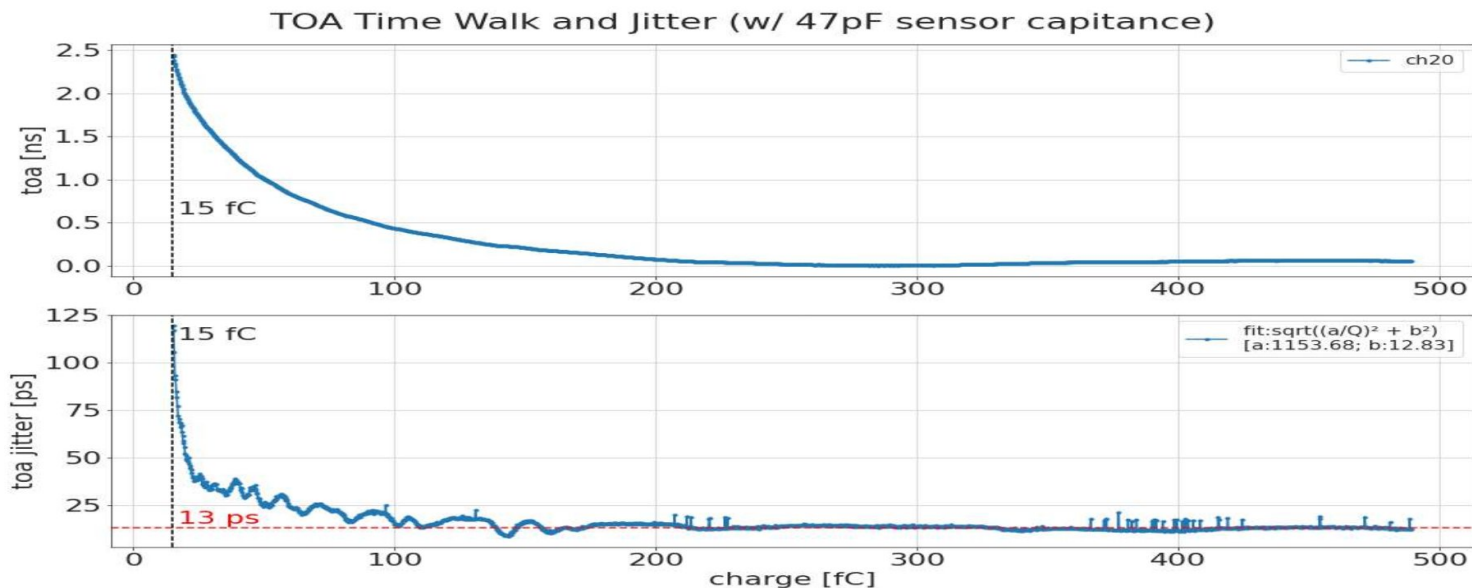
Timing ?



Zoom on timing

Omega

- ~2.5 ns time walk, 13 ps jitter for $Q > 100 \text{ fC}$ at $C_d = 47 \text{ pF}$
- Fits also well MCPs for PID @EIC (HRPPD)



C. de La Taille CALOROC 1A/B/C overview