SiD R&D
Schedules, Milestones, Technology Choices

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Timescales relevant to SiD R&D. (DCR, CDR, TDR,…)

- DCR - Detector Concept Report
– contributions for subsystems descriptions and R&D should have been be submitted!

Detector Performance -> John Jaros
Detector Hardware -> Editor (e.g. W. Lohmann for Cal.)
- copy to Chris Damerell
(circulate to all SiD! - Harry)
Last chance to review contributions at this meeting.
Editing/reviewing at ECFA/Valencia

- CDR – Conceptual Design Report
Approximate goal: mid-2008.
Two detector concepts only by then?? Or four concepts to be reduced to two??
Much depends on formation of mergers/alliances in next 18 months… are there strategic R&D allianced SiD should pursue now?

Timescales relevant to SiD R&D.
(DCR, CDR, TDR,...)

CDR – Conceptual Design Report (continued)

- Concern over need for definitive answers on e.g. digital hadron calorimetry (first beam tests of RPC/GEM in early 2008)

- From the standpoint of R&D, how should we best position ourselves for the expected reduction in number of concepts? Narrow technology focus/choices soon?

- Are we missing any R&D opportunity that would give us a competitive edge in the CDR reduction/evaluation process?

- What is the role of R&D alliances/collaborations (CALICE, SILC,...) in the merging process?

Scope of SiD Detector R&D

Questions for SiD Subsystems:

- what is still "generic"?
- what is directly focused on a subsystem technology choice?
- to what extent is our current profile of R&D leading to a complete set of results from which we can define a fully functional ILC detector with performance meeting the required physics goals? Wider view – beyond CDR -> TDR?
- with (still) limited manpower/support, are we focused on the correct priorities (e.g. simulations)?
- how should we approach the task of technology selections for SiD subsystems?

Funding for SiD R&D

(see also tallk by Jim Brau)

- Expect O($3M) for detector R&D in 2007

~$1M is "priority advance support" for time critical projects.

- ~$2M for enhanced regular LCDRD in 2007.

- how will the advanced funding for high priority R&D and the 2007 regular LCDRD support affect continuation/completion of SiD R&D projects?

- Expect priority funding to be available in Spring 2007

- Regular LCDRD funding proposals ~late 2006

Technology Choices for SiD

General considerations

A coherent set of technology choices for SiD subsystems in two scenarios:

- Case of four CDR's – makes SiD look stronger as a completely specified, integrated design, BUT we will not have ALL the test results in hand to fully support the choices – rely on simulations.

- Case of two CDR's – makes SiD an attractive collaboration to join, BUT leaving some(?) technology choices open may give us more flexibility in merger negotiations.

- Potential gain/loss of people to SiD as a result of choices?

Technology Choices for SiD

Elements of technology choices:

Performance vs. physics goals

Cost

Status of development/R&D

Results from prototypes

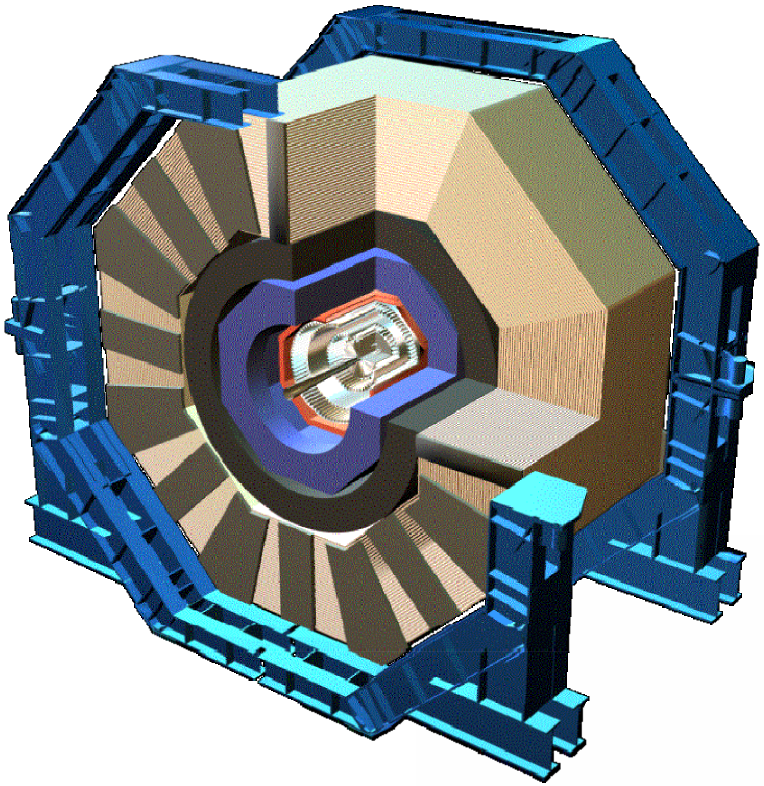
Results from simulations

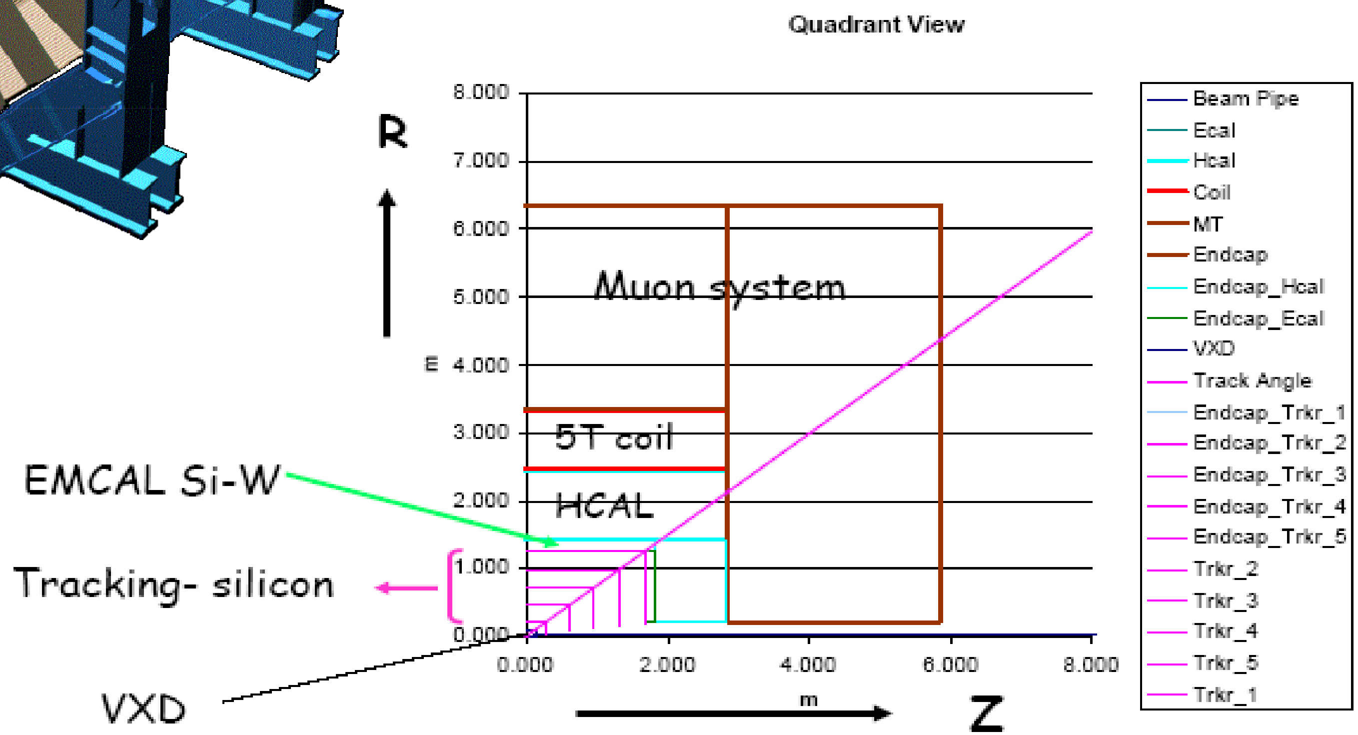
Compatibility with overall SiD design

Previous experience with technology in other experiments

Maturity of technology, risk vs. gain

The SiD Detector





SiD R&D Areas

Vertex Detector (Ron Lipton, Bill Cooper, Su Dong)
Main vertex detector technology(s): Many competing technologies. Aiming for thin devices.

Tracking system (M. DeMarteau, R. Partridge)
Main technology(s): Monolithic pixels; Long and short ladder Si-strips; long shaping time/thin design.

Electromagnetic Calorimetry (R. Frey, D. Strom) Main technology: Si/W Pix chip.

Hadronic Calorimetry (H.Weerts, G. Blazey, A.White)
Main technology(s): Digital GEM- and RPC-based with steel or tungsten, ASIC's. Scintillator tiles/SiPM's, Scintillator/SiPM TCMT?

Forward Calorimetry (Bill Morse) Beam Cal, Lumi Cal, GamCal.

Muon system and tail catcher (H.E. Fisk, H. Band) Main technology: Scintillator planes or RPC's.

Electronics (M. Breidenbach) KPix,…

Magnet (?) Main technology: CMS-style superconductor

Machine Detector Interface (P. Burrows)

Examples of technology choices/issues

All SiD subsystems will continue to evolve.

A final SiD detector may well have very different, configurations and/or technology(s) than we imagine in 2006 due to advances in electronics, materials, clever ideas, etc.

However, for the period through mergers/CDR's we must make the best choices.

SiD's approach is to make a definite choice for a baseline technology for each subsystem, understand how the overall detector design works with these choices and to study the overall physics performance for this configuration. Then allow alternative technologies and study impact on performance.

Examples of technology choices/issues

For some subsystems the choice seems clear e.g. the main tracker using silicon strips, Si/W ECal.

For others there is ongoing R&D that will take extended periods to “complete”.

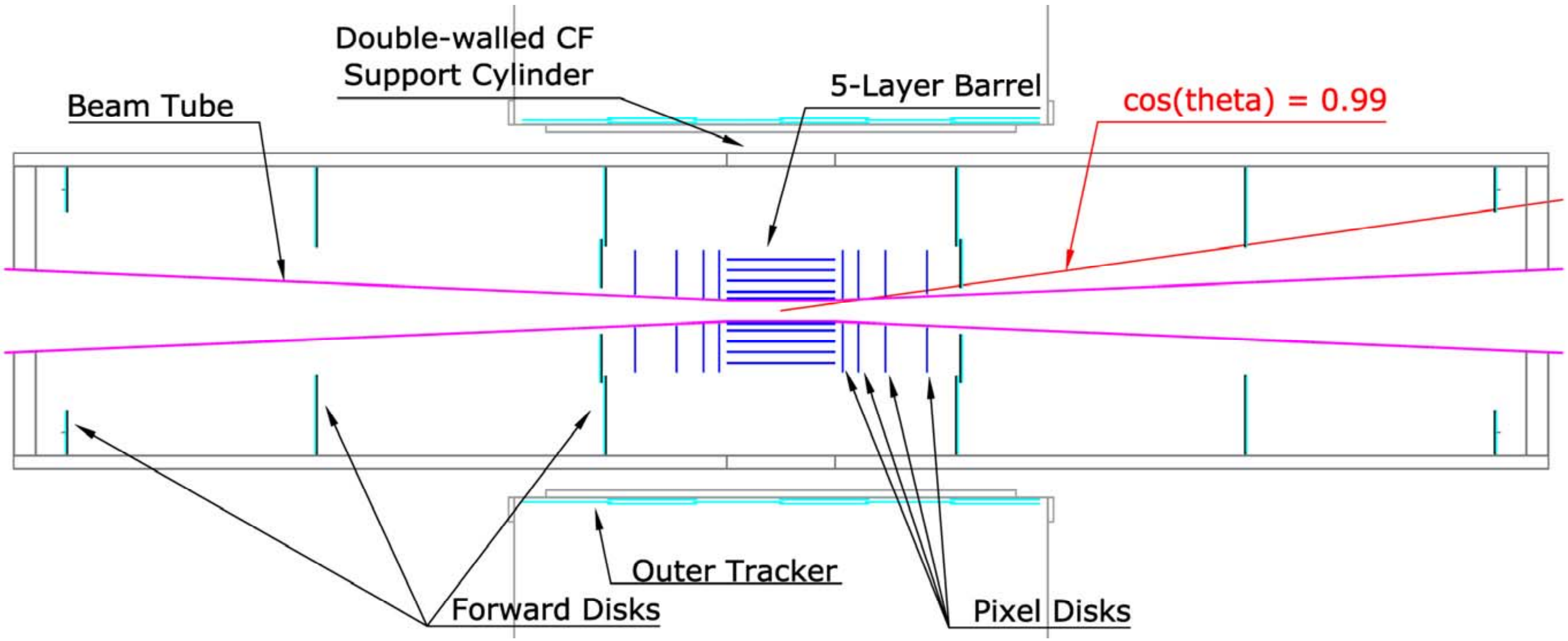
Two examples for:

1) The Vertex Detector sensor technology.

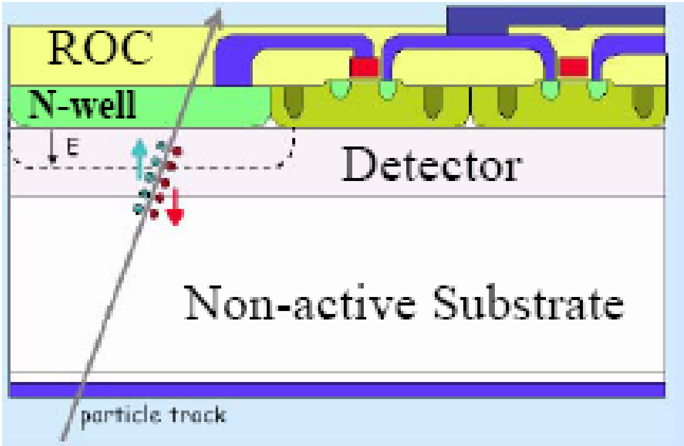
2) The HCal active layer technology.

Vertex Detector

5-layer pixel barrel: z = ±62.5 mm; 14 mm < R < 61 mm
4 pixel disks per end: Z = ± 72, ± 92, ± 123, ± 172 mm; R < 71 mm

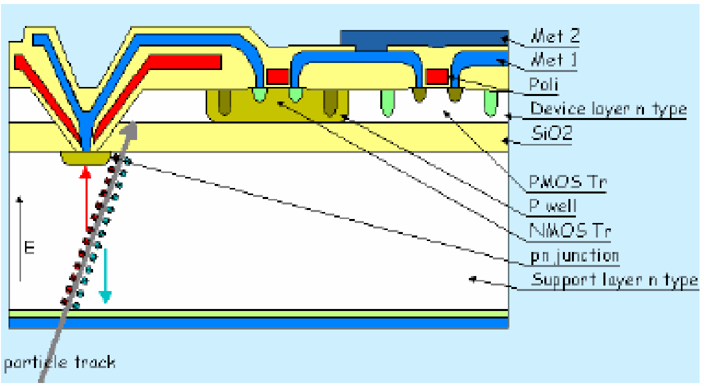


Vertex Detector

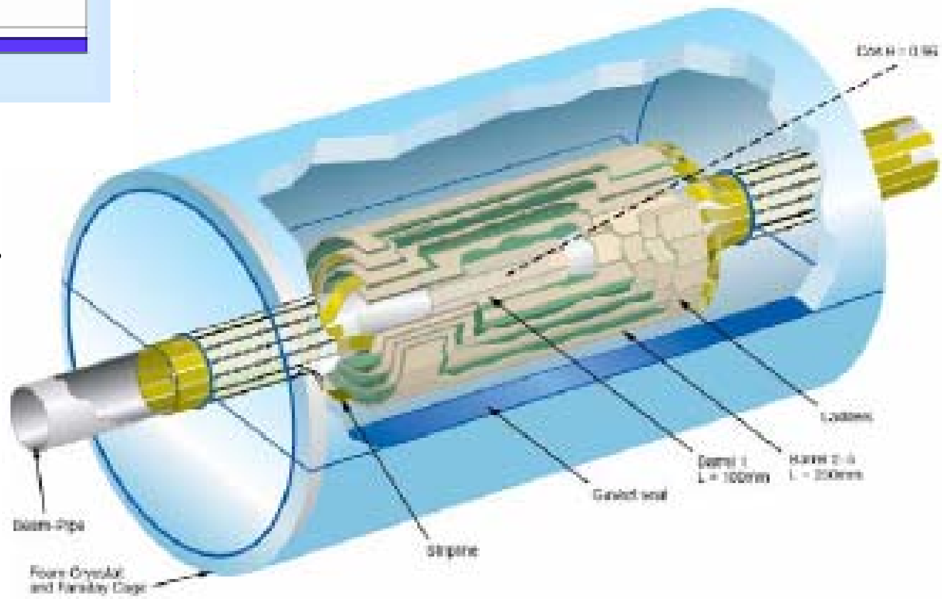


MAPS Principle

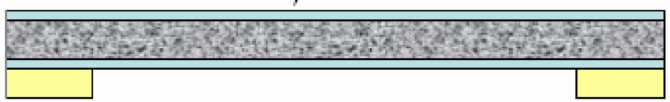
Sensor technology development



Silicon on Insulator



RVC foam (foam thickness 1.5 mm)



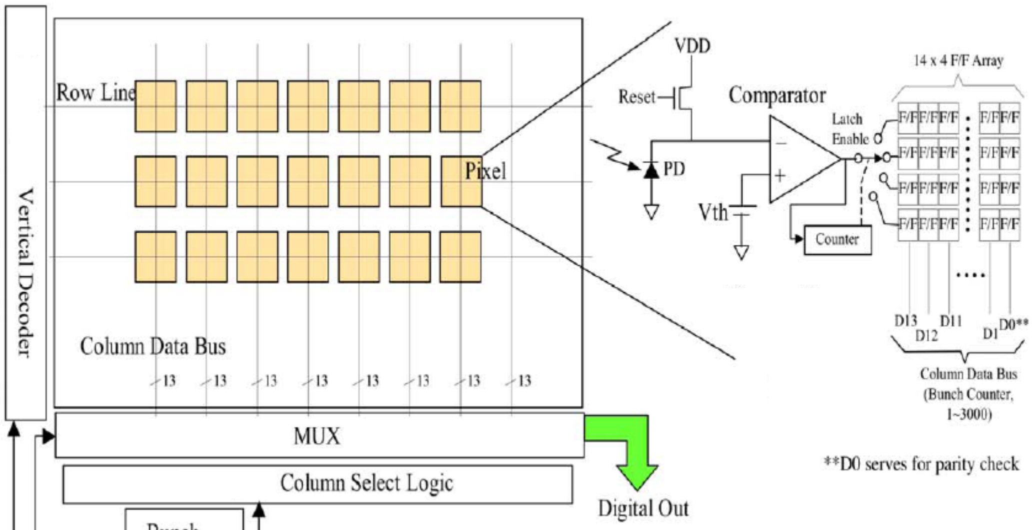
Silicon Carbide foam (foam thickness 1.5 mm)

Materials R&D

SLAC/Oregon/Yale – "Chronopixel"

- The current design is for chips up to 12.5 cm x 2.0 cm in size with a single layer of 10 μm x 10 μm pixels.
- Each pixel has its own electronics under it, but both the sensitive layer and the electronics are made of one piece of silicon (monolithic CMOS) which can be thinned to a total thickness of 50 to 100 μ m, with no need for indium bump bond.
- The time of the hit is stored in each pixel, up to a total of four different hit times per pixel, with sufficient precision to assign each hit to a particular beam crossing.
- Occupancy of ~1% reduced to ~10^{-5} with time stamping.

Chronopixel Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Vertex Detector – Sensor Technology

- Demonstration of a viable sensor technology could be 2-3 years away (vs. CDR timescale?)

- Chronopixel – aggressive design with v. small (60nm) feature sizes -> long development time?

- Column parallel CCD's – looks viable, under active development at RAL.

- SOI, device submitted, first results end of 2007…

- MAPS – working device?

Technology choice - a multi-dimensional challenge:

- Not a scorecard for comparison of technologies: big variations within some options!
- Not all issues created equal
- Only a guide of where each effort must focus

+ = no problem
0 = difficult but probably OK
– = needs new ideas to overcome challenges

	CPCCD	FPCCD	DEPFET	xAPS	3d/SOI	ISIS
Hit Density	–	–	–	–	–	–
Avg. Power	+	+	+	0	0	+
Inst. Power	–	+	–	–	–	+
EMI	–	+	–	–	–	+
Radiation	–	–	+	+	+	0
Ready 2010?	+	+	+	0	–	–

Possible that no option will deliver what we need: an enormous challenge

Tim Nelson/VLCW06

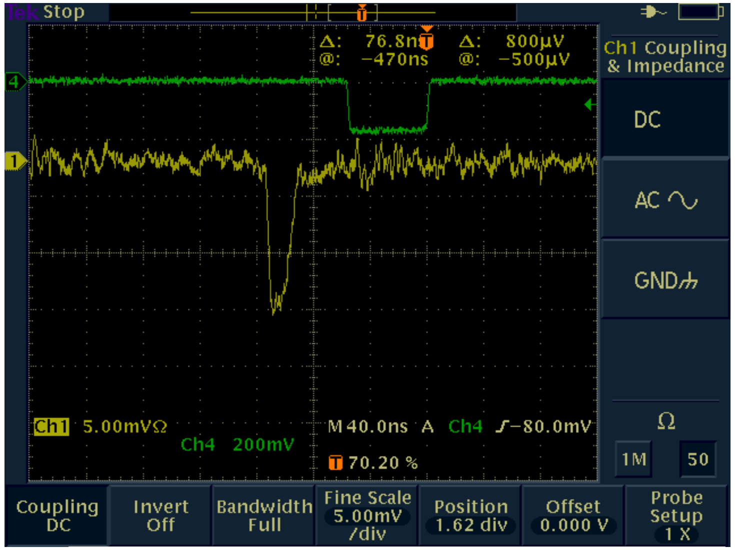
Hadron Calorimeter Technologies

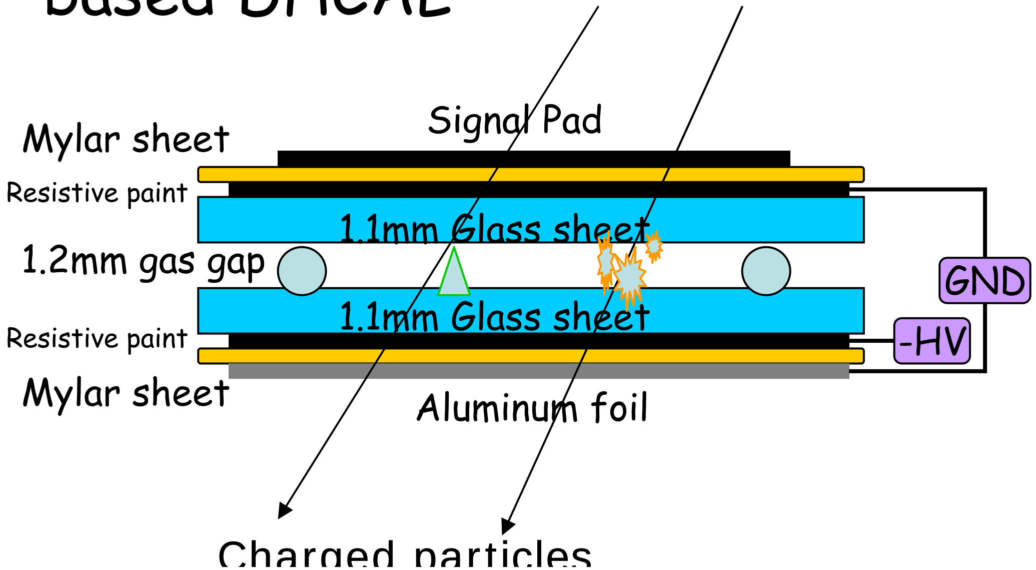
- Digital RPC or GEM (+new ideas on Micromegas)
- Analog Scintillator/SiPM's

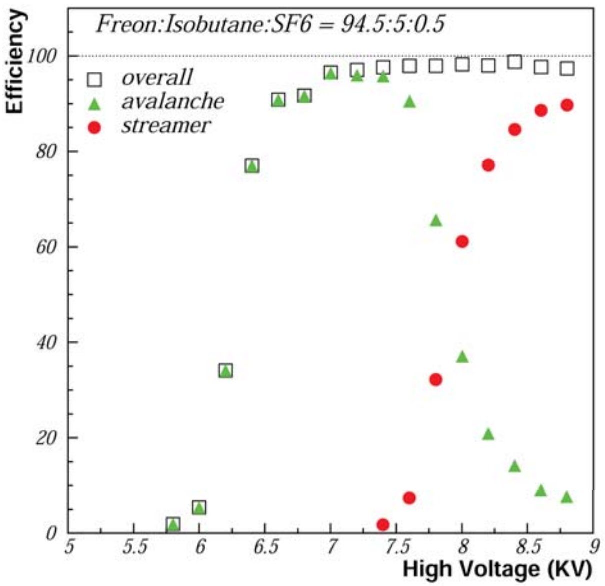
Status of R&D, beam tests, schedules,...

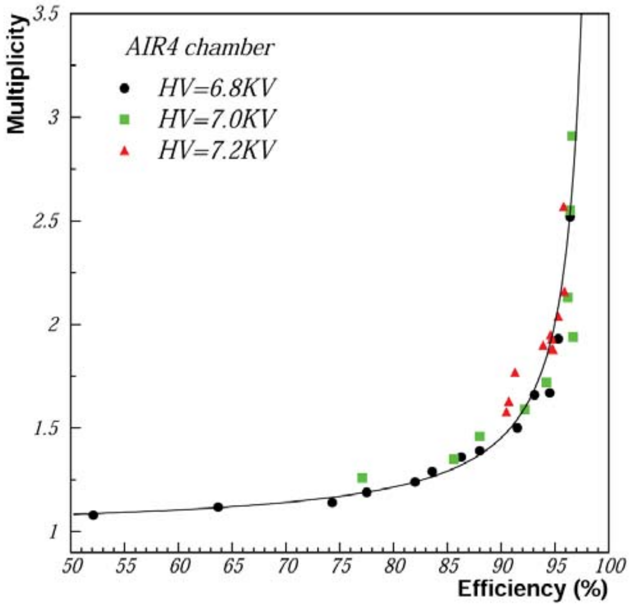
Hadron Calorimeter – digital RPC

(2) Resistive Plate Chamber-based DHCAL

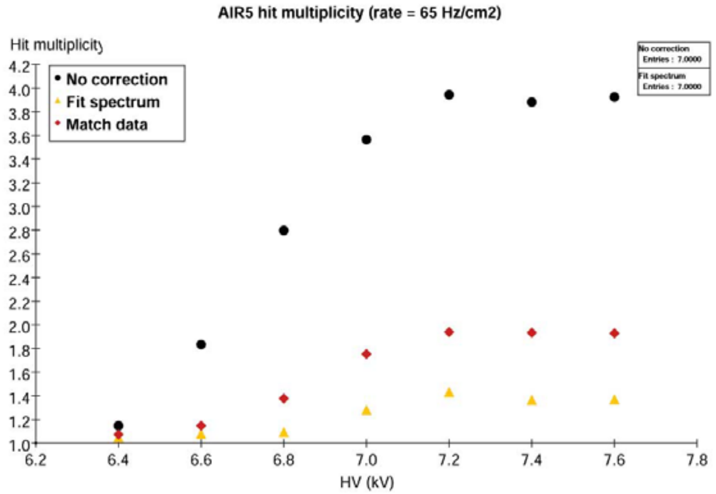


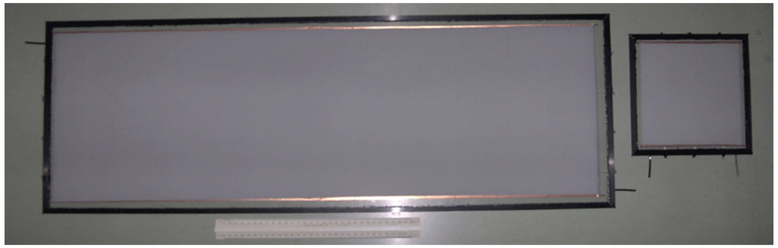




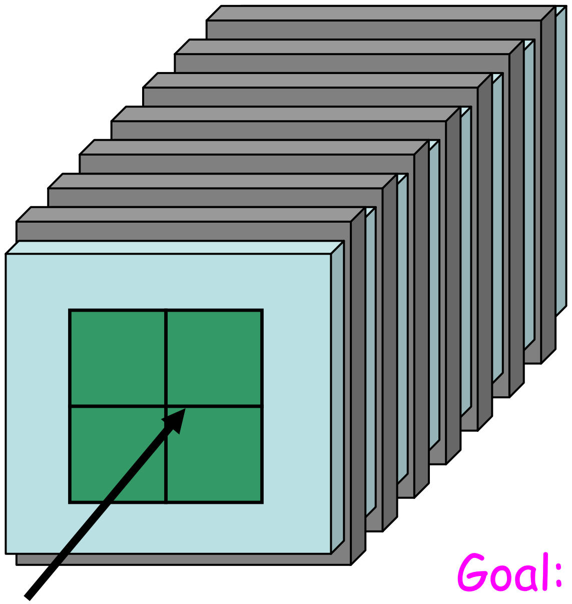


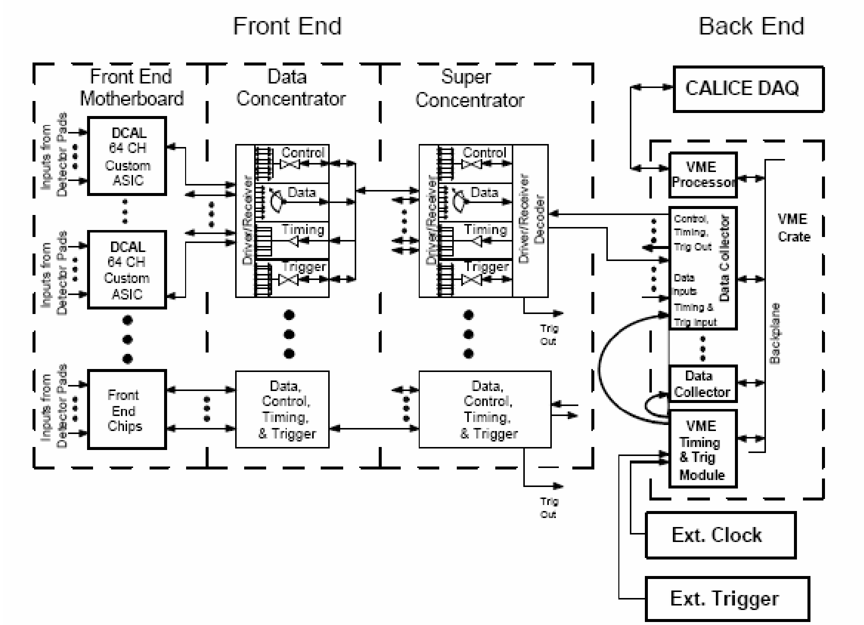
Hadron Calorimeter – digital RPC





Fermilab Feb '06 test beam results

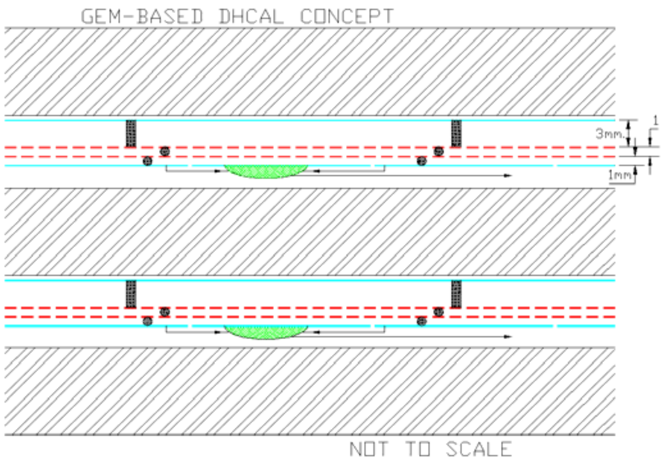


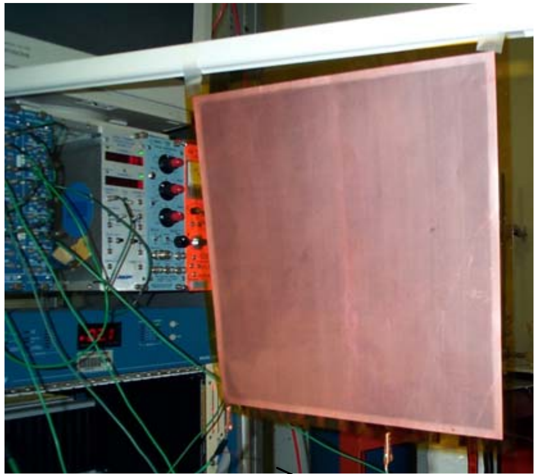


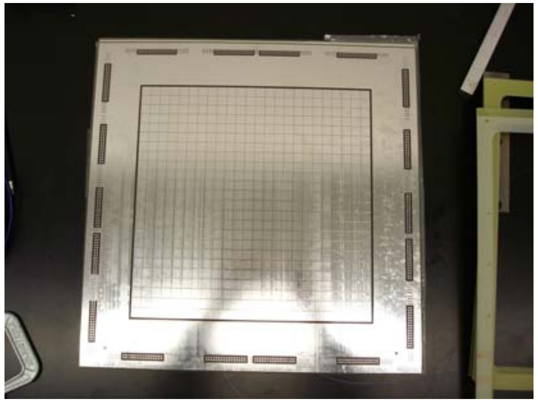
Goal: Test beam at Fermilab 2007-8

Hadron Calorimeter - digital GEM

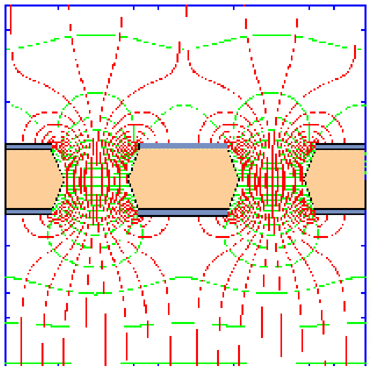
Gas Electron Multiplier (GEM) - based DHCAL

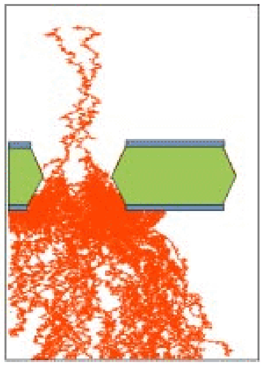


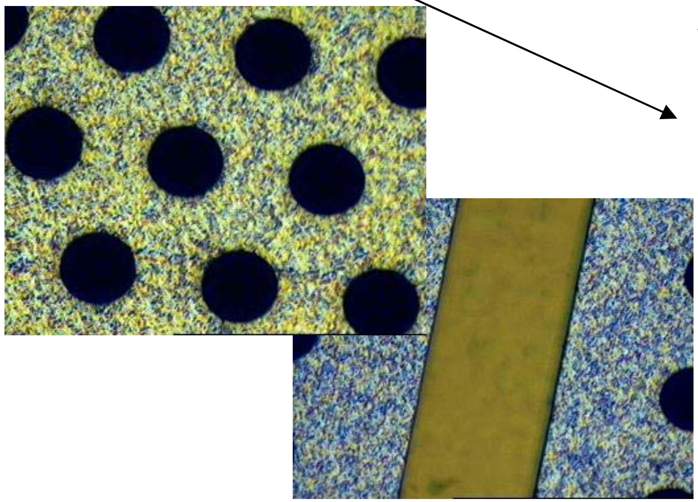




500 channel/5-layer test
30x30cm^2 foils

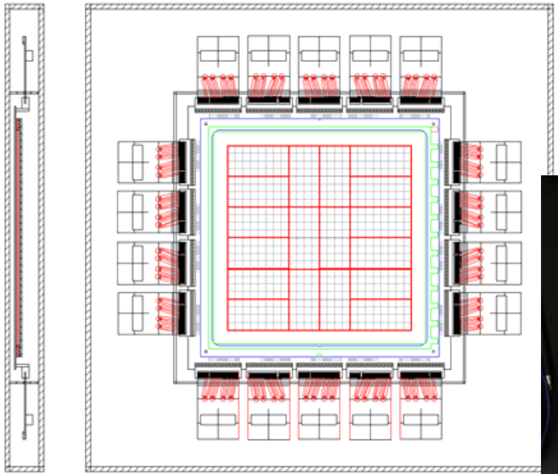


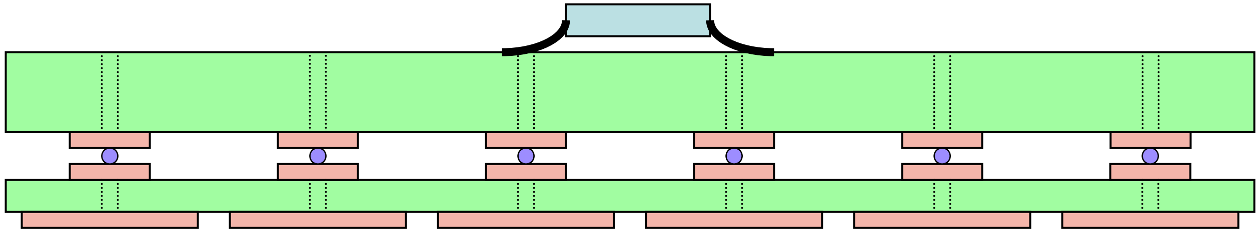


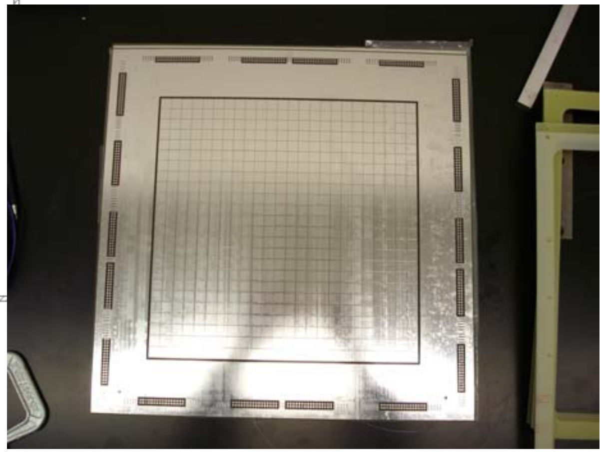


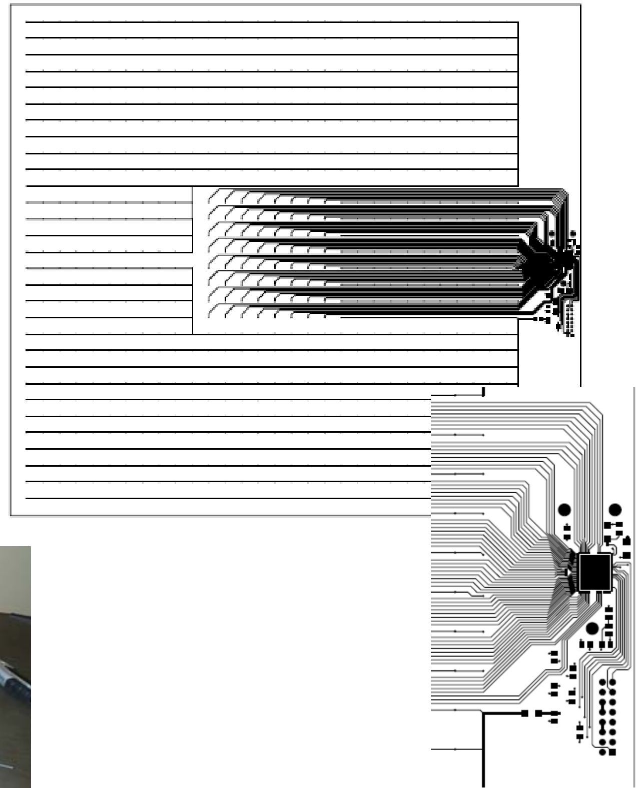
Details of new 30cm x 30cm foils from 3M

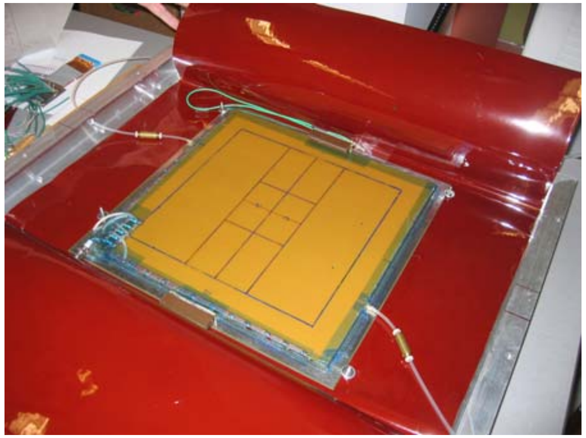
Hadron Calorimeter – digital GEM

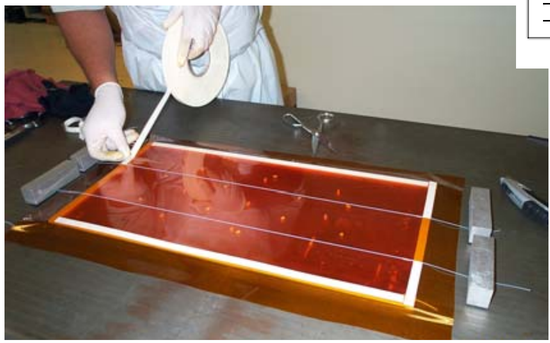






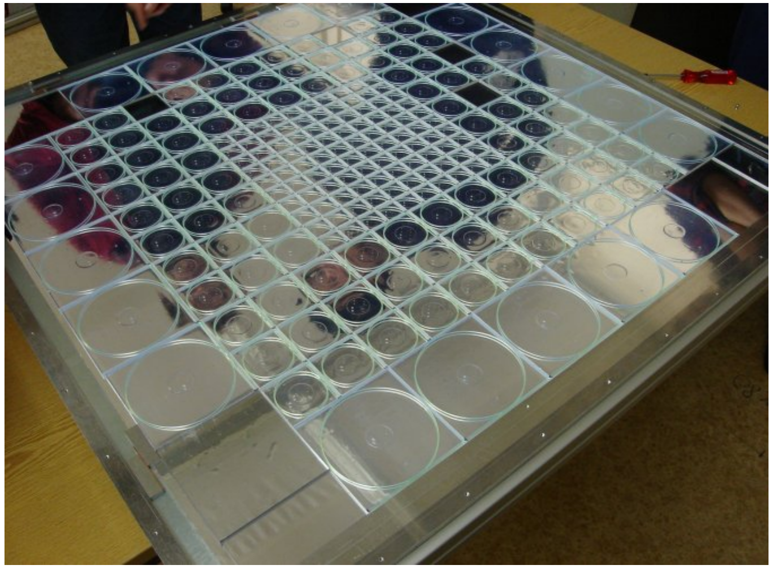






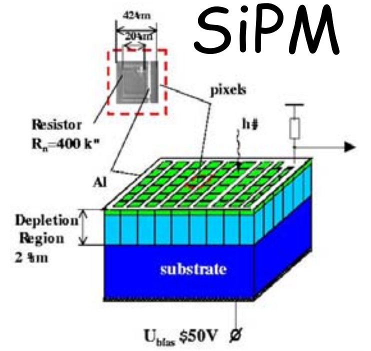
Goal: Test beam at Fermilab 2008

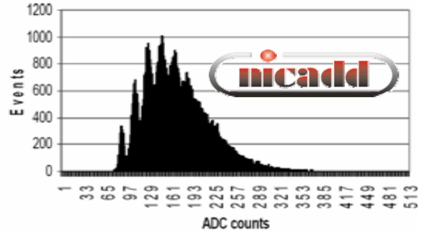
Hadron Calorimeter - Scintillator

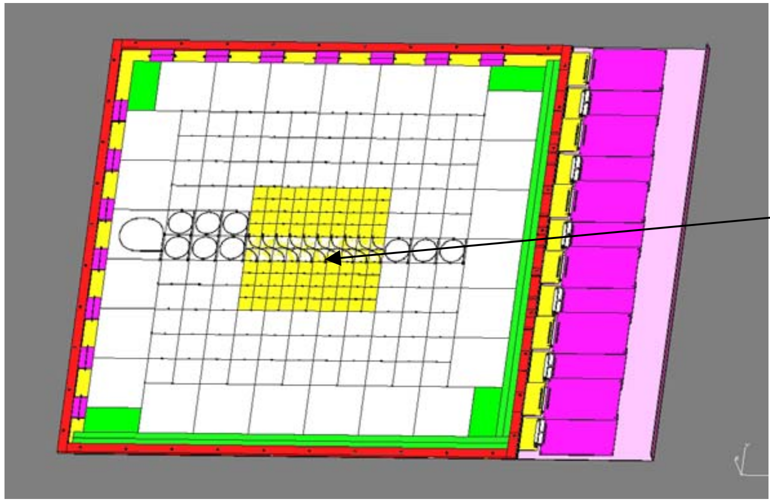


Full 1m^3 prototype stack – with SiPM readout. Goal is for CERN/Fermilab test beams exposure in Fall 2006/Spring 2007. 2/3 depth-layer stack now at CERN!

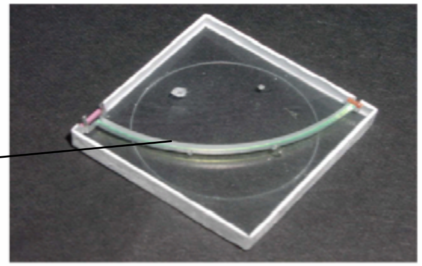
SiPM

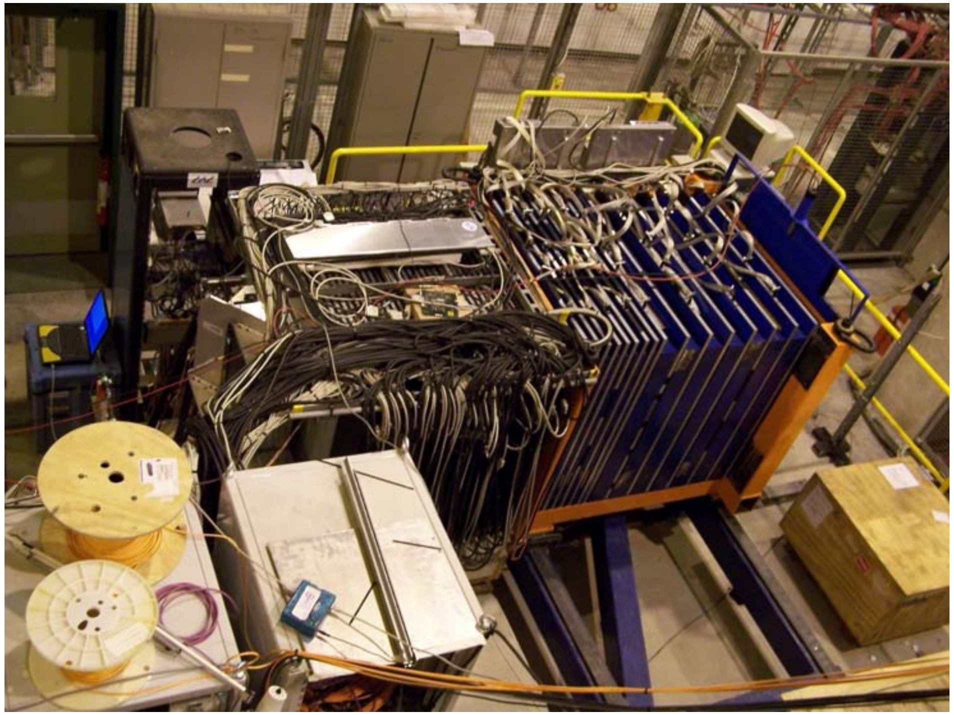






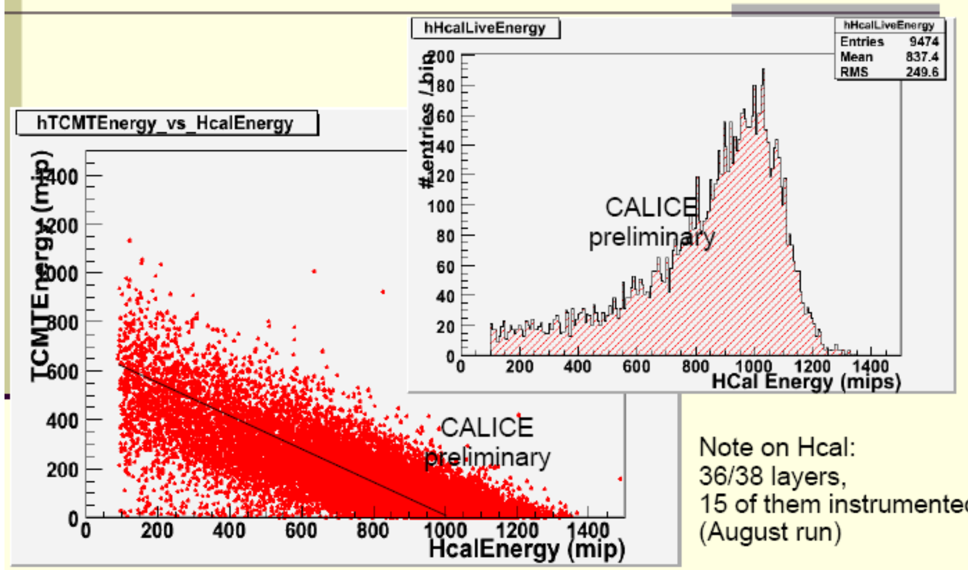
Ready 3x3 tile





Scintillator/SiPM HCal and TCMT

80 GeV pions: Hcal x TCMT correlation



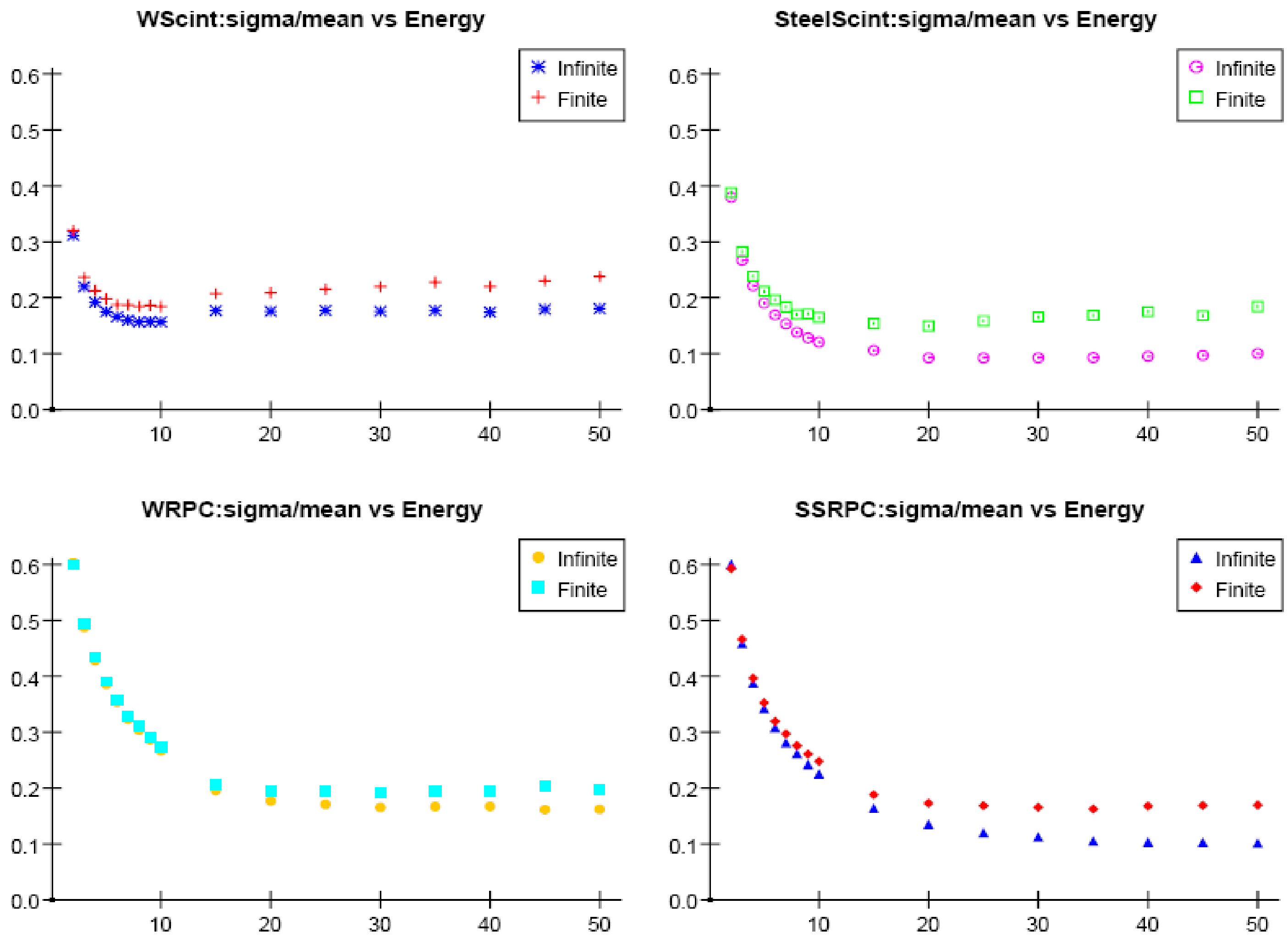
Note on Hcal:
36/38 layers,
15 of them instrumented
(August run)

AHCAL(CALICE)/TCMT – full depth (39 layers) module in test beam at CERN -> data/comparison with simulations in 2007.

DHCAL/RPC/GEM –

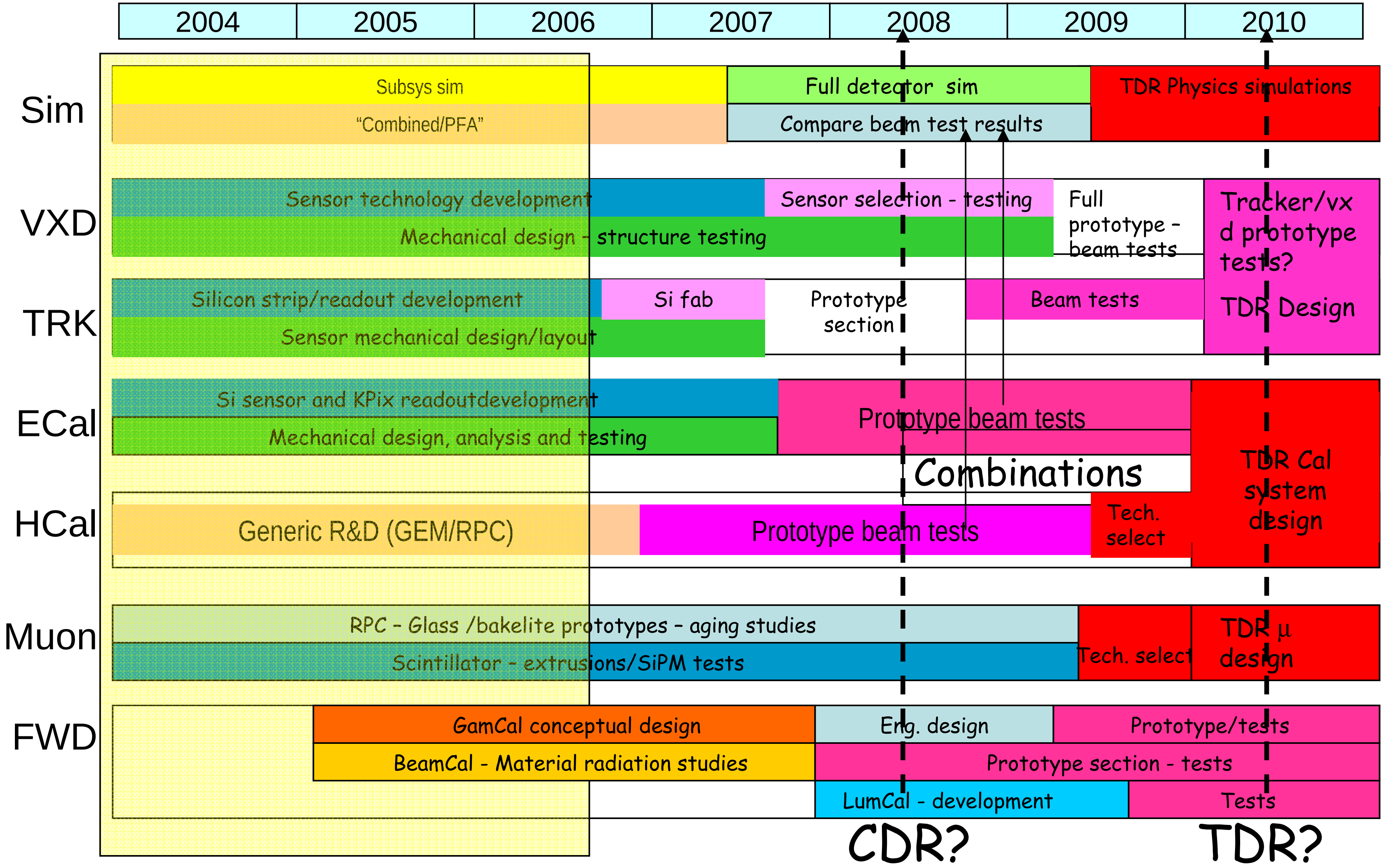
Individual chamber test done – devices well characterized. Slice Test in 2007 (mainly electronics test), full $1m^3$ stacks in 2008: how long to understand digital calorimeter performance vs. simulation?

Full set of results and simulation comparison probably not available for CDR??



HCal simulations – e.g. neutral hadron response (Ron Cassell/SLAC) interesting comparisons of active layer/absorber – but can we make a technology choice without a full set of prototype beam tests and fully developed PFA's to understand the impact on resolution and physics?

Possible timeline for SiD R&D -> TDR



SiD R&D Conclusions

- DCR contributions converging.

- CDR goal ~ mid-2008. Number of CDR's not yet clear.

- Some technology choices before CDR may be possible.

- Some choices will be made using simulation – but verification may take much longer -> tDR?

- Some areas of SiD R&D are on long timescales – some down-select may be possible before CDR, but not unique choice.

- Expecting raised funding level for LCDRD in FY07 – together with the priority funding, this will help accelerate R&D.

- Must keep up the momentum on R&D and simulations!