SCIPP R&D on Long Shaping-Time Electronics

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The SCIPP/UCSC ILC HARDWARE GROUP

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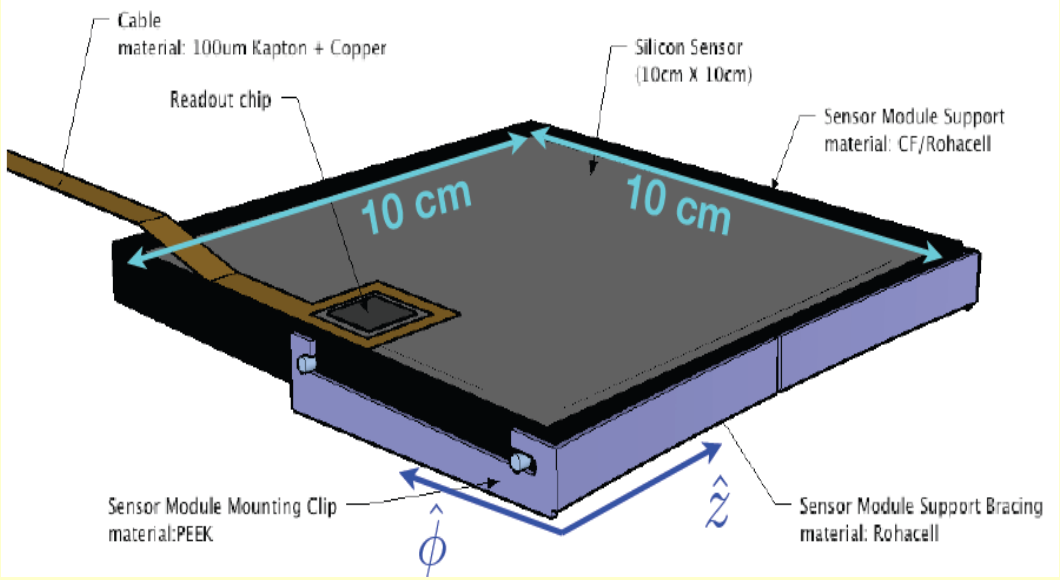
(Students are undergraduates from physics)

Alternative: shorter ladders, but better point resolution

The LSTFE approach would be well suited to use in short-strip applications, and would offer several potential advantages relative to other approaches

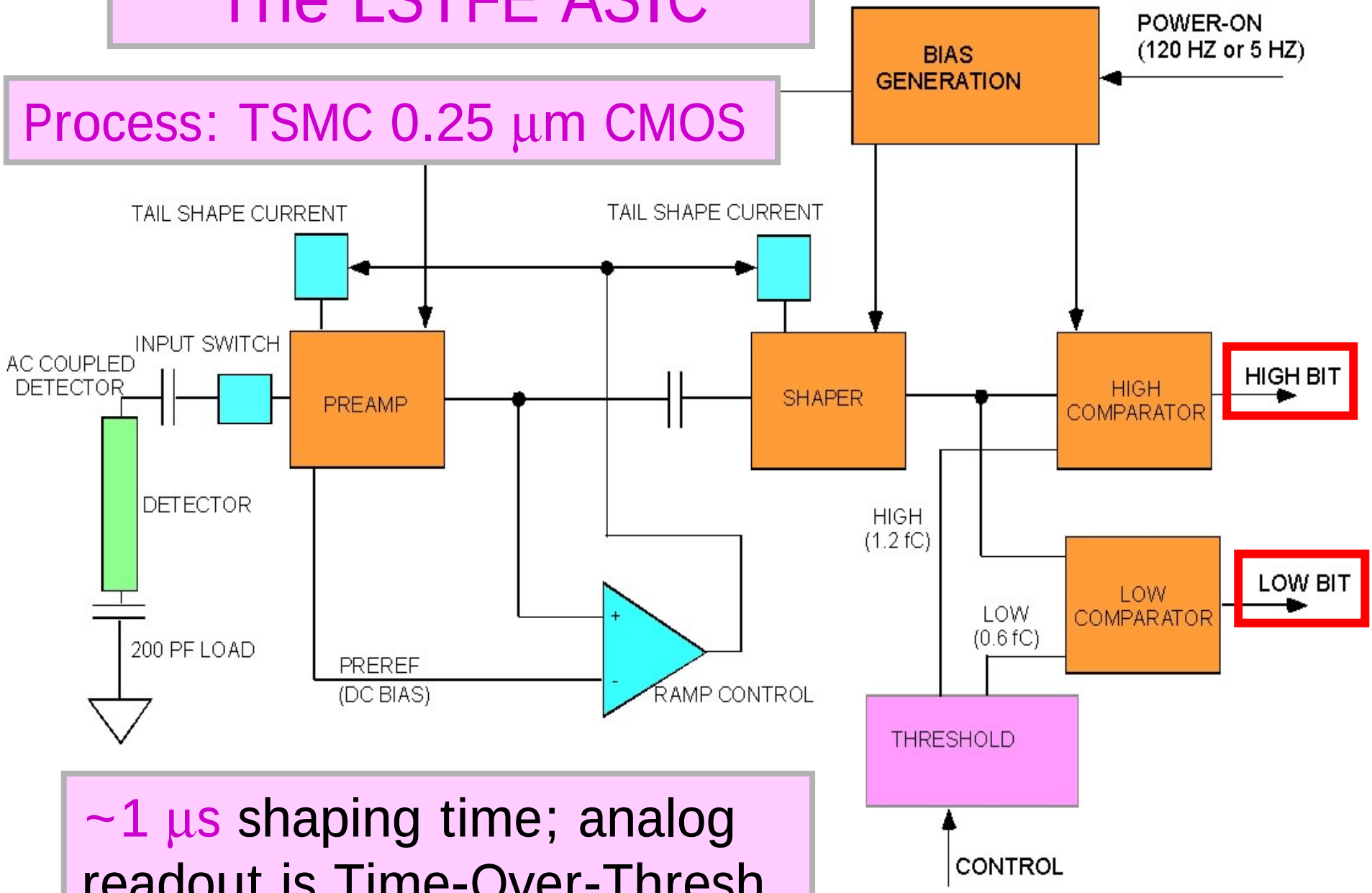
- Optimized for LC tracking (less complex)
- More efficient data flow
- No need for buffering



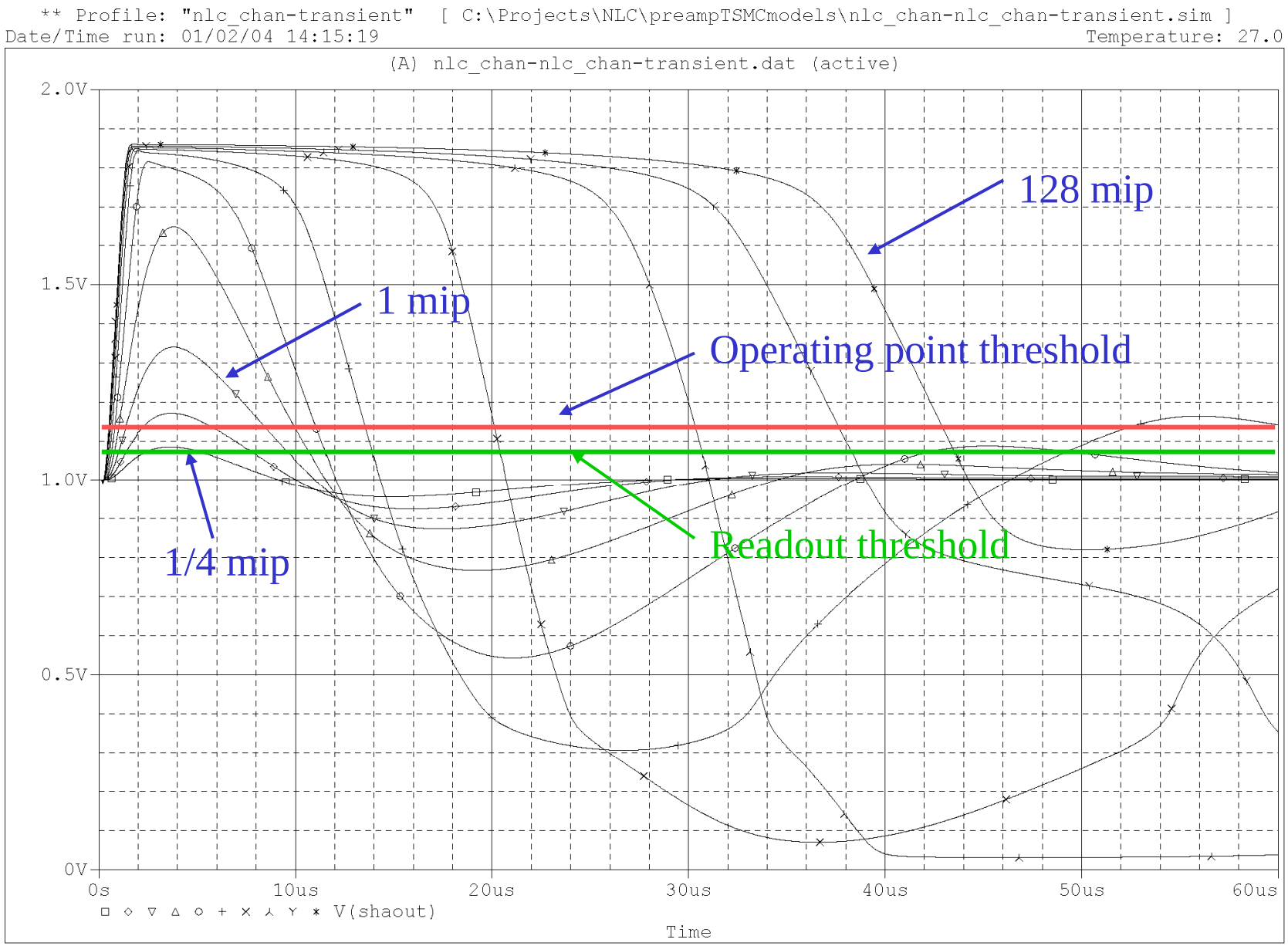
Would require development of 2000 channel chip w/ bump bonding (should be solved by KPiX development)

The LSTFE ASIC

Process: TSMC 0.25 μm CMOS



~1 μs shaping time; analog readout is Time-Over-Thresh


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
Time
V(shaout)
128 mip
1 mip
Operating point threshold
Readout threshold
1/4 mip
Date: January 02, 2004
Page 1
Time: 14:18:43

Electronics Simulation

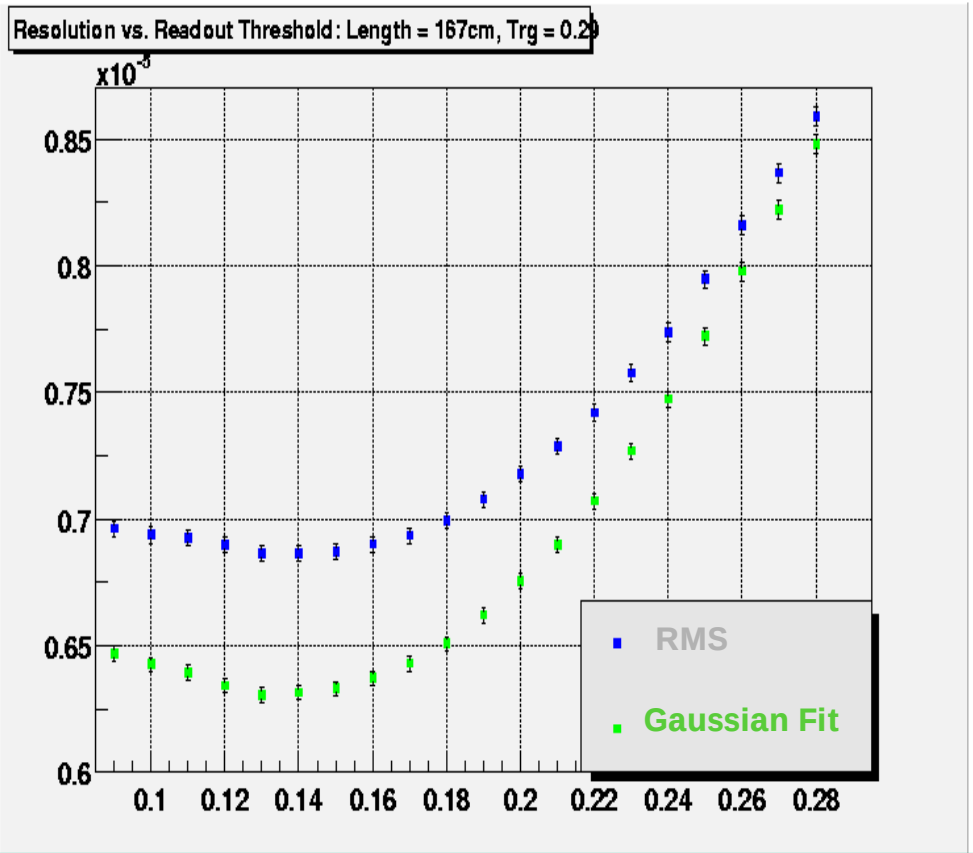
Detector:

167 cm ladder, 50 μm pitch, 50 μm readout

Analog Measurement:

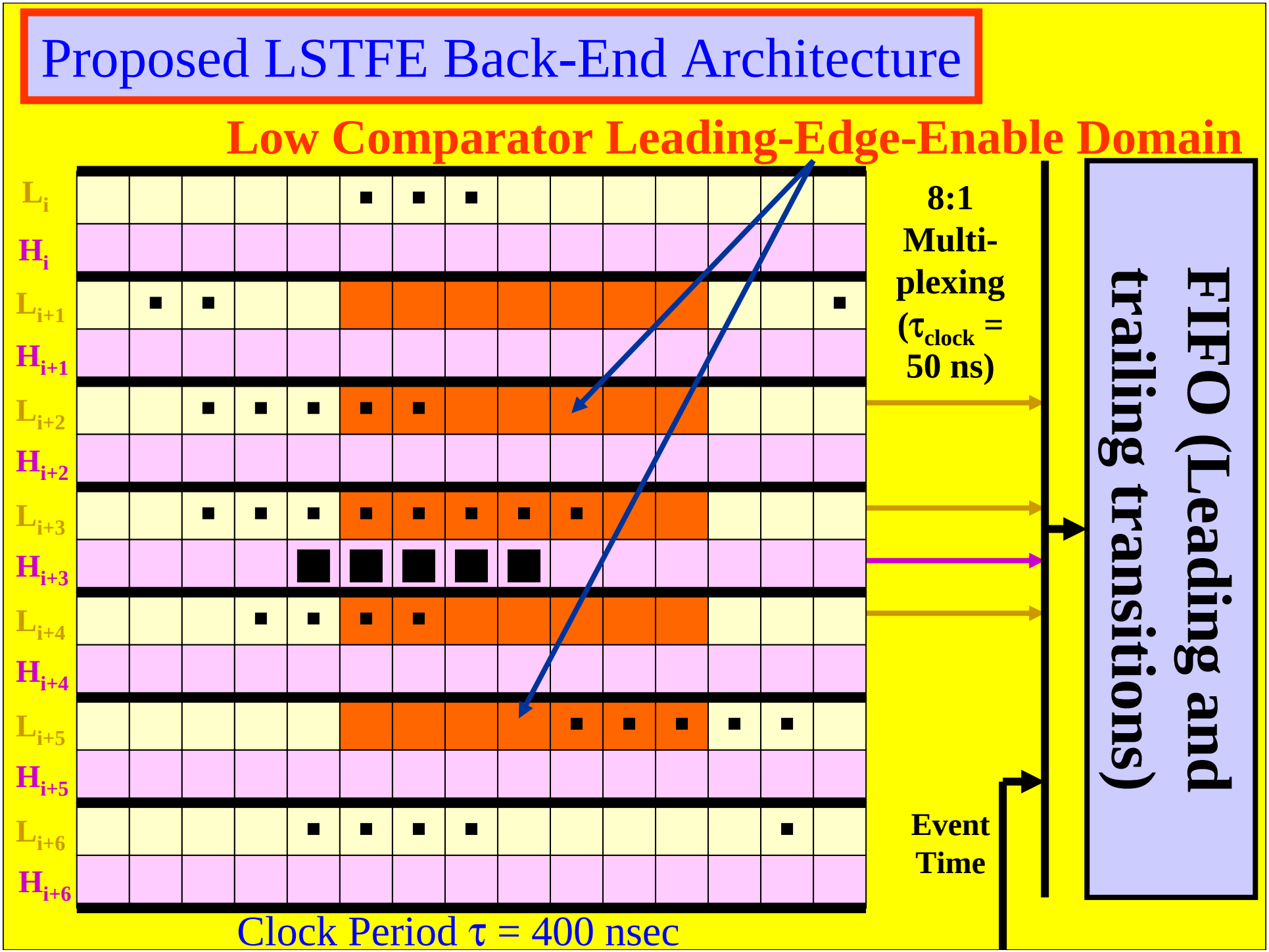
Employs time-over-threshold with 400 ns clock period; lookup table provides conversions back into analog pulse height (as for actual data)

Essential tool for design of front-end ASIC

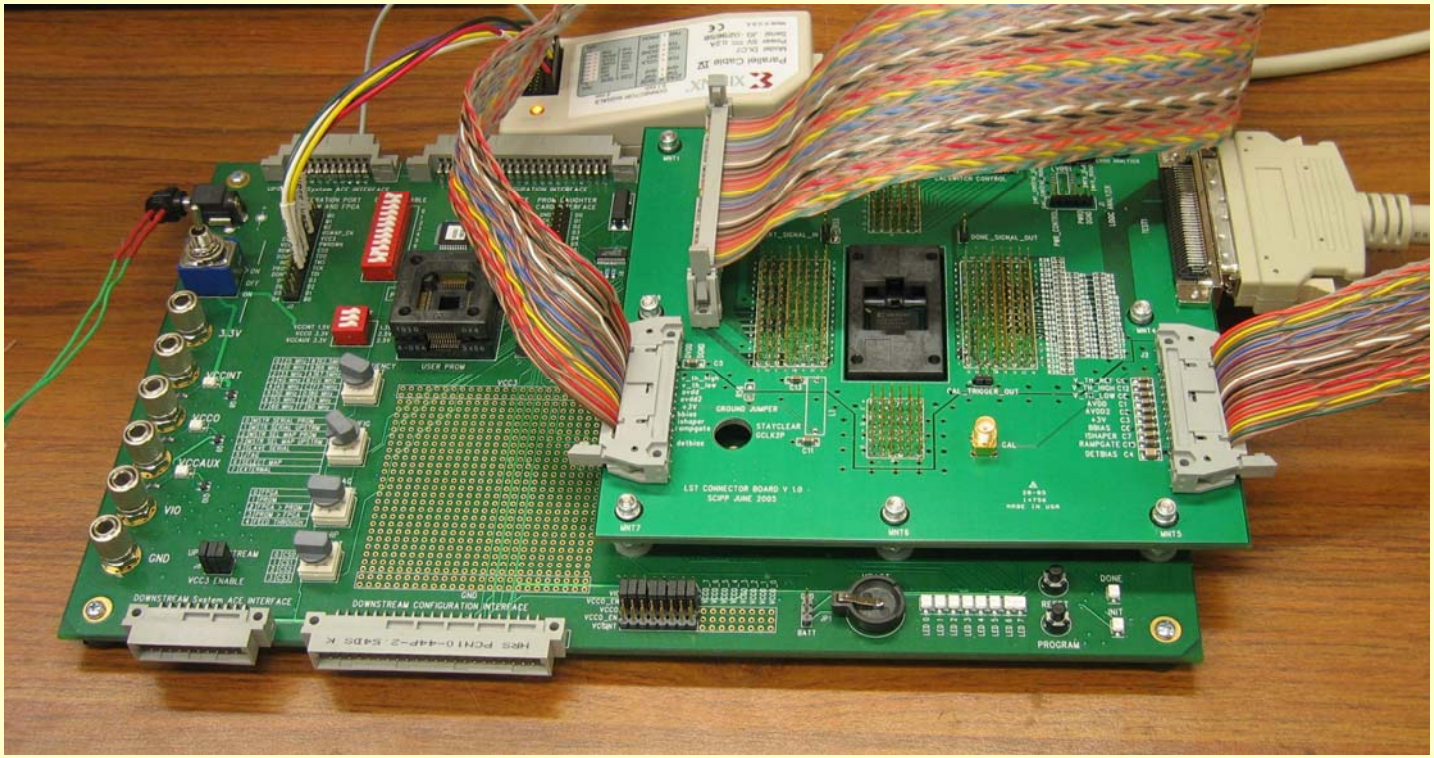


Detector Resolution (units of 10μm)

Proposed LSTFE Back-End Architecture

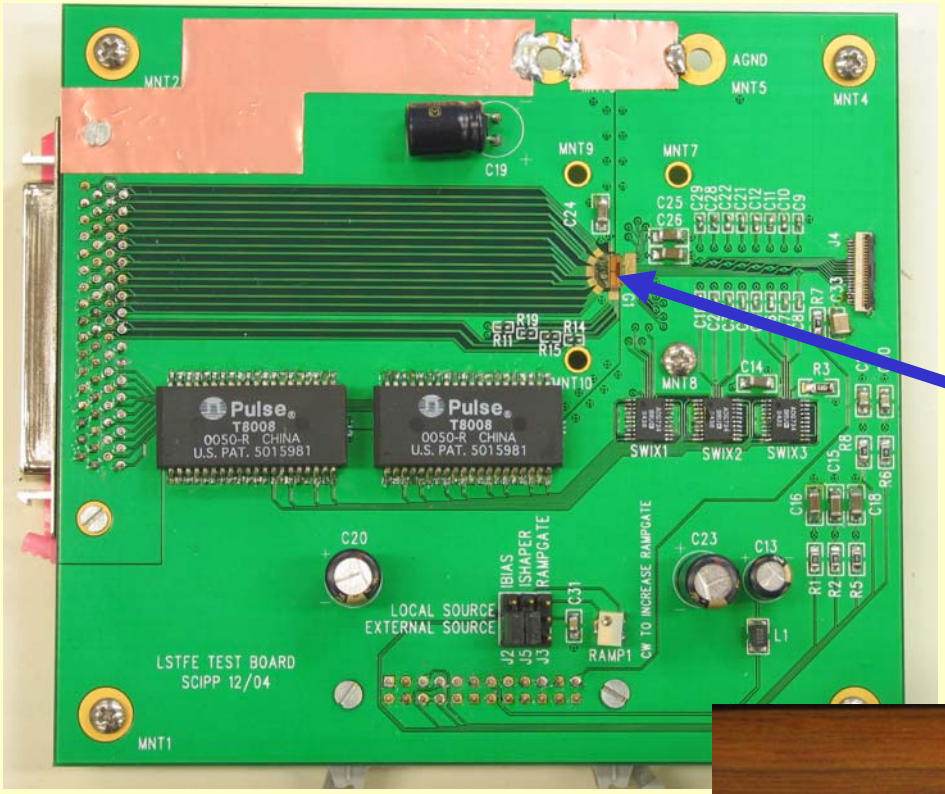


DIGITAL ARCHITECTURE: FPGA DEVELOPMENT

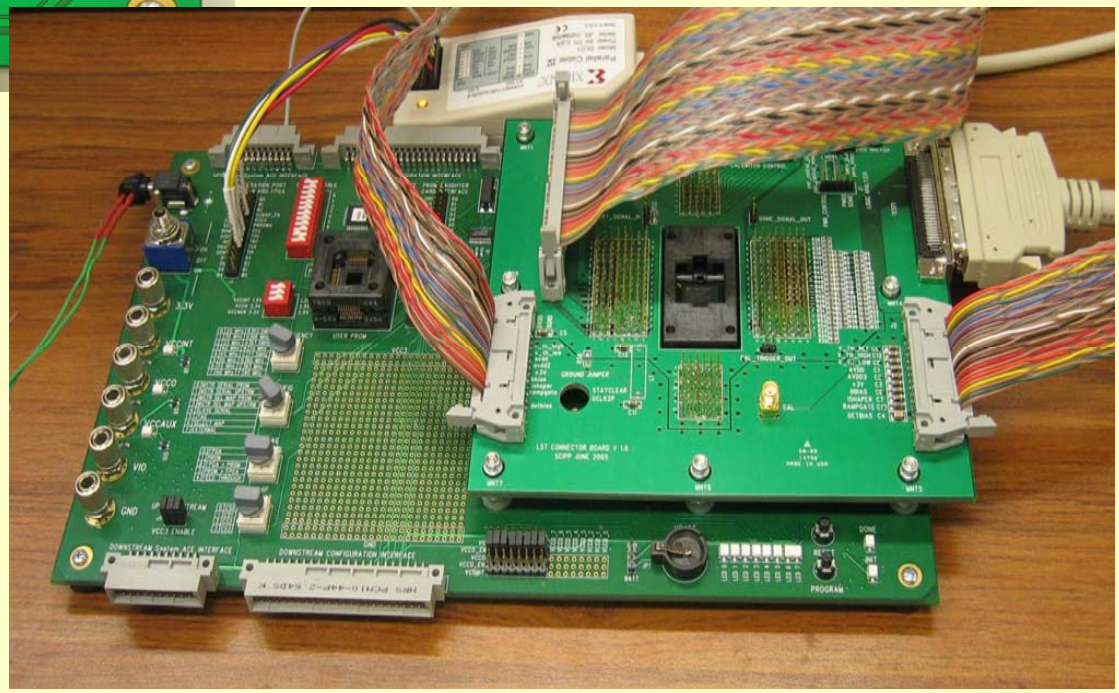


Design permits real-time accumulation and readout of hit information, with dead time limited only by amplifier shaping time

INITIAL RESULTS



LSTFE-2 chip mounted on readout board



FPGA-based control and data-acquisition system

Comparator S Curves

Vary threshold for given input charge

Read out system with FPG-based DAQ

Get

```
1-erf(threshold)
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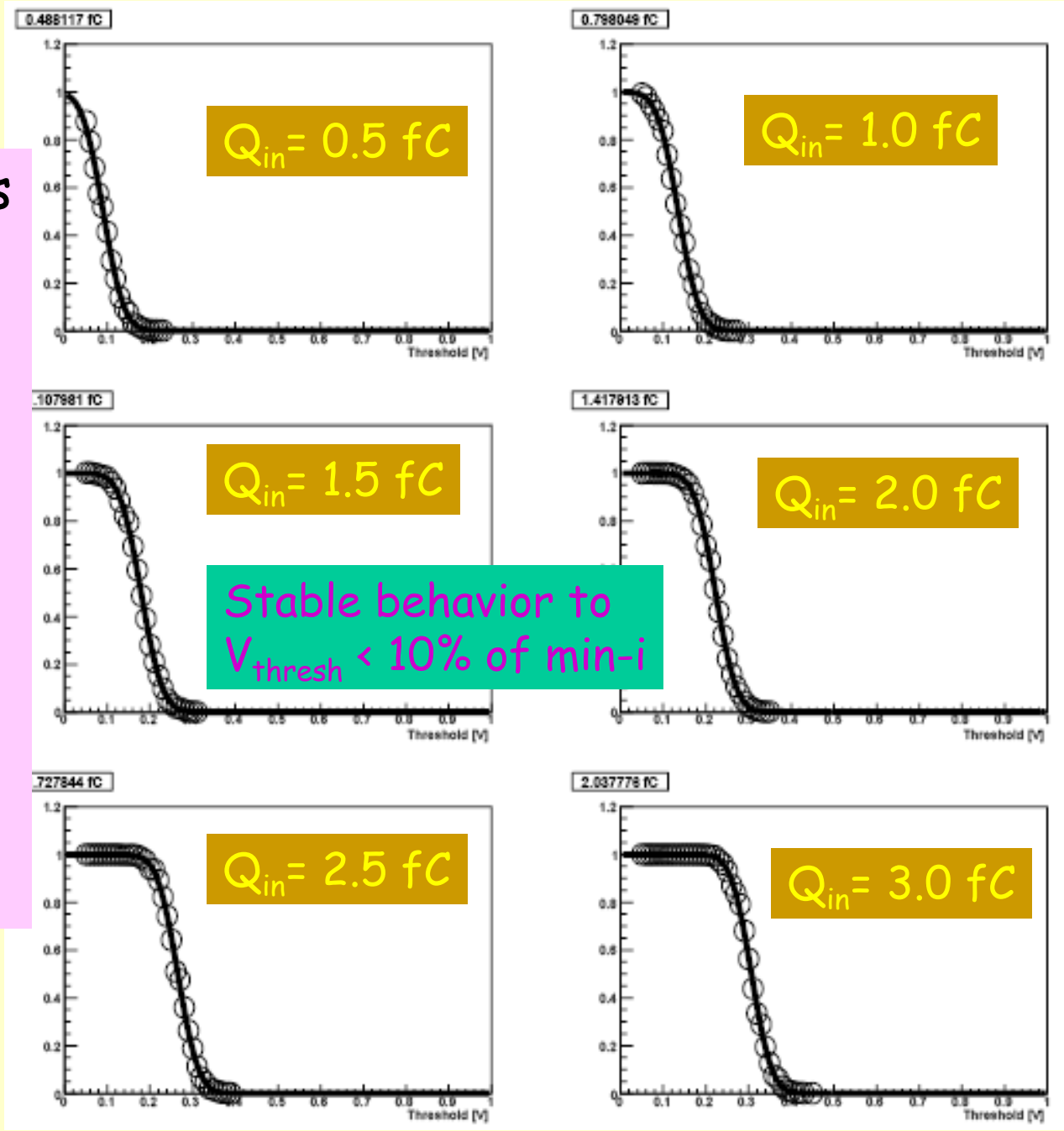
with 50% point giving response, and width giving noise



Noise vs. Capacitance (at τ_{shape} = 1.2 μs)

Loaded with Capacitor

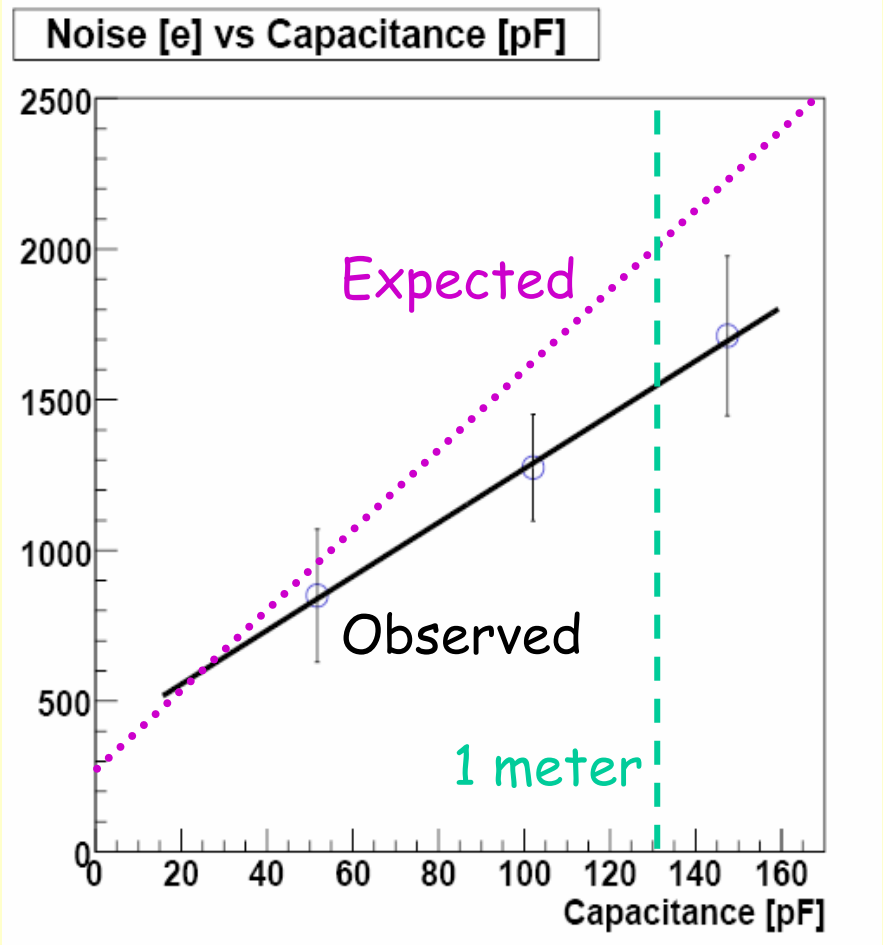
Measured dependence is (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with C in pF.

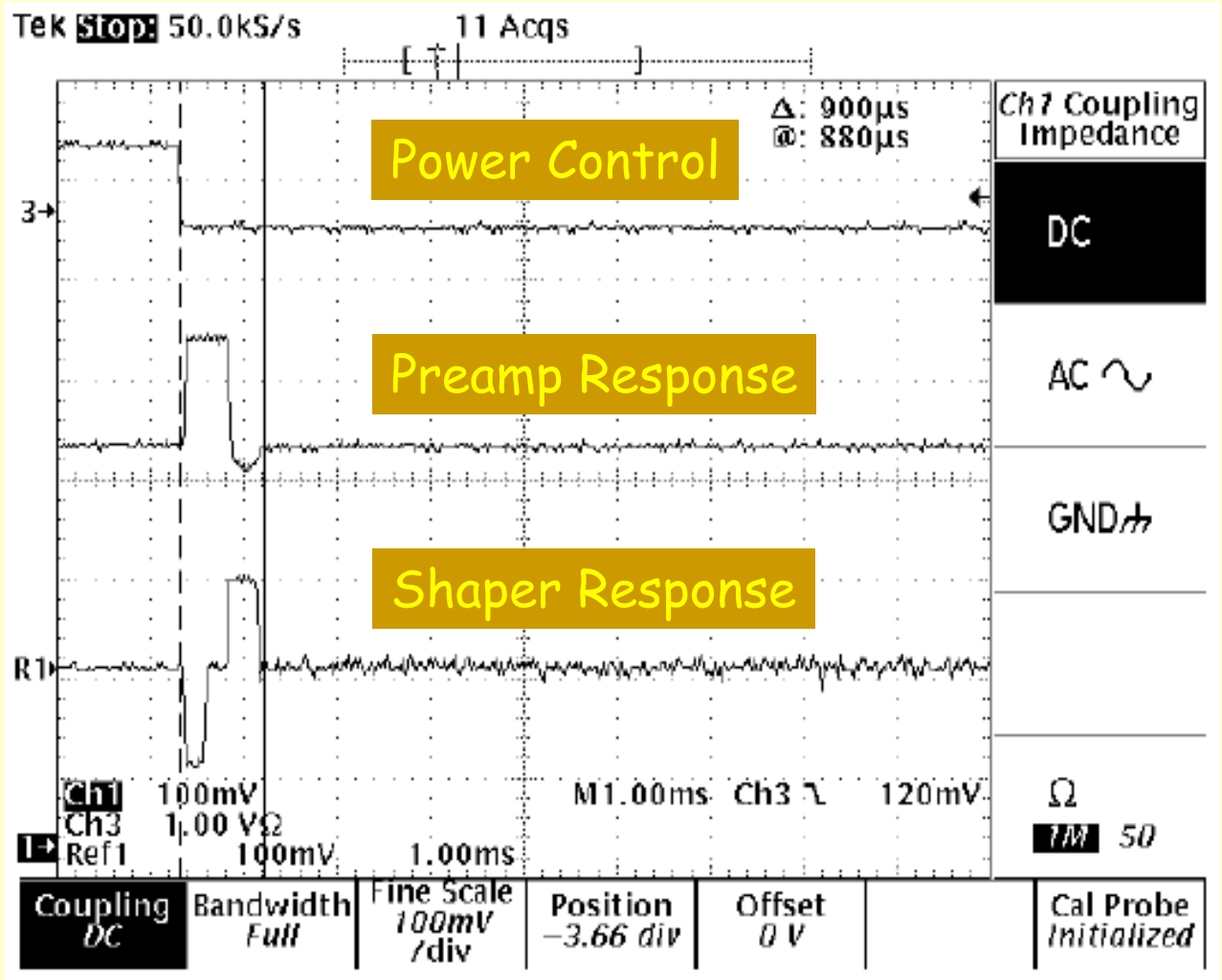
Connected to Ladder

Noise is approximately 30% worse; are currently exploring long shaping-time shielding requirements



Power Cycling

- As designed: Achieve 40 msec turn-on due to protection diode leakage
- Injecting small (< 1nA) current: Achieve 0.9 msec



LSTFE2 will incorporate active feedback to maintain bias levels of isolated circuitry when chip is "off".

LSTFE2

The LSTFE2 is currently under development; submission expected by end of year

- Retain 1.0-1.5 μs shaping time
- Further S/N optimization (still geared towards long ladders)
- "Off" state feedback to achieve power cycling goal (< 1 msec switch-on)
- 64-128 channels, with multiplexing of comparator outputs (pad geometry)