SID Vertex Detector

Summary of status and issues

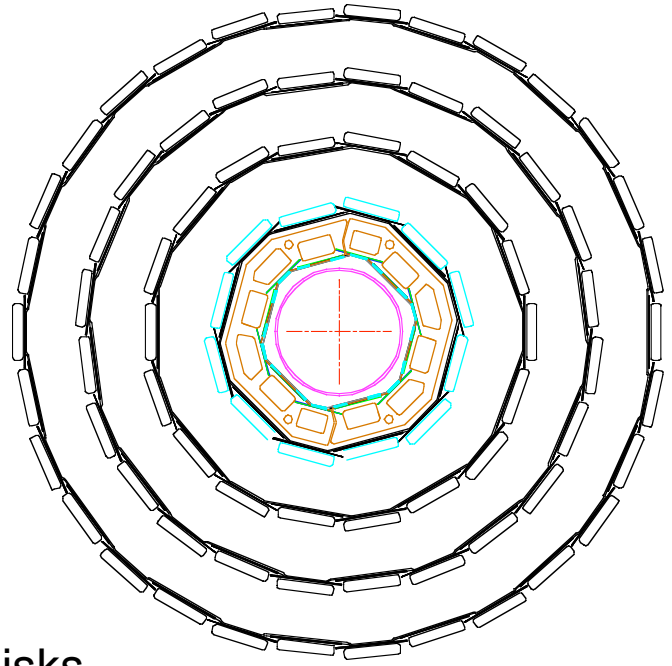
- SiD vertex design is based on extremely successful SLC CCD vertex tracker
- SiD in turn bases it's tracking on vertex information
  - 3D hits, excellent pattern recognition
    - No stereo in strip tracker
  - Must be robust
    - 5 barrel layers
    - 4 endcap disks/side
    - Backgrounds from the IR
    - EMI - experience from SLD suggests that this may be a problem
  - Minimum radius set by beam backgrounds
- Vertex barrel design is similar for most detector concepts

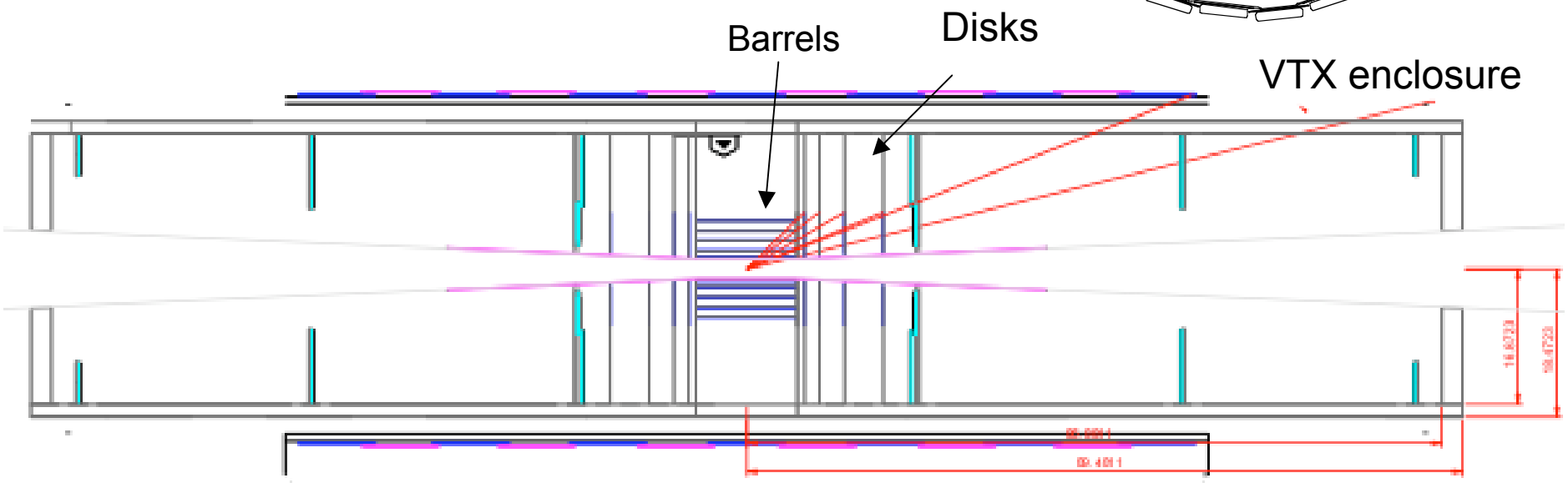
SiD Vertex Detector DOD Design

Barrel/disk design concepts:

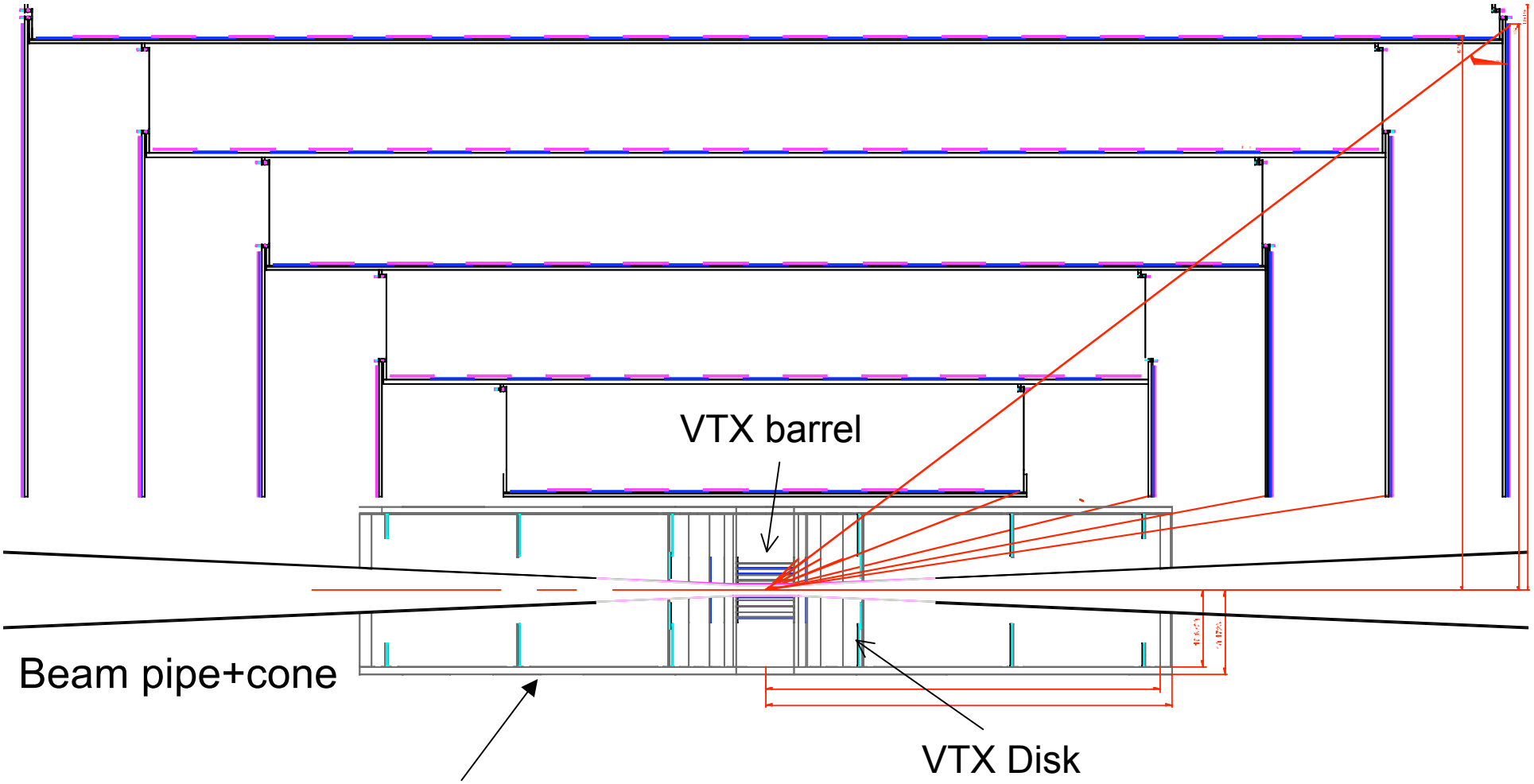
- 5 barrel layers
- 4 disks/side
- Large gap between outer vertex barrel and inner tracker barrel
- Installs as 2 halves
- Enclosure also supports the beam pipe assembly
- Inner tracker disks carried on the vertex support

End View





Vertex and half tracker



Vertex barrel ~ 150,000 mm^2
Vertex Disks ~ 120,000 mm^2

Performance Goals

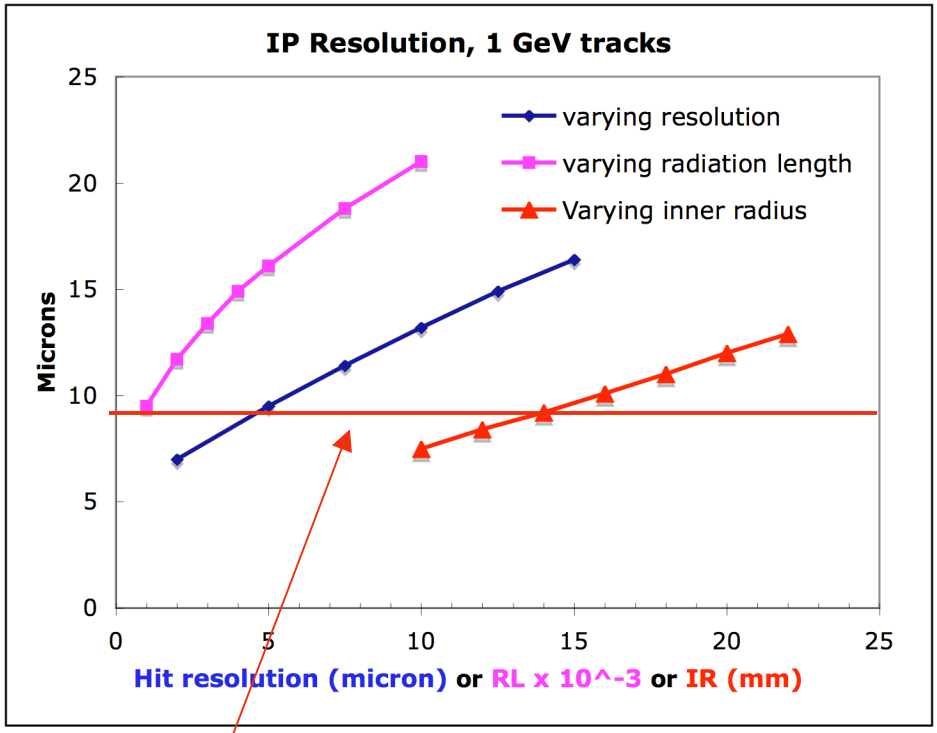
- Basic concept-independent “requirements”
  - Barrel resolution should be ~5 microns or better
    - Can be achieved in several technologies - but impacts power, readout speed, pixel design
  - Thickness should be minimal ~0.1% RL
    - Thinned silicon - a handling problem but can be manufactured.
  - Time resolution better than 50μs
    - Technology dependent - candidate designs range from 1 crossing (~300ns) to 50μs
- These goals appear achievable - and we assume them in the simulations. Much of the physics reach is technology independent - if the above goals are achieved. But there are usually compromises. Where can they be safely made?

Design Considerations

- Minimize inner radius
  - Constrained by beam backgrounds
- Minimize mass
  - Simplify services, low mass power and interconnects
- Robust design
  - Insensitive to temperature and power variations
  - Redundant where possible
  - Good time resolution
  - Resistant to EMI
- Power budget <20W average power in barrel
  - Set by gas flow considerations
  - Can be met by power cycling but high instantaneous power can cause problems due to resistive and inductive voltage drops

Performance Factors

- Inner radius
- Material
- Position resolution (<5 microns)
  - Binary or analog
  - Charge collection diffusion (MAPS) or drift (3D, SOI)
- Power dissipation (related to material)
- Time resolution (optimize pattern rec.)
- Cost - small area so sensors can be rather costly/mm^2
- Integration with tracker (especially disks)

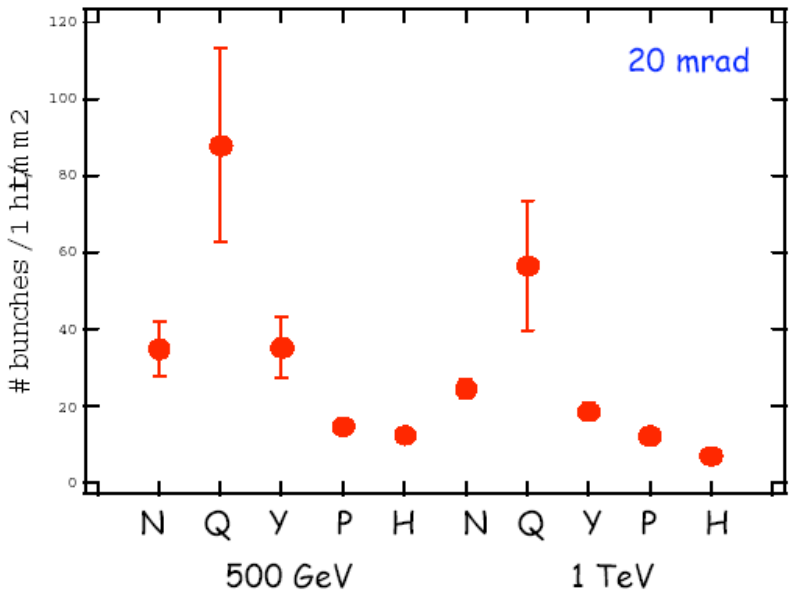


Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resoluton
- 1.4 cm inner radius

Varying each parameter

Backgrounds in the Vertex Region

GEANT3 modeling for SiD
By Takashi Maruyama



N – nominal
Q – Low Q
Y – High Y
P – Low P
H – High Lum.

Cécile Rimbault, Phys. Rev. ST Accel. Beams 9:034402,2006

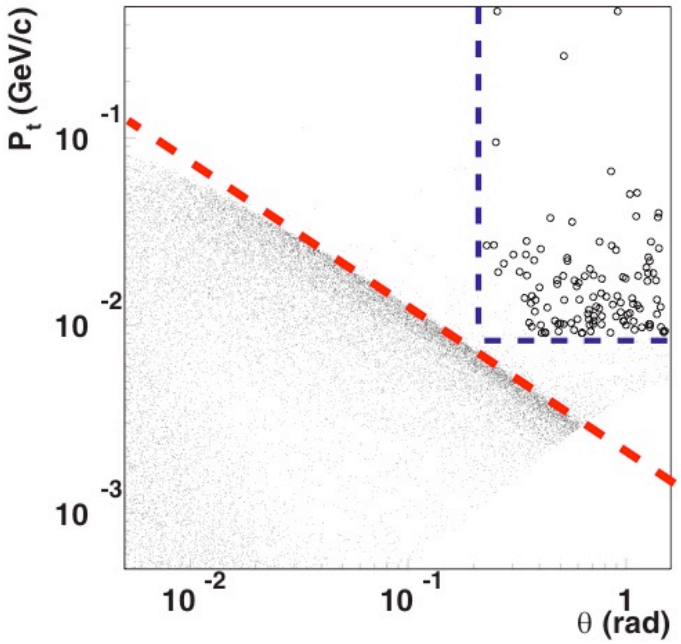
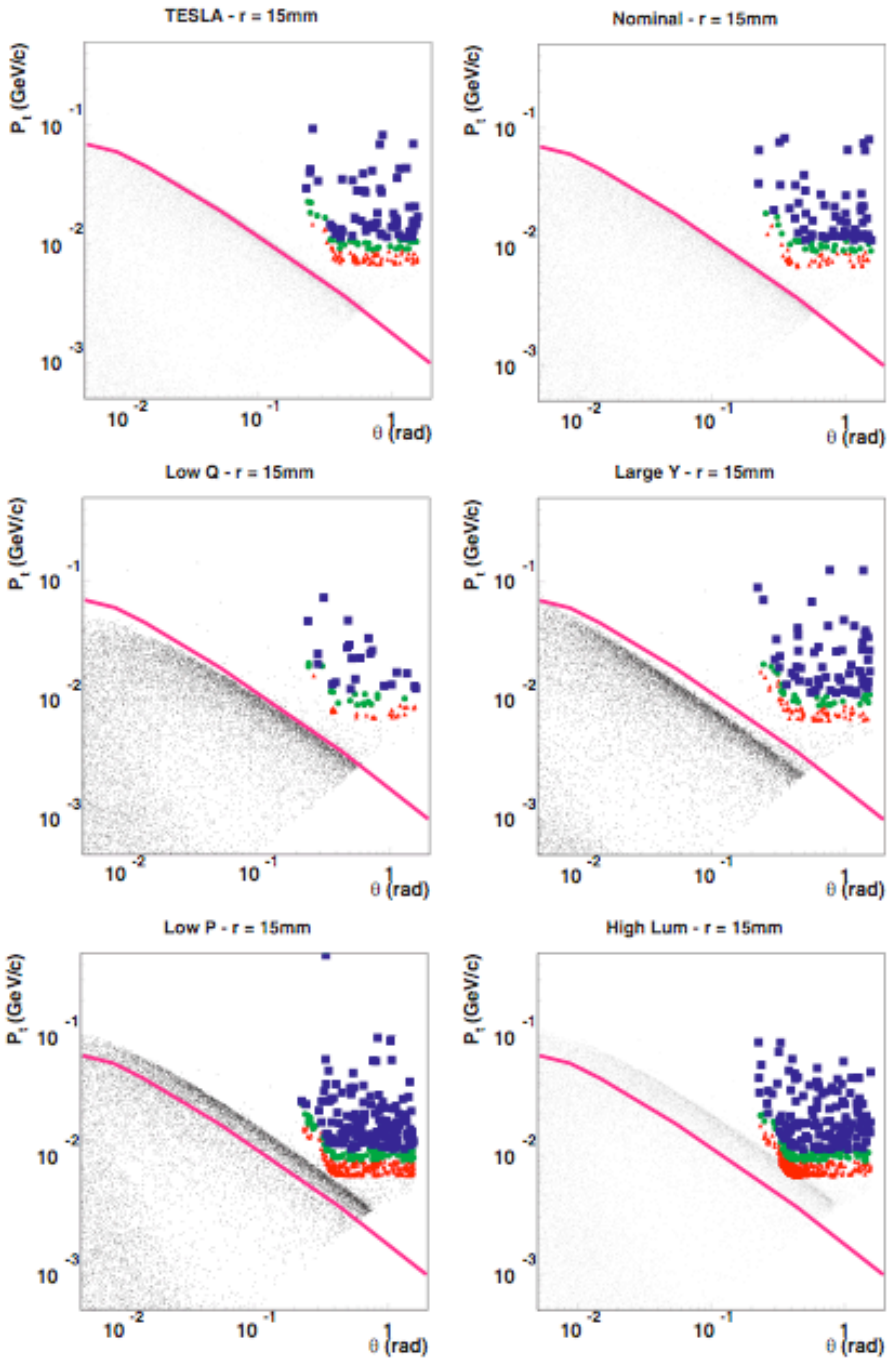


FIG. 7. (Color) Distribution of P_t versus θ for electrons from IPC processes. The region corresponding to particles reaching the VD (circles) is indicated with the two dashed lines for the detector configuration described in the text. A thick dotted line highlights the edge of the beam-beam deflection induced accumulation zone.

Beam backgrounds in various machine scenarios for r=15mm
B = 3, 4, 5 Tesla

(C. Rimbault*, P. Bambade, K. Monig, D. Schulte, Phys Rev. ACCELERATORS AND BEAMS 9, 034402 (2006))



Nominal

Low power

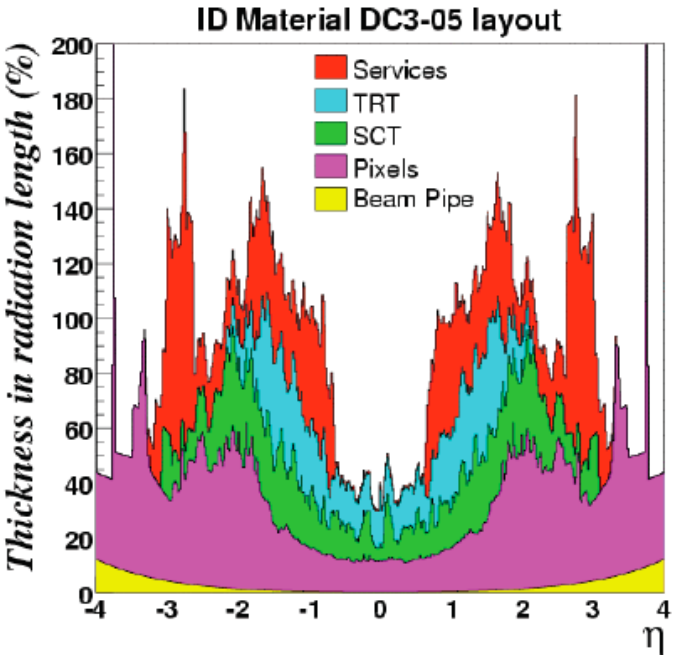
High Lum

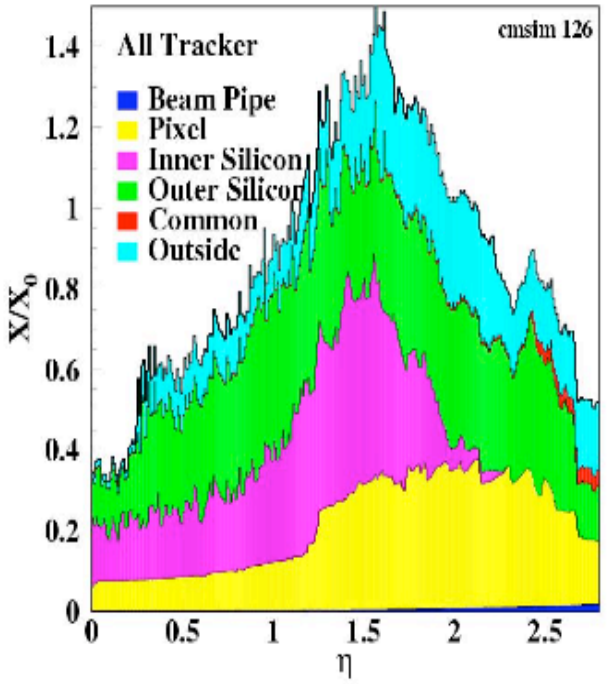
Material

VXD Barrel Material

	SLD VXD3		SiD VXD	
Beampipe liner	Ti 50μm	0.14%	Ti 25μm	0.07%
Beampipe	Be 760μm	0.22%	Be 400μm	0.07%
Inner gas shell	Be 560μm	0.16%	(Note 1)	0
Ladder/layer		0.41%		0.11%
Outer gas shell	Be mesh	0.48%		0.28%
Cold N2 Gas		0.05%		0.05%
Cryostat coating	Al 500μm	0.58%		0.22%
Cryostat foam	Urethane	0.44%	NilFlam	0.12%

Note 1) Cooling gas can be brought in from two ends if overall power is low enough to for gas cooling.





You can't always get what you want …
Much of this is cooling..

Material Distribution from DOD

Sensors are ~42% of total Material in the DOD model

Readout and services are really guesses in the absence of a technology choice.

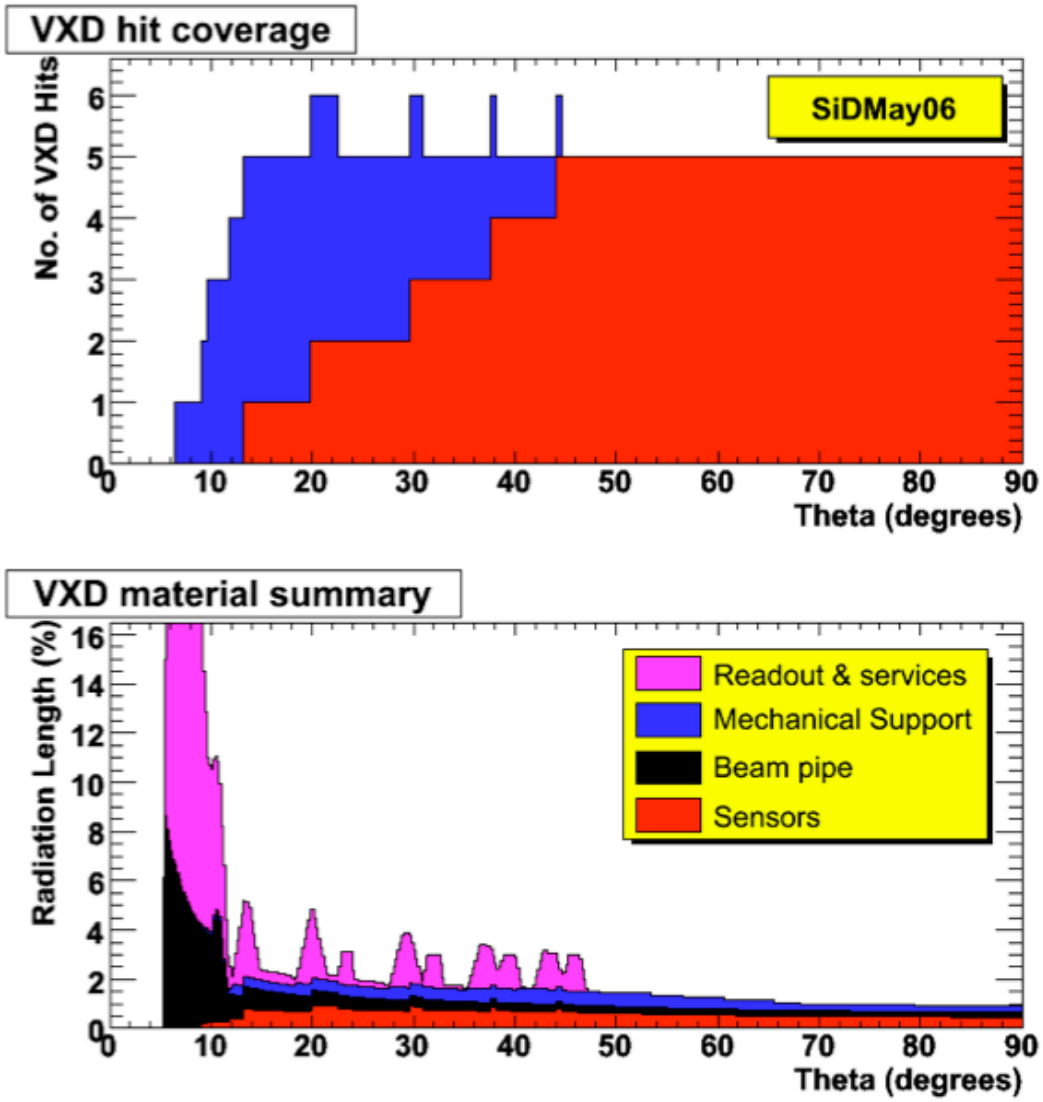


Figure 33 VXD hit pattern and material summary as a function of polar angle.

Physics and Simulation

- A first pass full simulation of detector was implemented in 2004
  - Migrated to org.lcsim
  - Hit digitization -
    - CCD model implemented in org.lcsim
  - pattern recognition
    - First pass completed for Snowmass, redo for planar devices
- Physics simulation
  - Quality factors
    - Vertex reconstruction
    - Flavor tagging
    - Quark charge determination
    - Luminosity cost (cheaper to build an efficient detector)
  - Studies of specific final states (ILC benchmarks) to be done

$$e^+e^- \to Z^0H^0, BR(H^0 \to b\bar{b}, c\bar{c}, \tau^+\tau^-)$$

$$e^+e^- \to W^+W^-$$

$$e^+e^- \to t\bar{t}(6\,jets)$$

$$e^+e^- \to f\bar{f}$$

Simulation Results (from DOD)

Pattern recognition based on vertex:

- CCD simulation
- 3 point 3D search algorithm - sensitive to background combinatorics
- Efficiencies are robust against backgrounds
- Vertex disks?

ttbar events

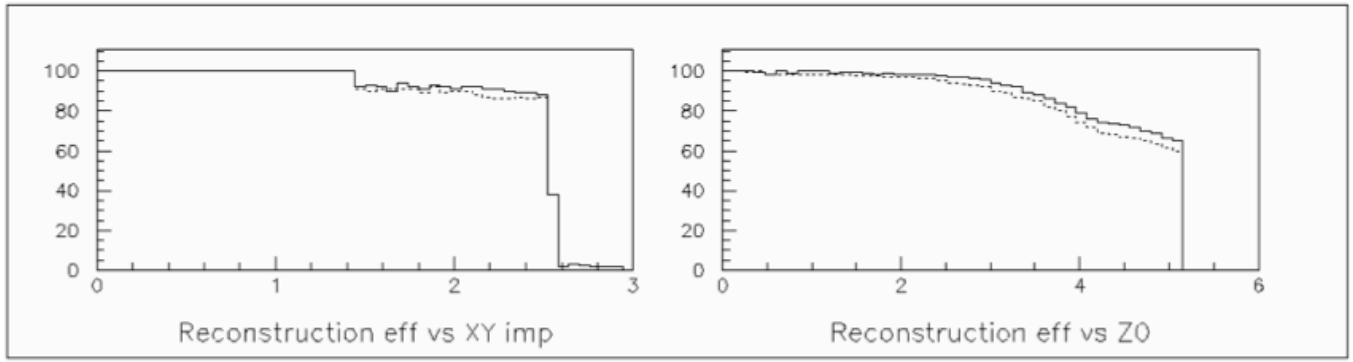


Figure 39 Reconstruction efficiency as a function of track impact parameters. Reconstruction cuts are set at 3.0 cm for the XY impact parameter and 5.0 cm for Z. Solid lines correspond to high Pt (> 1 GeV), dashed to low Pt (< 0.5 GeV) tracks.

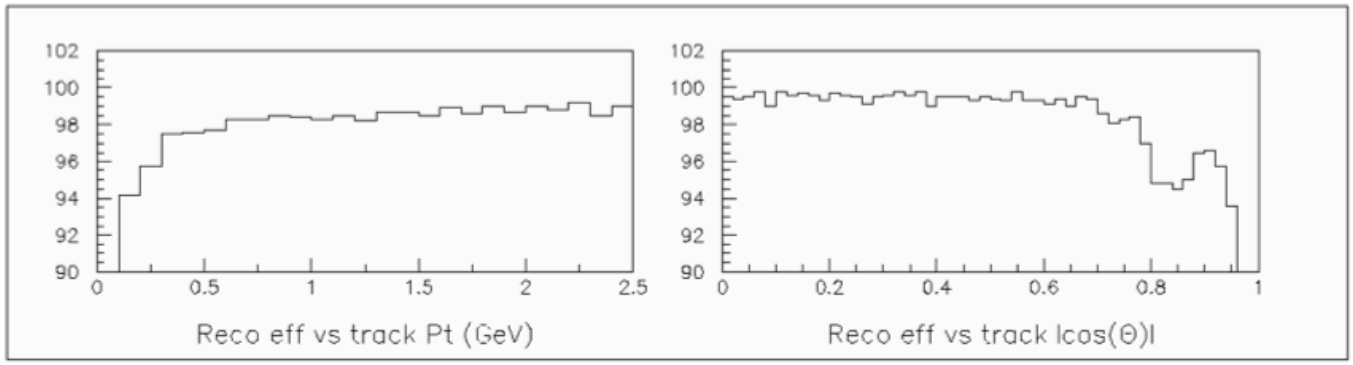


Figure 40 Reconstruction efficiency as a function of tracks Pt and dip angle.

Candidate Technologies

- CCD
  - Column parallel
  - ISIS
  - Short column pair
  - Fine pixel
- CMOS MAPs
  - Chronopixel
  - Mimosa line
  - FAPs, CAPs
- SOI
- Vertically integrated (3D)
- DEPFET

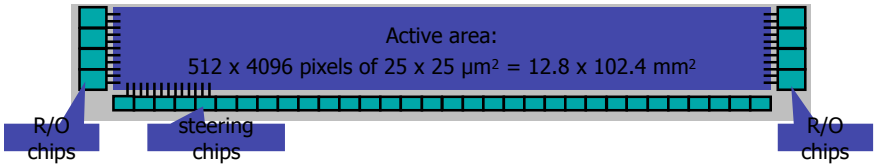
This stuff is sexy and interesting
but not the subject of this talk
At least one of these will work…

But they do affect the design

Impact of Technology on Design

Assume all technologies achieve 50μs time resolution, 5 μ space resolution, 100 μ detector thickness

- DEPFET require support outboard chips for readout, clearing field, could be partially self supporting



- CCDS require support chips for clock generation. Low temperature environment, cryostat.
- MAPS require "stitching" of reticle sized sensors. Lack of pmos means additional chips are needed or more complex circuits.
- 3D chips will require stitching or inter-chip connection, dead area at the edge could be minimal so tiling may be possible.

Design of the vertex detector depends on amount of dead space around the active area, outboard chips and services, tiling possibilities …

Power has a large impact. CCDs and DEPFETs use no or minimal per pixel front end power.

Power Considerations

Power cycling is necessary/desired for many technologies

- instantaneous power = average power x 950-100) (achievable rise/fall times). 20W=>2kW
- At 1.5 V peak current ~666 A, 3 cm diam. of copper/side needed for 50mV drop
- Serial powering can reduce peak currents
  - Individual ladder regulators
  - V*n, I/n, ΔV tolerances relaxed with local regulation
  - Requires local regulator circuitry
  - Being pursued for SLHC, primarily by ATLAS
- Serial powering is promising, but needs R&D.
  - How much added material?
  - Rise times
  - Integrate power control with readout IC
- Minimize power consumption in any case…

Serial Powering

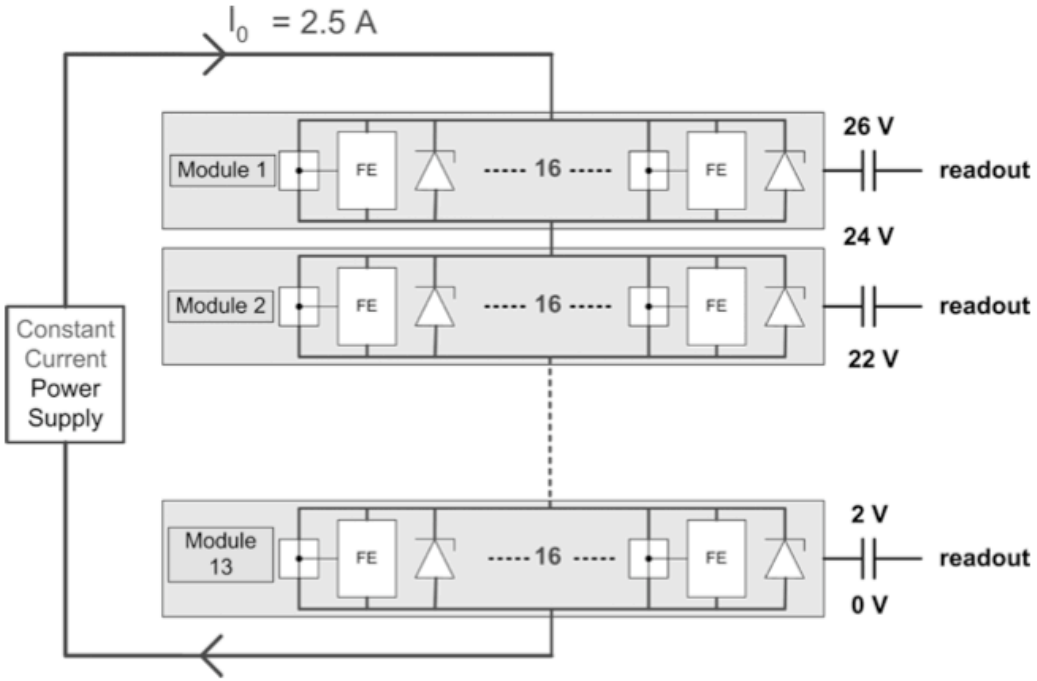


Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt regulator generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

Atlas SLHC design

Initial tests indicate good noise performance

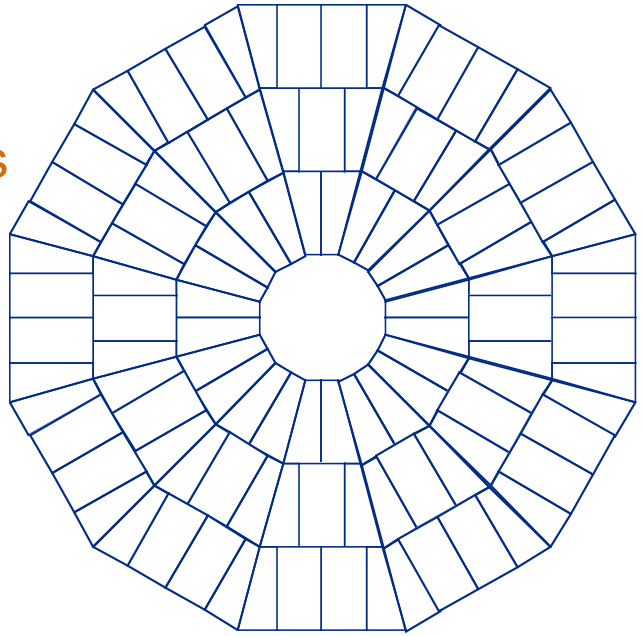
Power: 1000W/side
V = 1.5 V
Wire inductance ~ 3 μH
Rise time - 1 ms
V_{ind} ~ 2.4 V

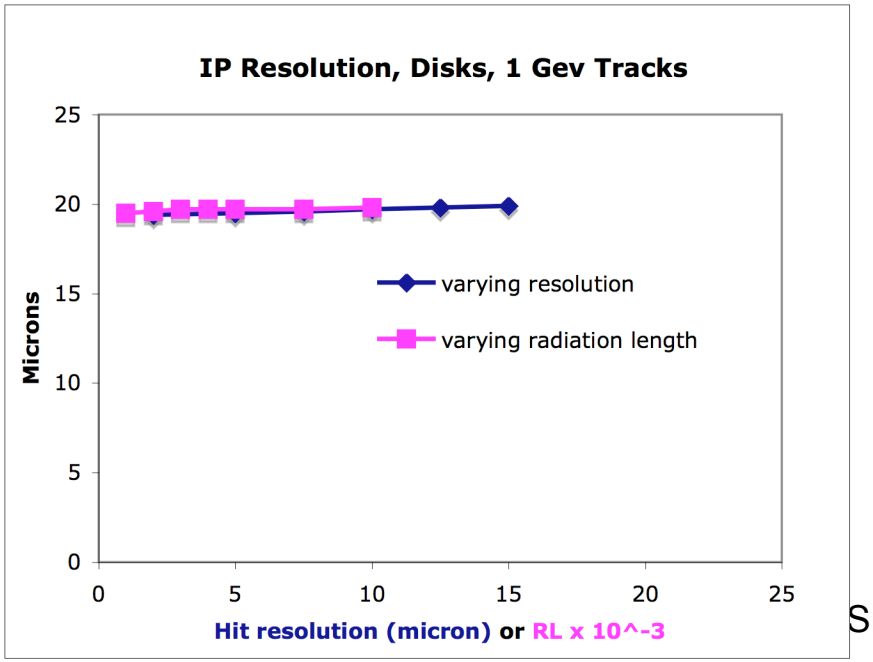
Serial powering(12x)
V_{ind} ~ 0.2 V

Probably can handle ~0.5V variations, but we need to look at control and regulation issues

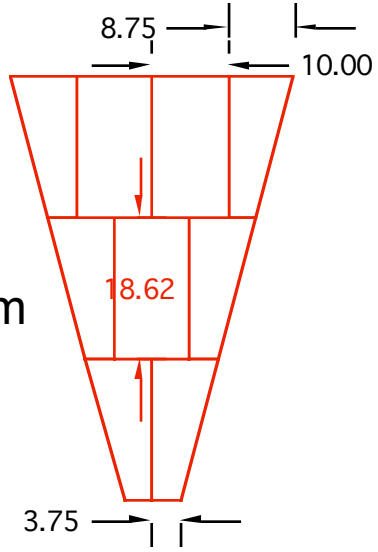
Forward Disks

- Less detailed thought has gone into the design
  - Necessary resolution, Thickness constraints
- Where do pixels give way to strips?
  - Occupancy
  - Resolution/pixel size (is >10 μ acceptable?)
  - *How much does small angle incidence degrade barrel pixel resolution?*





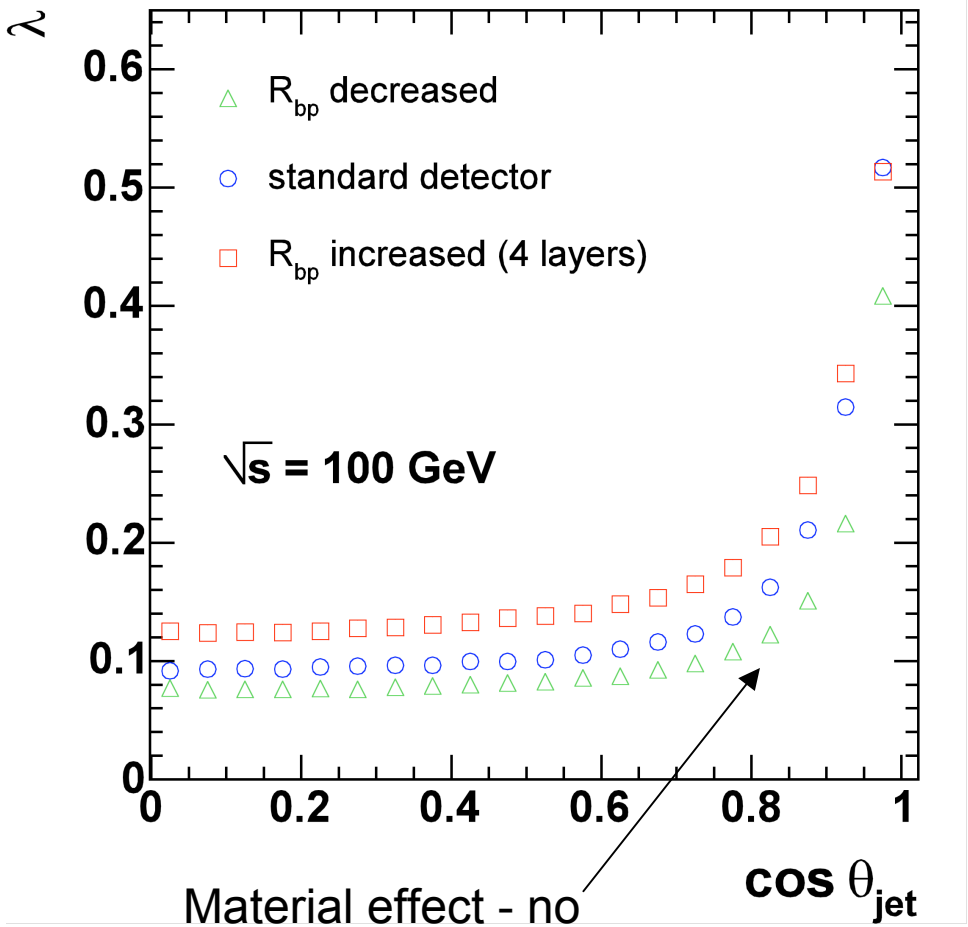
Example of
a disk formed from
3 types of CMOS
or 3D sensors



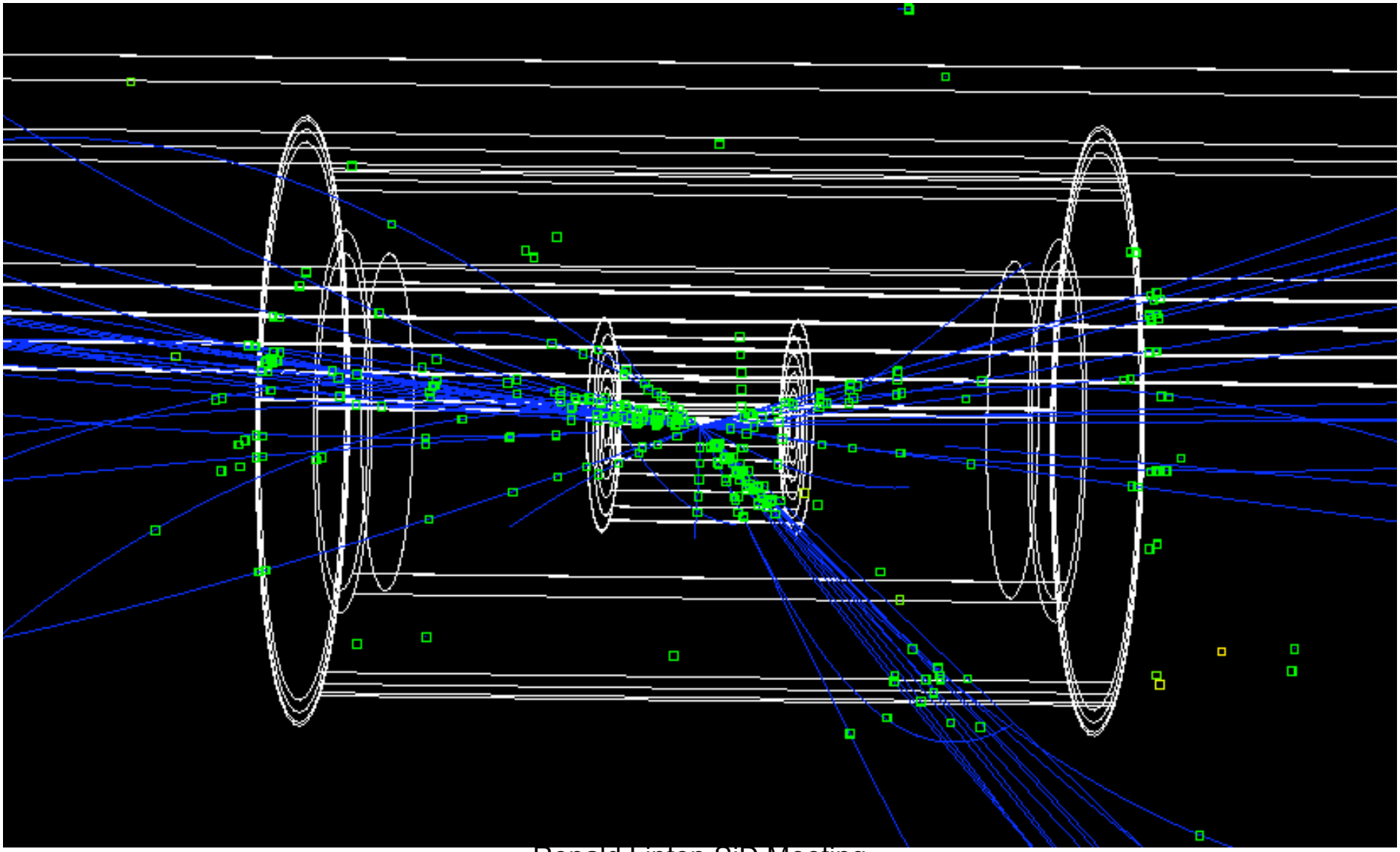
Forward Physics

- A_{fb} asymmetry good test of forward vertex quality
  - Hillert-studies of vertex charge (λ~jet charge "leakage")
  - How does hit resolution degrade vs θ?
- What vertex disk segmentation is needed for pattern recognition in complex events?
  - Zh, $\tau_1\tau_1$
- SiD has more freedom to optimize the forward tracker than TPC-based detectors - could be a significant advantage
- Avoid overdesign, power savings lead directly to reductions in material

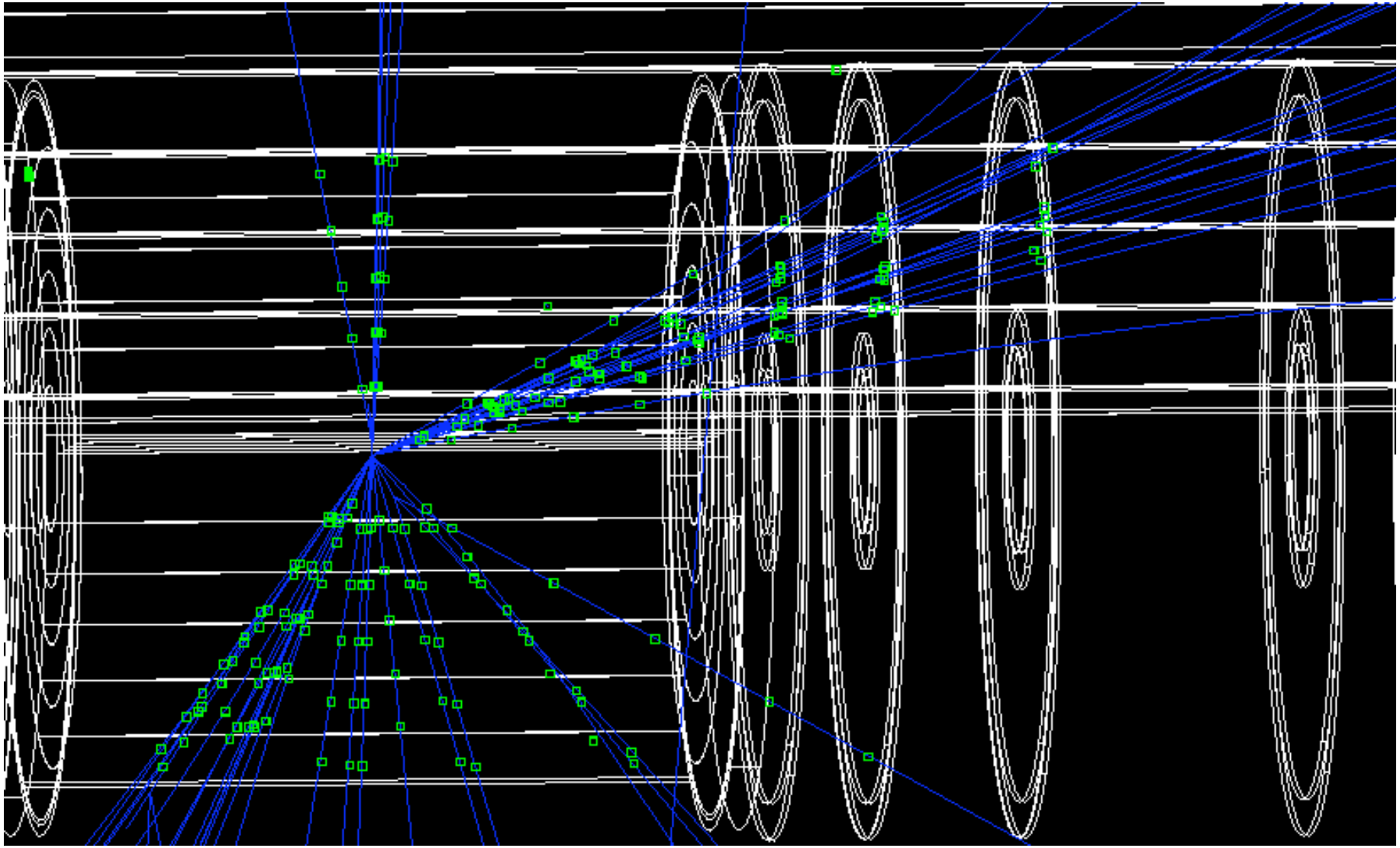
(S. Hillert-Snowmass)



Zh Event

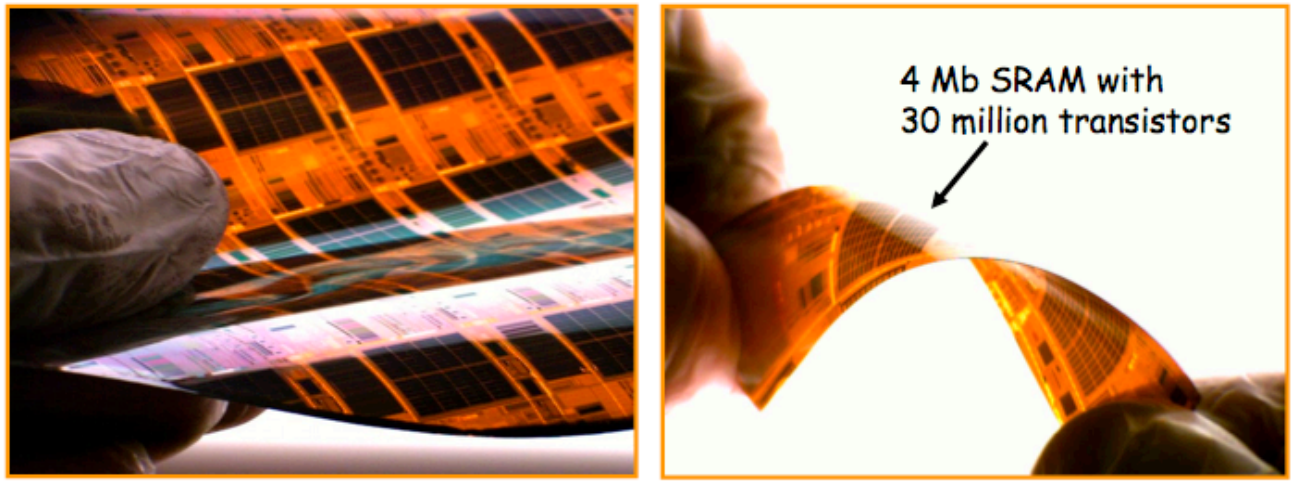


Zh event 2



Fabrication

- We need to gain experience working with thin silicon
  - Industry usually uses handle wafers
  - How to bond?
    - 20 micron silicon shatters with ultrasonic bonds, 50 microns may be OK
  - Laminate to CF support structure?
  - Thin silicon is flexible - new design issues - opportunities
  - Thermal stresses on thinned materials



Wafer thinned to 6 microns and mounted to 3 mil kapton (MIT LL)

Conclusions

- I believe that a vertex detector meeting the ambitious ILC goals can be built
- Technical issues are difficult but many are issues that the semiconductor industry also is addressing
- Barrel region is reasonably understood
- We need to know more about forward requirements
  - Backgrounds and pattern rec.
  - Required resolution
  - Integration with tracker
  - Physics studies.
- We need to study mechanical and power issues in more detail