# SiD ECAL Status and Plans

David Strom – University of Oregon

- Detector concept
- Second sensor prototypes
- Energy resolution
- Cable status
- KPiXs news

Si-W work – personnel and responsibilities

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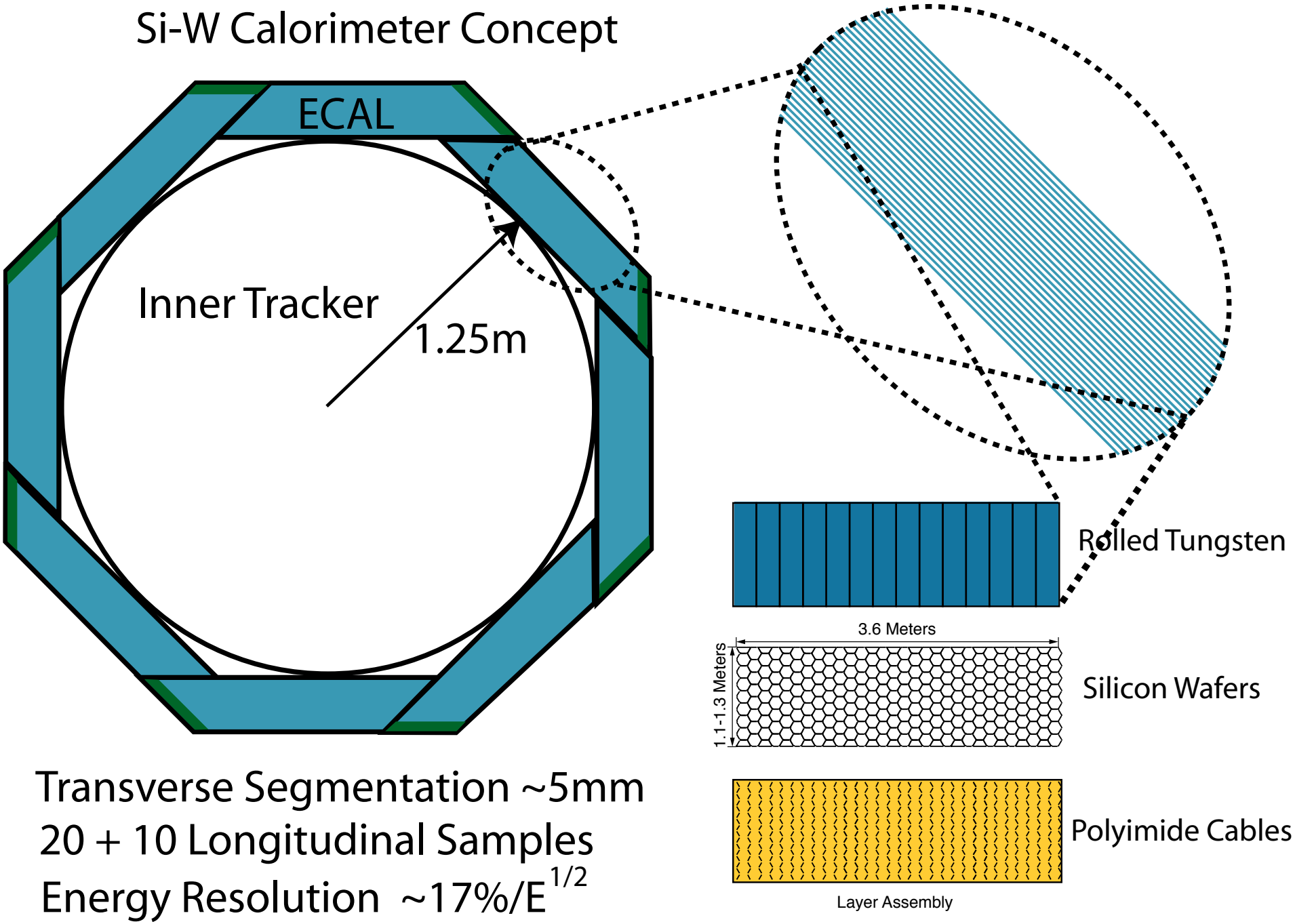
|---|---|---|---|---|
| Annecy | BNL | UC-Davis | Oregon* | SLAC |
| **Mechanics** | **Electronics** | **Bump Bonding**<br>**Cabling**<br>Mechanics | **Si Detectors**<br>Mechanics<br>Simulation | **Electronics**<br>Mechanics<br>**Simulation** |

* This work includes contributions from Oregon students Mary Robinson and Asher Tubman.

# Si-W Calorimeter Concept



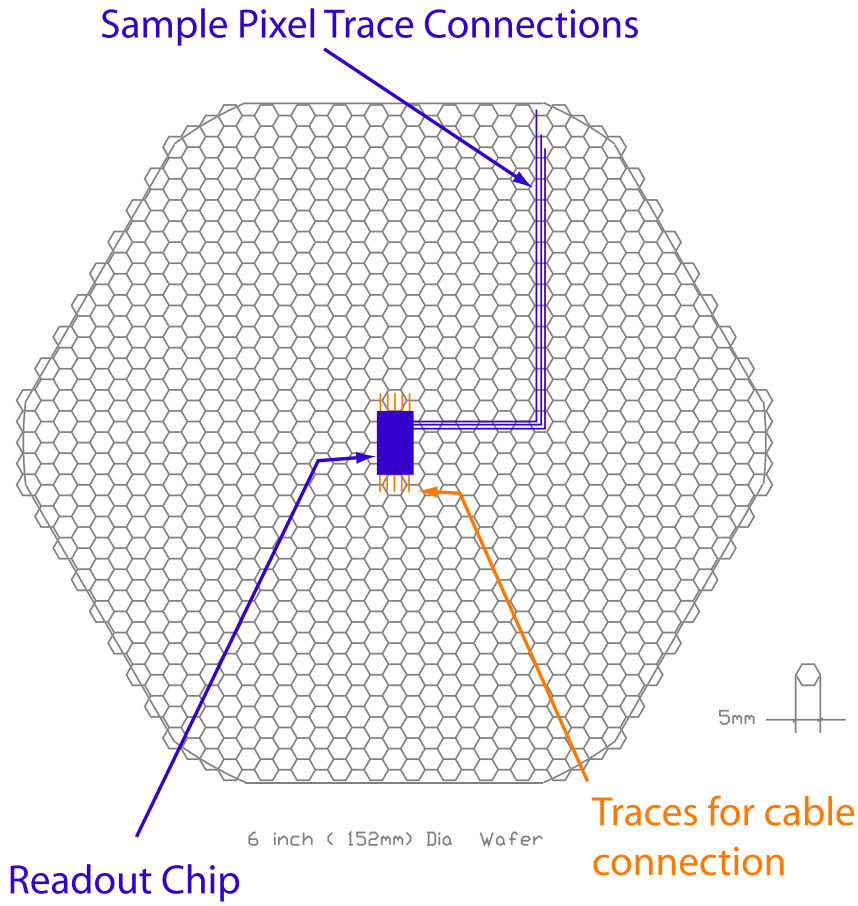

Transverse Segmentation ~5mm

20 + 10 Longitudinal Samples

Energy Resolution ~17%/$E^{1/2}$

# Silicon Concept

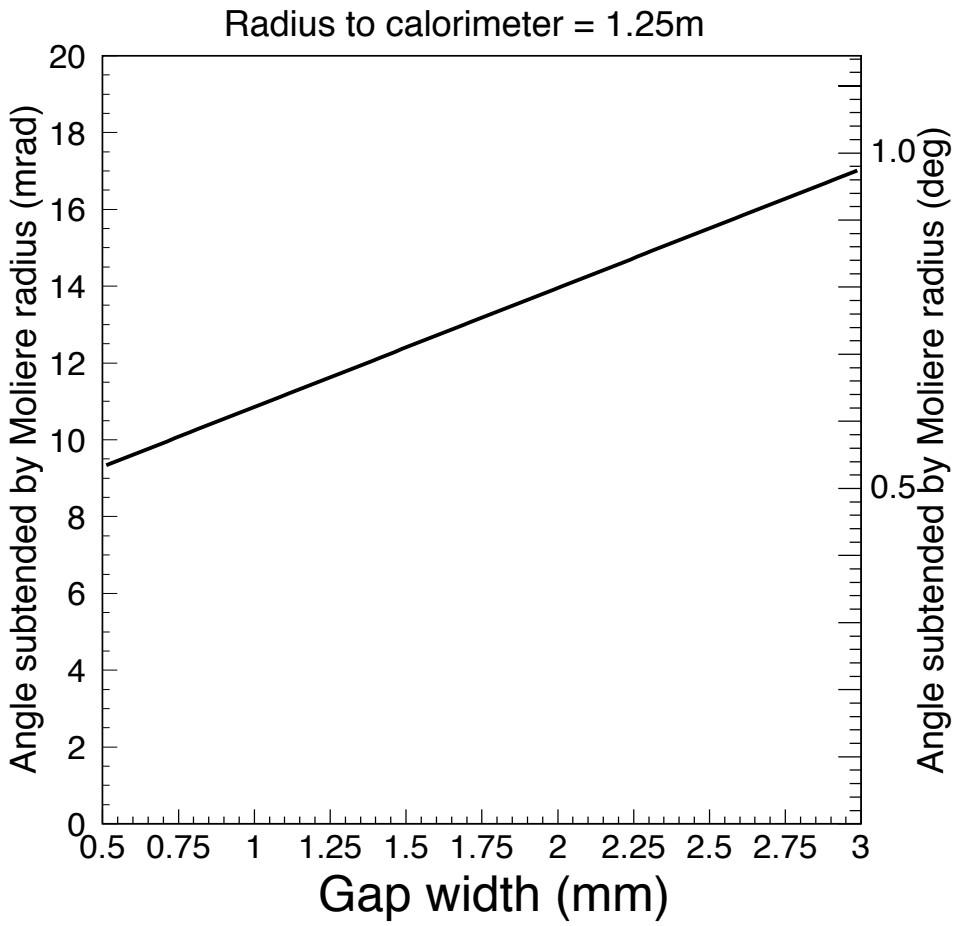
- Readout each wafer with a single chip
- Bump bond chip to wafer
- To first order cost independent of pixels /wafer
- Hexagonal shape makes optimal use of Si wafer
- Channel count limited by power consumption and area of readout end chip
- May want different pad layout in forward region



Critical parameter: gap between tungsten layers.

| Config. | Radiation length | Molière Radius |
|---|---|---|
| 100% W | 3.5mm | 9mm |
| 92.5% W | 3.9mm | 10mm |
| +1mm gap | 5.5mm | 14mm |
| +1mmCu | 6.4mm | 17mm |

Assumes 2.5mm thick tungsten absorber plates




**Need to separate EM clusters so that track-EM cluster association can be performed**

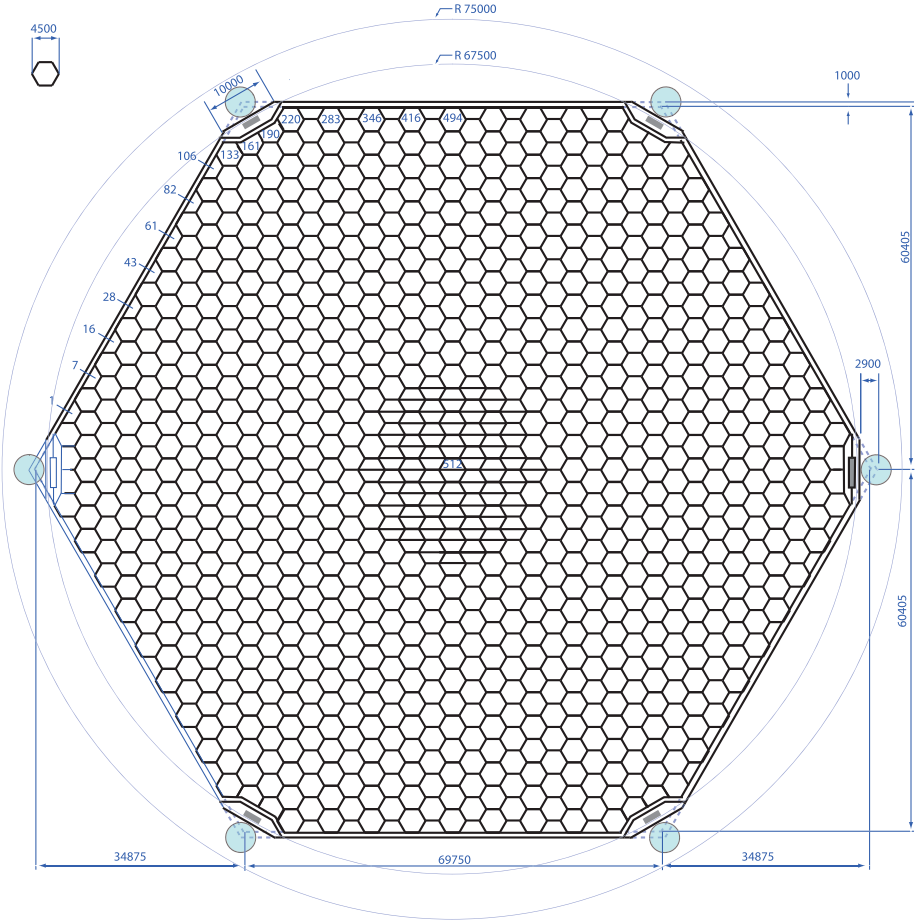
**Impact of gap on PFAs is not yet quantified with simulations**

Changes to sensor geometry

- Current detectors have 757 pixels. Try for 1024 pixels
- Optimize stray capacitance for cold machine
- Current detectors do not have vertices removed

# New detector layout

- $973 + 51$ pixels
- Possible top side bias
- Vertices removed to allow for spacers
- Long dimension of the pixel is 4.5 mm
- Pixel area is $(3.63\,\mathrm{mm})^2$
- Maximum radial dimension of active area is $< 67.5$ mm



## Implication for dead space

- Dead space is dominated by edges

- Hexagonal detectors give lowest possible dead space

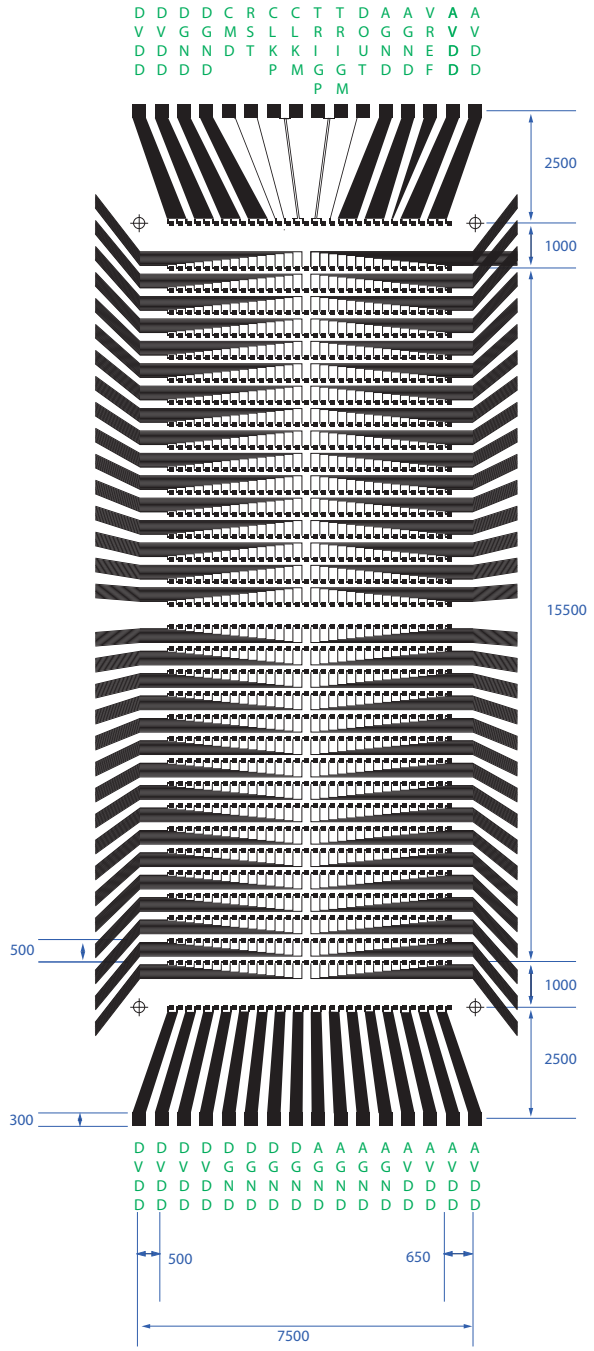
$$f_{dead} = \frac{4(w_g + c)}{\sqrt{3}h} \sim 5\%$$

where $w_g$ is the guard ring thickness (1mm) and $c$ is half the clearance between detectors (0.4mm). For proof http://arxiv.org/abs/math.MG/9906042/

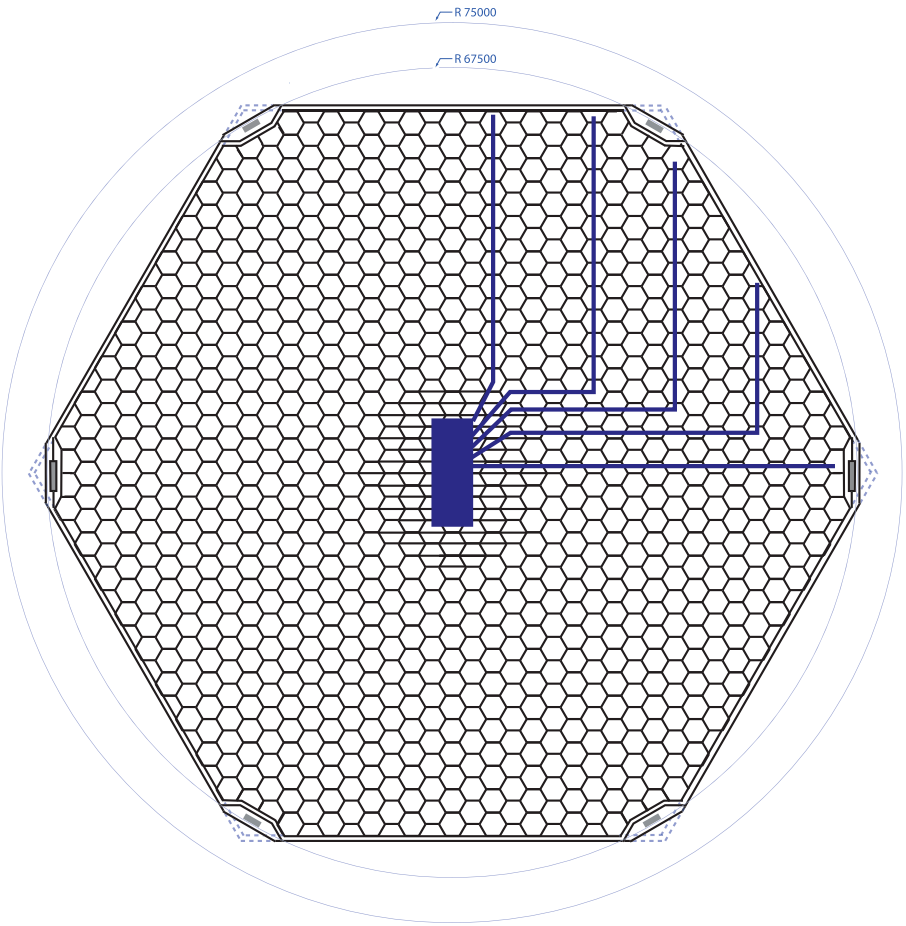
- Lost area at vertices is about 0.7%

- Lost area for top side bias is about 1.4%

- Trace layout minimizes maximum capacitance
- Use thinner traces near KPiXs chip
- Low resistance power and ground connections.
- Symmetric clock signals



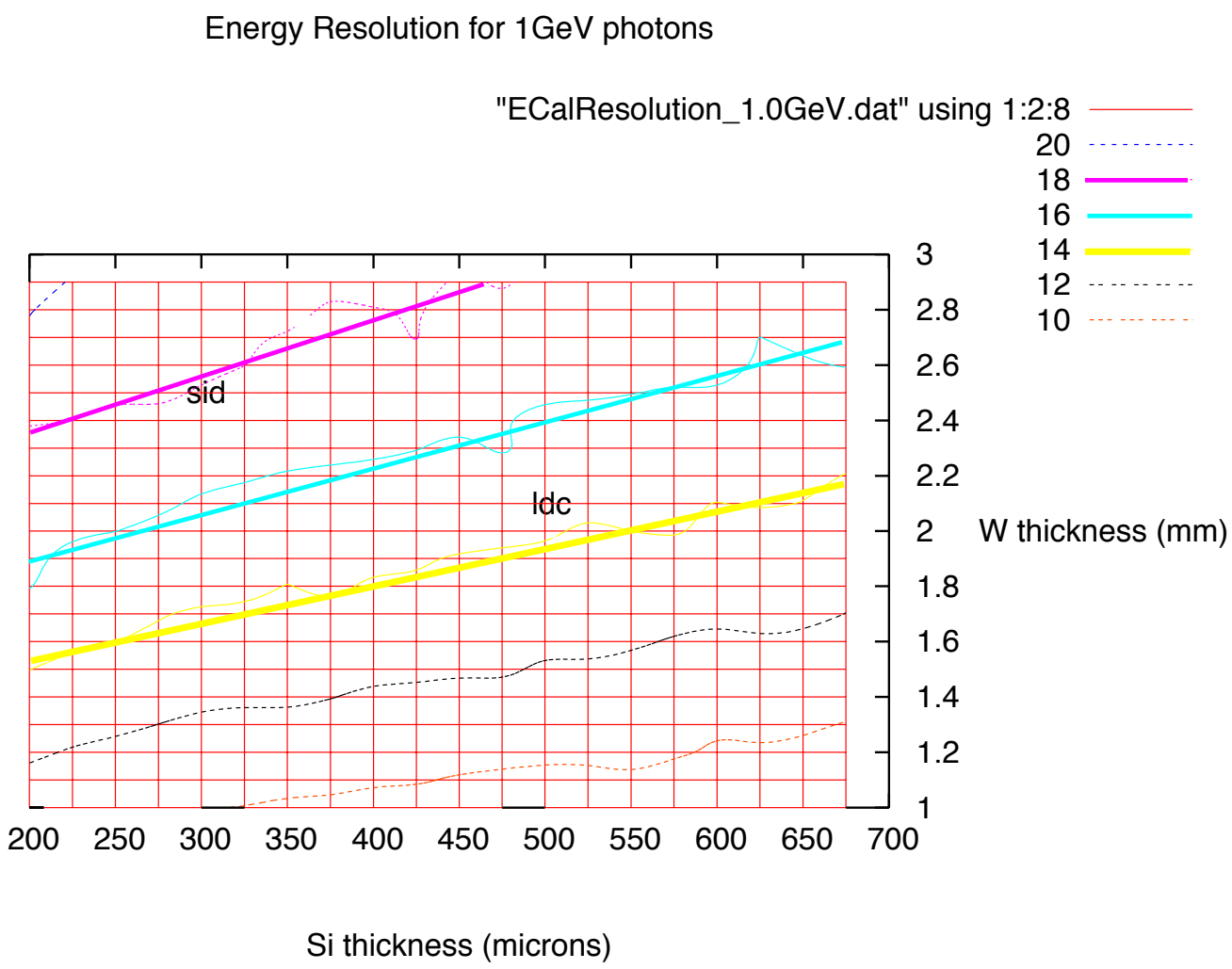
- Suggested trace routing



# Energy Resolution

Energy resolution depends on

- Tungsten thickness
- Silicon thickness
- Detector depth




Iso-resolution contours from Norman Graf

Line fit by eye (Strom)

Norman finds the resolution is given by

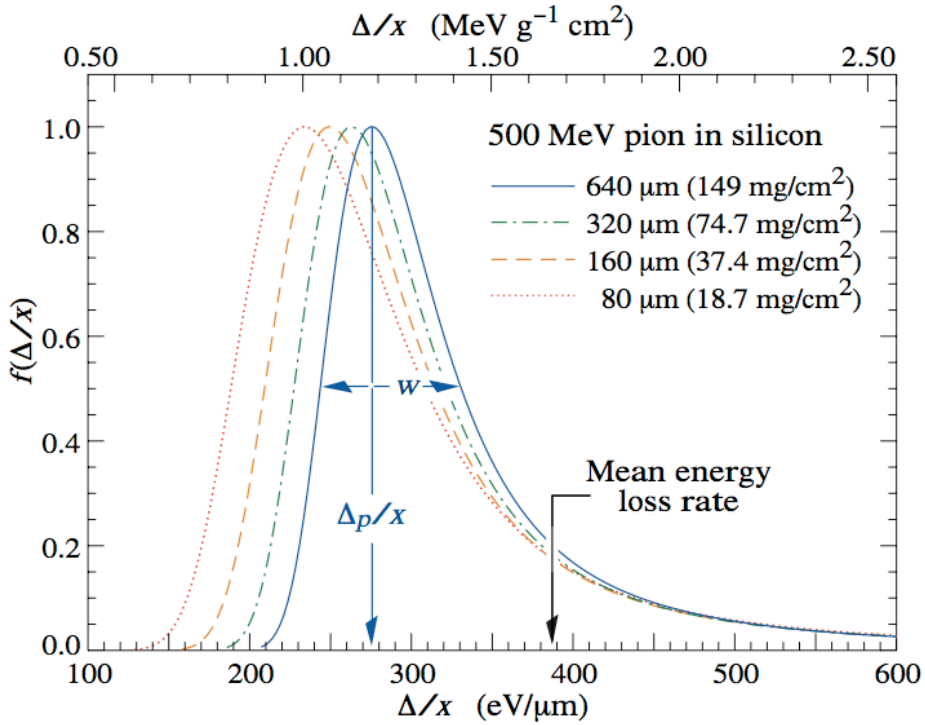
$$\frac{\sigma}{E} \simeq \left[ -1.8 \left( \frac{t_{Si}}{300\mu\text{m}} \right) + 11.5 \left( \frac{t_W}{2.5\text{mm}} \right) + 8 \right] \%$$

where $t_{Si}$ is the silicon thickness and $t_W$ is the tungsten thickness

- Doubling silicon thickness to 600$\mu$m would reduce resolution by 1.8%
- Decreasing tungsten thickness by 5% would reduce resolution by 1.4%

Optimization of ECAL sampling and study of digital HCAL to catch leakage not yet complete

Ray Frey found that change in resolution is consistent with the expected change in fluctuations in energy deposition with silicon thickness



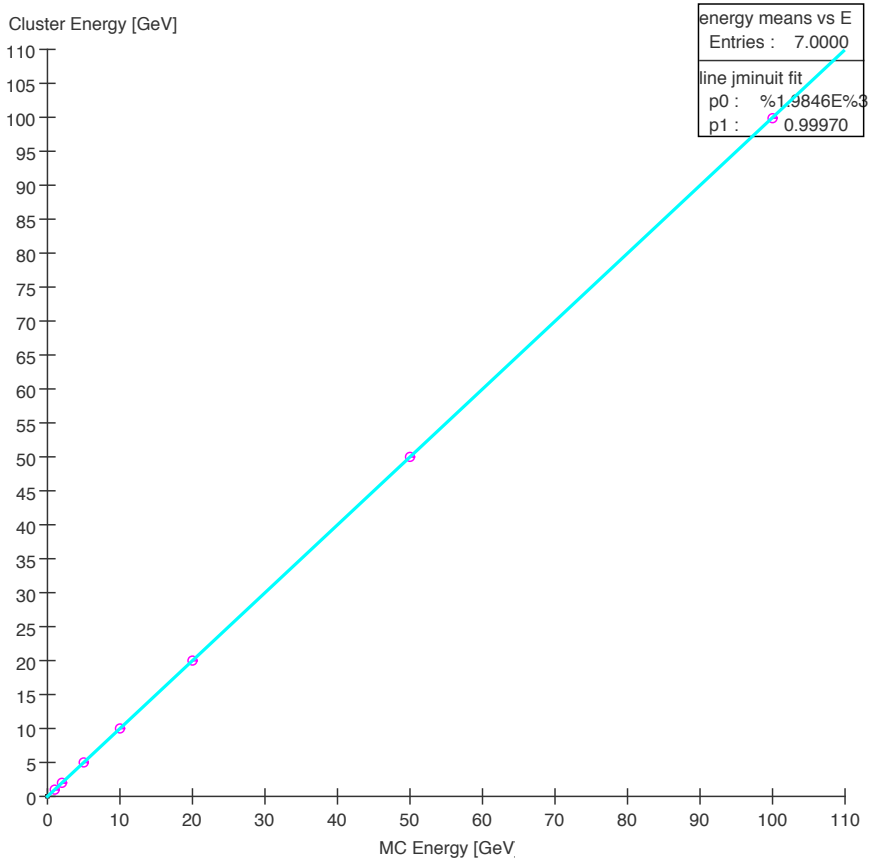

PDG, H. Bichsel, Rev. Mod. Phys. 60, 663 (1988).

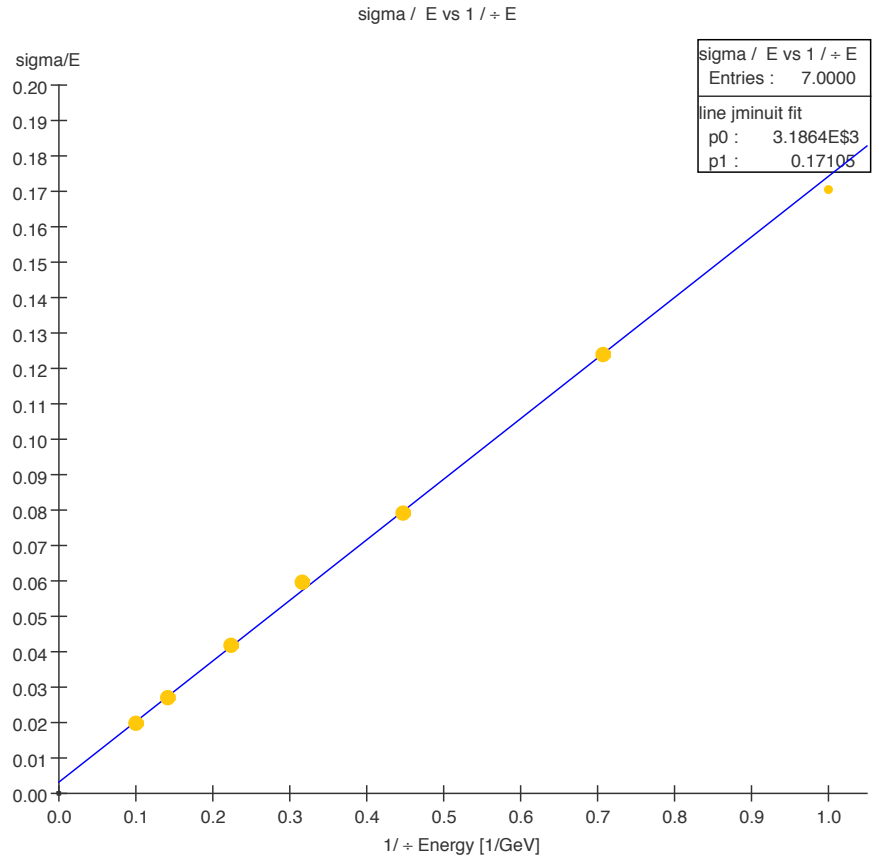
For $t = 320\mu$m $\frac{w}{\Delta} = 2.884$
For $t = 640\mu$m $\frac{w}{\Delta} = 3.883$

Here $\Delta$ is mean and $w$ is full width at half max

Default configuration: 20 thin layers (2.5mm, dens24 )
10 thick layers (5.00mm, dens24)

Norman Graf finds ideal behavior with proper weighting, energy and resolution scales ACME0605 with dens25, ecal 2.71mm, 5.43mm, 7.5mm hcal +scint



Physics case for better energy resolution unclear:

- Jet energy resolution depends mostly on few GeV photons:

  $\Rightarrow$ implies finer sampling in front of calorimeter
  $\Rightarrow$ better Molière radius of thicker sampling probably will give better jet energy resolution

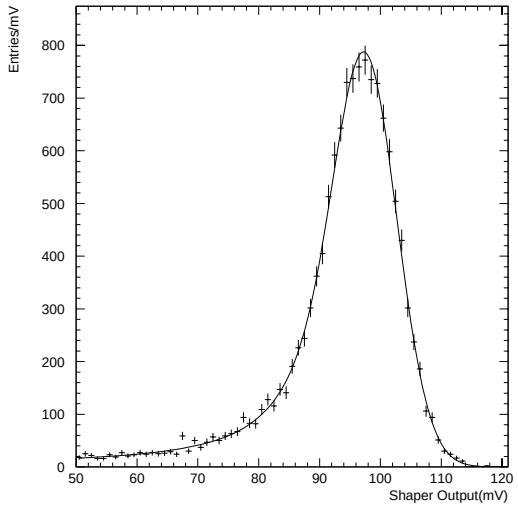
- Is there a physics case for energy resolution below 2% for high energy clusters?

  e.g. $H \rightarrow \gamma\gamma$
  see hep-ph/9610417, hep-ph/9607360
  New work coming J. Yoh (Fermilab)

This process can be measured at the LHC. Requires measurement of $\gamma\gamma \rightarrow h$

Better resolution for high energy electromagnetic showers would require sub 1% calibration. This will be challenging.

• Use 60KeV Gamma's from $Am^{241}$ to determine values of calibration capacitors in each channel of KPiX (we have enough bits to do this) after module assembly but before they are shielded by tungsten.

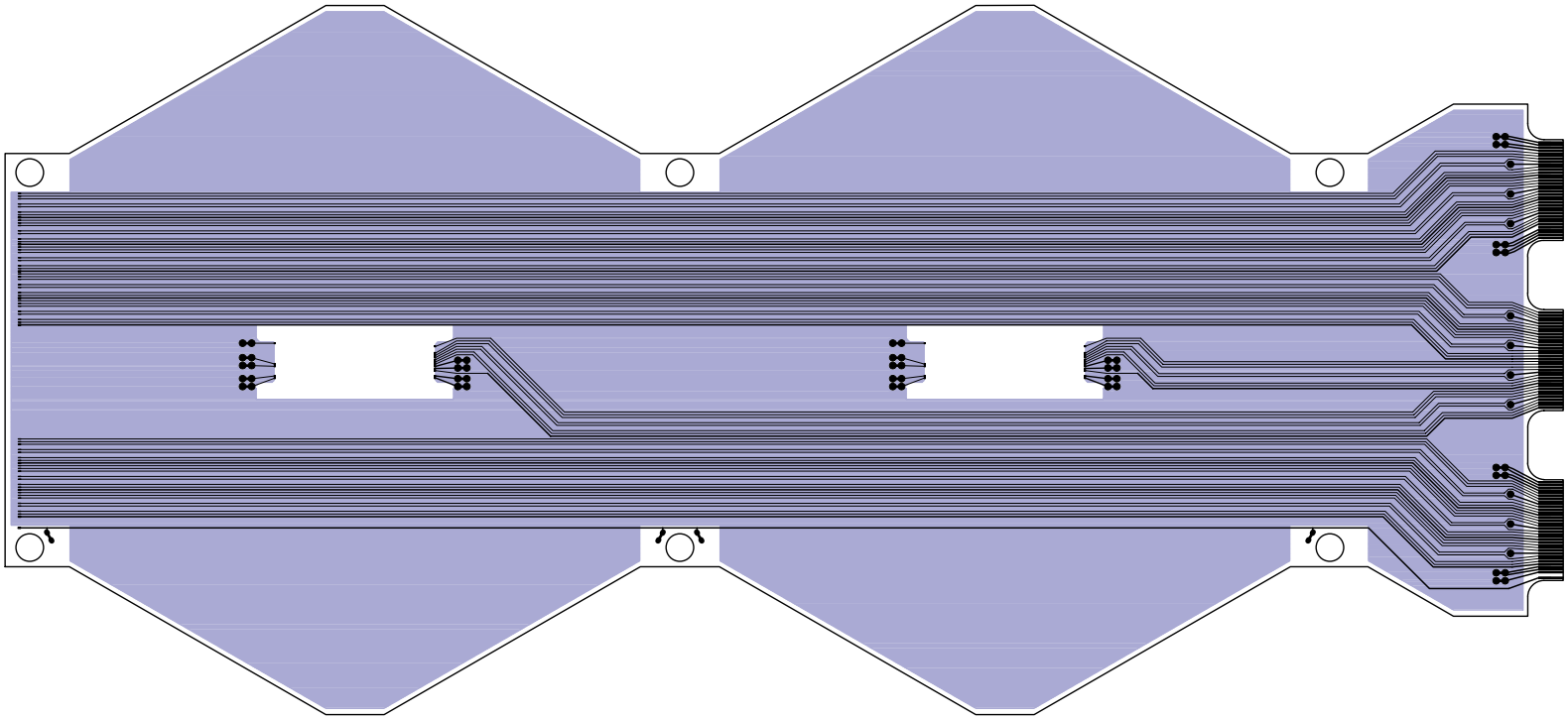



• Control external calibration voltage to better than 1%

• Perform electronics calibration often

• Some offsets in KPiXs calibration depend on transistor properties that may not be stable. Must be studied.

# Cabling (UC Davis):

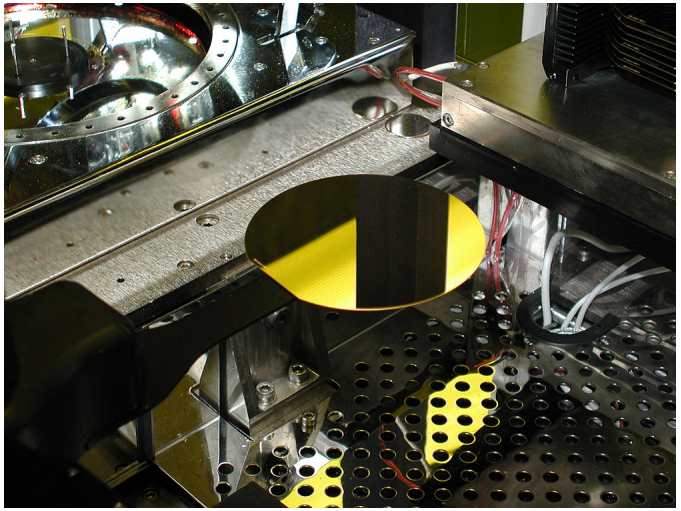


cable_20060915.pcb – Tue Oct 03 10:08:39 2006

Two station prototype cable nearly ready for submission for fabrication.

# Bump bonding (UC Davis)

Most commercial bump bonding is wafer scale:



International Micro Industries

- We need chip scale bump bonding – one die to each detector

Provided by UC Davis group for test beam

$\Rightarrow$ Difficult to clean excess photoresist at edge of devices

- Should we wait to saw detectors until after bump bonding?

Decided not to do this

# What thickness(es) of detectors should we order?

Depletion depth is given by

$$d = \sqrt{2k_{Si}\epsilon_0\mu\rho(V + V_{bi})}$$

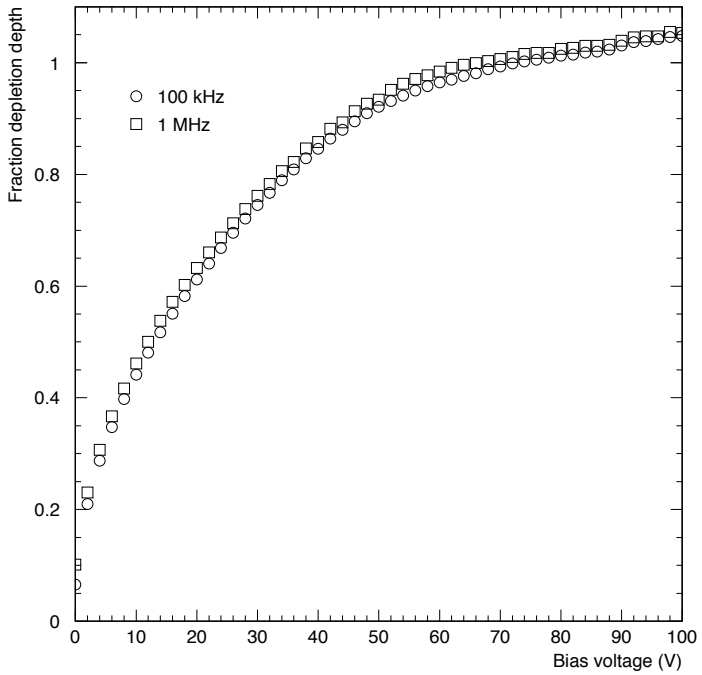
where

$\mu$ is the mobility,

$\rho$ is the resistivity,

$V$ is the bias voltage,

$V_{bi}$ is the built in voltage.

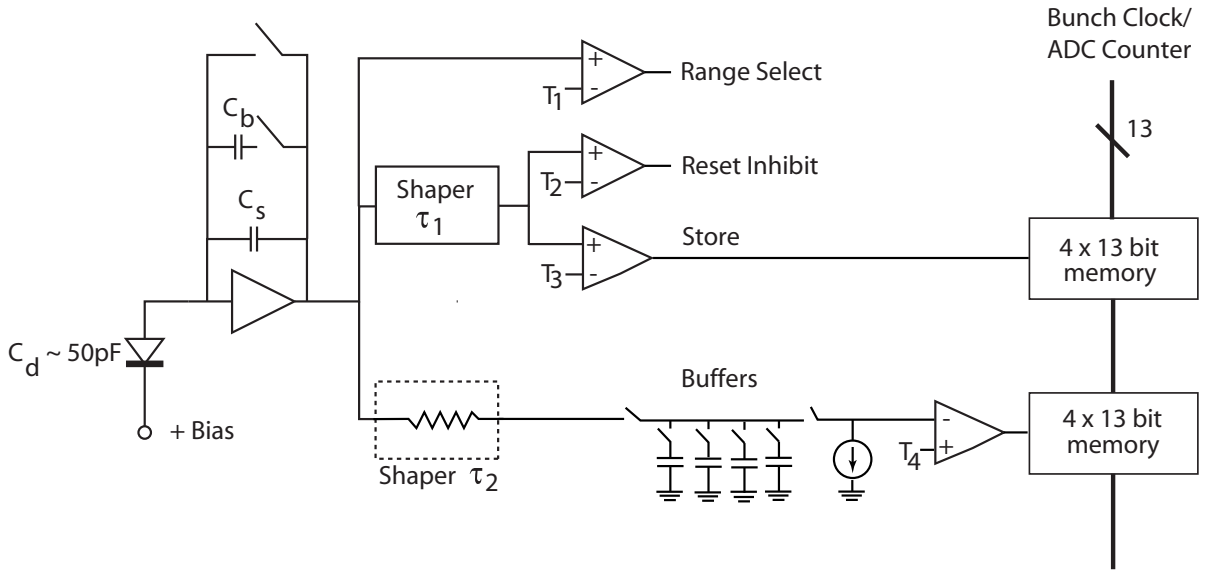



- Increasing the detector thickness to 500$\mu$m could require bias voltages as high as 300 Volts.

- To keep detectors cheap we want to have minimal requirements on $\rho$

# KPiXs News

## Extremely Simplified Schematic

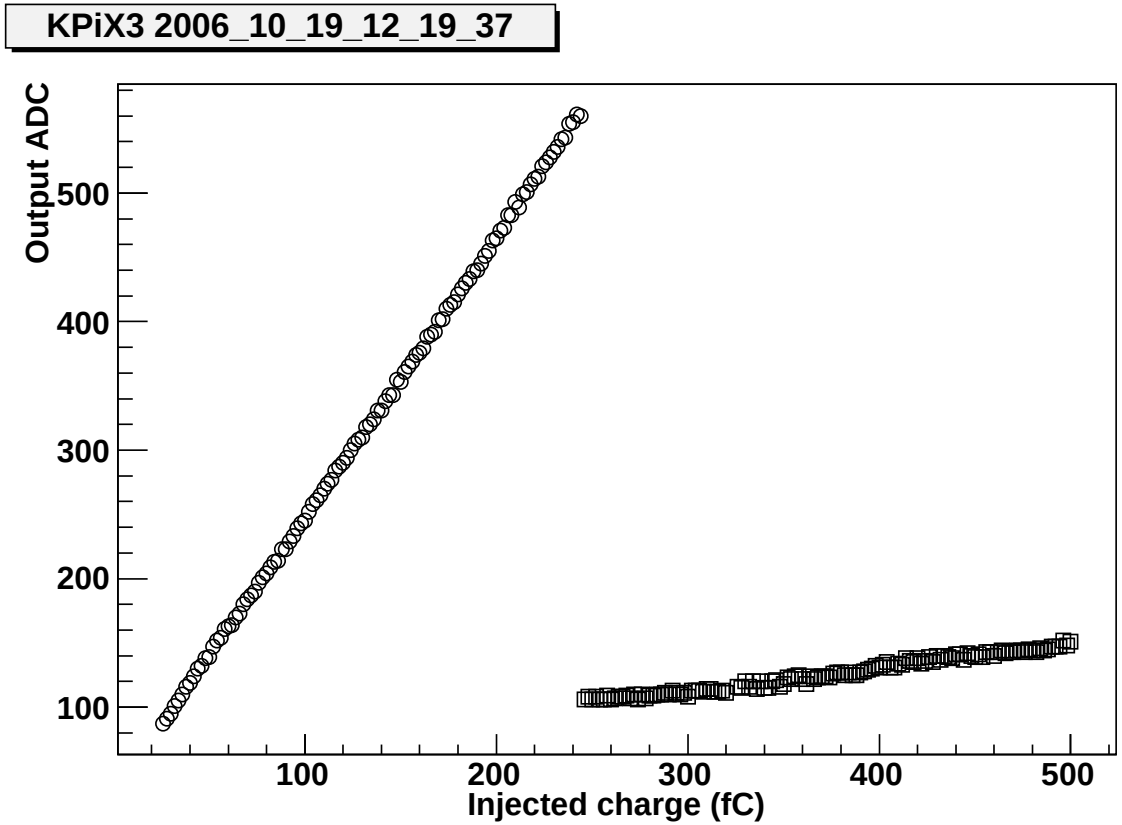



- KPiX can store up to four four pairs of analog charges and time stamps per train
- Low noise performance at output of shaper paramount
- Power pulsing causes no problems
- Digitization occurs between trains
- Novel scheme feedback scheme used to get 16 bit dynamic range ($C_b = 25 \times C_s$)
- Range switching occurs at about 1V

## New Features on KPiX 3

- Improved Analog/Digital isolation
- Polarity switching (not shown)
- External trigger for test beam use

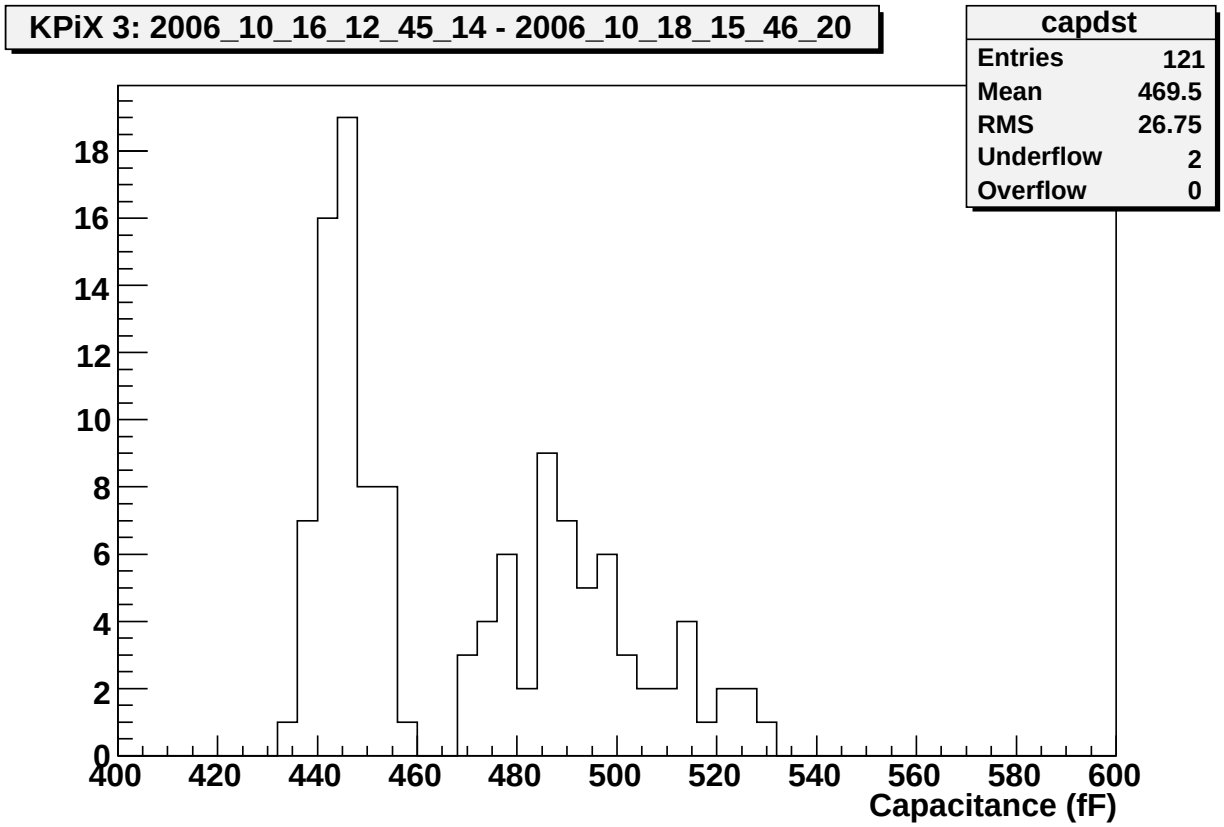
Novel Feature works:

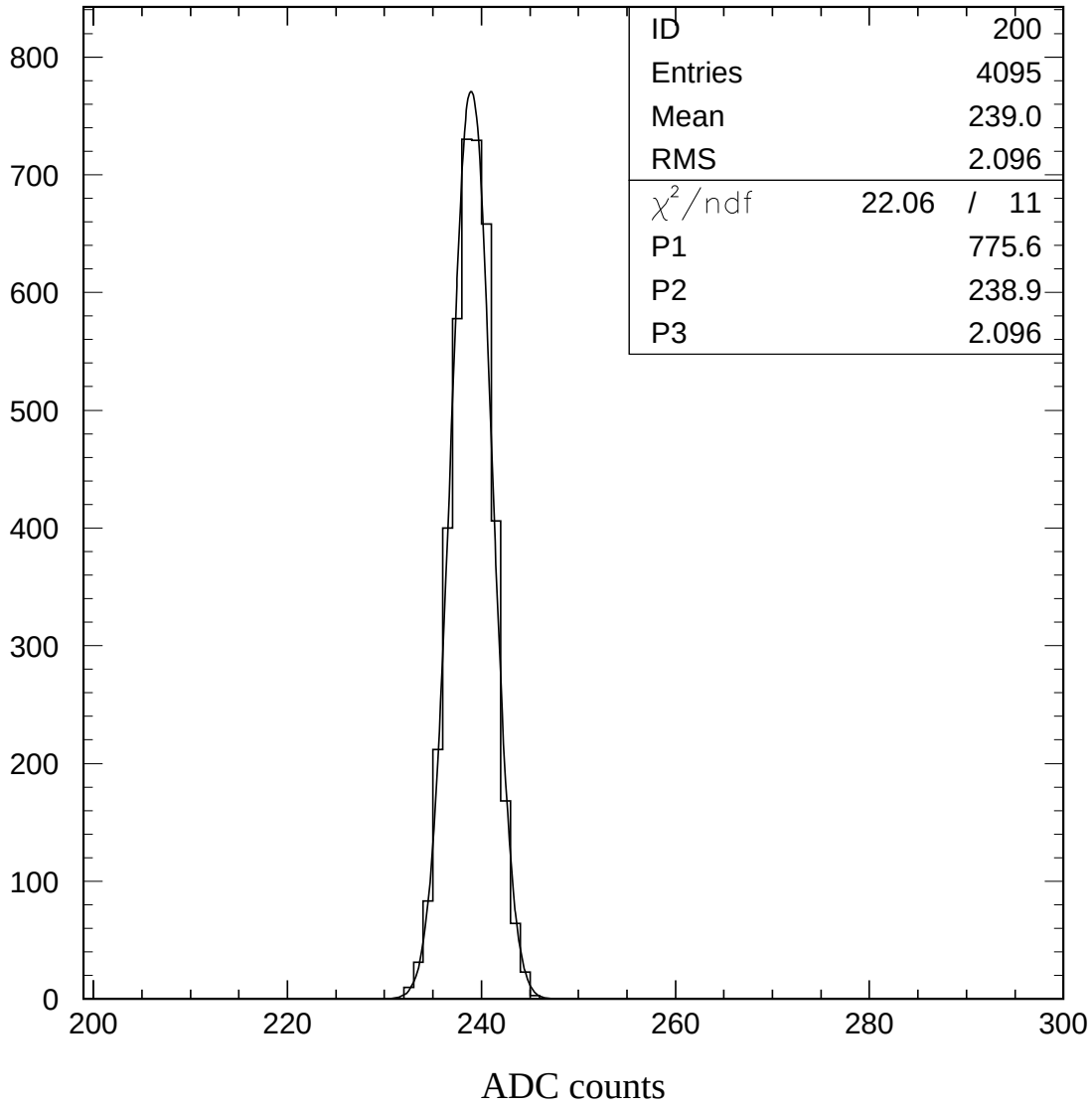



Range switching level adjusted to occur at 200 fC rather than 400 fC for illustration.

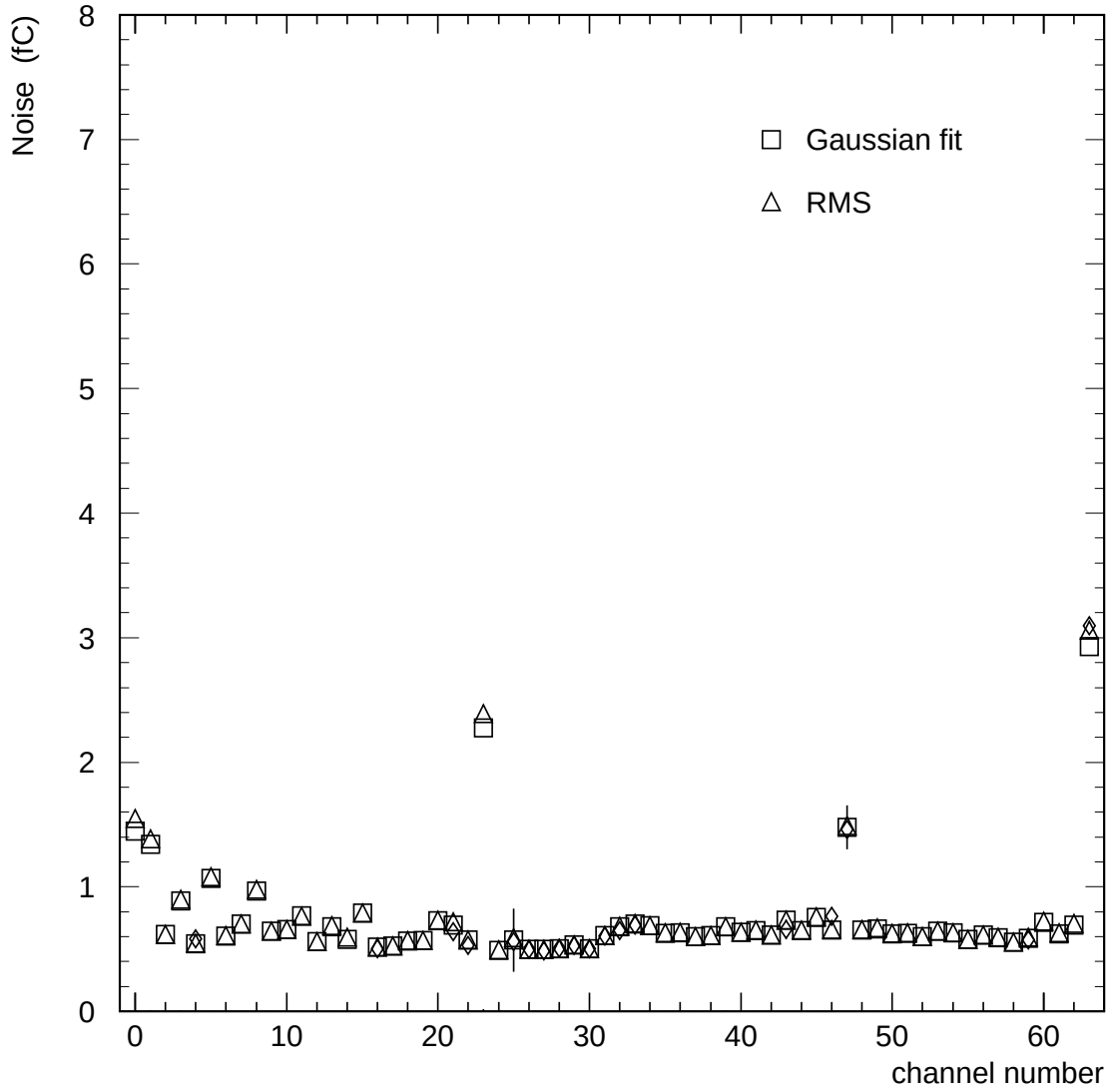
Shows whole chain works properly.

One can adjust the range threshold to measure the charge amp gain, or equivalently the size of its feedback capacitor






Typical noise in the ADC corresponds to less than 1 fC.




Some of the outliers are channels with extra connections.

## Status

• Still optimizing digital timing of control signals on chip (most things are adjustable).

• Initial tests are done with many internal digital and some internal analog signals brought out for testing

• This allows the design of the chip to be verified, but interferes with low noise testing

$\Rightarrow$ Have not yet verified expected low noise performance for small signals

## Fabrication Plans

Submit KPiX4 soon (Nov 15?):

- Improved shaper
- Better current sources for ADCs
- Nearest neighbor logic for tracking
- Improved analog/digital buffering.

$\Rightarrow$ Allows for much lower digital voltage.

Move to KPiX 1024 when operation of KPiX4 is demonstrated. May require KPiX5.

## Testing plans – including testbeam

- Test KPiX-n with 6 cm $\times$ 6 cm detectors with 1 cm $\times$ 1 cm pixels – could be tested in beam
- Bump bond a KPiX-n chip to an existing 757 pixel prototype detector, use prototype cable – test in beam
- Test single KPiX1024 and prototype II detectors – test in beam
- Build 30 $\times$ 1 wafer prototype – test in beam

## Summary

- New sensor design ready for fabrication
- Prototype cable ready for fabrication
- Much of KPiX functionality is demonstrated
- Testing schedule will depend on KPiX