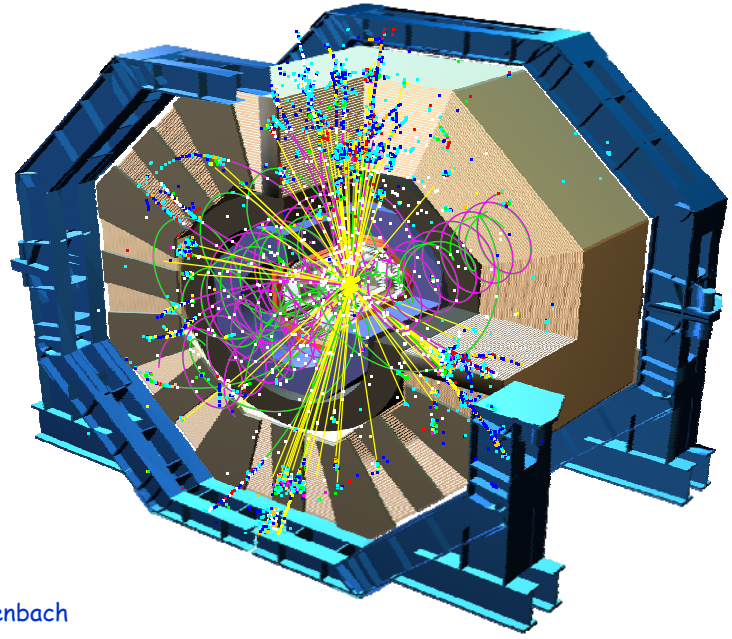
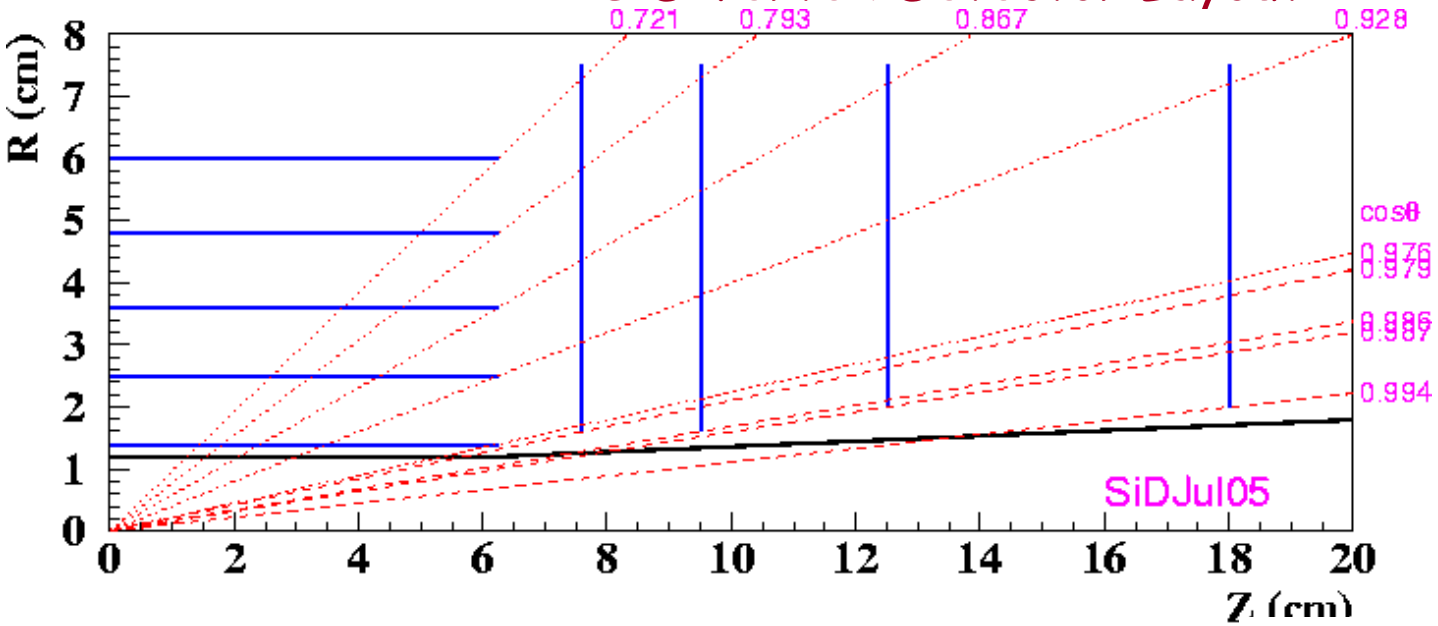
The ILC should be a high luminosity machine…

- Each bunch train has substantial luminosity and background-
- Simple CCD solution – integrating through train and reading out in the intertrain period does not work – too much confusion to untangle.
  - Japanese FPCCD might be exception.
- There is no obvious "perfect" candidate for a sensor…
- There are > 10 sensor development projects going worldwide
  - DEPFET's, MAPs, CPCCD's, ISIS, etc.
  - No time to attempt a critical review, so I'll mention two that are of some interest to SiD.

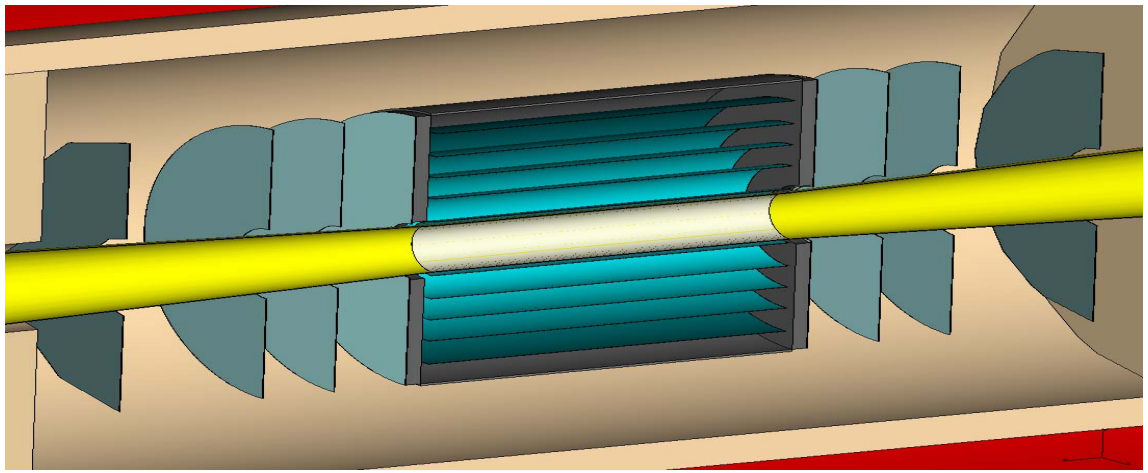


SiD Vertex Detector Layout

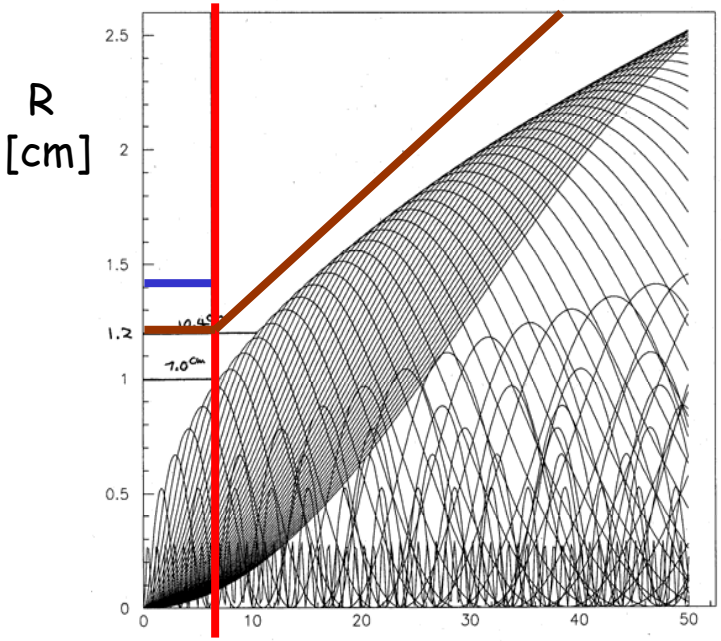


5 barrel layers
4 end disks

5 Tesla

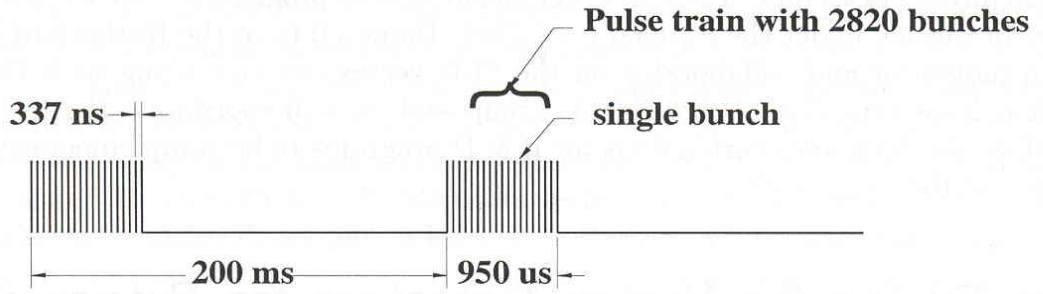


M. Breidenbach

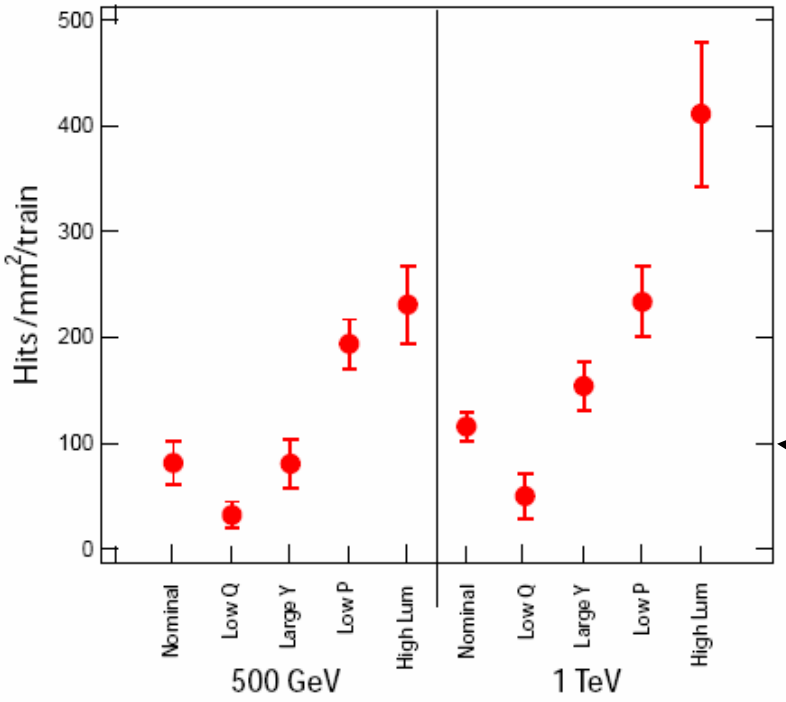


Z= 6.25cm

Time Structure for the ILC



Backgrounds



~0.035/mm²/bunch

The ideal detector for the ILC has

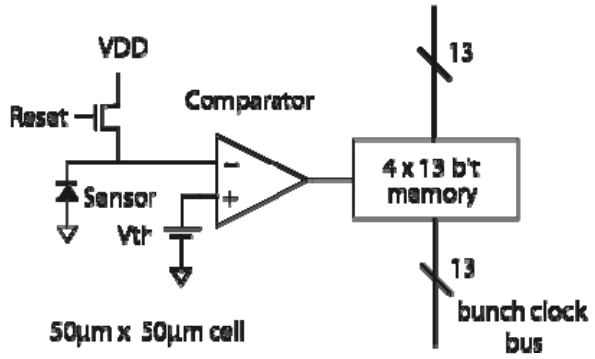
- Spatial resolution ≤ 5 microns
- Small pixels consistent with high hit density
  - 50-100 hits/mm2 per train – but see next point
- Temporal resolution of one bunch
- Thickness consistent with ≤ 0.1% X_0 per layer
- Average power ≤ 40 watts
- Peak current small enough so Lorentz forces do not perturb position of sensor.
- No problem with the "EMP" from the beam charge
- Adequate radiation hardness
- Technology consistent with full scale sensors by 2010

But these requirements may be not only difficult but inconsistent!

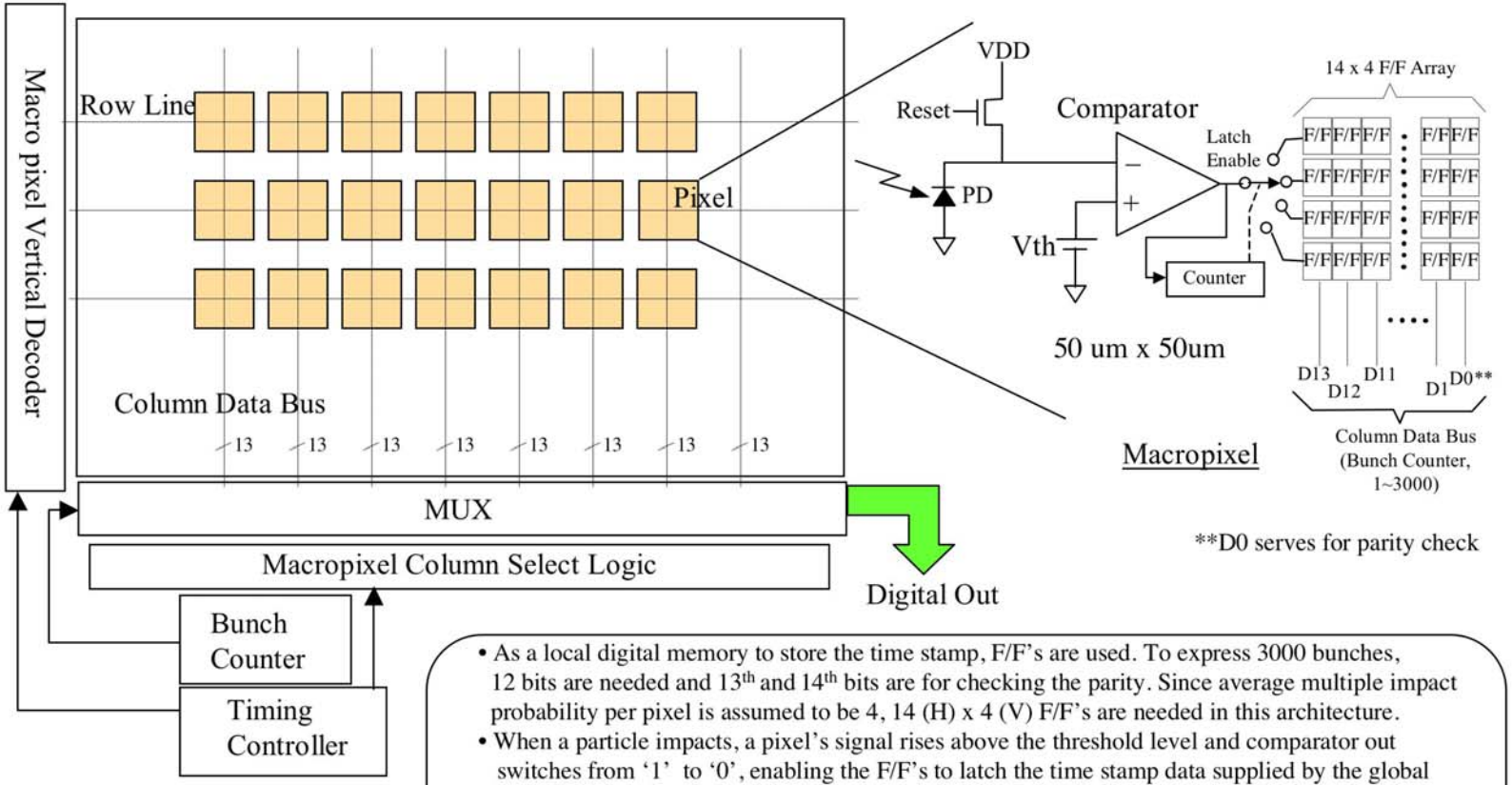
MacroPixels
Yale, Oregon, Sarnoff

- Monolithic CMOS sensor.
- Time tag hits in each pixel with registers strobed by discriminator.
- Simple architecture, but a lot of transistors per pixel…

Pixel Architecture



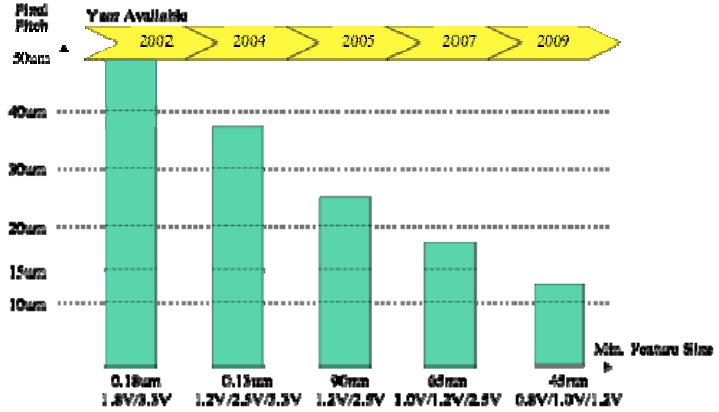
Macropixel Array Architecture



- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Current Design

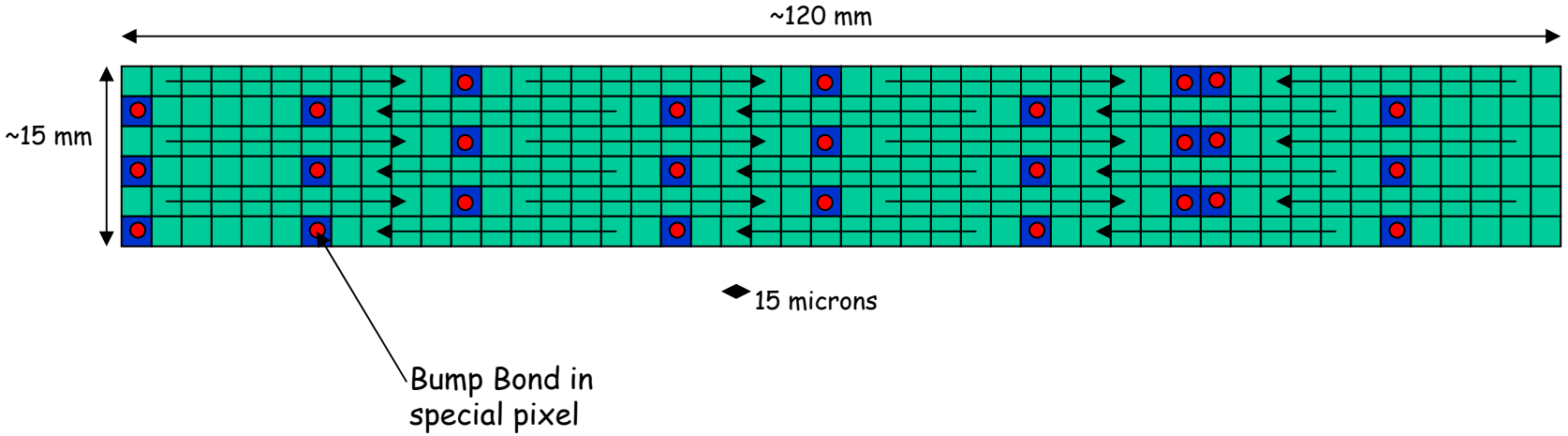
- Monolithic CMOS Process
- Single Layer of 10 micron x 10 micron Pixels
- Detect Hits above adjustable Threshold
- Store time of Hit, up to 4 hits/pixel
- Record data over Bunch Train, Readout during 200 msec between trains
- Digital Readout



- But may require 45 nm process. Will this be economically viable for large sensors? 2009?
- Current estimate is ~40 Amperes/sensor during the train!!! May come down, but a significant concern. (Average power may be ok)
- Now in prototype design stage with 50 micron^2 pixels and 0.18 micron process.

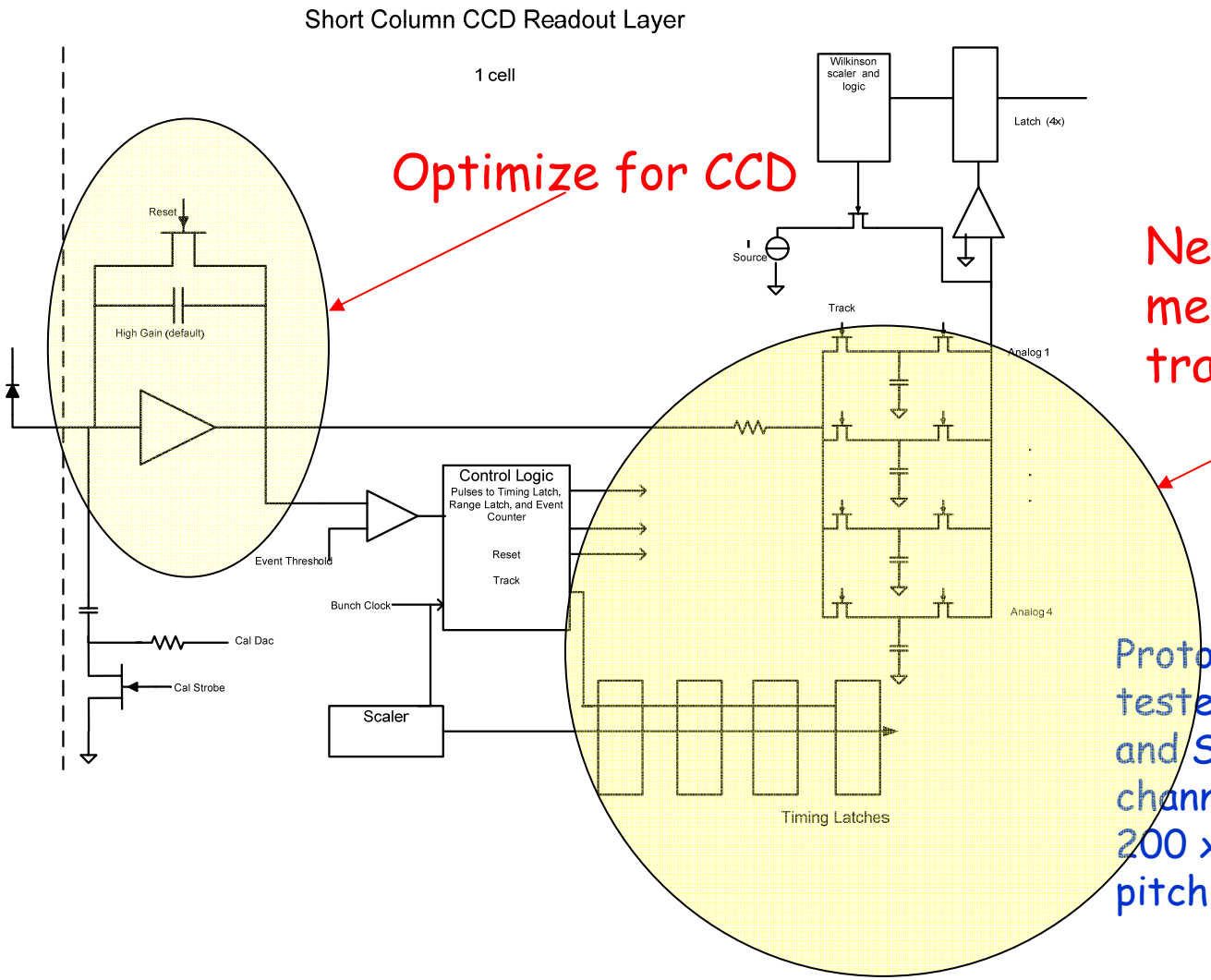
Another (probably crazy) idea: Short Column CCD's

- Make CCD's with short columns ~512 pixels and no rows.
- Design CCD so charge sharing likely across columns.
- Design CCD so adjacent columns move in opposite directions.
- Bump bond to a readout layer of KPiX like CMOS.
- 15 micron pixels, 3 clocks/bunch (~10 MHz) , and ~500 pixels in a row have satisfactory background rejection.



There is probably nothing fundamental about the columns being parallel to the long dimension.

KPiX Cell

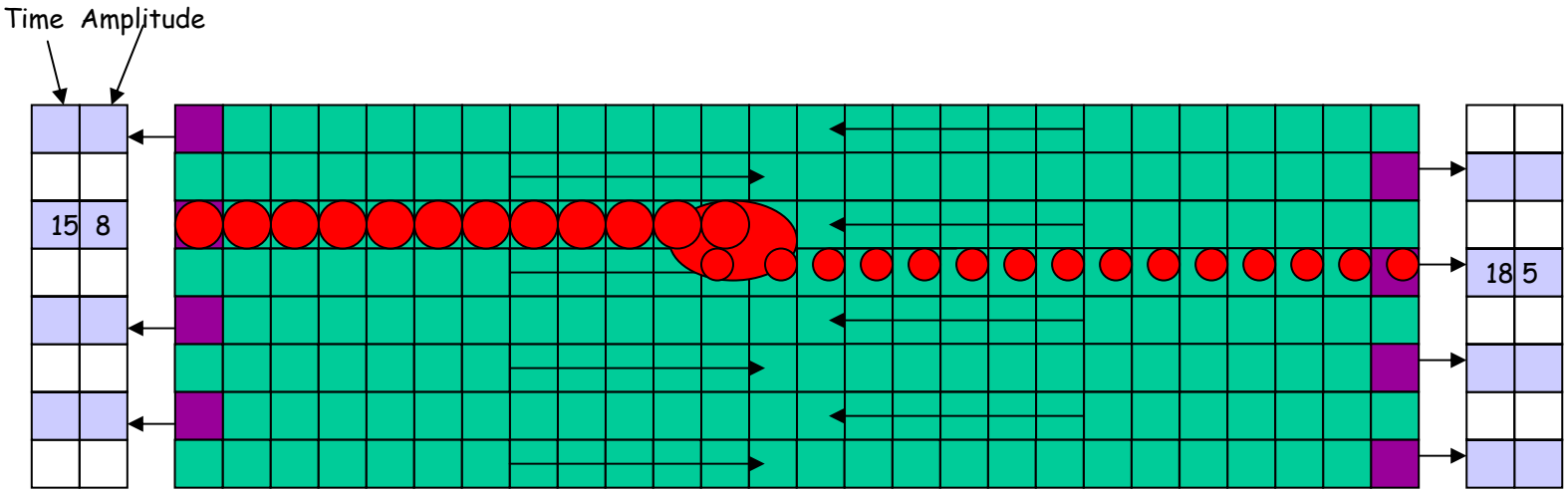


Need ~20 measurements/ train. (Now 4)

Prototype now being tested for SiD EMCal and Si Tracker. 1024 channels per chip on 200 x 500 micron pitch.

SCCCD Animation

Bunch



CCD Clock

SCCCD Features

- Utilizes CCD correlation of position with bunch twice to "solve" for position and bunch time.
- Reduce number of readout cells by CCD column length - ~500. Power using KPiX numbers seem close.
- Clock CCD at ~10 MHz, cf 50 MHz for CPCCD.
- Use very standard CCD technology for the sensor part. Both 2 and 3 phase clocks appear possible.
- Use standard 0.25 micron CMOS for readout.
- Use LHC style bump bonding for connections.
- Occupancy of a short column/column read time ~0.5 (inner layer)
- Once the bunch is identified, then ~no ambiguity for position. (CPCCD is the same).

Status: Still talking about whether this should be developed…