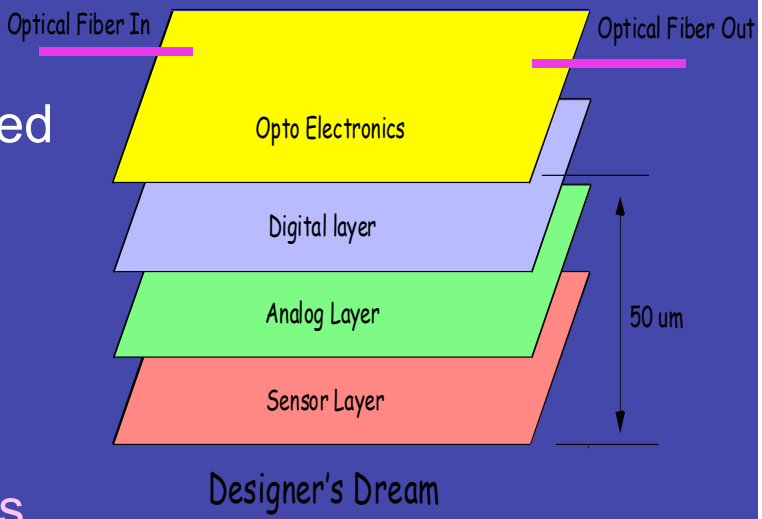
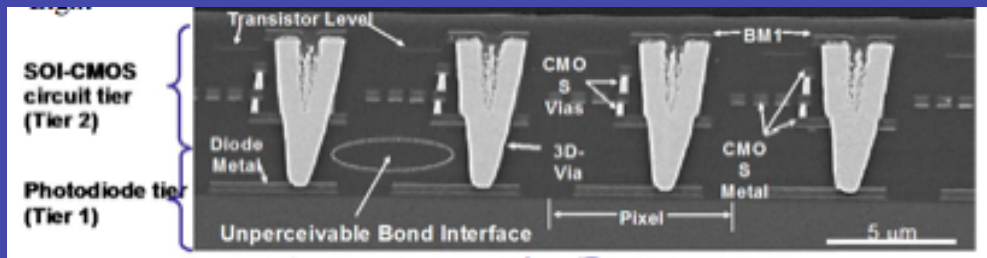
Vertically Integrated (3D) Detectors

A 3D chip is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a “monolithic” circuit.

- The layers (also called tiers) can be comprised of devices made in different technologies.
- The move to 3D is being driven by industry.
  - Going 3D reduces trace length, Reduces R, L, C
  - Improves speed
  - Reduces interconnect power, crosstalk
  - Reduces chip size
  - Processing for each layer can be optimized
- Fully depleted sensors can be naturally included as the base layer of the 3D stack



Designer's Dream



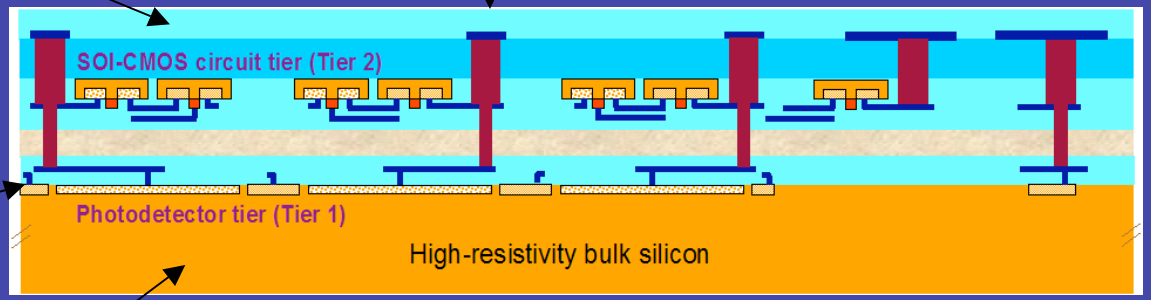
Drawing and SEM Cross section

8 μ pitch, edgeless, 50 μ thick fully depleted two tier imager from MIT-LL

3D Concept for HEP

CMOS SOI circuitry

Interlayer vias



Wafer bond
oxide, intermetallic
or epoxy

high resistivity silicon wafer,
Thinned to 50-100 microns

(MIT-LL)

Active edge
processing

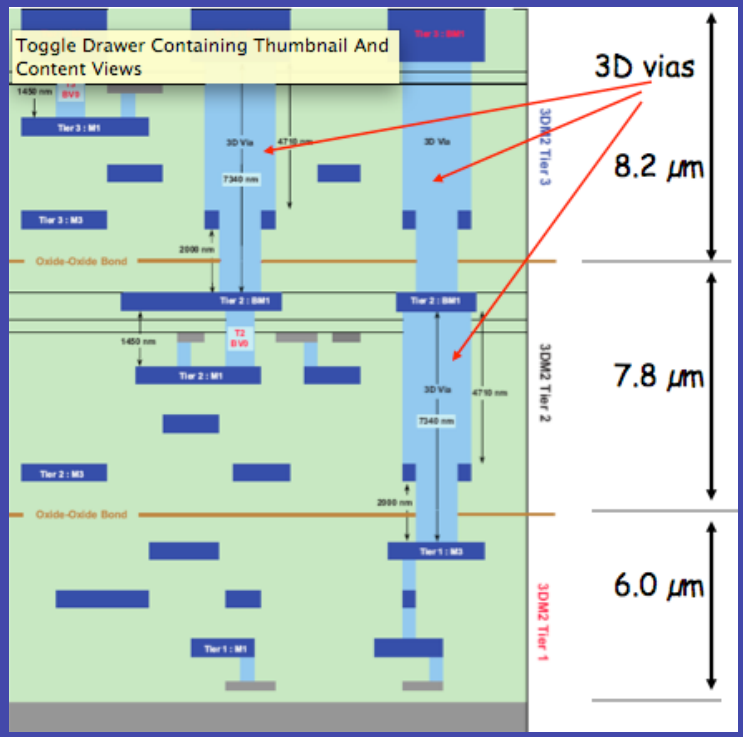
Backside implanted after thinning,
before frontside wafer processing
Or laser annealed after processing

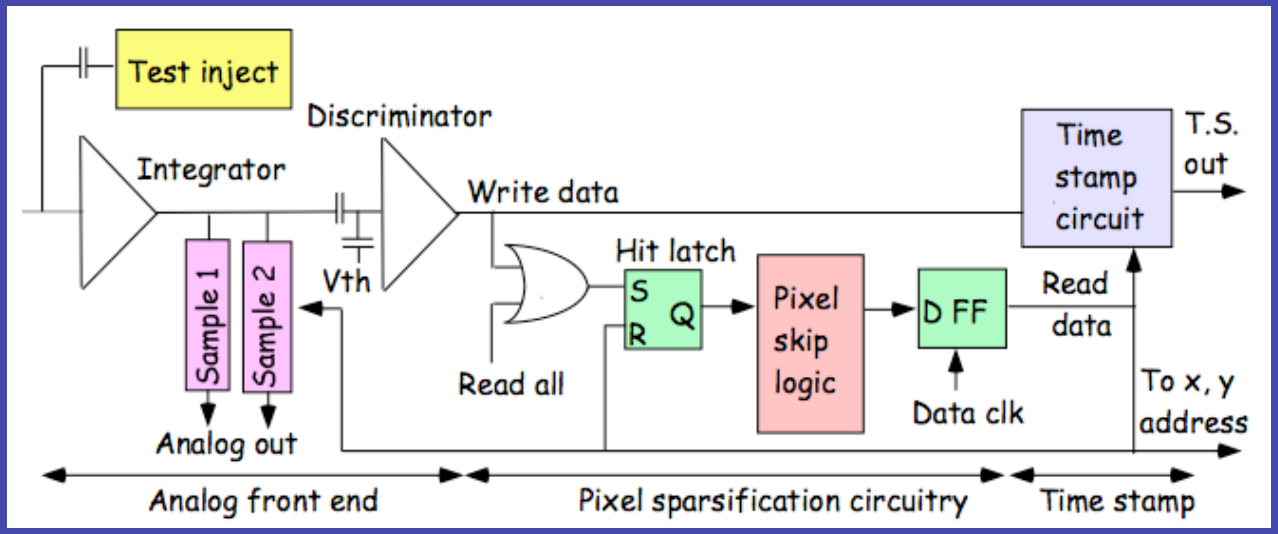
Advantages of 3D for ILC

- High resistivity substrate available for fully depleted diodes - large signal
- No limitation on PMOS usage as in CMOS MAPs
- Sense nodes can have *very* low capacitance
- Increased circuit density without going to smaller feature sizes
- Ability to process a field of pixels in upper tiers (reduce transistor count, cluster …)
- Technologies can be mixed. 3D may be used to add layers above MAPS, CCDS, DEPFETs or other devices under development.
- SOI Radiation hard to >1 Mrad, low SEU sensitivity
- SOI is a low power technology
- Can be made “edgeless”
- Thinning to 50 microns demonstrated
- Minimum charge spreading with fully depleted substrate
- 100% diode fill factor
- “Stitching” traces possible on top tier metal (full wafer mask)

3D ILC Chip

- Fermilab has contributed an ILC readout chip design to a MIT-LL 0.18 micron three tier SOI 3D multiproject run
- ~2.5 mm x 2.5 mm chip, 64x64 20 micron pixels
- Does not include sensor integration
  - Bond readout circuit to an independent sensor wafer (precursor to full 3D integration run)
- Design includes amp/disc, time stamp, pixel control, token passing -





–Store analog and digital time stamps in the hit pixel cell.

–Store double correlated sample in pixel

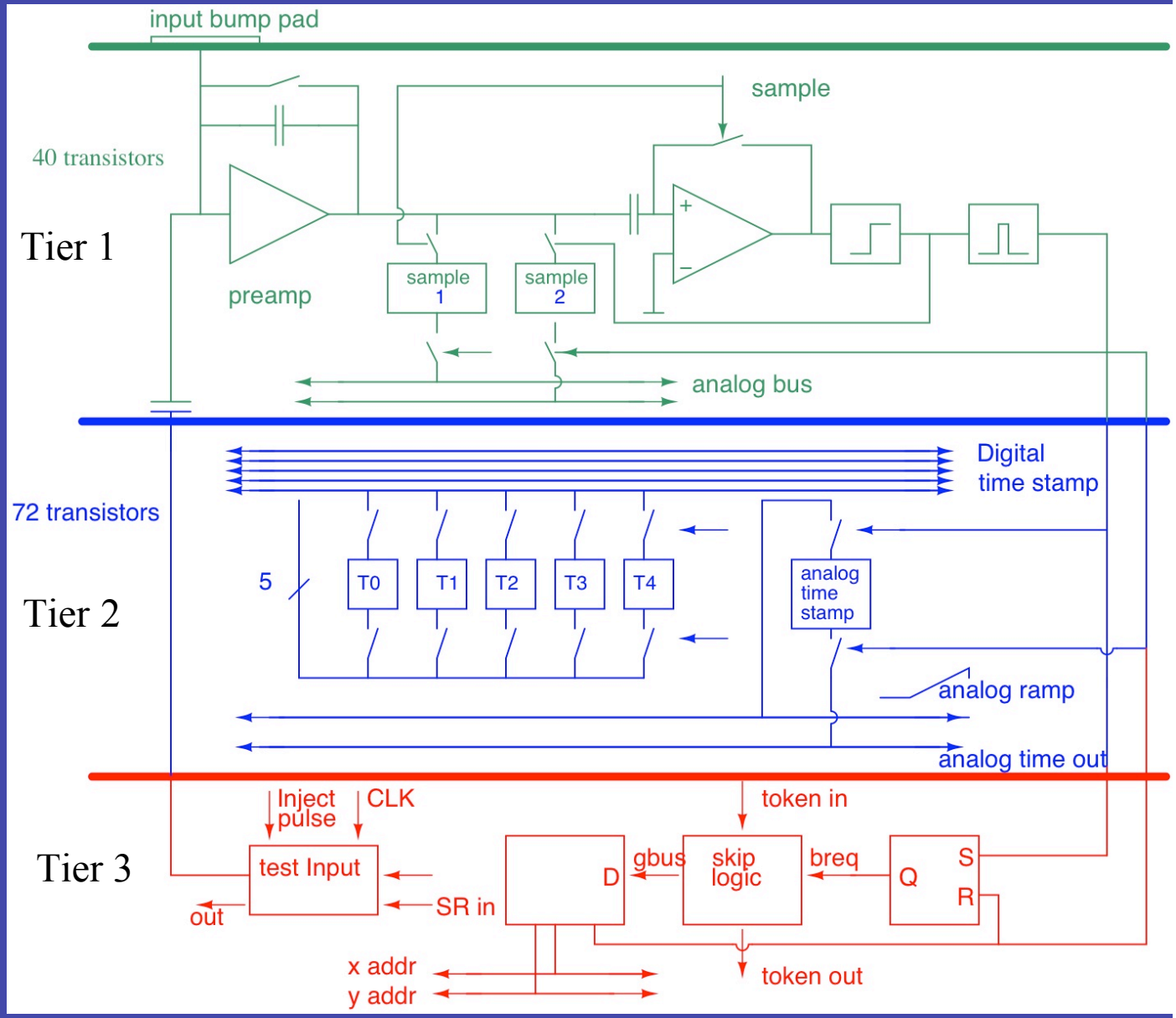
3D ILC Chip

Correlated double sample
Noise ~ 35 e- (??)
Adjustable disc. threshold
Few hundred nA/pixel
Most bias currents (times) adjustable.
750na/pixel front end current

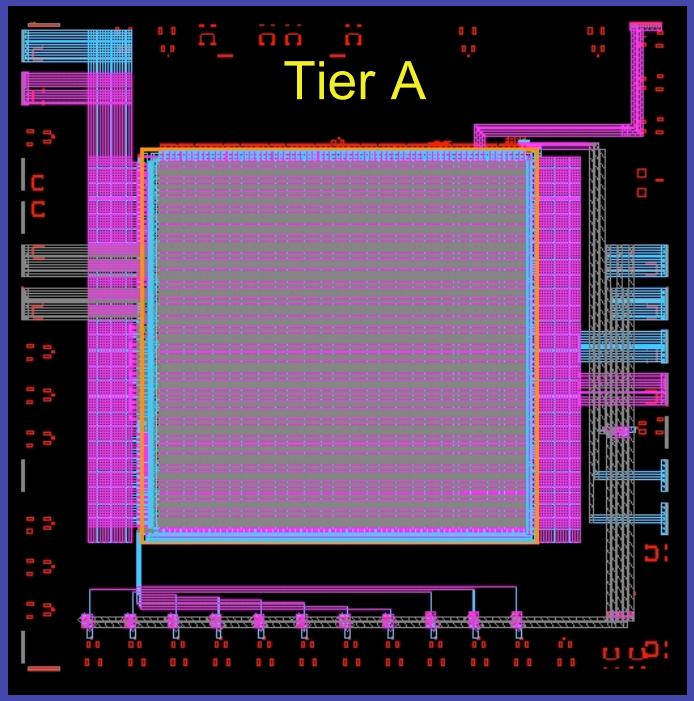
Analog and 5 bit digital time stamps
Analog resolution (?)

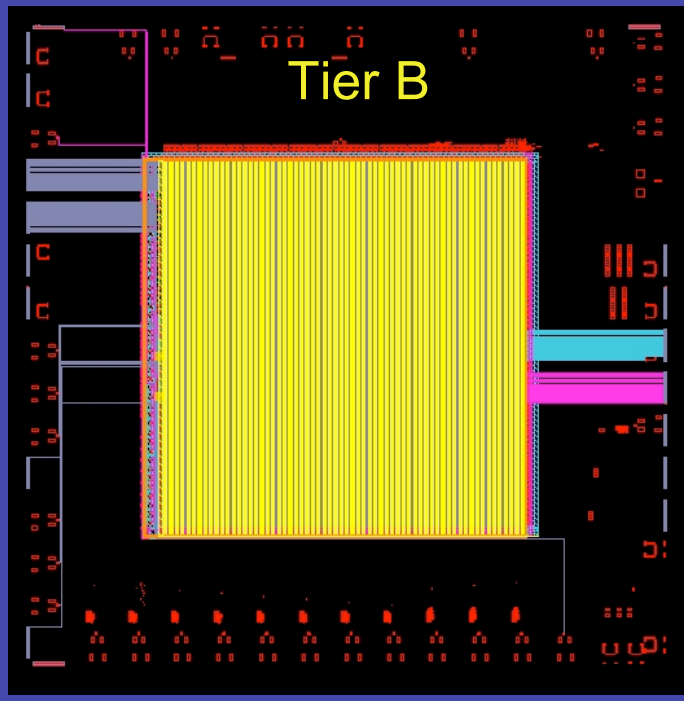
Sparse readout
Individual kill/inject

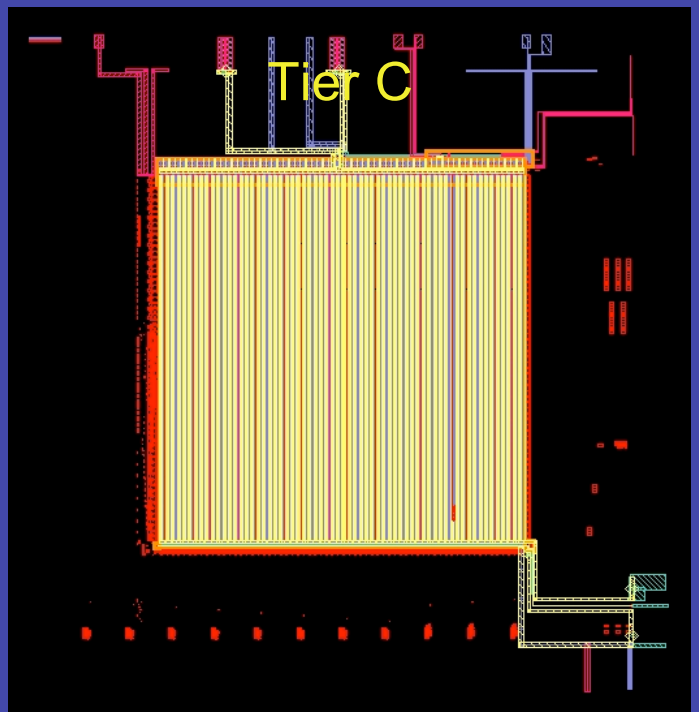
3 vias / pixel

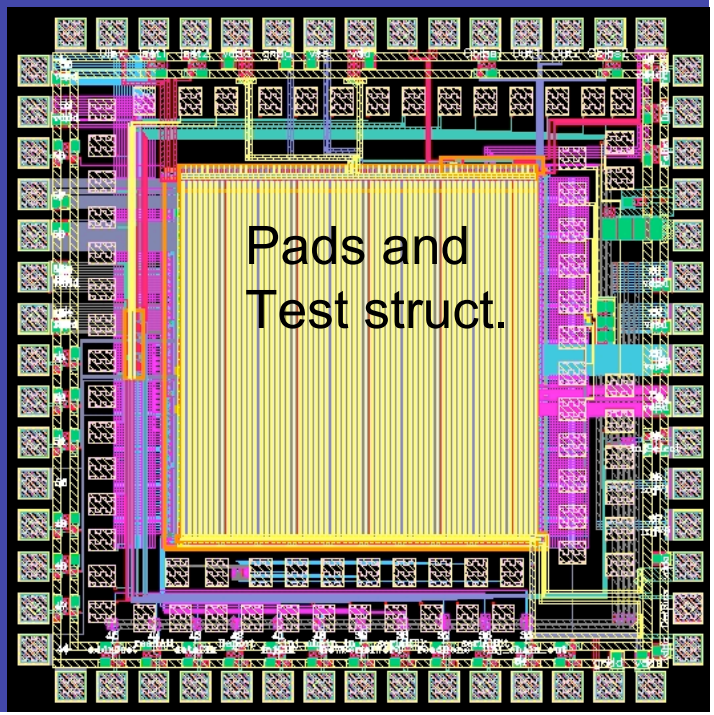


Completed Design







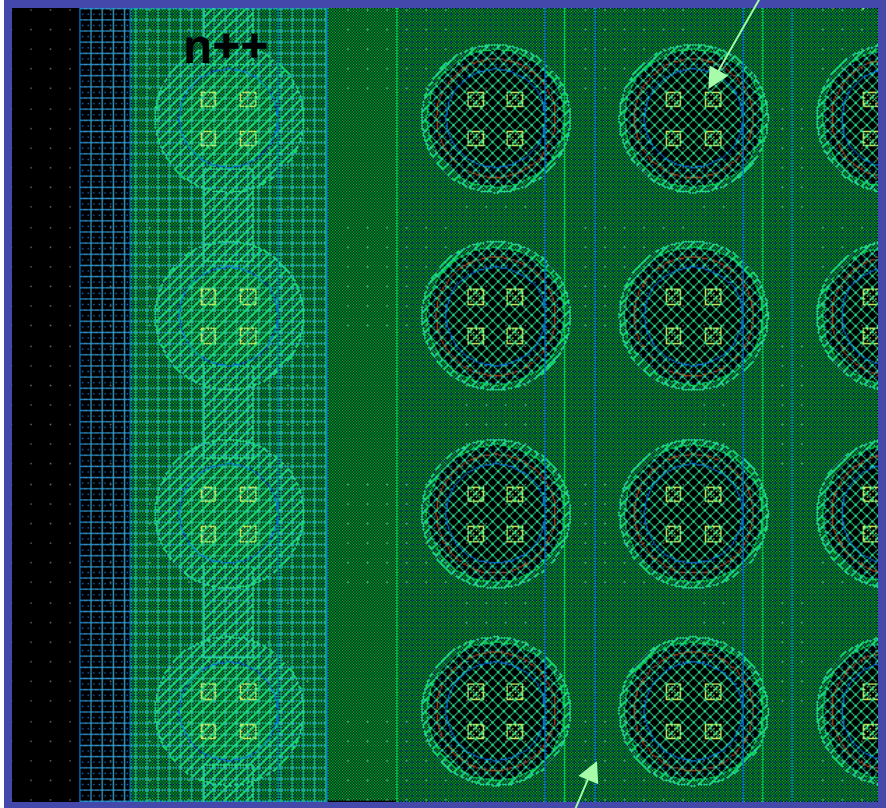


Mating Sensor Layout

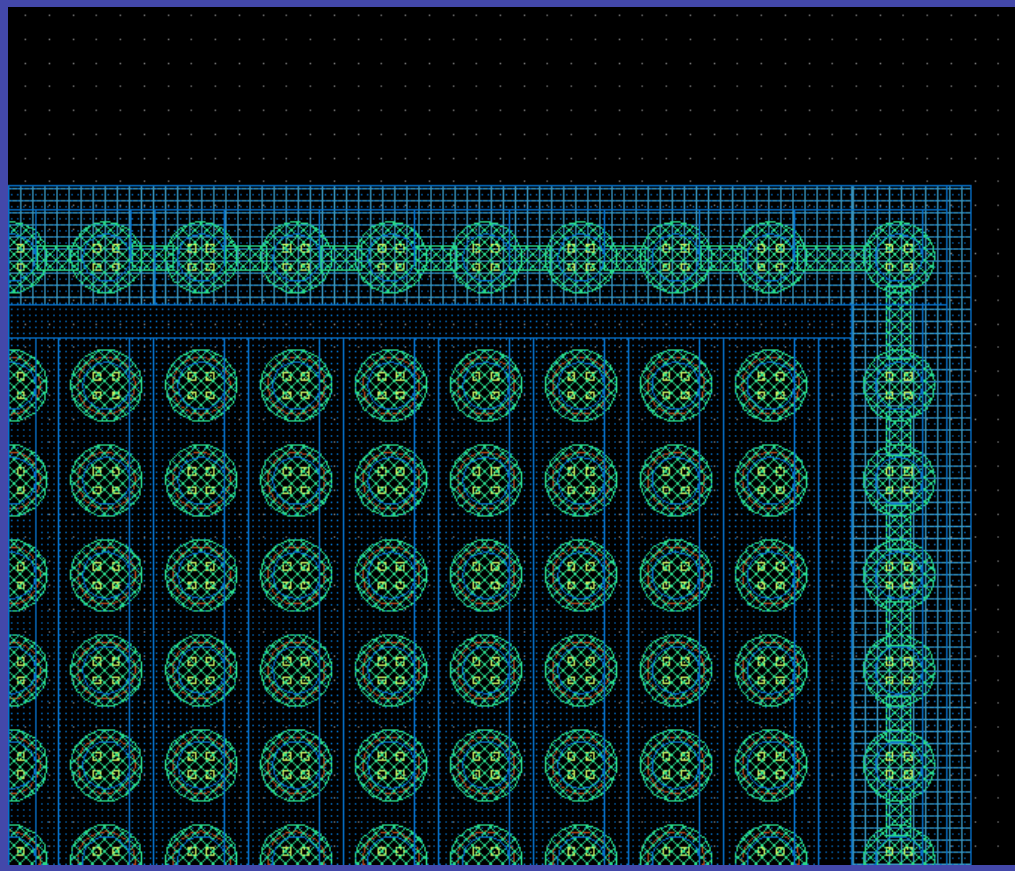
Completing design of a mating sensor to be fabricated at MIT-LL
50-100 microns thick
“edgeless” - no dead region

Design with n+ implant

Bump pads

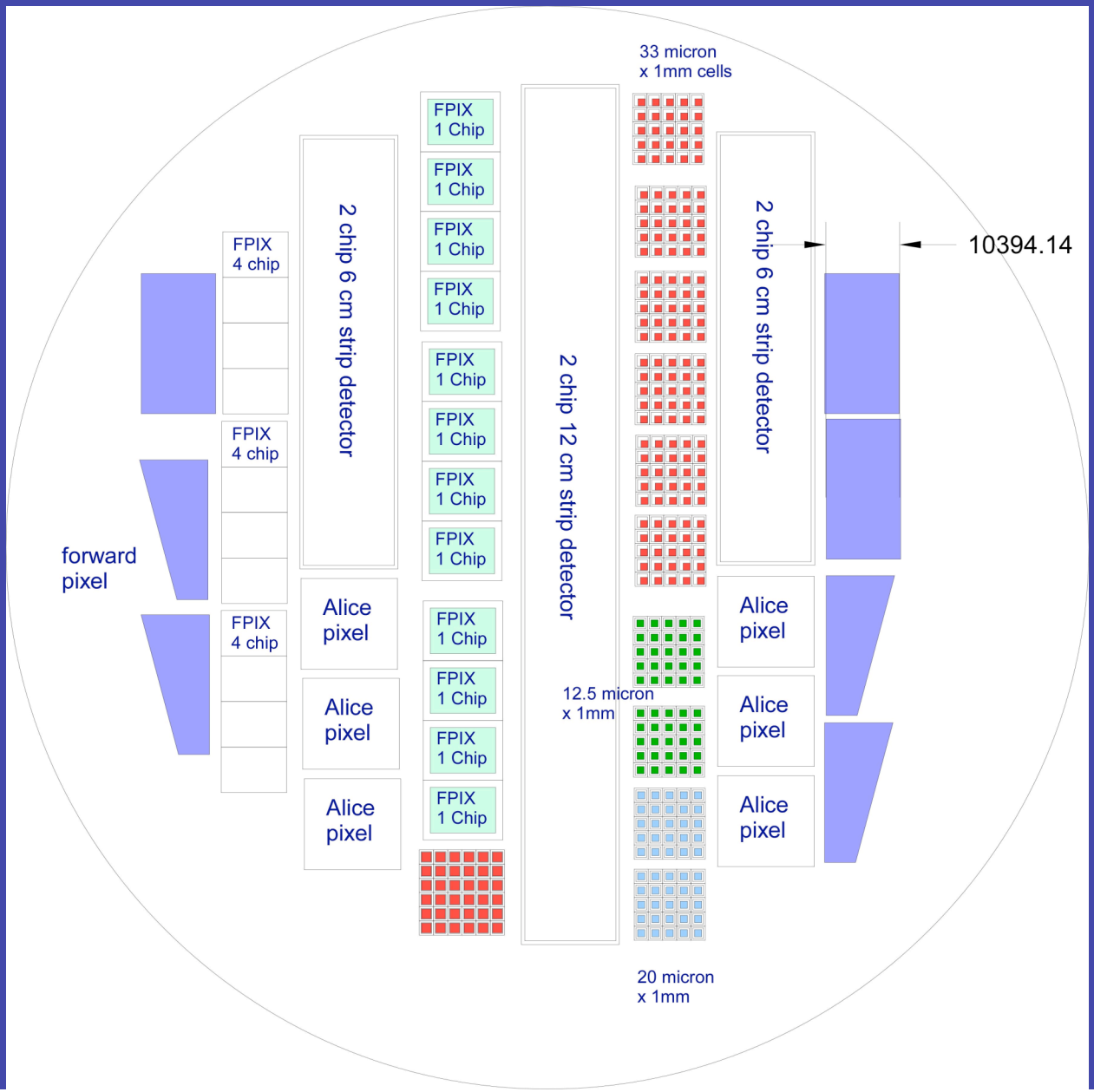


Design without n+ implant



 64x64 20 micron pitch pixels

Wafer Cartoon



Other Studies

- Sensor and chip thinning
  - FPIX thinned to 15 microns
  - Wafer thinned to 20 microns
- Bergamo group submitting a design variant with 25 μ pitch MAPS pixel in 90 nm technology.
- SOI (SBIR with American Semiconductor, OKI submission)
  - Laser annealing studies
  - Circuit design
  - Test submission
- Bump bonding of test chip and wafer