

Monolithic Pixel Detector in a 0.15 μm FD-SOI Technology

H.Aihara

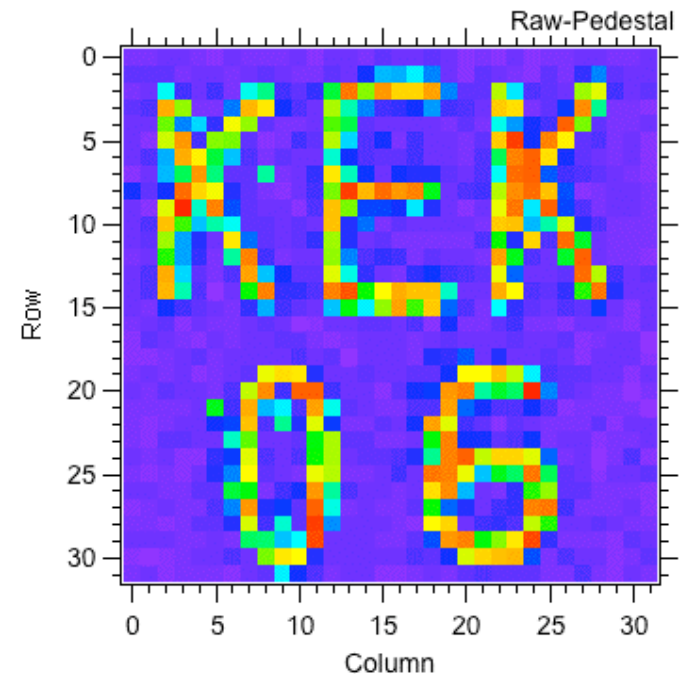
for

KEK Detector Technology Project : [SOIPIX Group]

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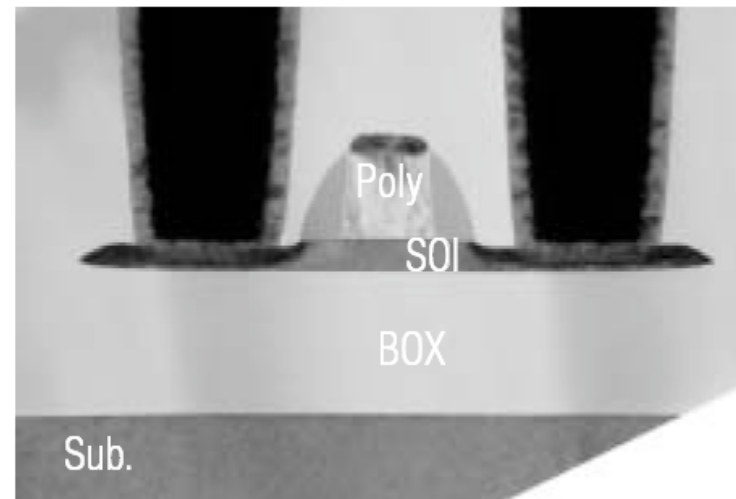
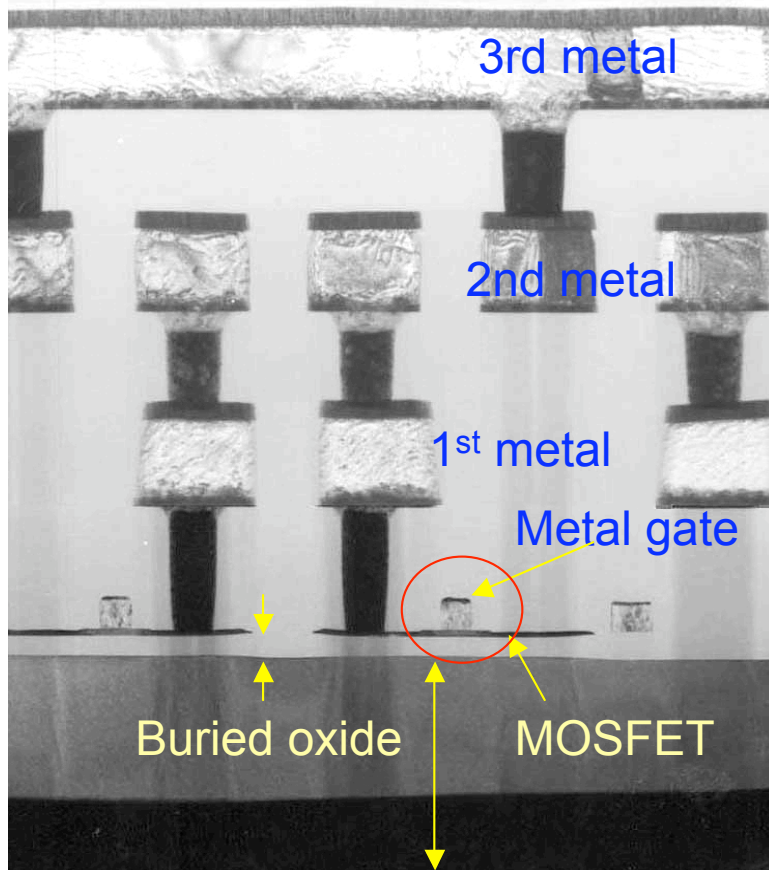
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36x36 20 μm



OKI Sol process

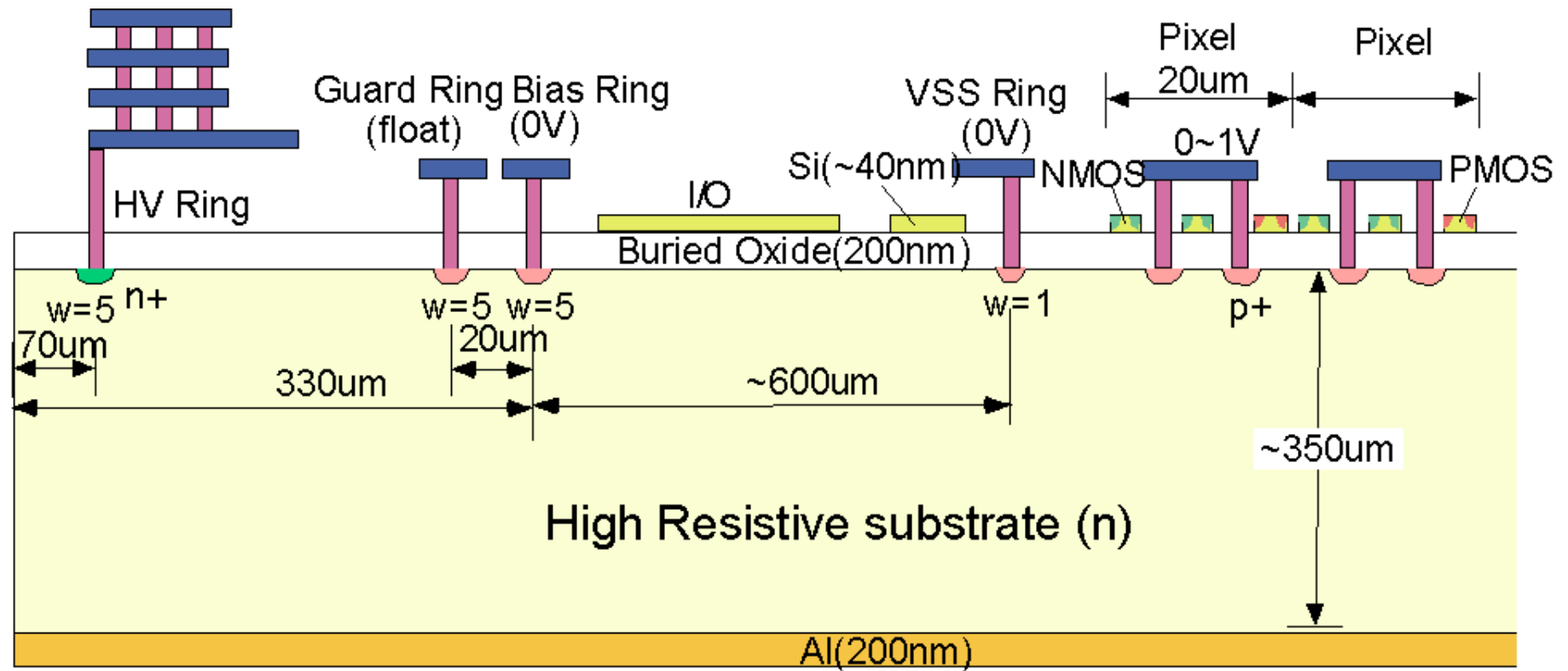
Process	0.15 μm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers, MIM capacitor
SOI wafer (SOITEC)	Wafer Diameter: 150 mm ϕ , Top Si : Cz, $\sim 18 \Omega\text{-cm}$, p-type, $\sim 40 \text{ nm}$ thick Buried Oxide: 200 nm thick Handle wafer: Cz $> 1\text{k} \Omega\text{-cm}$, 650 μm thick
Backside	Thinned to 350 μm , plated with Al (200 nm).



<http://www.okisemi.com/english/soi.htm>

Photo of 200nm Sol

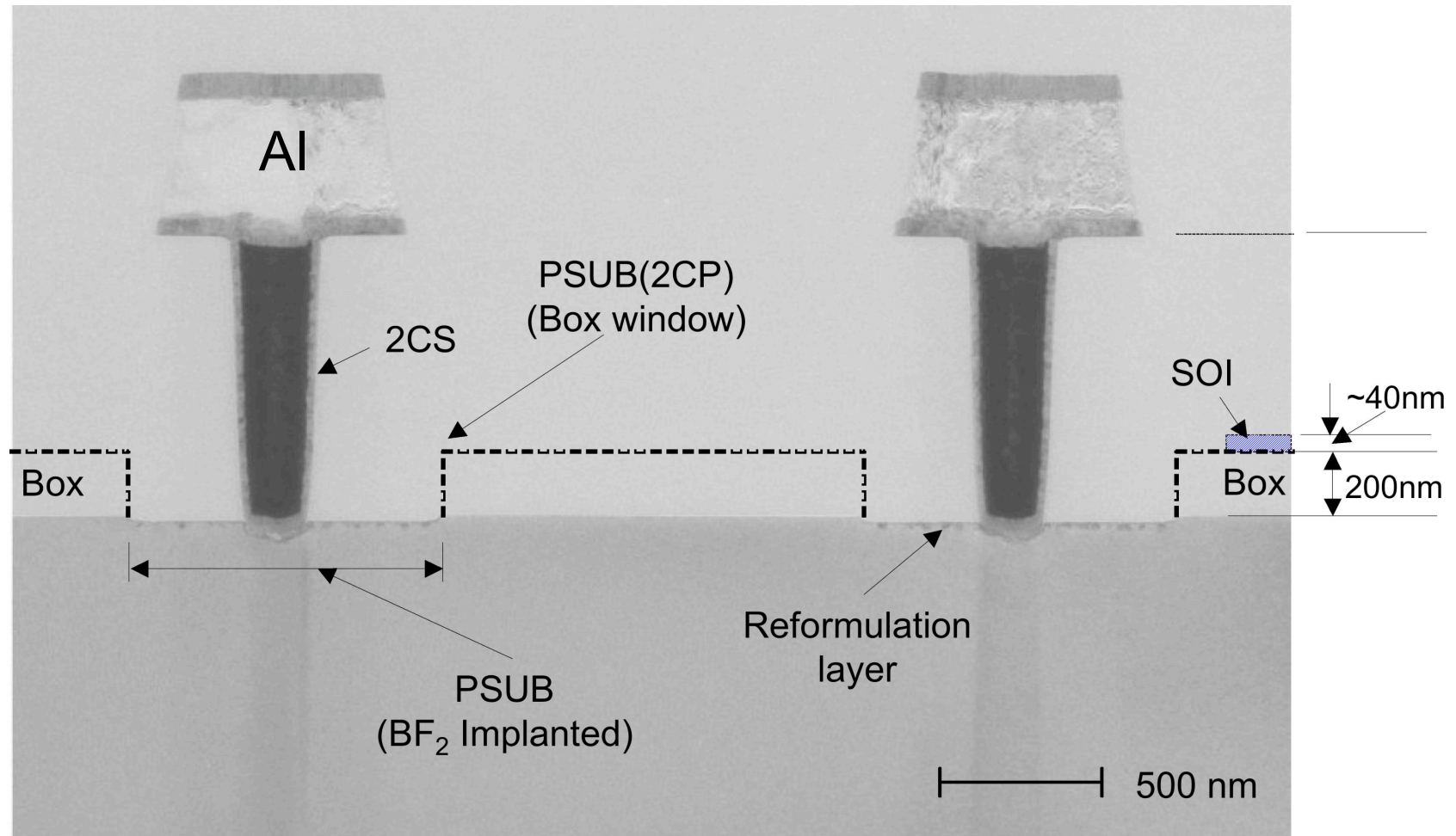
SOI Pixel Process



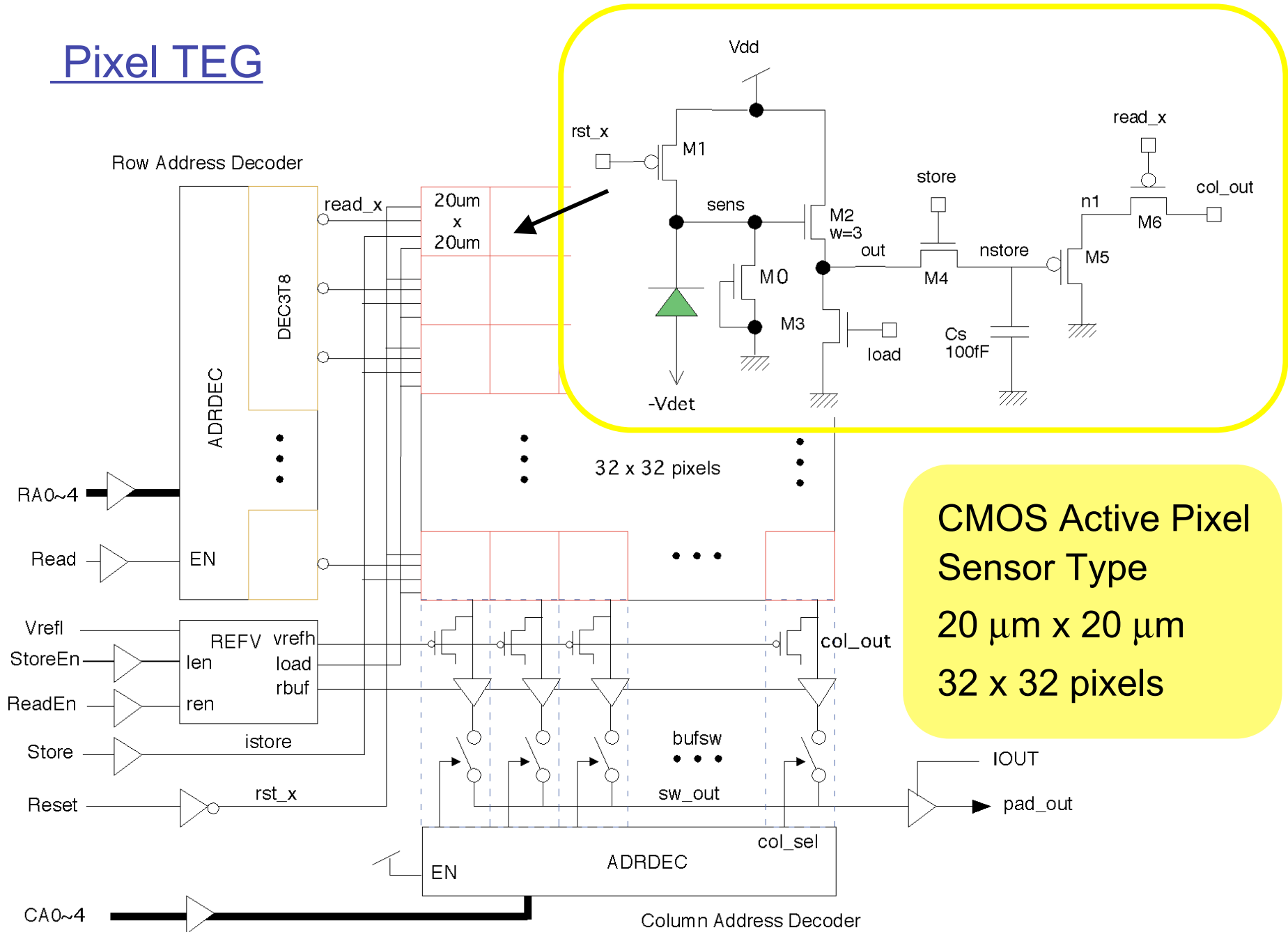
(This figure is not to scale)

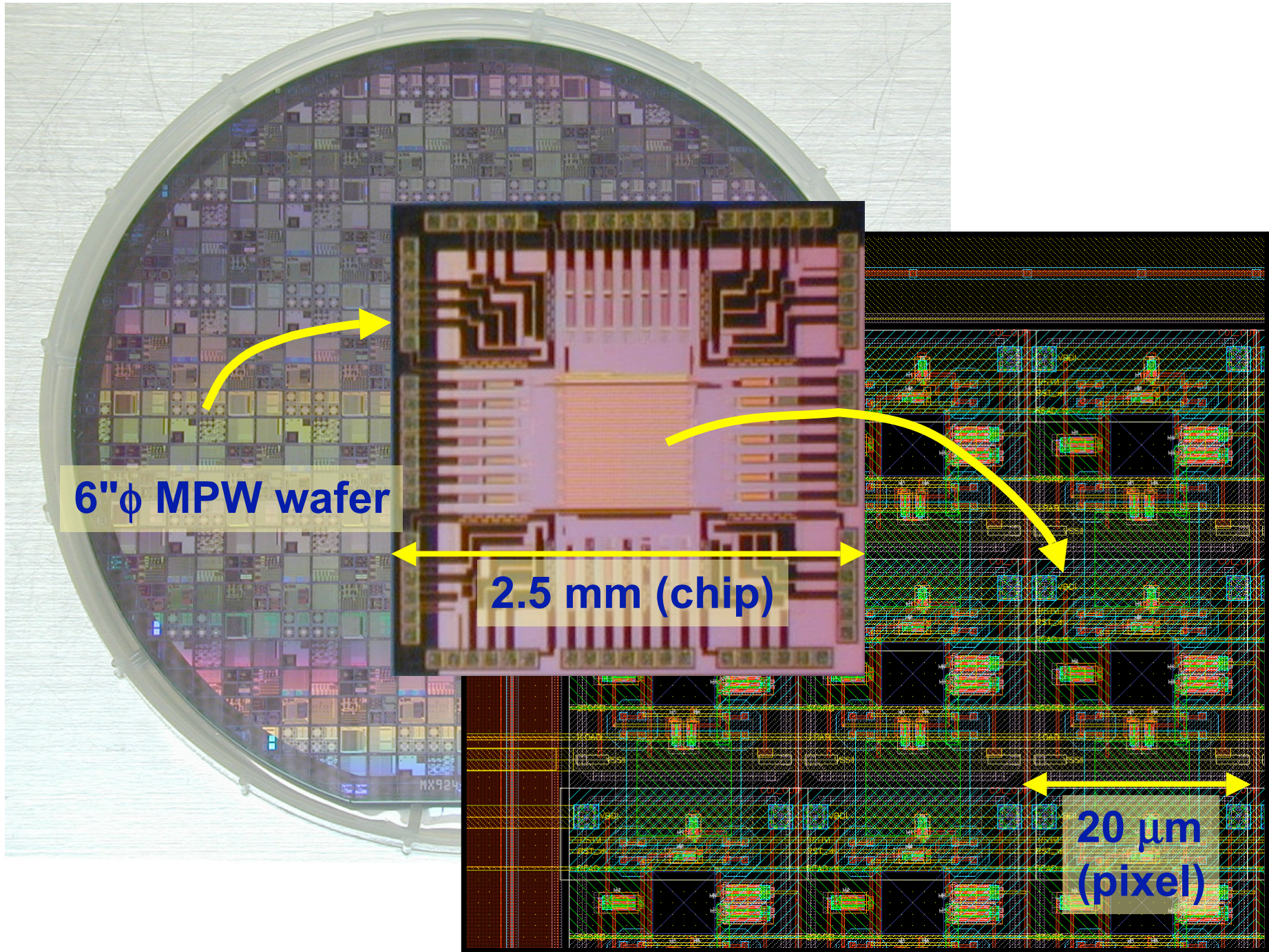
Diode TEG

Metal contact & p+ implant

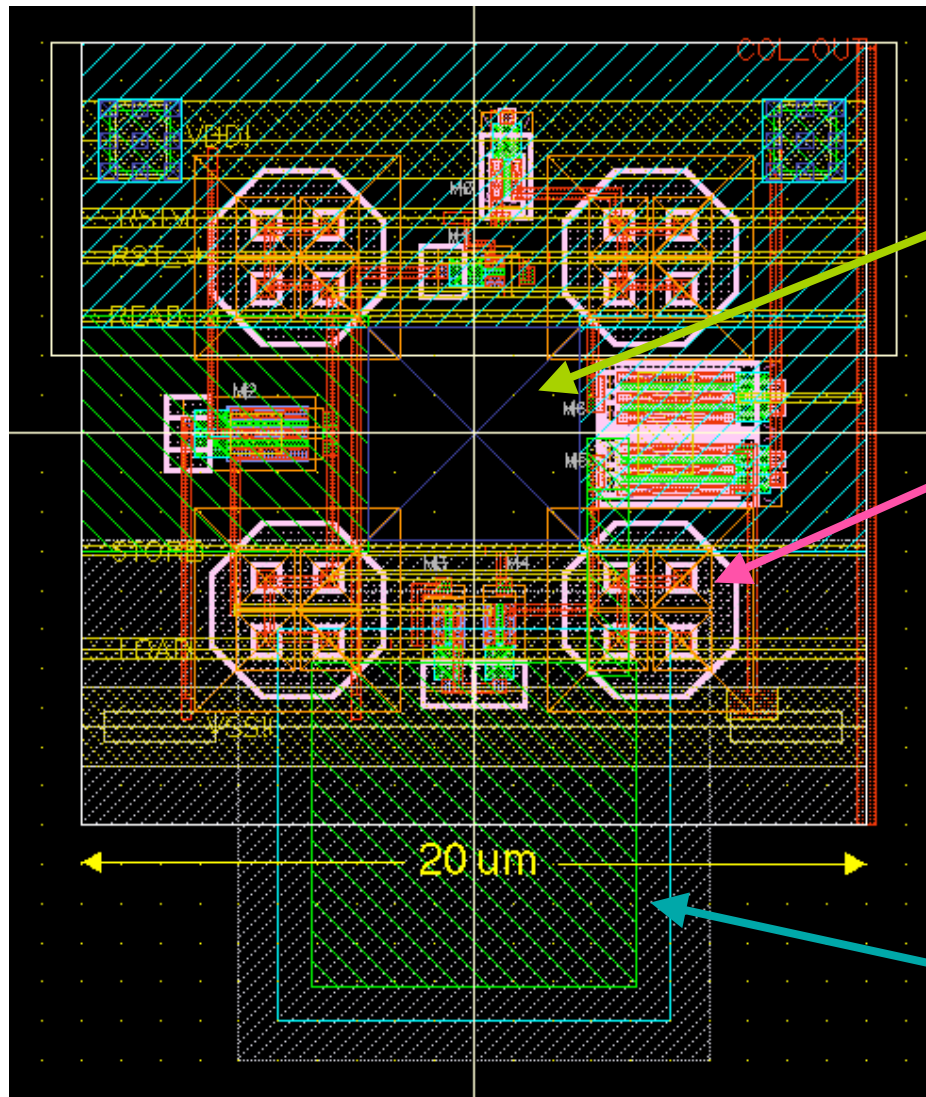


Pixel TEG





Pixel Layout

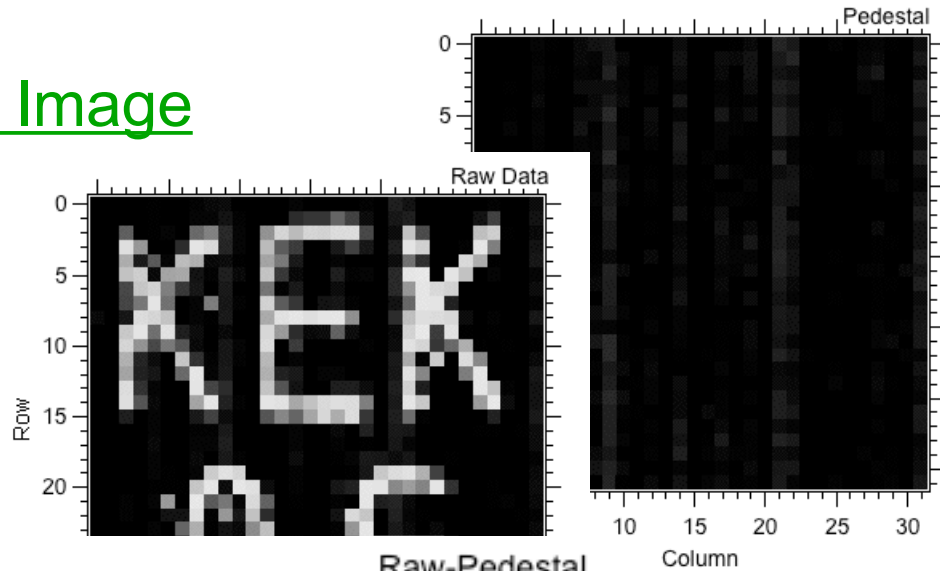


Window for Light Illumination
(5.4 x 5.4 μm²)

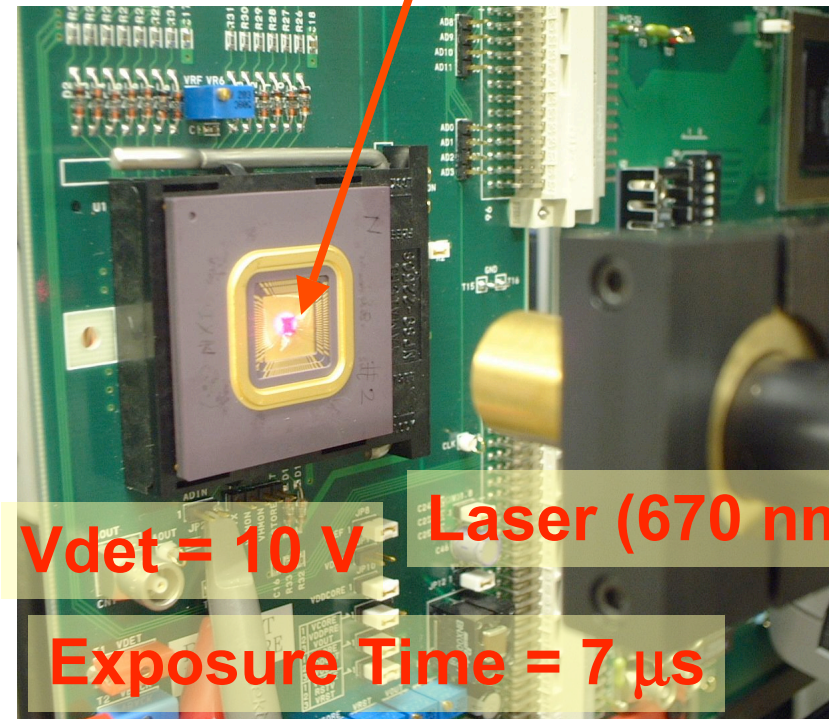
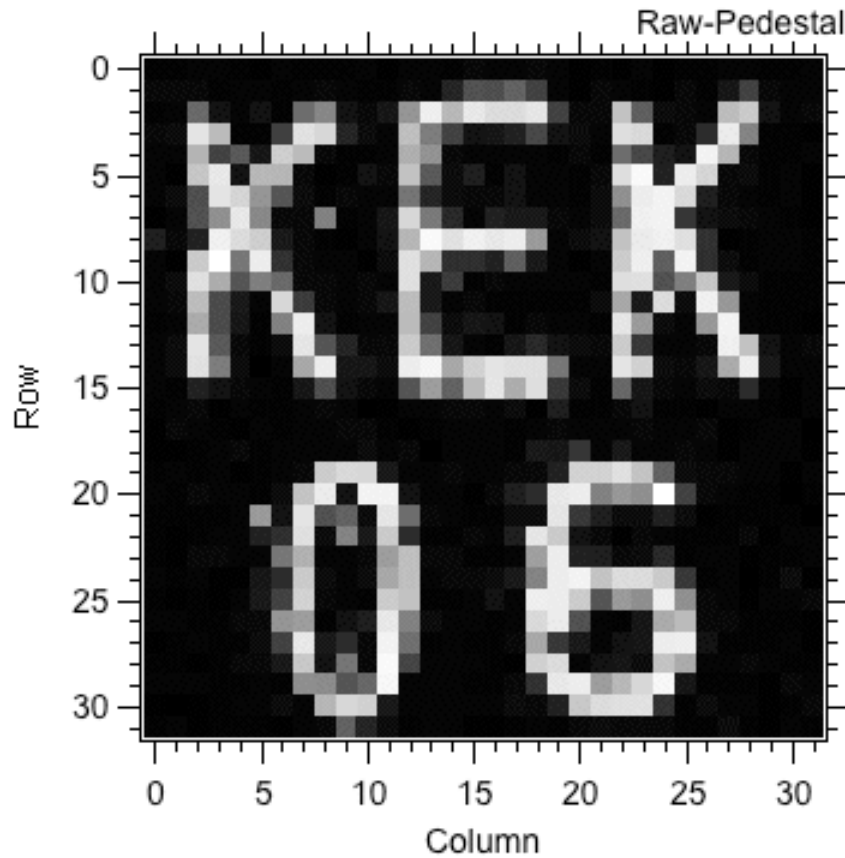
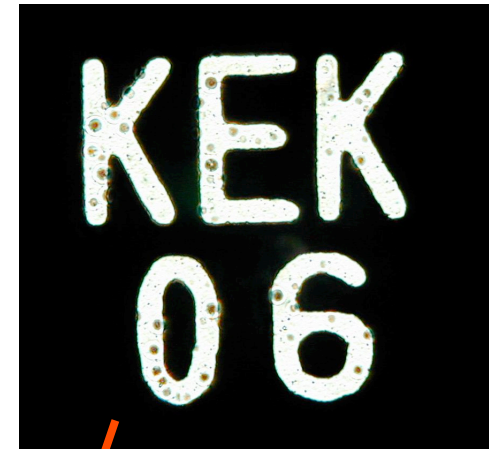
p+ junction

Storage Capacitance
(100 fF)

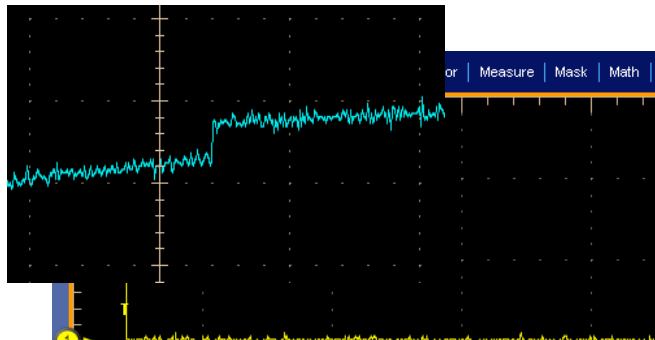
Photo Image



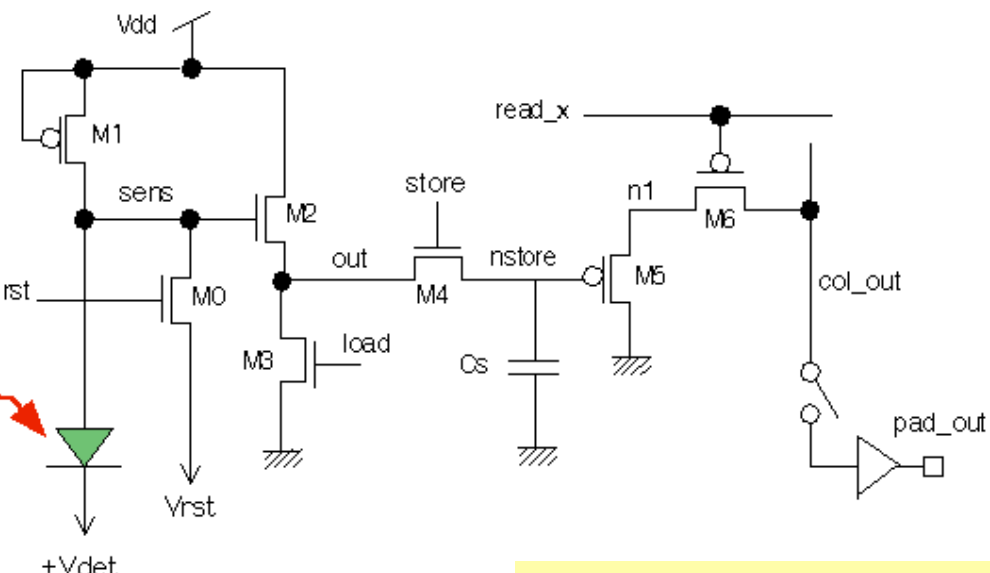
Plastic Mask



β -ray (^{90}Sr) Signals

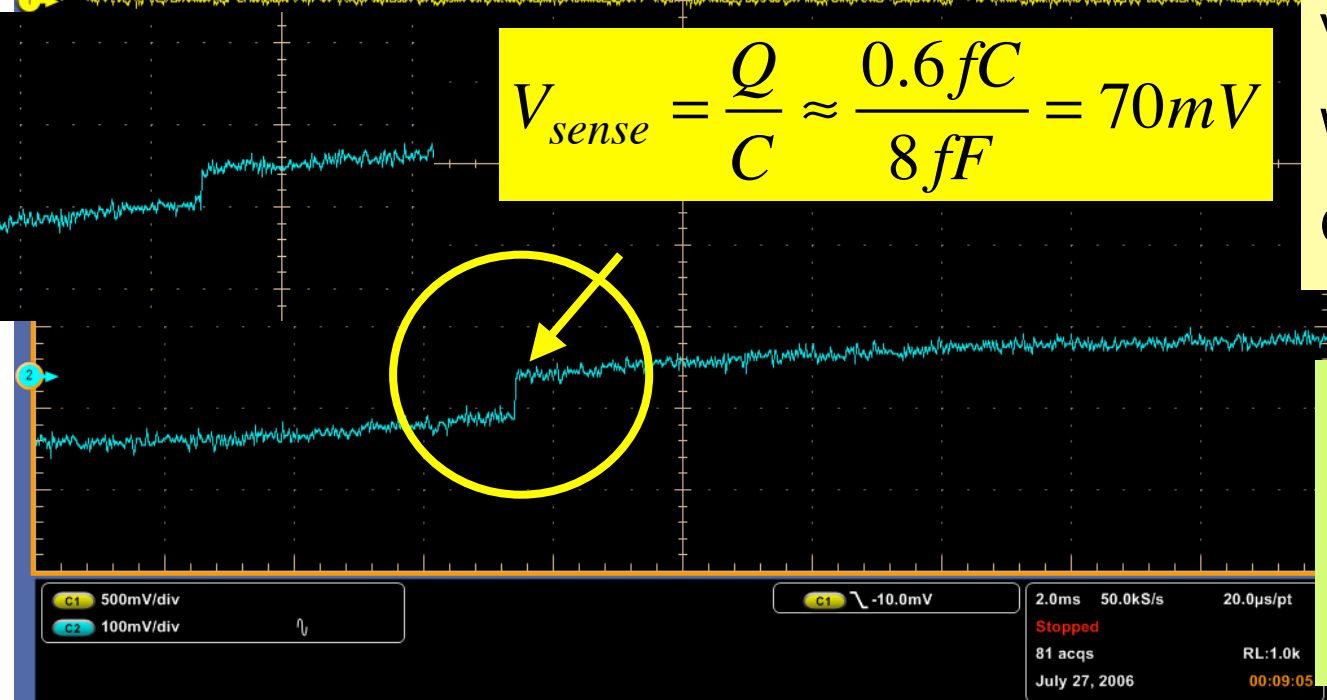


β -ray



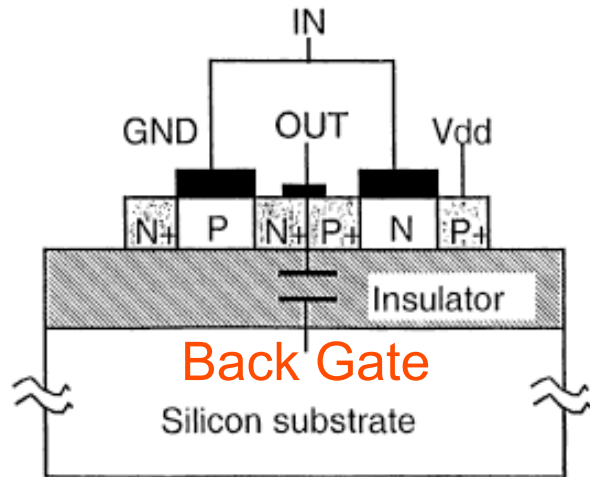
$$V_{sense} = \frac{Q}{C} \approx \frac{0.6 \text{ fC}}{8 \text{ fF}} = 70 \text{ mV}$$

$V_{det} = 10 \text{ V}$
 $W_{depletion} \sim 44 \mu\text{m}$
 $Q \sim 3500 \text{ e} (0.6 \text{ fC})$

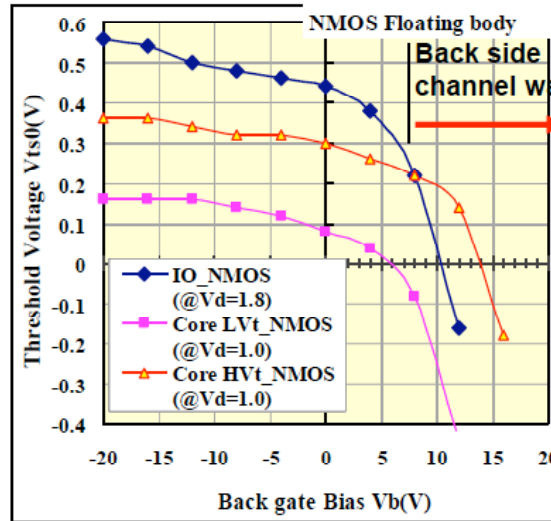


Expected signal amplitude was observed for β -ray.

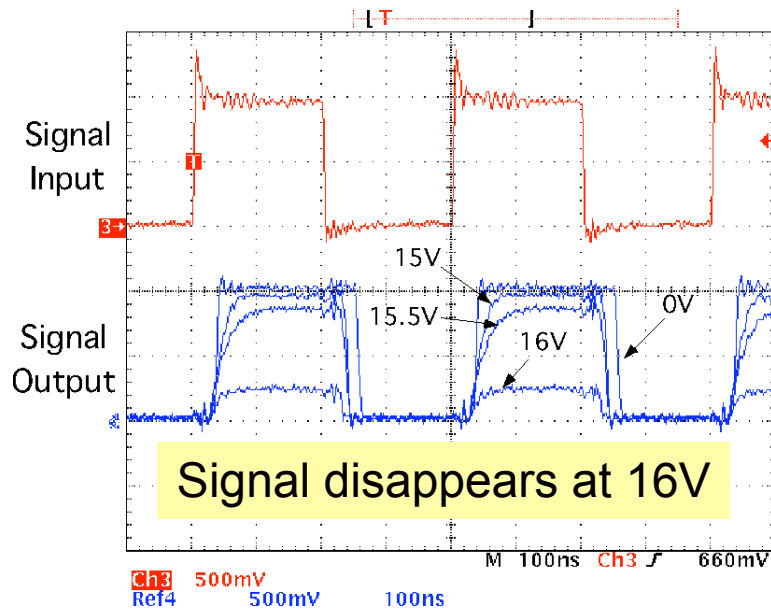
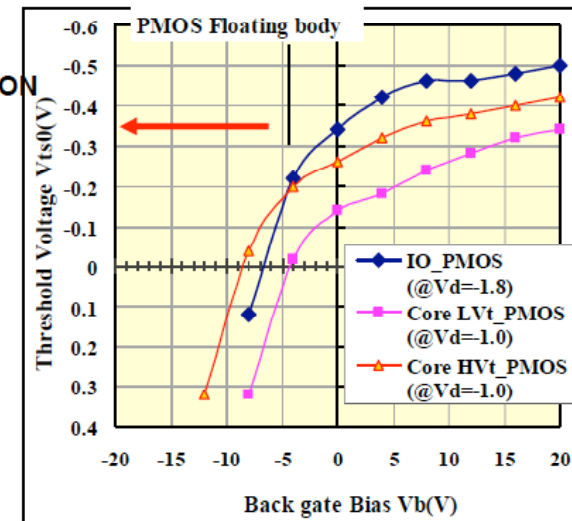
Back Gate Effect



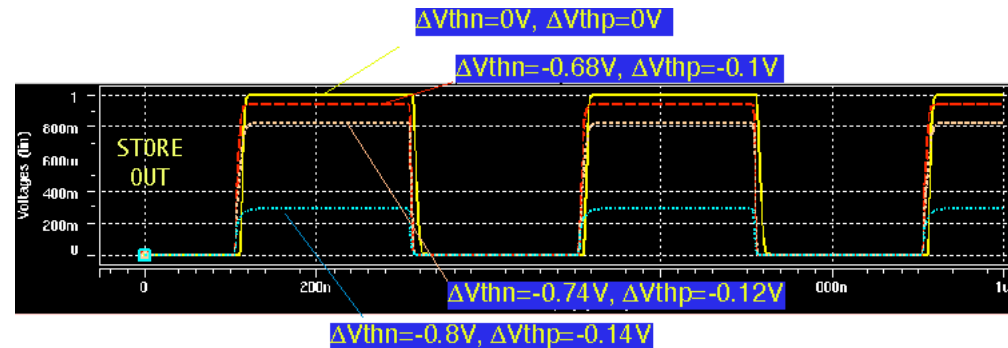
NMOS Threshold Variation



PMOS transistor



Substrate Voltage act as Back Gate, and change transistor threshold.



Consistent with SPICE simulation.

Summary

- A first SOI Pixel Detector (32 x 32 pixel with 20 um x 20um size) was successfully fabricated and tested.
- The detector has sensors in high-resistive Si and CMOS circuit in low-resistive Si.
- The detector is fabricated in a commercial 0.15 μm SOI CMOS process with 3 additional masks.
- Good images 'KEK06' with red laser light are taken.
- Signal for β-ray from ⁹⁰Sr is observed.
- Break down voltage of present sensor is about 100V and hot spot is identified.
- Back gate effect was observed. It is consistent with SPICE simulation, and studied with ENEXSS simulator.
- p+ implant near transistor greatly reduce the back gate effect.
- Next submission is scheduled in beginning of December.

Next Submission Plan

Next submission is our own **Multi Project Wafer** run.

Design Dead line ~ Dec. 5

Chip Delivery ~ End of Next March

!! Space is still available !!
2.5 x 2.5 mm² space ~ \$18k

