

RF System (HLRF, LLRF, Controls) EDR Plan Overview

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Chris Adolphsen

For

Ray Larsen, John Carwardine and Shin Michizono

EDR Assumptions

- EDR to be completed in three more years, i.e. end of FY09.
- Will include detailed technical and cost plans that are considerably more mature than RDR.
- Will include a schedule and funding profile consistent with the plans.
- Will be sufficiently mature to provide a basis for international funding requests, implying
 - *technology down-selects close if not already in hand*
 - *industrialization, industrial cost estimates close if not already in hand.*

Work Package Goals

- Work packages to be defined for two phases:
 - *R&D for FY08-09 (plans ongoing)*
 - *Engineering packages for industrialization of prototypes, early production runs (by EDR FY09)*
- Following lists topics for work packages for HLRF BCD, ACD designs
 - *Modulators, Klystrons, HLRF*
- Example: Klystron

Klystrons

- **BCD - MBK Klystron**
 1. *Commercial prototypes procurement, test plan*
 2. *Performance verification plans*
 3. *Cost analysis test systems*
 4. *Industry cost verification plans*
- **ACD - SBK Klystron**
 1. *Development plan, costs Unit 1*
 2. *Test plan, costs Unit 1*
 3. *DFM Unit 2 development, test plan, cost plan*
 4. *Factory Model, test, cost plan*
 5. *Maintenance model, cost analysis*
 6. *Industrialization plan, ramp-up, cost verification*

Task Table

SYSTEM	R&D WP	EDR WP
•BCD Modulator R&D	7	
•BCD Modulator Industrialization		4
•Marx Modulator Unit 1	3	
•Marx Modulator DFM	5	
•Marx Modulator Industrialization		4
•BCD - MBK Klystron		4
•ACD - SBK Klystron	2	5
•BCD - RF Distribution	1	
•ACD - RF Distribution	3	3
<i>Total</i>	21	20

Total 08-09 FTEs ~ 80

HLRF Summary

- All three major RF subsystems require aggressive R&D up to and beyond EDR time end FY09
- High emphasis needed on industrialization through work packages released (or ready to release) for DFM designs
- Technical risks relatively low for BCD designs, higher for ACD designs.
- Cost risk remains high for all due to lack of certainty of extrapolation to industrial quantities.
- XFEL will provide useful data to help reduce cost risk by EDR time of end FY09.

Controls from RDR to EDR...

- Develop RDR models into engineering design.
- Validate/prototype key concepts in RDR models, eg
 - *Network architecture.*
 - *Front-end model, technical system interfaces.*
 - *Synchronous 5Hz feedback infrastructure.*
 - *Standards, standardization, QA.*
 - *Diagnostic Interlock Layer.*
- Perform targeted R&D where it is needed, eg
 - *RF field regulation (phase & amplitude).*
 - *High availability implementation.*
 - *Fault detection and recovery.*
- Controls & LLRF support for test facilities.

WP model...

- Top-down objectives and initiatives, eg
 - *Investigate ATCA as a candidate platform for instrumentation electronics.*
- Bottom-up work packages can come from many sources:
 - *Lab proposals*
 - *Collaborative contributions*
 - *Overlapping interests with other activities.*
- Americas planning for FY08 identified a need for 10+ FTEs for controls on EDR and related R&D
 - *Assumes similar participation from other regions.*
 - *Does not adequately cover all anticipated work packages, eg for RDR validation & prototyping RDR design concepts.*

- Support for (test) facilities (XFEL, SMTF, STF)
- Crate evaluation
- FPGA board development having >26 ADCs.
- Software development
- High IF study

	2007				2008				2009			
	I	II	III	IV	I	II	III	IV	I	II	III	IV
DESY* FPGA board for XFEL ATCA board development Conversion of LLRF to ATCA Implement and evaluate ATCA LLRF Finalize LLRF for the XFEL Software development with SMCON-DSP												
FNAL 33 ch FPGA board for ILCTA (NML) Operational S in con system ATCA development FB algorithm high IF and sampling												
KEK 8 cavities vector sum control 32ch ADCs FPGA board (ATCA)** ATCA I/O interbck** IF mixture** 24 cavities vector sum												
* http://xfeldesys.de/content/e154/upbad/upbad_file/TDR/XFEL-TDR-Ch-10.pdf (XFEL TDR) ** JFY budget is still unknown.												