LLRF in ATCA for XFEL

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Outline

- The goal
- Development at DESY
- Standardization & HA
- Status report / plans
- Difficulties

The goal

Evaluate complete LLRF system based on ATCA at FLASH in 2007

Hardware

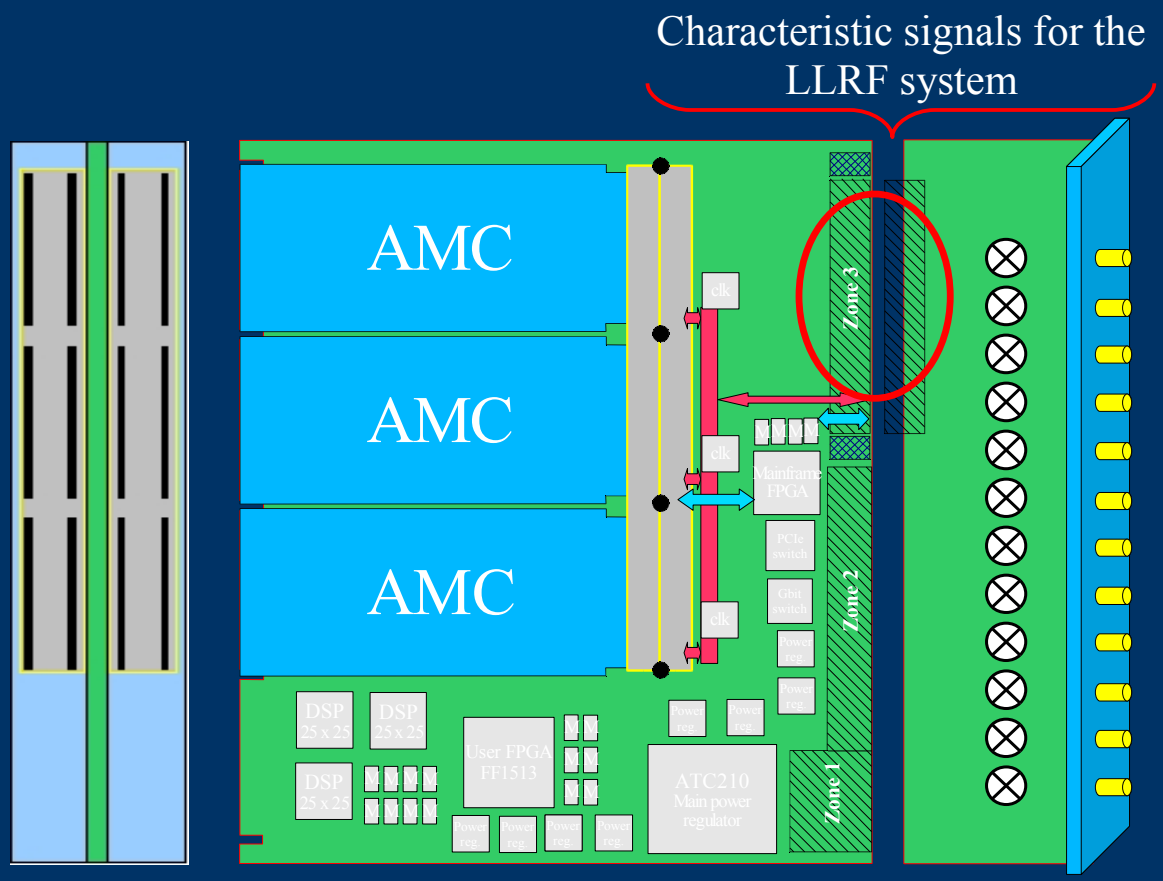
- down converters,
- processing unit,
- vector modulator,
- ...

Software

- distributed control system,
- loaded Q, detuning, IQ detection,
- ...

Development at DESY

- ATCA crate 14 & 5 slots
- ATCA carrier boards
- AMC modules
- RTM modules
- Boxes



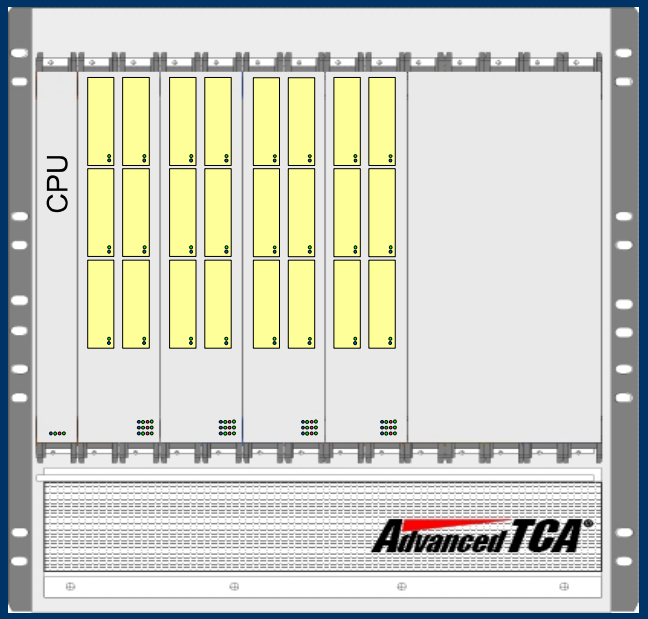
Development at DESY

System configuration

Board 1:
- 4 x ADC board (32 probe signals)
- 1 x timing
- 1 x VM

Board 2:
- 4 x ADC board (32 reflected power)
- 1 x communication module

Board 3:
- 4 x ADC board (32 forward power)
- 1 x ADC board (additional, spare channels)
- 1 x timing (redundant)
- 1 x VM (redundant)



Advantages

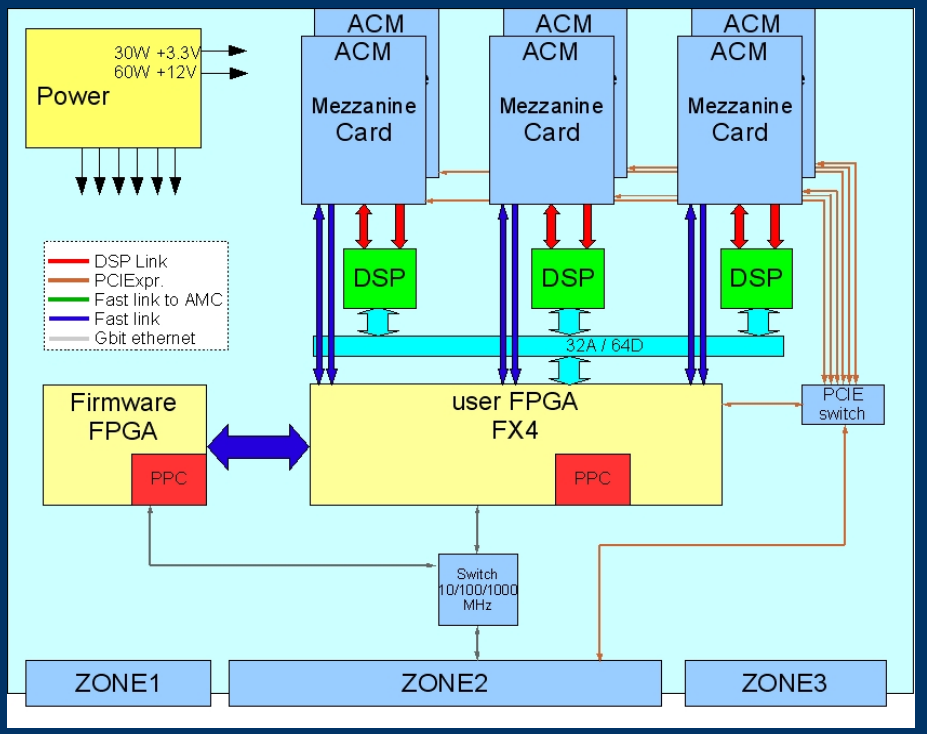
- Reduced latency
- Modular (distributed)
- Redundant (only critical parts – cots)

Development at DESY

ATCA Carrier board

- 6 x AMC slot (AMC.1)
- 3 x DSP
- standalone possible
- IPMI
- Gigabit Ethernet
- Low latency communication "on board"

Customize backplane for clock and trigger distribution



Development at DESY

AMC modules:

- 8 x ADC : 14 bits, SF 100MHz
- 2 x ADC : 12 bits, SF 2 GHz
- Timing receiver
- Communication module
- 8 x DAC (temporary module, needed for piezo driver)
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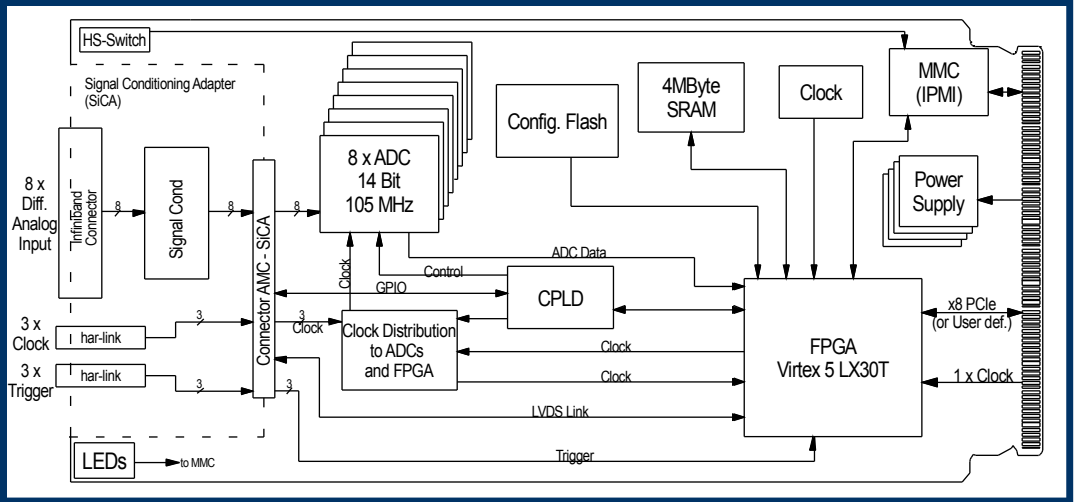
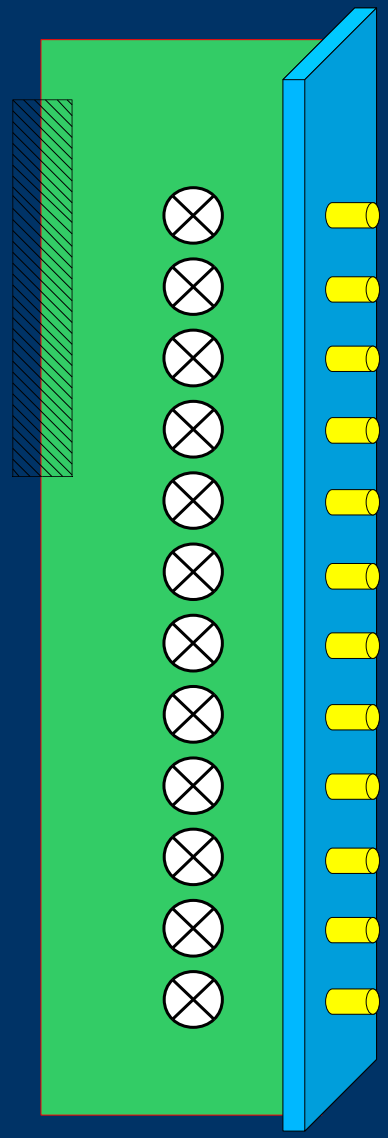


Development at DESY

RTM modules:

- 16 channels down converter (IF 1-50MHz)
- 32 channels down converter (IF 1-50MHz)



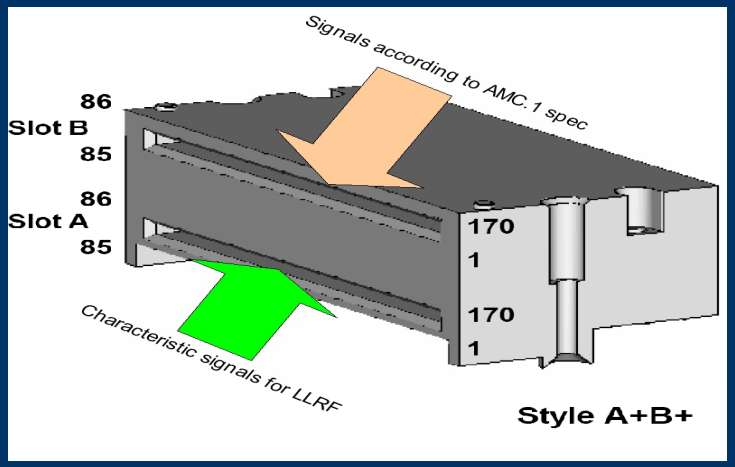
Development at DESY

Boxes:

- Piezo driver (communication module & driver
- WGT

Standardization & HA

- AMC slots
- Power Management (IPMI) for all hardware
- Connectors (RF, high speed digital lines, fibers)



Status report

- ATCA crate : delivered
- Source code for IPMI controller : available from industry, but must be adopted : in progress
- ATCA carrier board : in progress, but still some problems are not solved
- Evaluate PCI Express : in progress
- Analog and digital signals routing (long lines): in progress, no experience
- Simulation : ???
- Software : advanced

Status report

- AMC modules:
  - ADC : in progress
  - Timing Module : in progress, but delayed
  - VM : in progress
- RTM modules - in progress, but delayed
- Boxes - ???

Short and long- term plans

June'06 :

- Schematic for the “simple”ATCA Carrier Board
- Schematics for ADC, VM & Timing Module AMC boards

June/July'07:

- long lines & clock distribution

August'07 :

- ADC-AMC (8 channels)
- VM

September 2007 :

- ADC-AMC (2 channels),
- Timing Receiver

October :

- RTM down converter
- Final version of the ATCA carrier board

Fall 2007 : run “simple version” of the ATCA Carrier board

Difficulties

- ATCA designed for telecommunication market - adaptation for HEP needed
- no experience with long, differential analog signals
- no analog I/O card commercially available
- many modules must be customized (industry is not interested in design ...)
- IPMI – complicated protocol (we bought design from industry and freely can be modified)
- connector for RF/IF signals in ZONE 3
- Expensive debugging tools
  - PCIEx. 70 k$
  - Advanced (3D) simulation of PCB needed

µTCA

?

- Small form factor
- Limited number of links (latency)

Rather difficult to use in the control loop.