R&D Status/Plan for FPCCD VTX Detector

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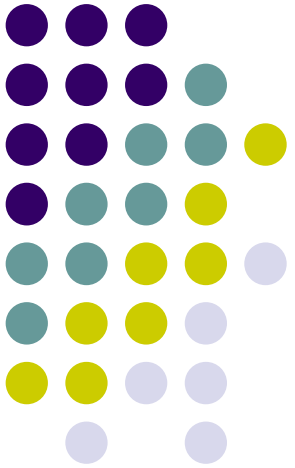
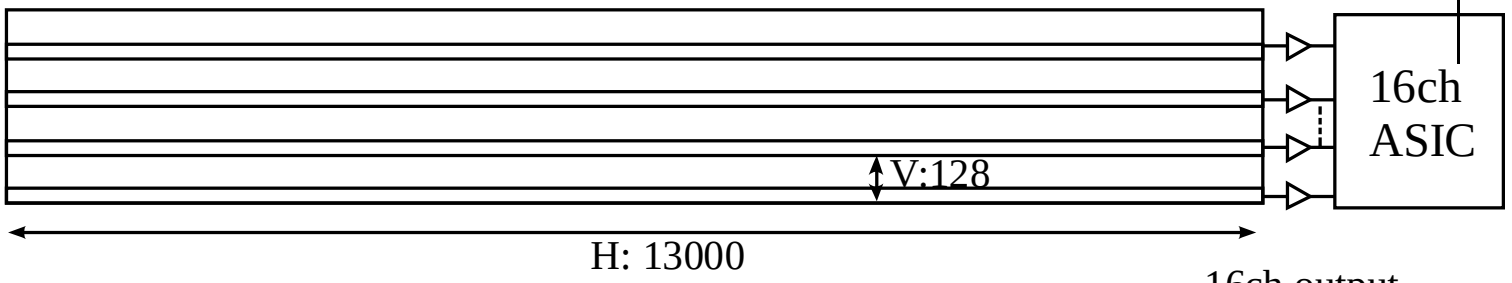
@LCWS2007



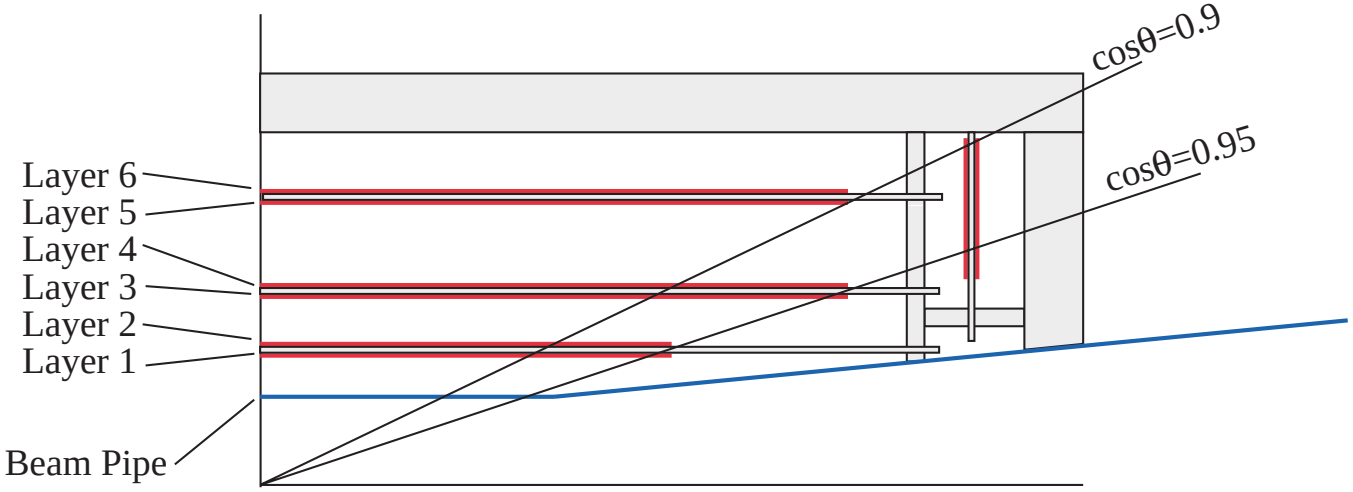
FPCCD Vertex Detector

- Accumulate hit signals for one train (2840 BX) and read out between trains (200ms) → Completely free from EMI
- Fine pixel of ~5μm (x20 more pixels than “standard” pixels) to keep low pixel occupancy
  - Spatial resolution of ~1.5μm even with digital readout
  - Excellent two-track separation capability
- Fully depleted epitaxial layer to minimize the number of hit pixels due to charge spread by diffusion
- Two layers in proximity make a doublet (super layer) to minimize the wrong-tracking probability due to multiple scattering
- Three doublets (6 CCD layers) make the detector (in GLD DOD)
- Tracking capability with single layer using hit cluster shape can help background rejection
- Multi-port readout with moderate (~10MHz) speed (Very fast readout (>50MHz) not necessary)
- Simple structure → Large area
- No heat source in the image area



16ch output
0.64mm pitch

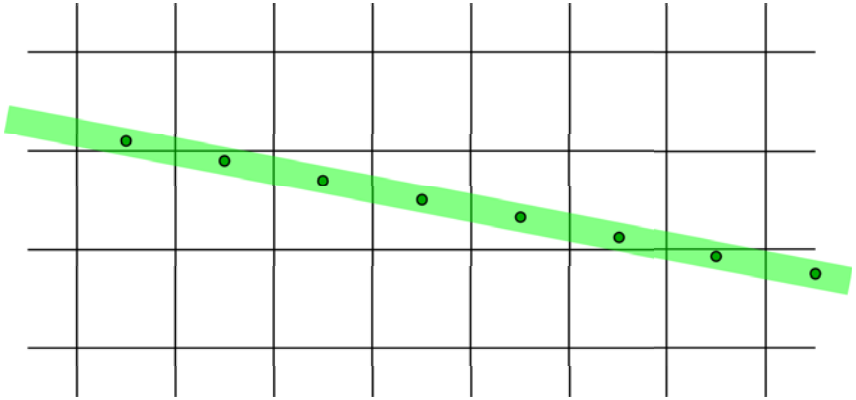
Size:
H; 5μmx13000=65mm
V; 5μmx128x16=10.24mm

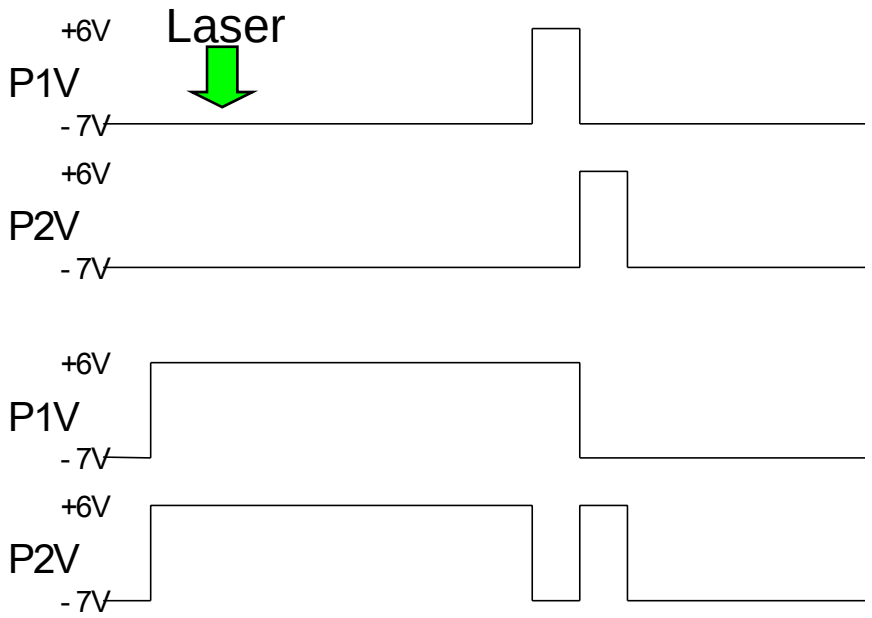


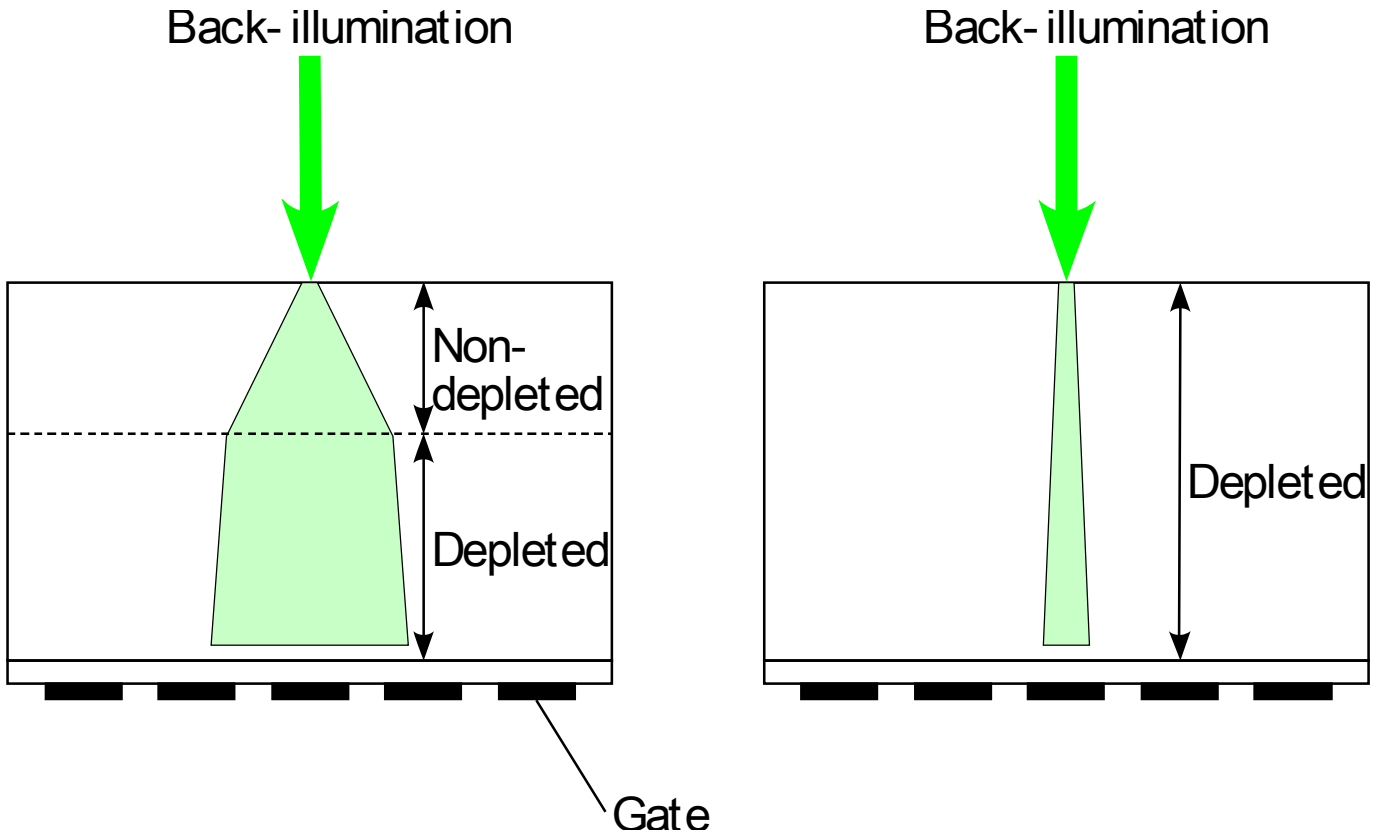
Layer	R (mm)
1	20 (18)
2	22 (20)
3	32
4	34
5	48
6	50

Development of Fully-depleted CCD by HPK

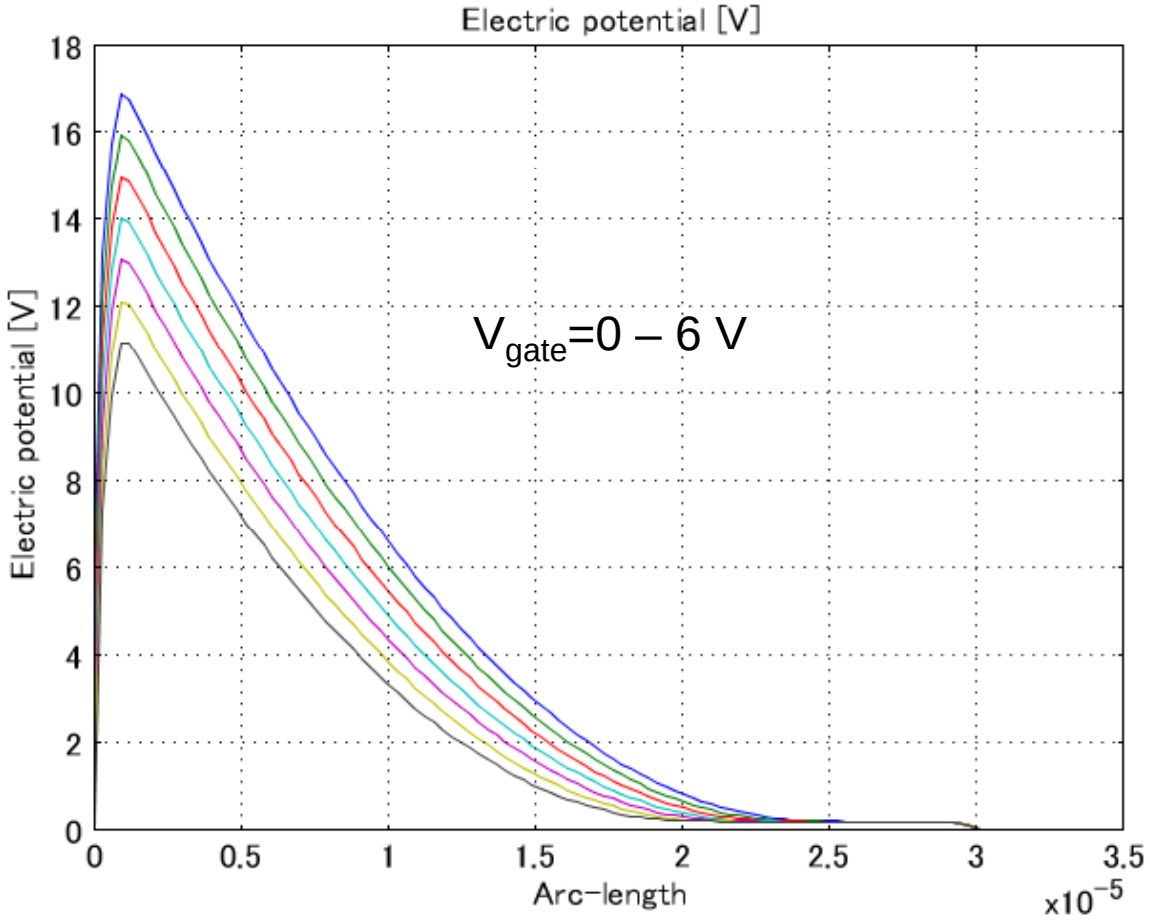
- Confirmation of full-depletion using line-focused LASER
  - LASER light (532nm) focused to a thin (<pixel size) line was illuminated to CCDs slightly inclined w.r.t. CCD pixel grid ➔Effectively scan inside a pixel
  - Compare signal distribution between V_{gate}=-7V and V_{gate}=+6V during LASER illumination
  - If distributions are same, the CCD is fully depleted in both cases



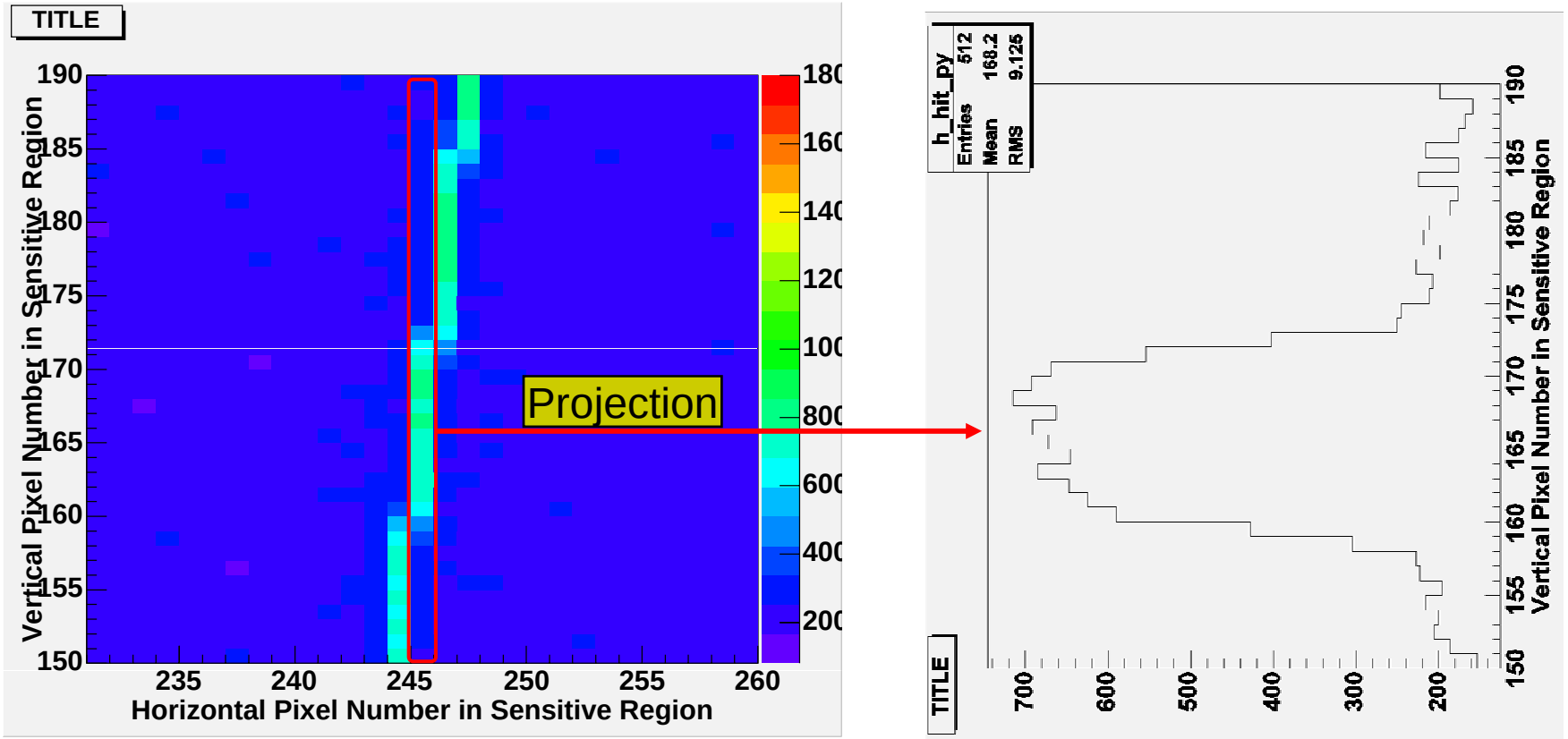



Back- illumination
Non-
depleted
Depleted
Gate
Back- illumination
Depleted

Potential v.s. Vgate



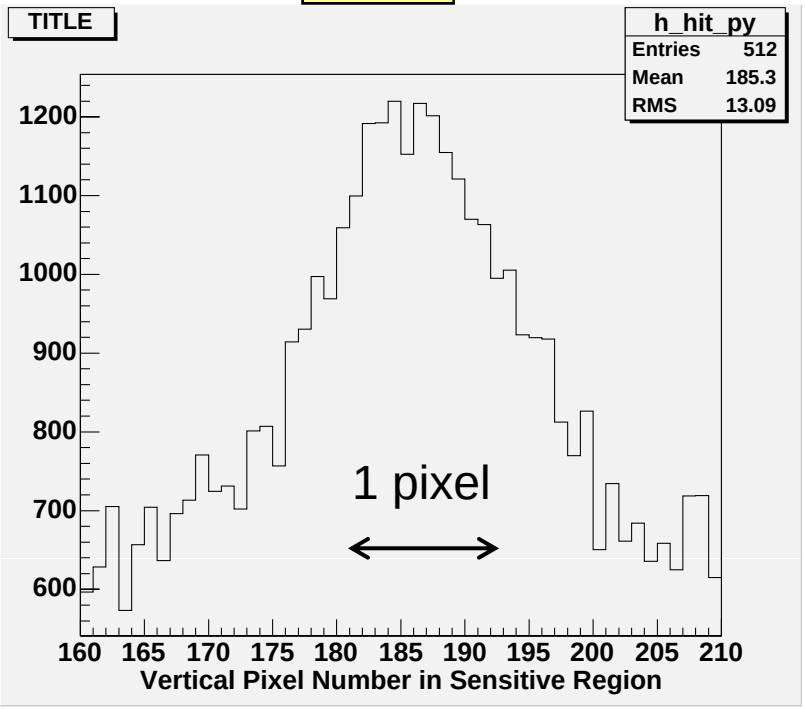
Results


TITLE
Vertical Pixel Number in Sensitive Region
Horizontal Pixel Number in Sensitive Region
Projection
h_hit_py
Entries 512
Mean 168.2
RMS 9.125
TITLE
Vertical Pixel Number in Sensitive Region

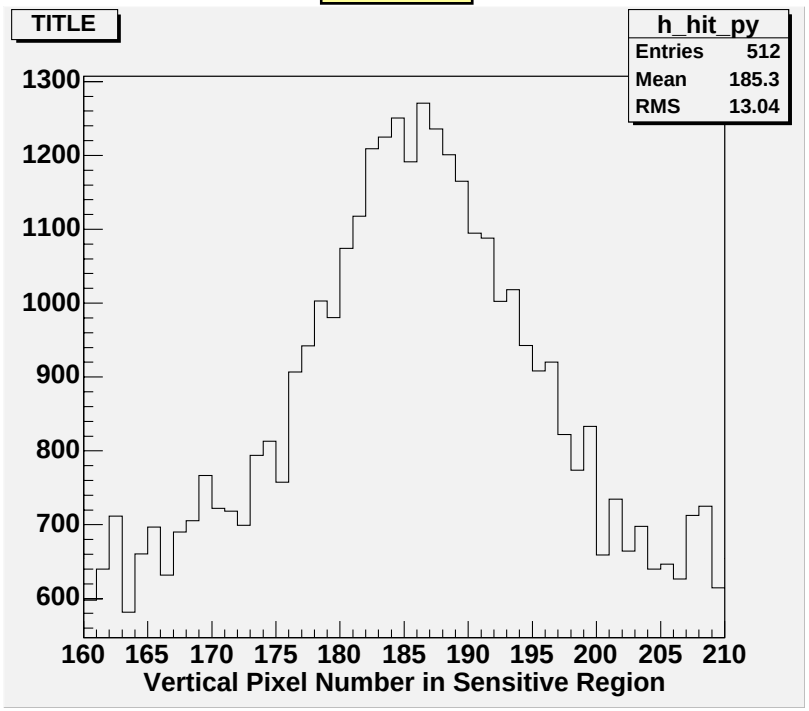
S7170 Standard

- Back-illumination
- Low resistivity epitaxial layer → thin depletion layer
- S.N.; BF3-006

-7V



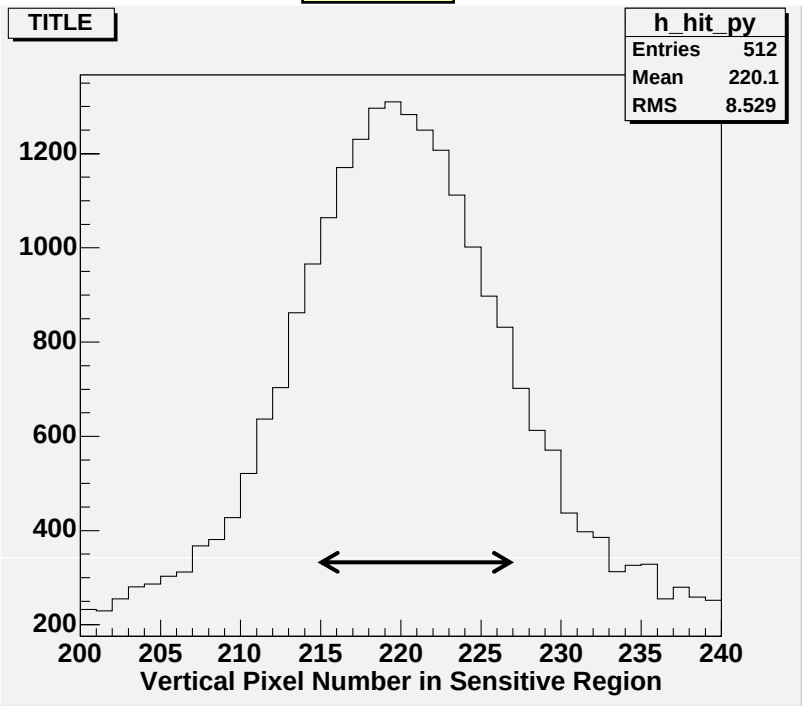
+6V



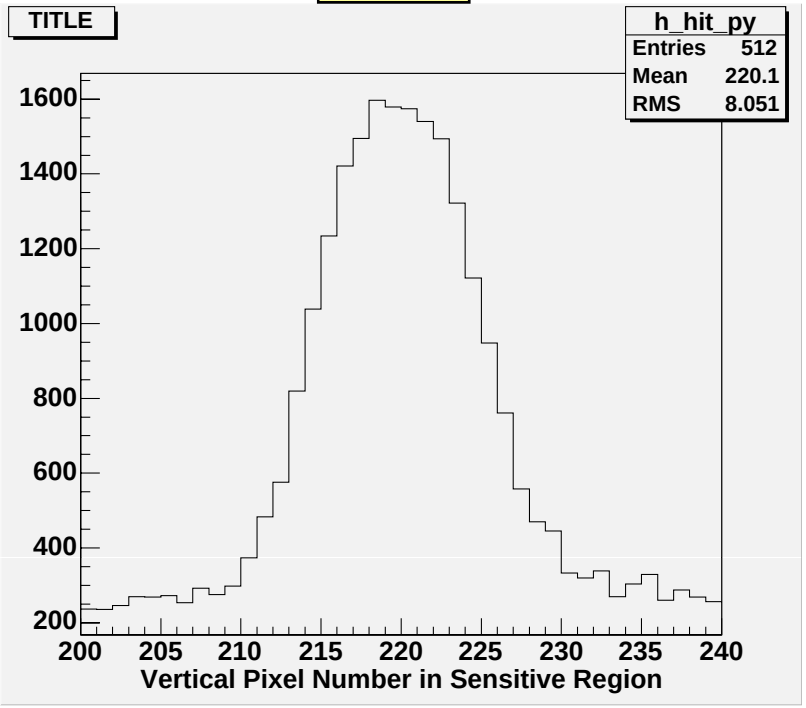
S7170 Deep2

- Higher resistivity 30μm thick epitaxial layer
- SN; FF16-011

-7V



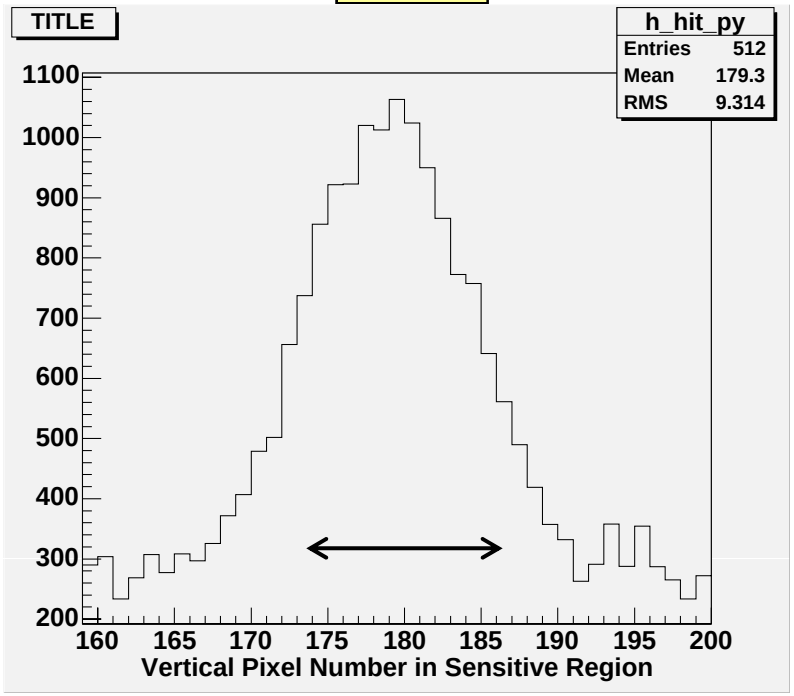
+6V



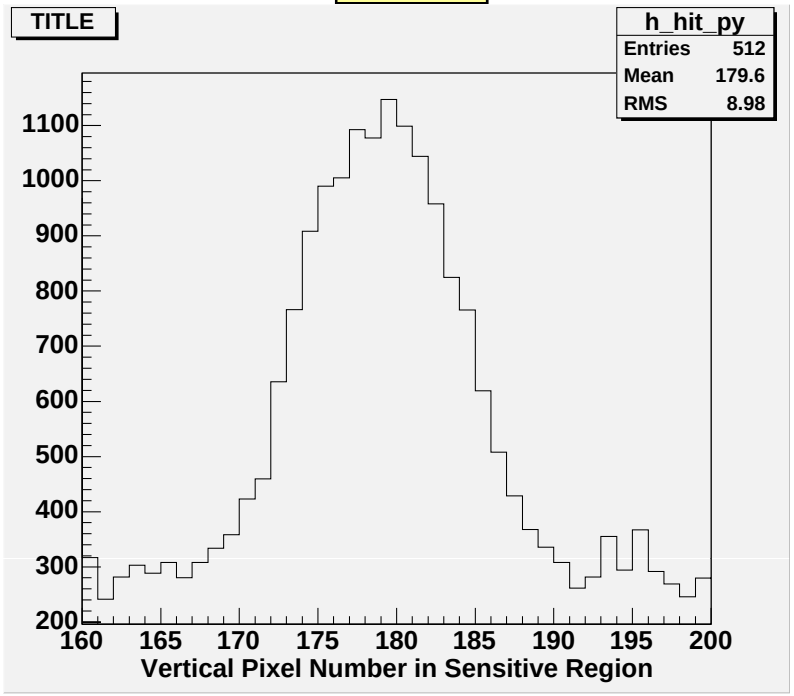
S7170 SPL 15μm

- Higher resistivity 15μm thick epi-layer
- SN;11-12

-7V



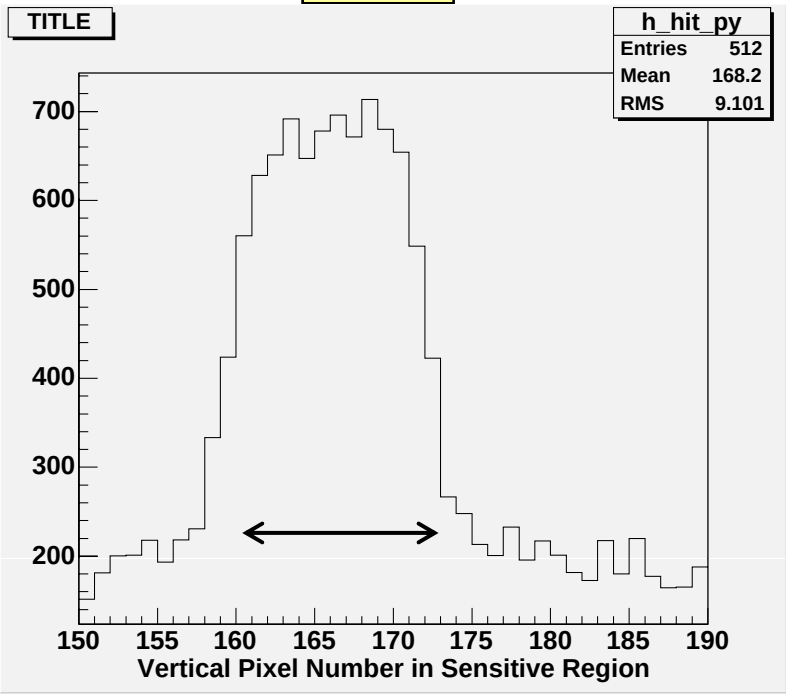
+6V



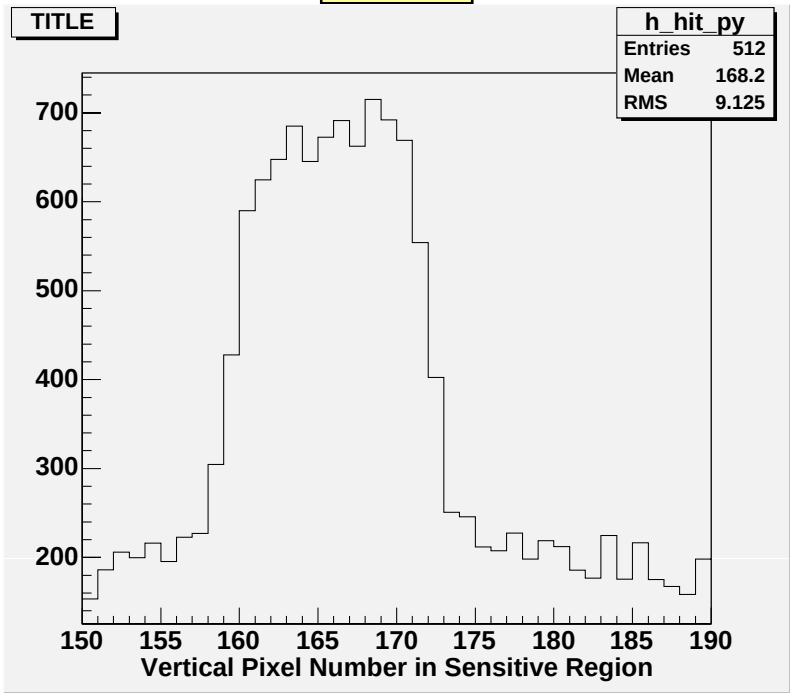
S7170 SPL 24μm

- Highest resistivity 24μm thick epi-layer
- SN; 22-20

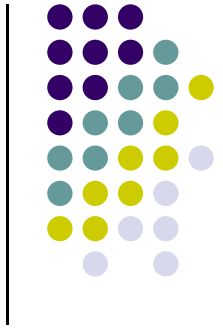
-7V



+6V



Conclusion



- Fully depleted epitaxial layer is the key issue of FPCCD vertex detector
- The signal distributions of a newly developed CCD, S7170-0909 SPL 24μm, at two different gate voltages of -7V and +6V during the LASER illumination were same
- From this result, we can conclude that S7170-0909 SPL 24μm is fully depleted even at the gate voltage of -7V
- Measurement of Lorentz angle and study of radiation hardness of this CCD are planned in this FY
- Fabrication of smaller pixel, multi-port readout CCD and ASIC for readout of the multi-port CCD are also planned in this FY