SiD KPiX Electronics

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- Electronics requirements
- KPiX concept
- Performance
- Plans

Si-W work – personnel and responsibilities

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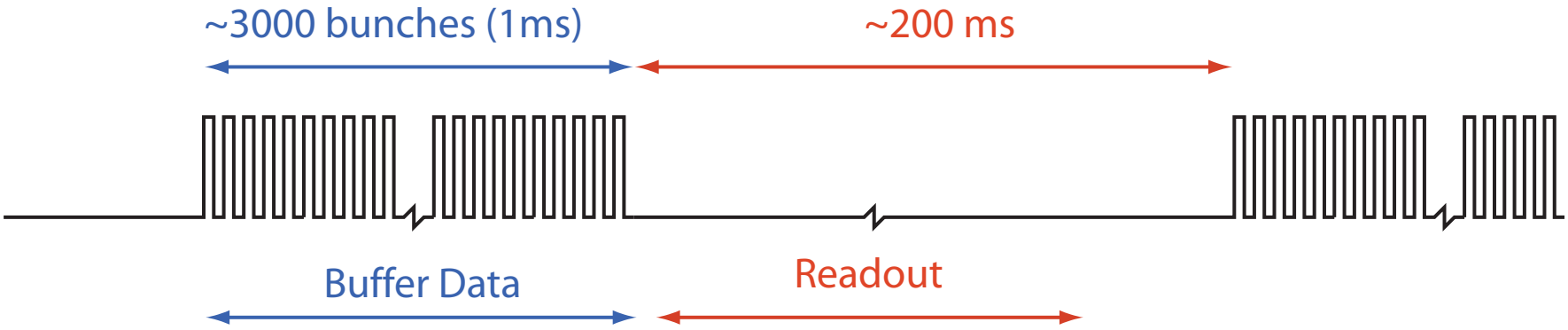
Mechanics	**Electronics**	**Bump Bonding** **Cabling** Mechanics	**Si Detectors** Mechanics Simulation	**Electronics** Mechanics **Simulation**

Bunch Structure at the ILC



- Duty cycle of bunches is low, $\sim 1/200$

$\Rightarrow$ Only provide high current to front end during bunch train

Reduces power

- In the high granular SiD concept, occupancy is low

$\Rightarrow$ Buffer data during the bunch train

Minimizes digital interference to analog signals

How many buffers are needed?

Study* with Luminosity $= 3 \times 10^{34}$, 2820 bunches/train

The following processes were simulated:

- $e^+e^- \rightarrow hadrons\ e^+e^-$
- $e^+e^- \rightarrow \mu^+\mu^- e^+e^-$
- $e^+e^- \rightarrow e^+e^- e^+e^-$
- Bhabhas
- Radiative bhabhas

showed that with 4 buffers, we have less than 1% dead time, everywhere in the ECAL (down to $\theta = 120\, mrad$).

HCAL occupancy should be lower.

* Ron Cassel, SiD LCWS mini-workshop 17 March 2005.

Dynamic range

- Electromagnetic Calorimeter (300 μm silicon sensors)
  - smallest signals 1MIP (1MIP = 24,000 electrons = 3.8 fC)
  - largest signals 2000 MIPs (8.0 pC)

- GEM based HCAL
  - typical signals 5 to 30 fC (depends on gain used)

- RPCs
  - typical signals $\sim$ 0.2 to 10pC avalanche mode

(more than 100 pC for streamers, depending on gas)

$\Rightarrow$ Design electronics for $\sim$ 0.3 fC to $\sim$ 10 pC

Difficult to achieve this dynamic range in a low voltage CMOS process:

Max signal 1.0 V implies noise of 30 μV ?

Power requirement – Can we get the heat out?

Back of the envelope calculation
of Δ temperature in ECAL

Thermal Conductivity:
- W alloy 120W/(K-m)
- Cu 400W/(K-m)

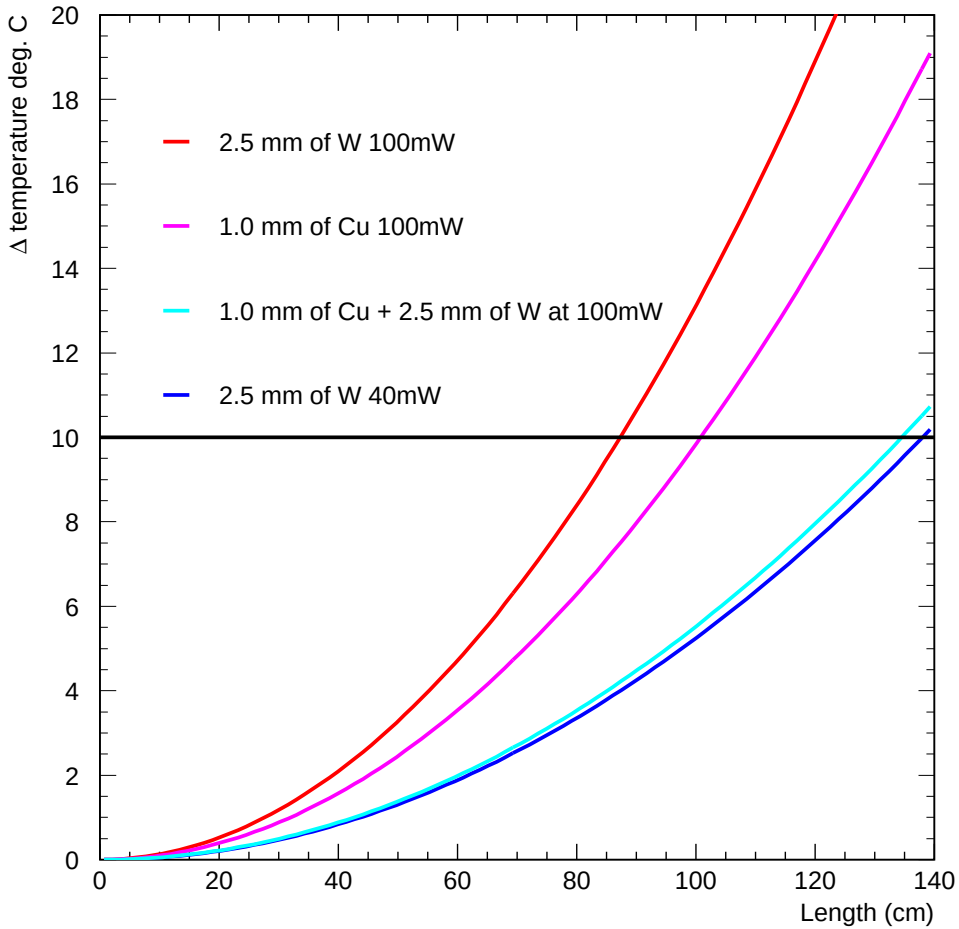
Need to reduce heat to below 100mW/wafer ($\sim$ 1mW/cm^2).

- HCAL will be easier

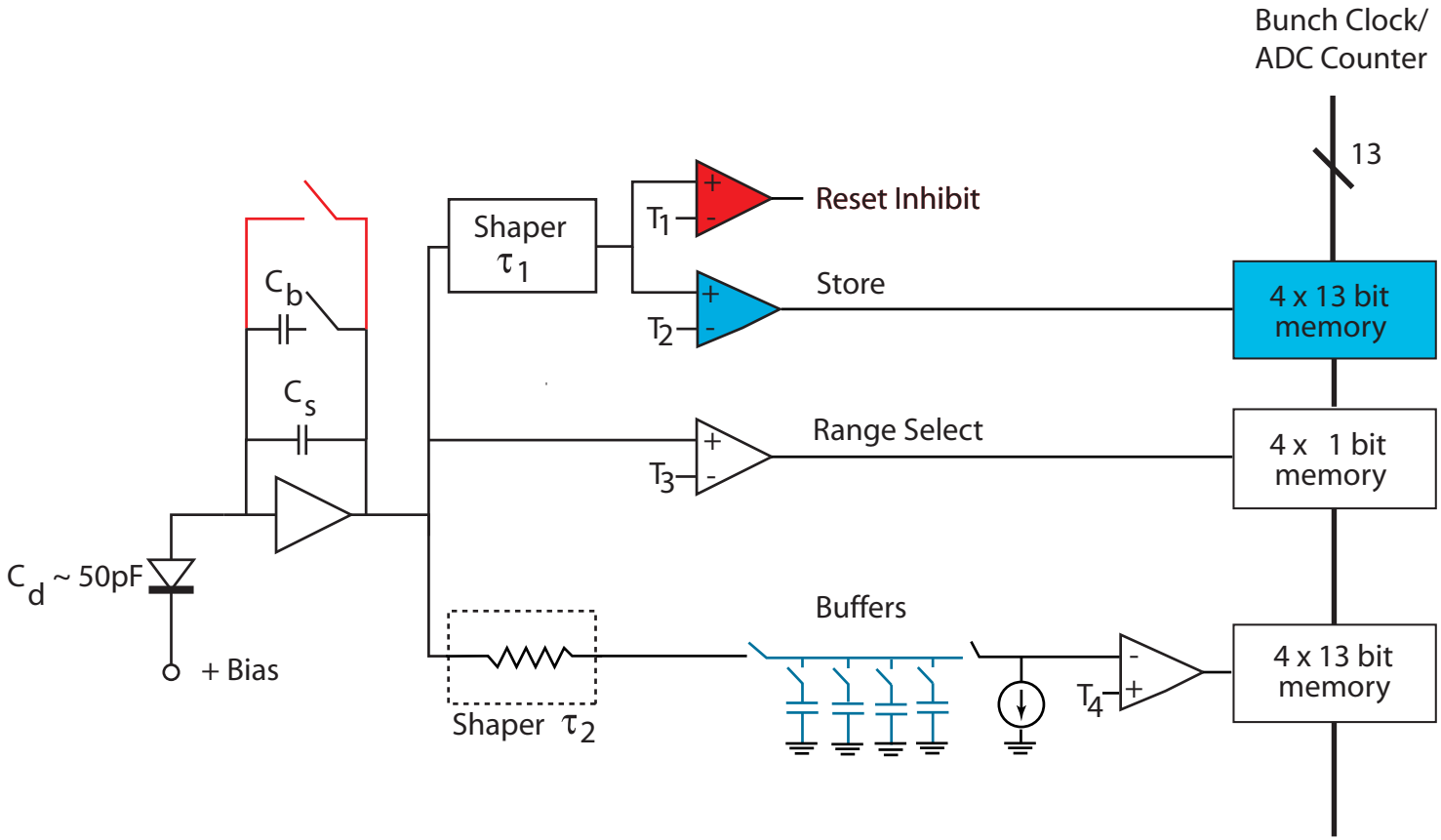
$\Rightarrow$ lower channel density

$\Rightarrow$ thicker absorber

Present design $\sim$ 20 mW
Consistent with prototype measurements

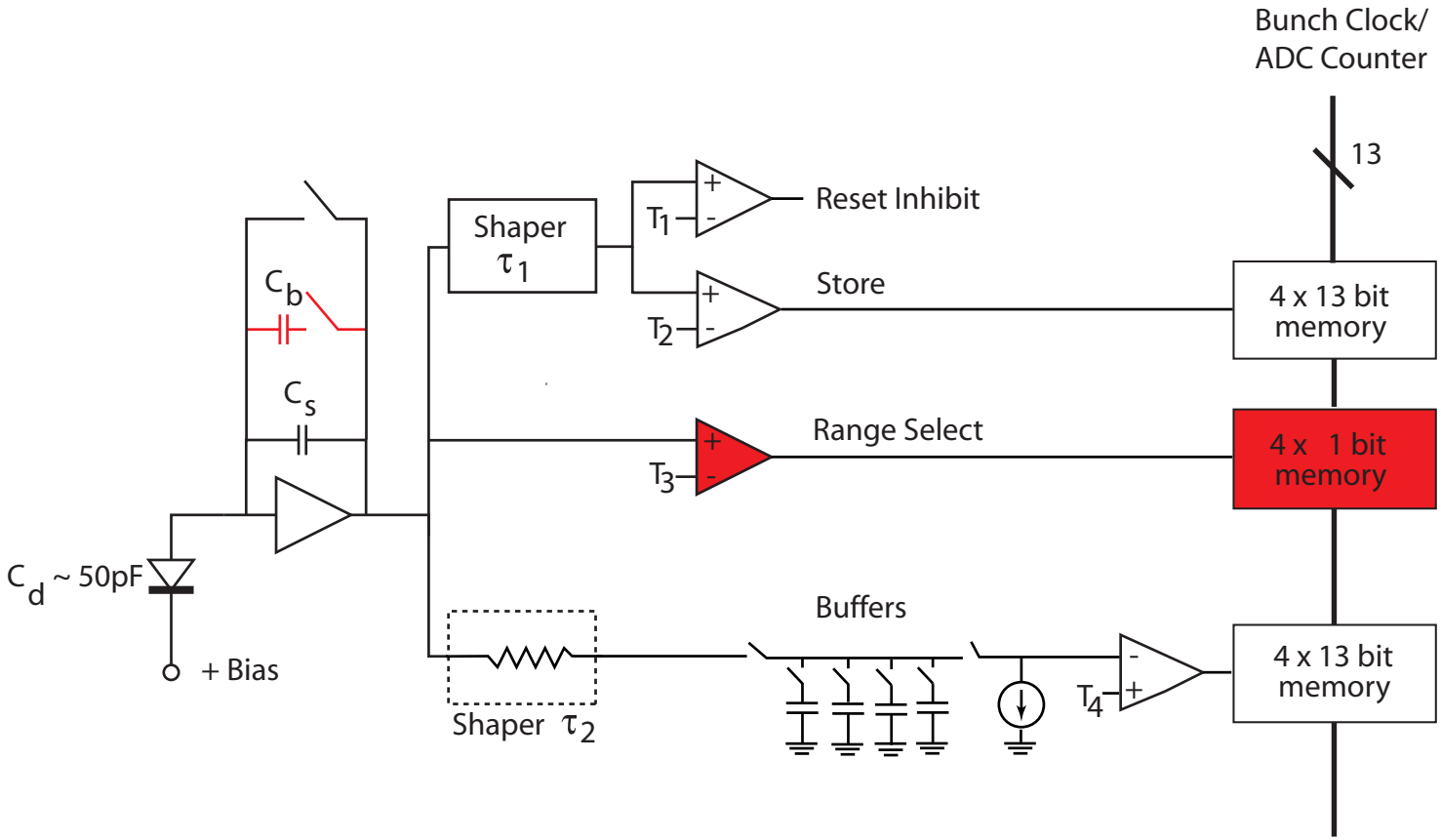


KPiX Concept – saves up to 4 samples from each train



- Threshold T_1 is used to inhibit resets (set at 2 × noise)
- Threshold T_2 is used to enable data storage (set at 4 × noise)
- Bunch clock (time) is stored in SRAM (13 bit precision)
- Analog charge is stored on capacitors (13 bit precision)

Range Switching



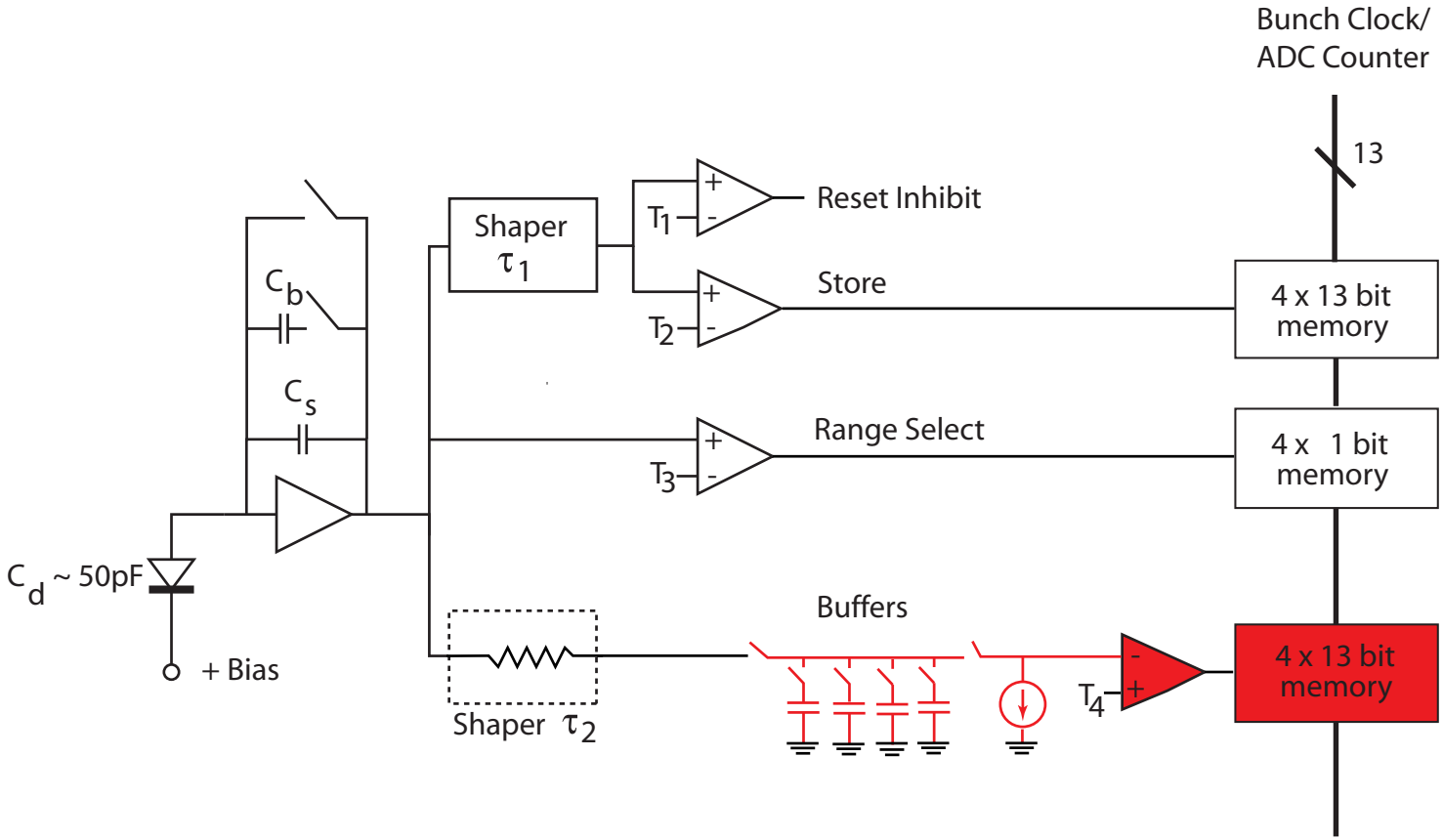
- Dynamic range switching (driven by threshold T_3) selects C_s or $C_b||C_s$

$\Rightarrow$ Feedback capacitor $C_b = 10\,\text{pF}$ stores up to 10 pC

$\Rightarrow$ Feedback capacitor $C_s = 400\,\text{fF}$ (0.3 fC gives 0.7 mV)

N.B. Switches to capacitors closed for several RC times so signals settle

Charge Digitization (between bunch crossings)



- Time needed to discharge each capacitor stored in 13 bit memory
- Time is combined with range bit to correct amplitude

Additional features not shown in simple schematic:

- Built-in calibration system with up to 4 injections per bunch train
- Choice of two values for reset and trigger thresholds
- Bias current servo system for DC coupled detectors

Additional features added in prototype versions 3 or 4:

- Polarity selection (mainly for GEMs)
- External trigger for test beam
- Nearest neighbor trigger logic
- Staticly selectable feedback capacitor for tracker

All these features are tested and working

Chip Size

- Chip is implemented in TSMC 0.25μm CMOS
- Single analog channels comfortably fits into 200μm by 500μm cell
- Overall chip size (1024 channels) approximately:

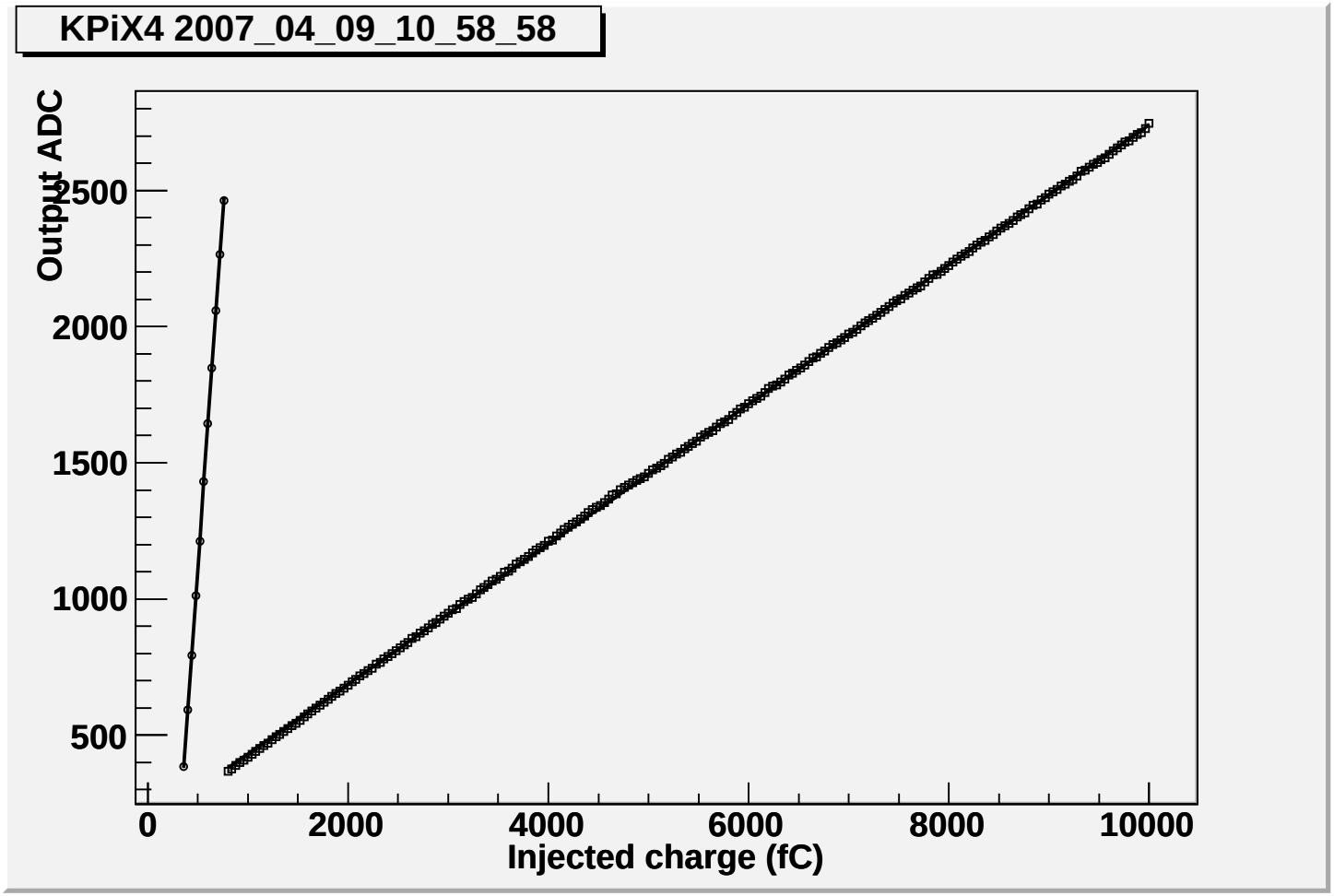
$$18\,\mathrm{mm} \times 6.5\,\mathrm{mm} \sim 1.2\,\mathrm{cm}^2$$

- Aspect ratio helps in routing traces on silicon boards
- Could not reduce chip size without making bump bounding more difficult

Overall chip size close to optimal

Performance – 64 channel prototype

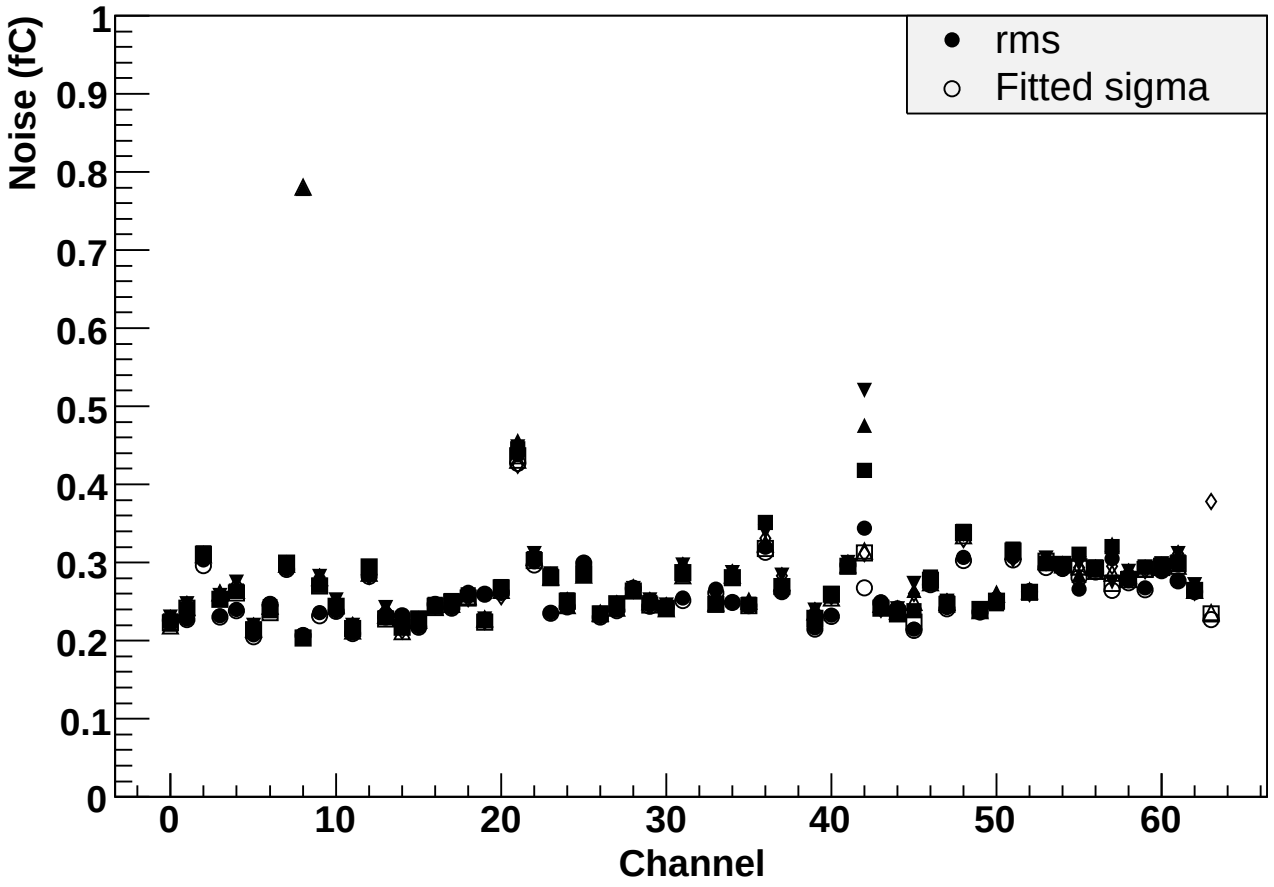
Range switching feature works as designed



Linear behavior extends to 10 pC

(Nonlinear behavior extends range by 50% or more)

Noise in the digitized charge value (with modest capacitive load)

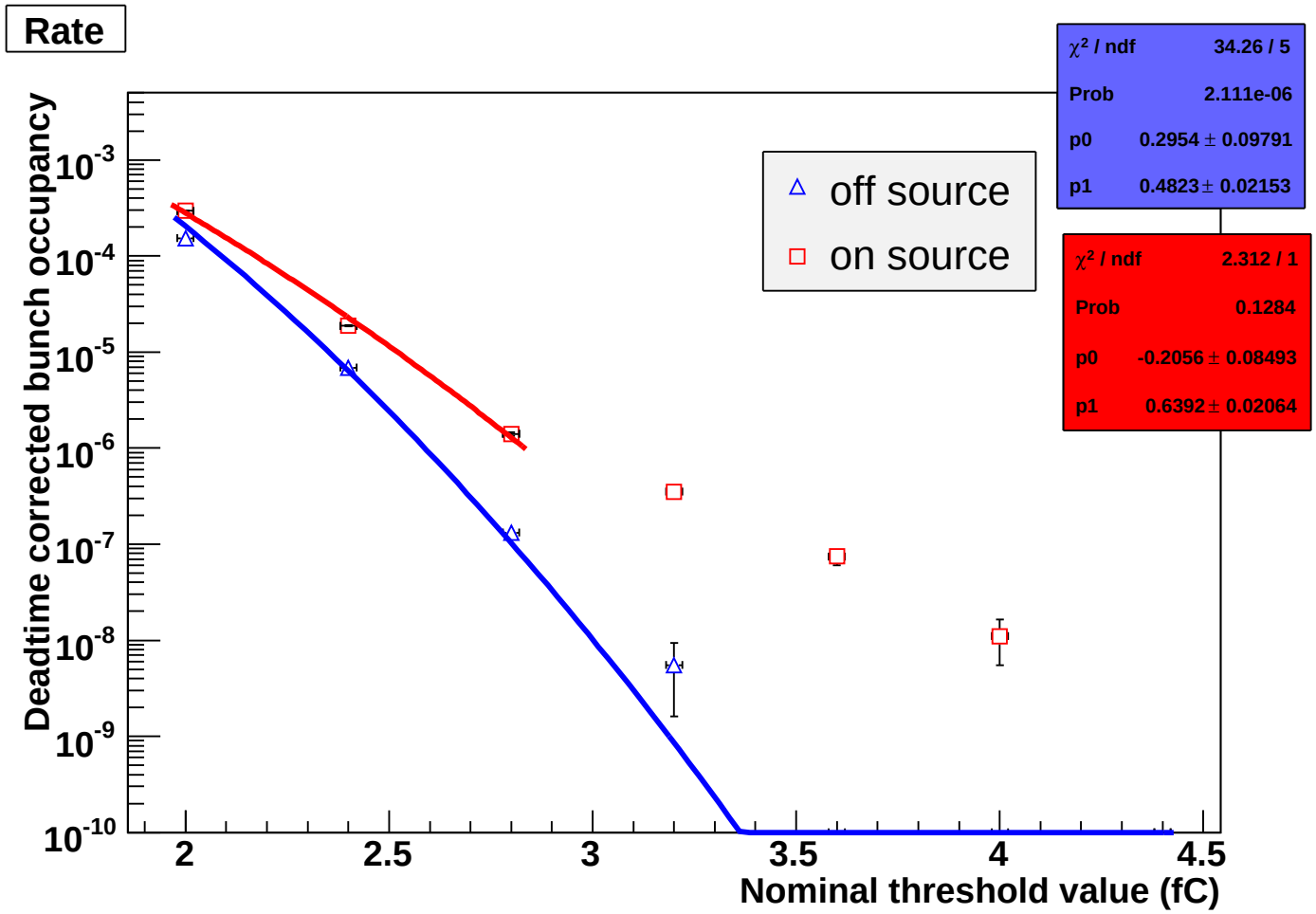


Different symbols correspond to the four buffers on each channel

- Meets spec of signal noise 8:1 for MIPs in ECAL
- Tracker would like signal to noise of 20:1

Performance adequate for externally triggered ECAL test beam

Self triggering with and without Am source (2.6 fC)



- **Noise is Gaussian over a large range (fit to erfc)**
- **Can easily set trigger at $\frac{1}{2}$ MIP (1.9 fC)**

Plans

- Continue testing KPiX 4
  $\Rightarrow$ Silicon at SLAC, Oregon and GEMs at UT - Arlington)

- Submit KPiX 5 (64 or 128 channels) in early summer, main features:
  - Optimized default shaping time for trigger and reset inhibit
  - Improve biasing of MOS capacitors in threshold circuit
  - Add additional power bus for comparators
  - Remove some temporary diagnostic connections

Possible submission of KPiX 1024 this fall