Control/LLRF WBS plans and status at KEK

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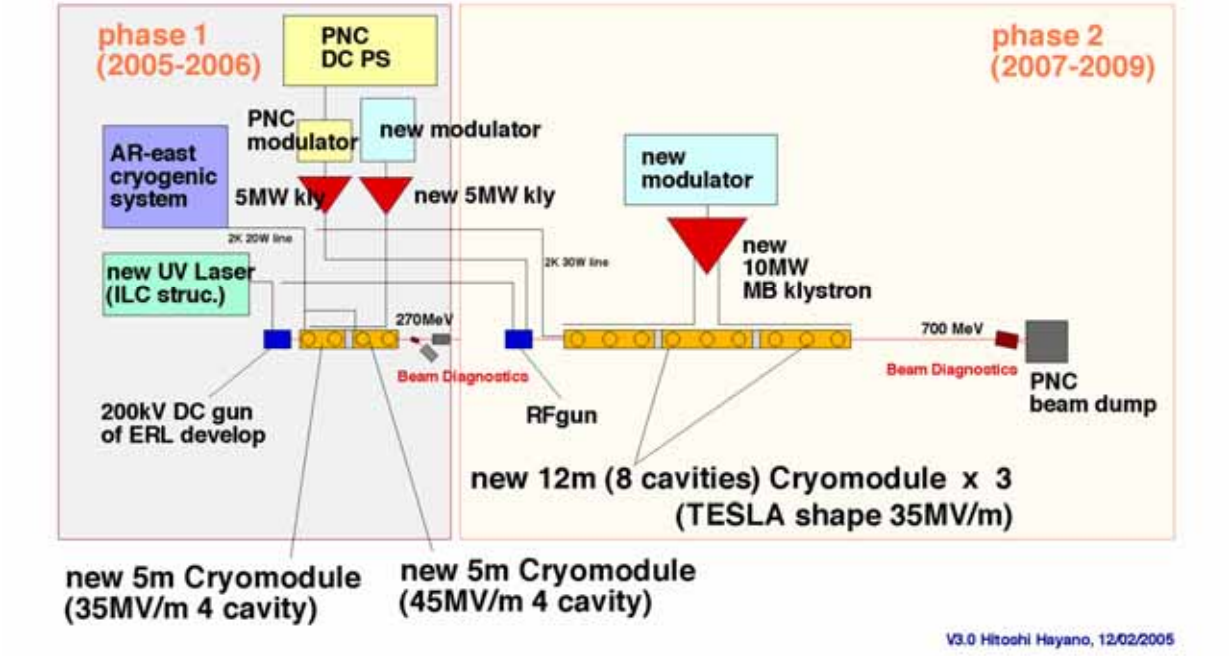
STF schedule

- LLRF group in KEK works mainly for the STF support (S2).

	feature	construction	operation	HLRF	LLRF
STF-0.5	2 cavities	-2007	July,2007	#1 mod.	cPCI
STF-1	8 cavities+ gun	-2008	2008	#2 mod.	cPCI
STF-2	26 cavities+ gun	-2010	2010	#2 or #3 mod.	ATCA (?)

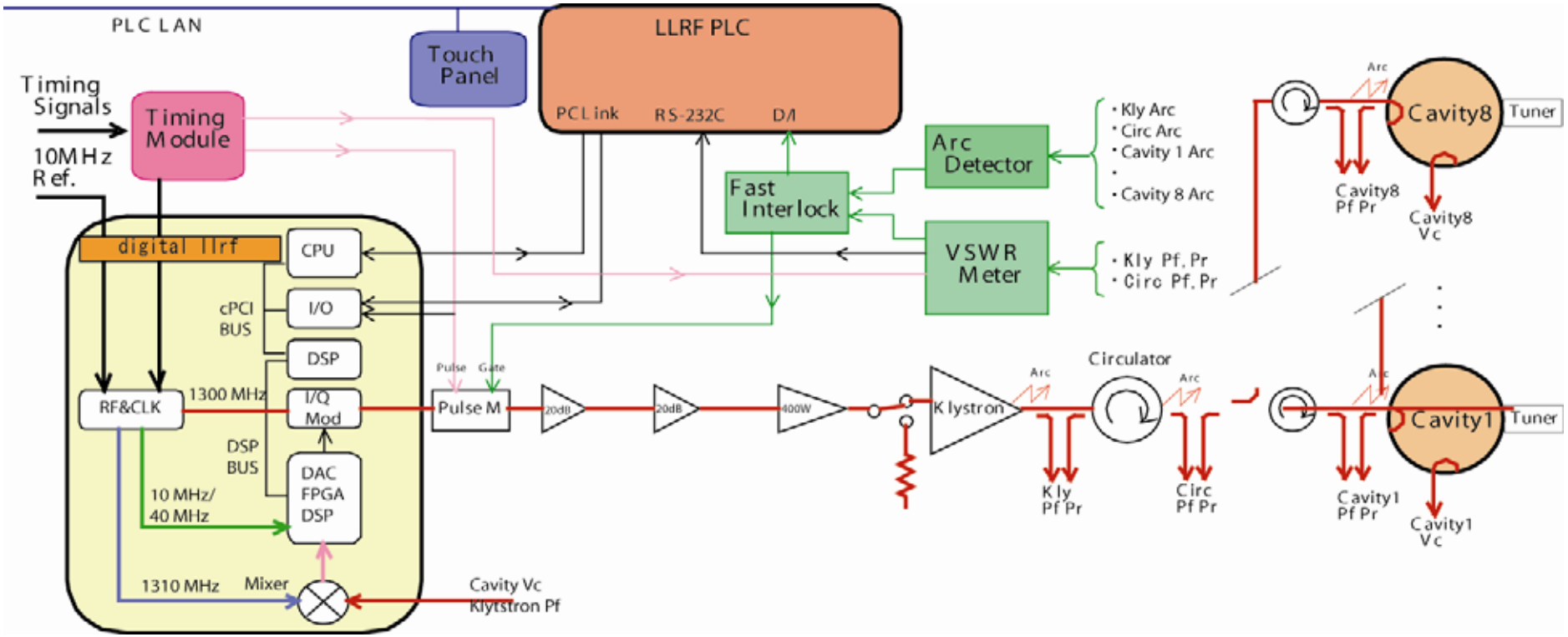


Work package

- Current work package at KEK llrf/control (JFY2007)
  - ***S2:llrf system for STF modulator #1:drive 2 cavities***
  - ***S2:llrf system for STF modulator #2:kly test & can drive 26 cav.***
  - **S2: LLRF network server and EPICS installation**
  - **R&D for ILC**
    - FPGA interlock system
    - Arc detector
    - IF-mixture
- Future work package(JFY2008-)
  - **S2: FPGA board with 32ch ADCs (ATCA or AMC)**
  - **ATCA/uTCA evaluation**
  - **S2: llrf system for STF modulator #3**

LLRF system for STF

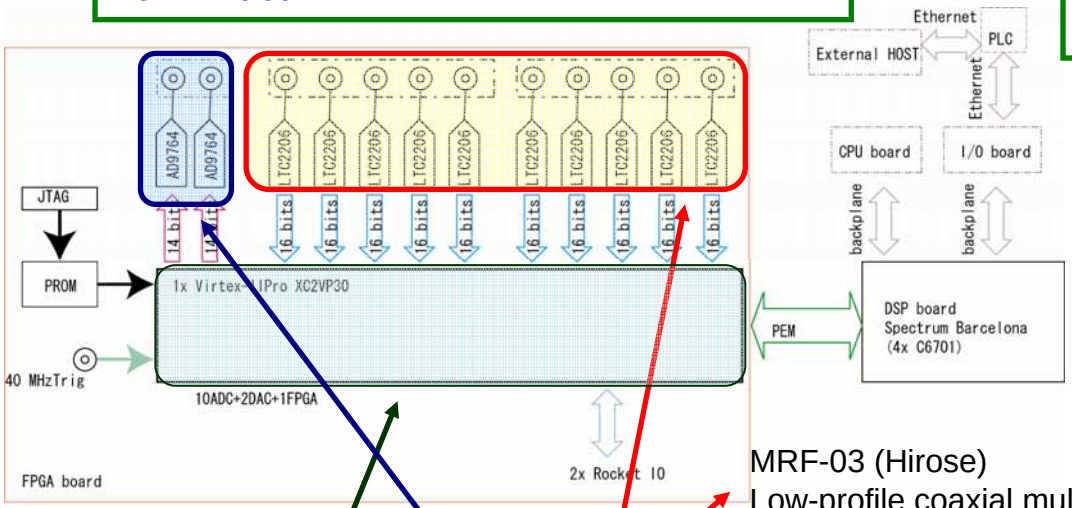
- LLRF system is based on J-PARC proton linac.
- The main parts are PLC, FastInterlock and digital FB.
- PLC manages all on/off and communicates with control room.
- FastInterlock detects such as Arc discharge and stop rf.



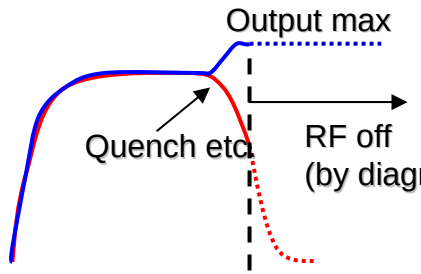
FPGA & DSP boards @STF Phase1

Custom FPGA board
: Mezzanine card of the commercial DSP board
10 **16bit-ADCs** and 2DACs + 2Rocket IO
40 MHz clock

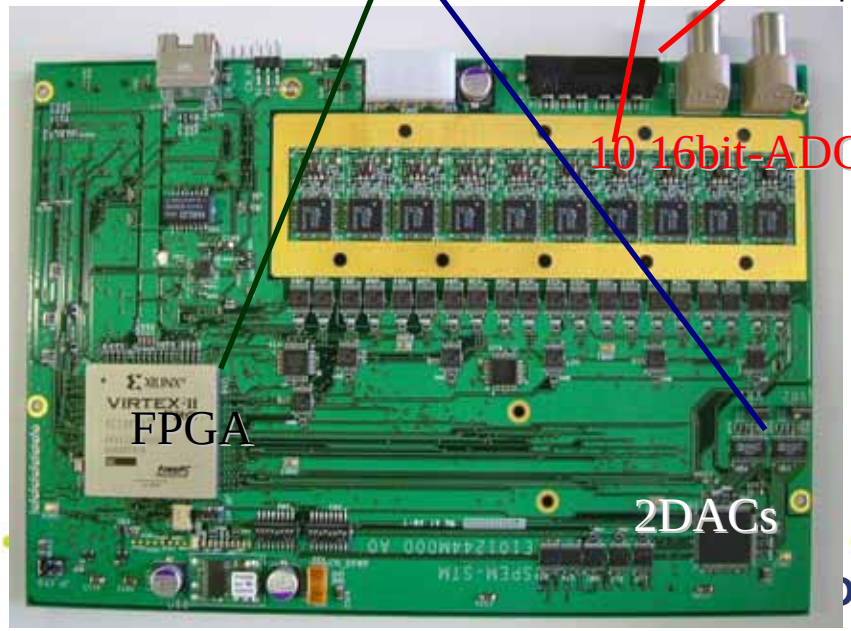
Commercial DSP board (Barcelona)
(same to J-PARC system)
:4x TI C6701 DSPs
Can access to FPGA like an external memory of DSP

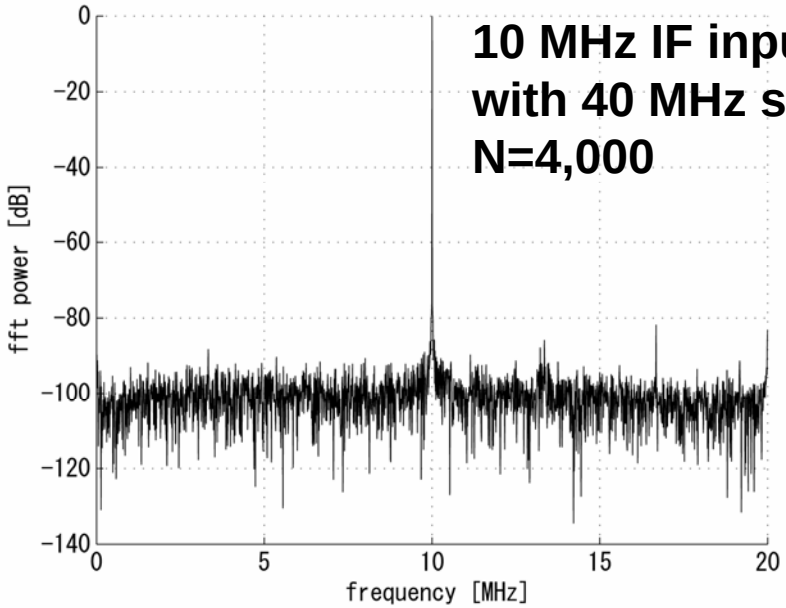


Real time intelligent diagnostics by DSP board

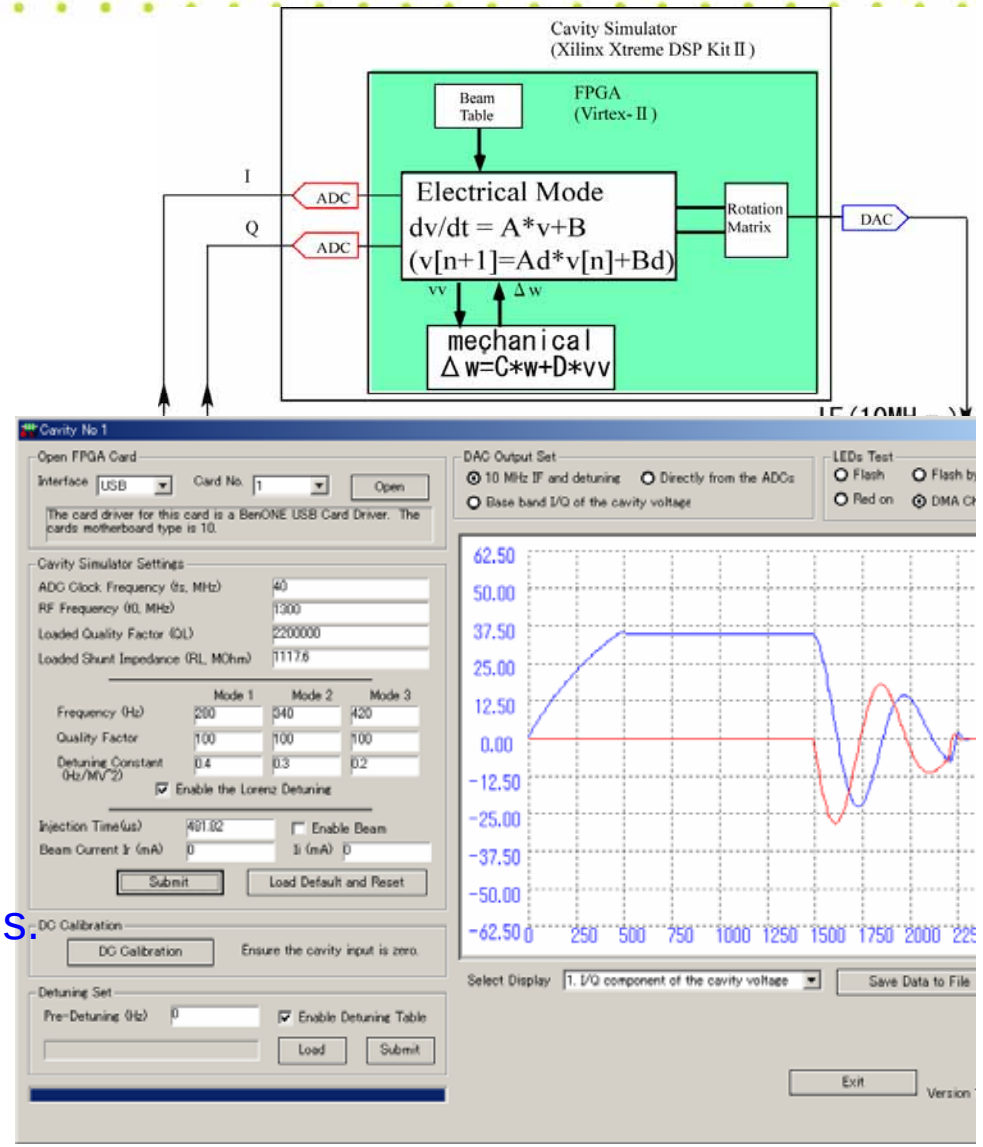


MRF-03 (Hirose)
Low-profile coaxial multiple contact connector



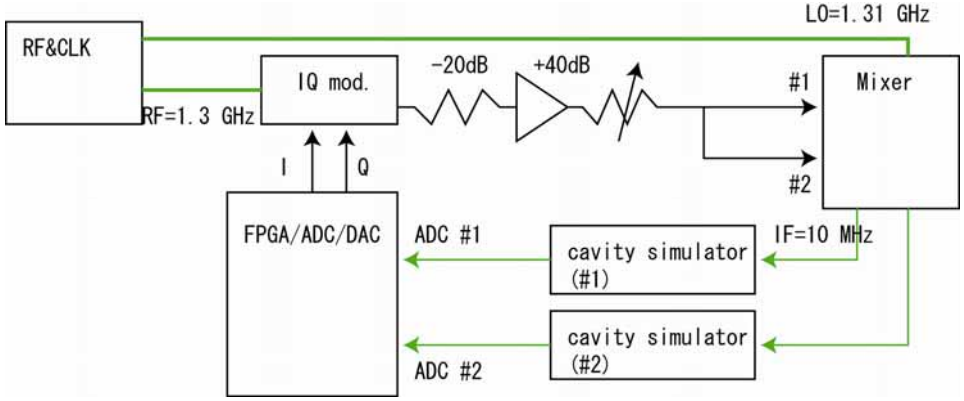


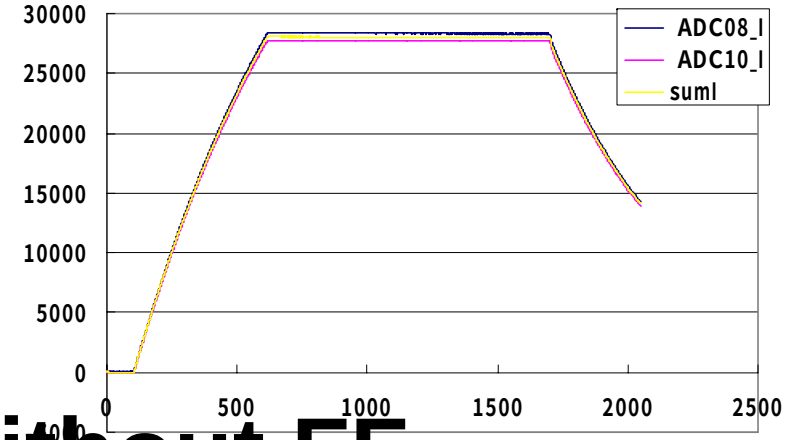
Cavity simulators installed into PC



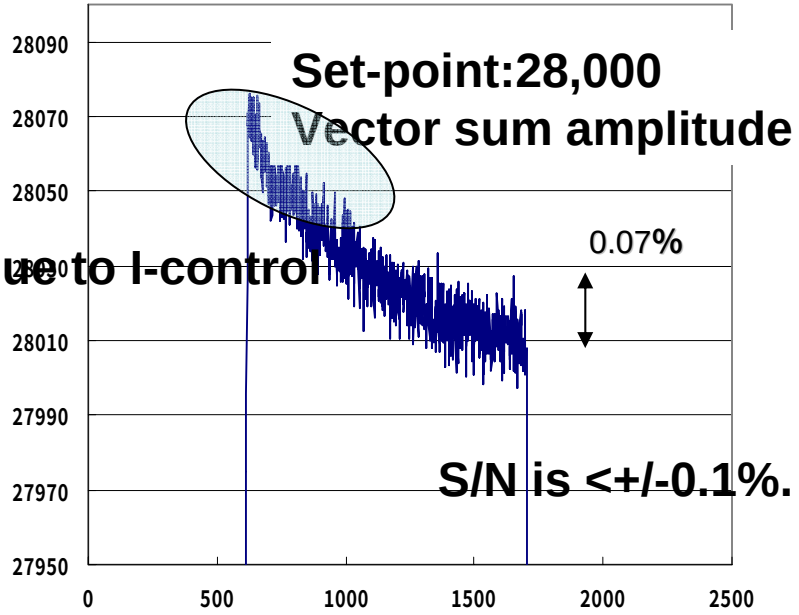
- XtremeDSP was used for cavity simulator.
- Four XtremeDSPs are installed into PCI bus. (corresponding 4 cavity simulators)

FB results 1



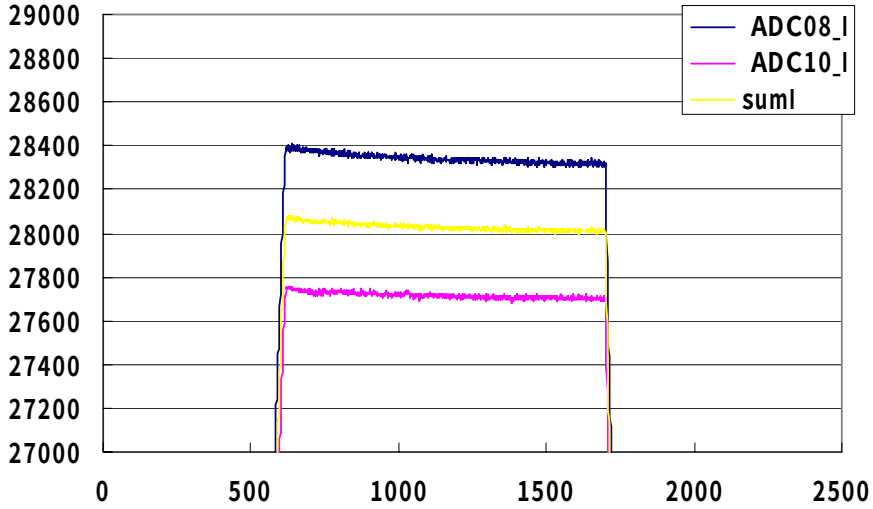


PI-control without FF

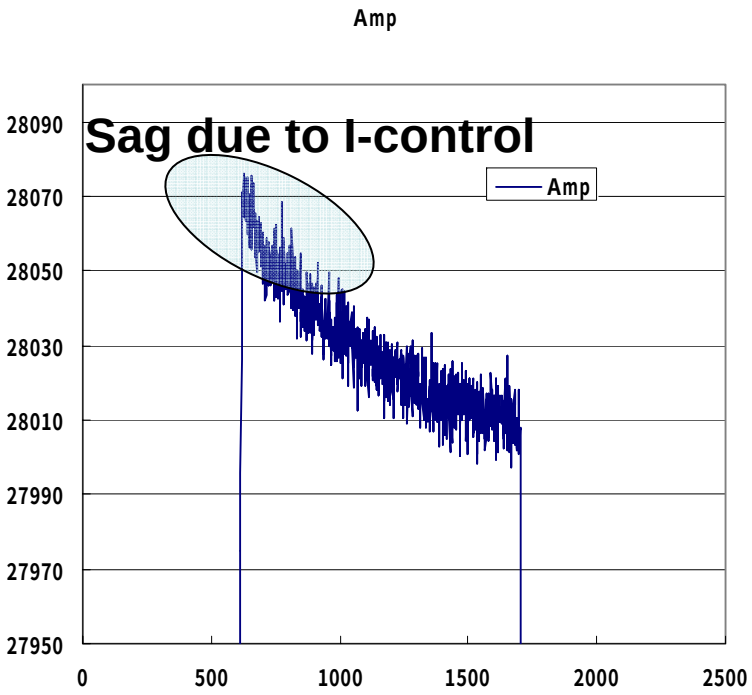


Sag due to I-control

S/N is <+/-0.1%.

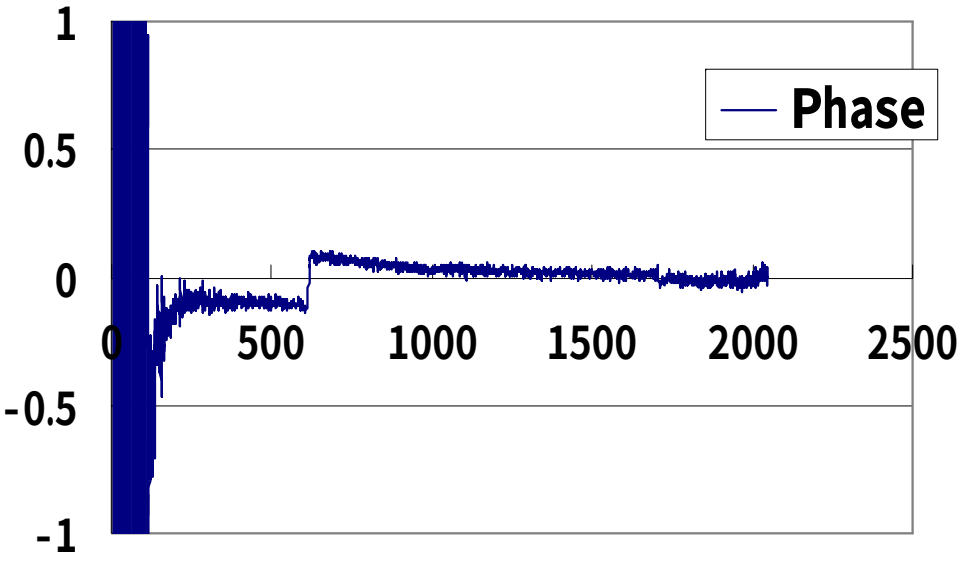


FB results 2



Set-point:28,000
Vector sum amplitude

Set-phase: 0 deg.
Vector sum phase



Phase stability is <+/-0.1 deg.

Work package

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  - **llrf system for STF modulator #1:drive 2 cavities**
  - **llrf system for STF modulator #2:kly test & can drive 26 cav.**
  - ***LLRF network server and EPICS installation***
  - **R&D for ILC**
    - FPGA interlock system
    - Arc detector
    - IF-mixture
- Future work package(JFY2008-)
  - **FPGA board with 32ch ADCs (ATCA or AMC)**
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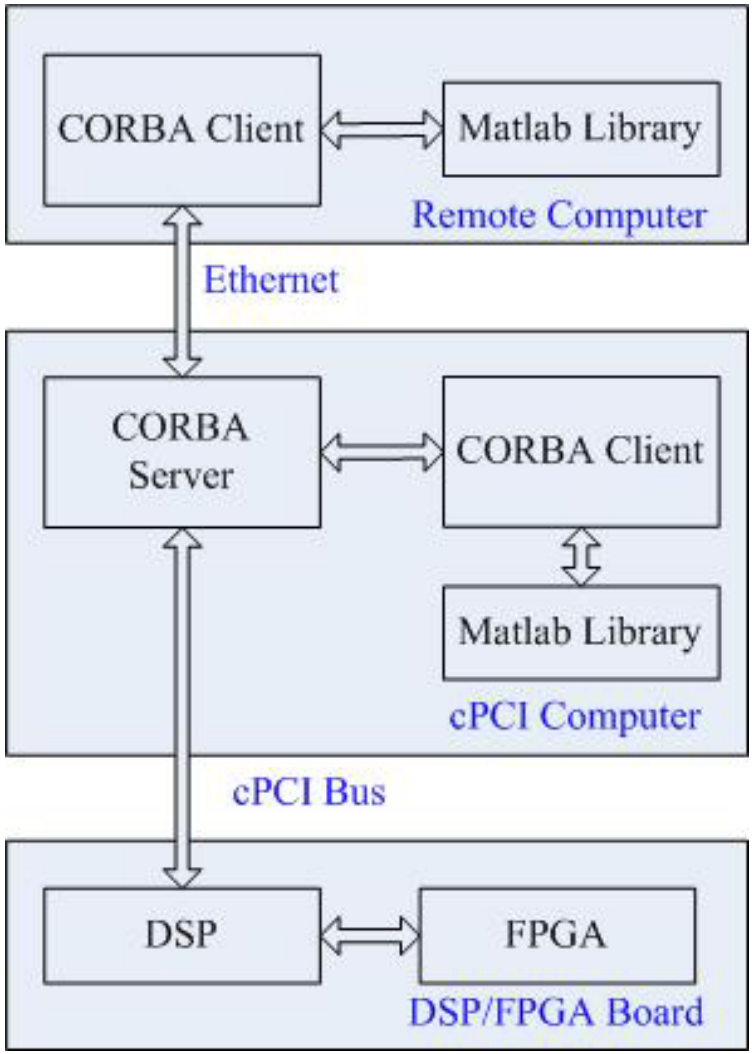
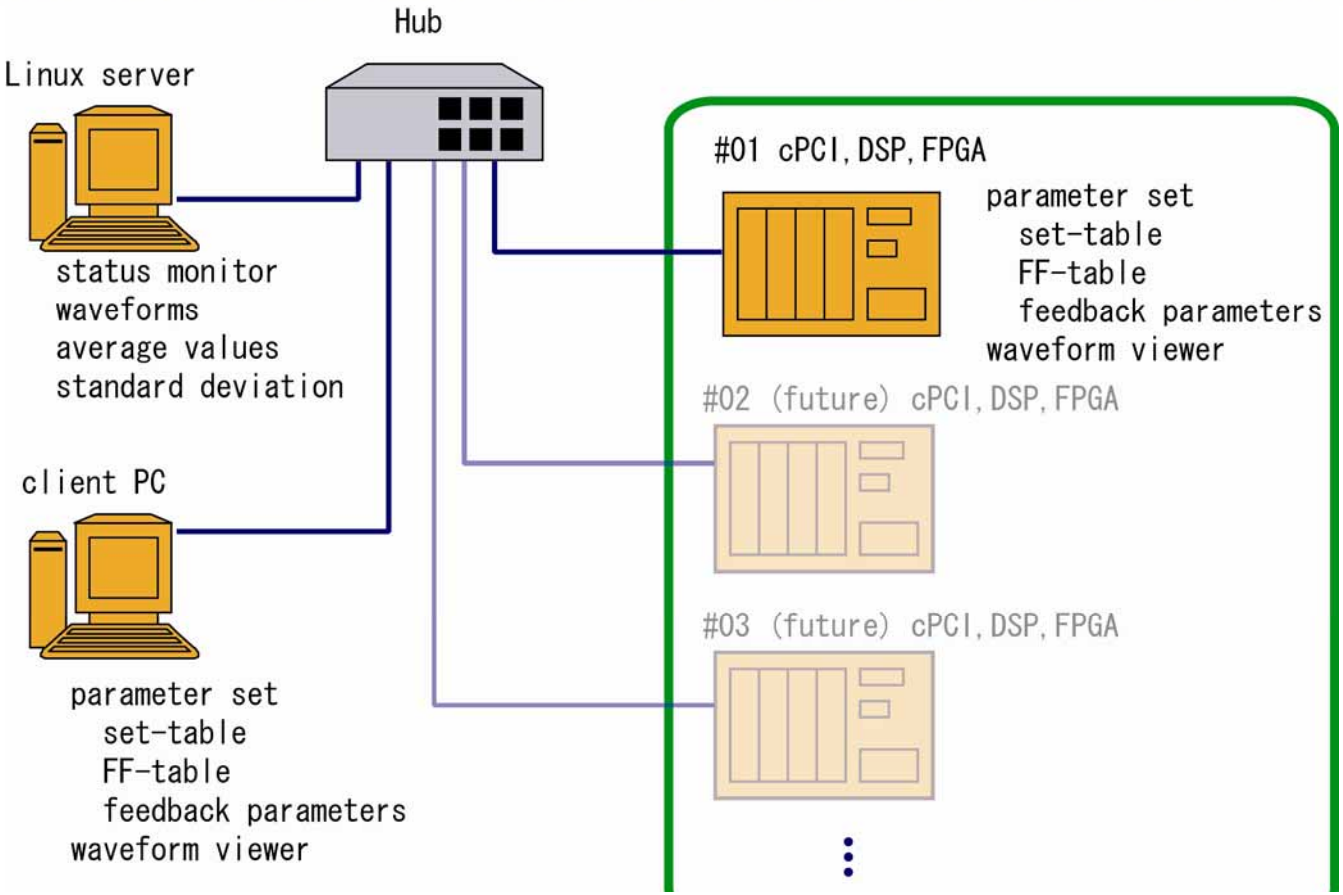
LLRF control by CORBA



- CORBA is used as a platform for developing distributed control software
- Client PC can access to FPGA through CORBA
- Matlab library is used to read the DSP data directly into Matlab workspace, so that it can be further analyzed with the strong tools provided by Matlab.
- Combine the CORBA client function into MEX library, we can access the CORBA server directly in Matlab.

LLRF data acquisition network



- Some cPCIs can be connected this network
- Status is monitored at Linux server
- Waveforms and average data are stored in Linux server.
- Client PC can change FB parameters and can monitor waveform.
- cPCI will be EPICS IOC this year.

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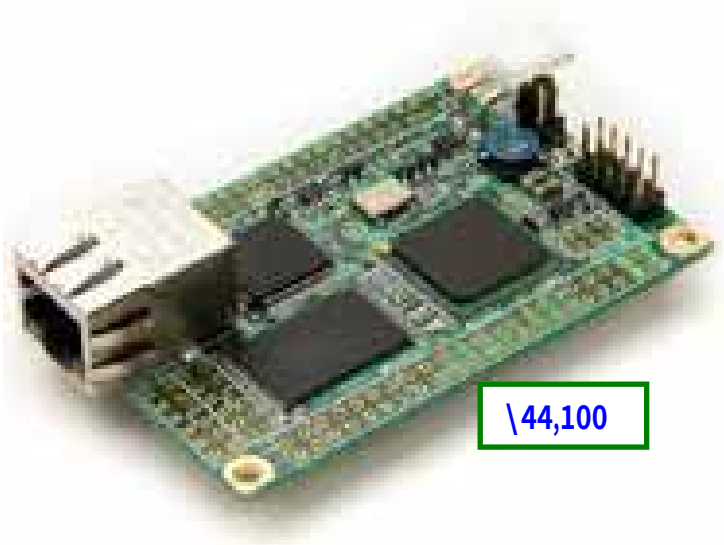
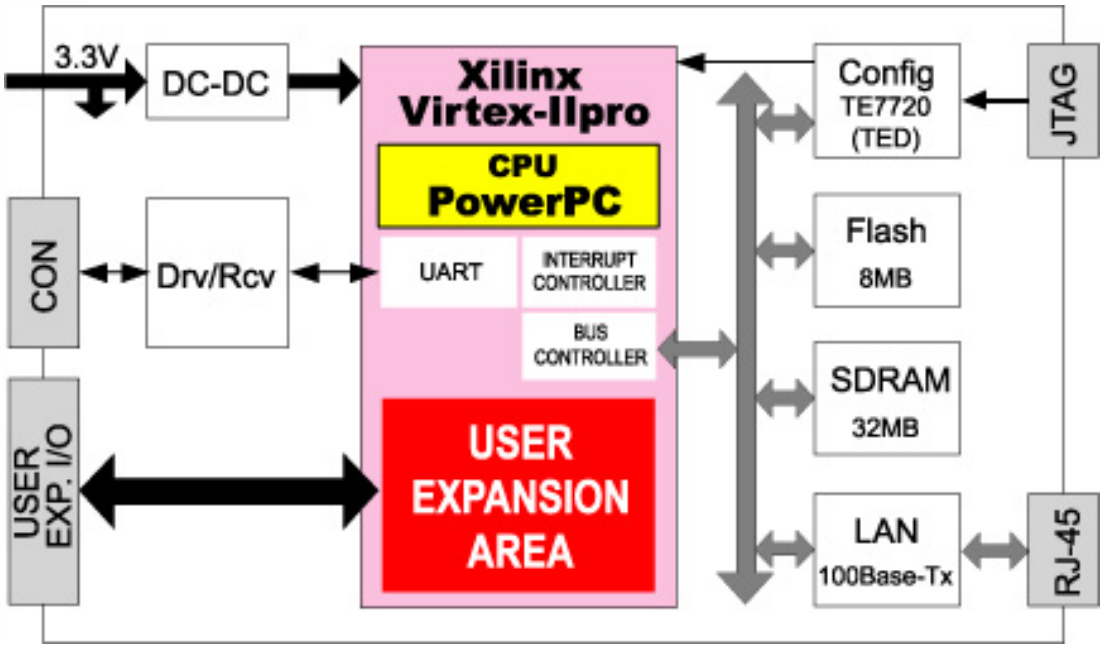
FPGA interlock system

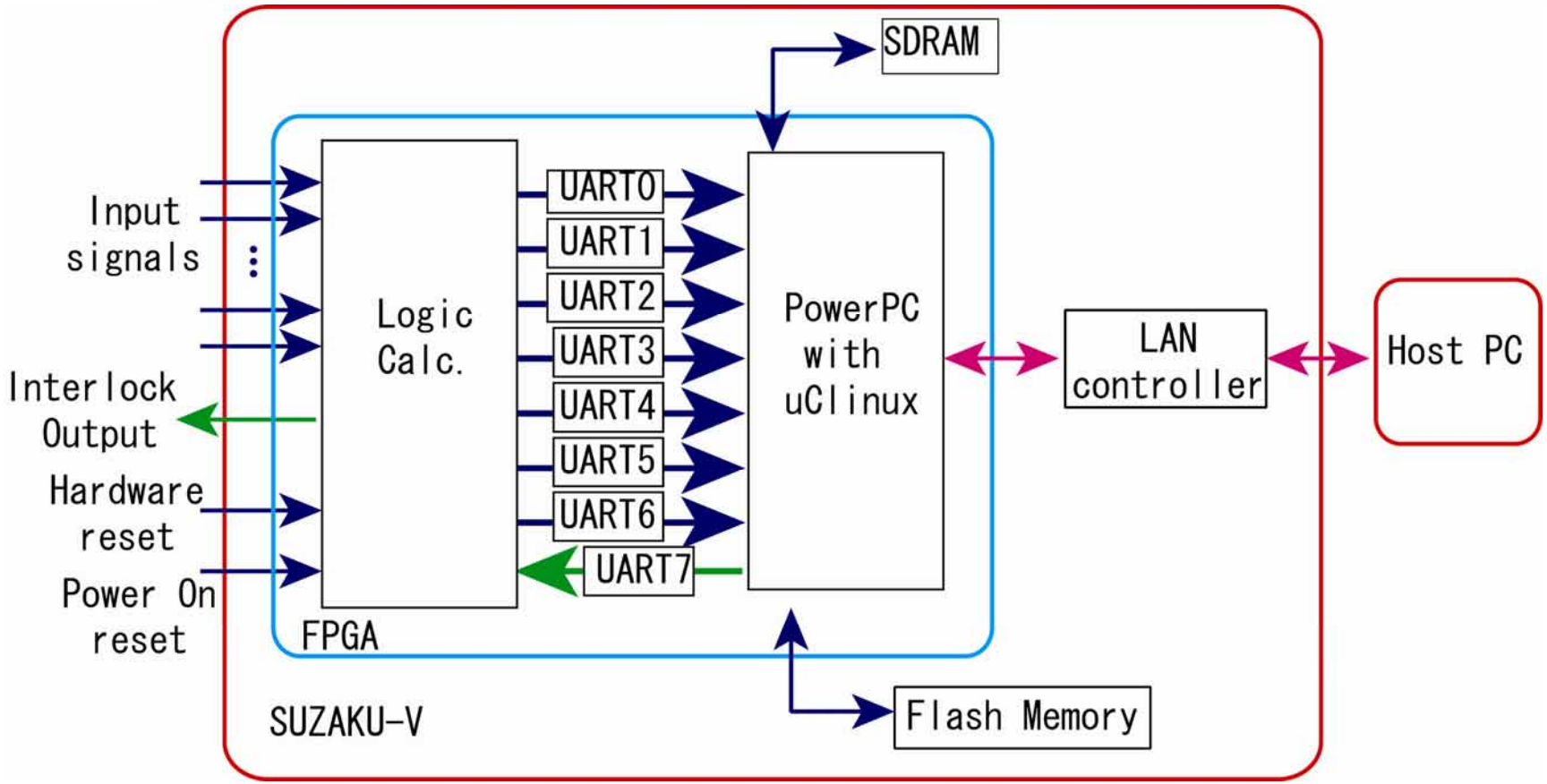
SUZAKU-V (SZ310-U00) by ATMARK TECHNO
FPGA(XC2VP4) with 70 I/O and LAN
OS: Linux
MPS by FPGA and monitor by Ethernet





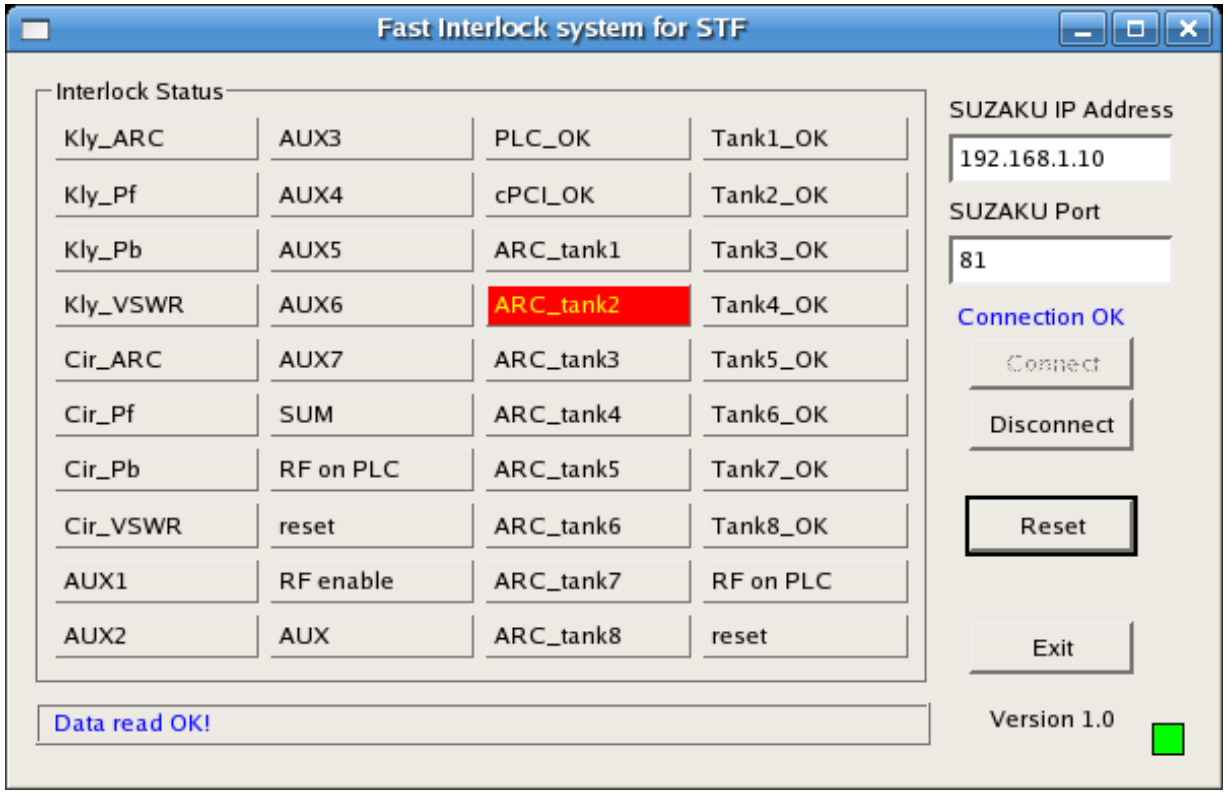
Cheap commercial FPGA card instead of PLC and touch pannel

Interlock system inside FPGA



- Interlock logic was calculated (simple ‘or’ logic) and send the output in 20us.
- The status can be monitored from another PCs via PowerPC inside FPGA.

1. Xilinx EDK provides some API functions and libraries for driver development.
2. Socket server and client program with TCP protocol.
3. GUI program for monitor the interlock status or reset it.



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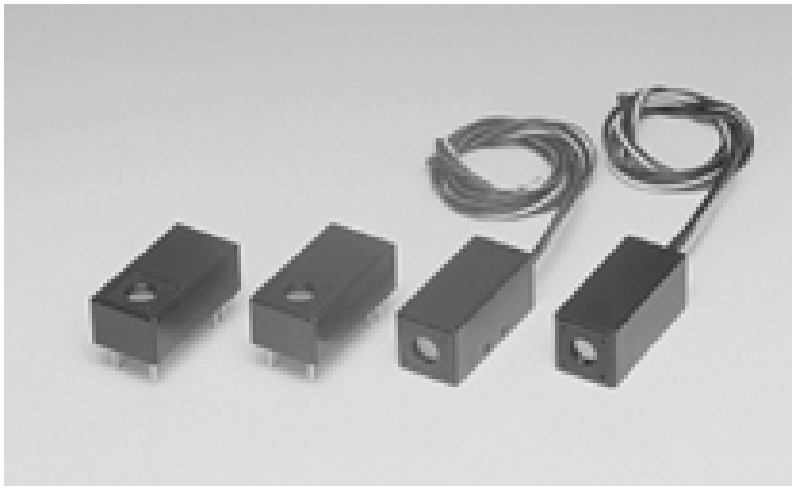
Arc detection

- Conventional arc detectors are photo-coupler with thick optical fiber (such as 1 mm in diameter).
- Instead of this, we adopted high sensitive photosensor (H5783).
- Owing to the high sensitivity, we can use commercial multi-mode optical fiber (50 um in diameter)
- H5783 needs not HV supply



- Head on module using Metal package PMT Spectral response of 300nm - 650nm.
- Has no amp and uses a low power consumption HV supply
- Capable of detecting light levels 1/10000 as low as those detectable with semiconductor photodiodes.

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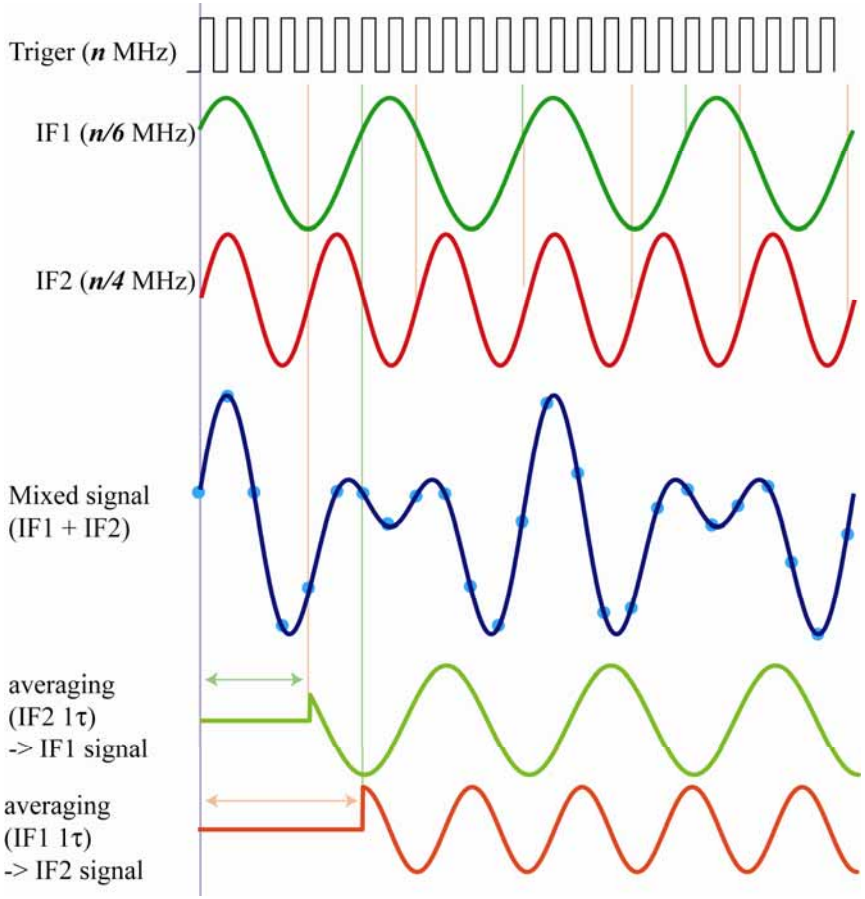
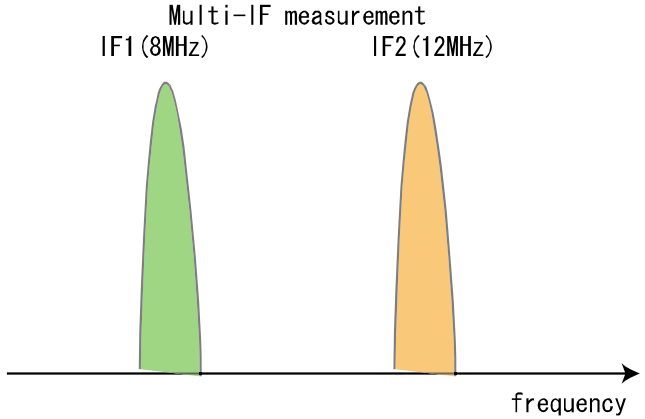
IF (intermediate frequency)-mixture

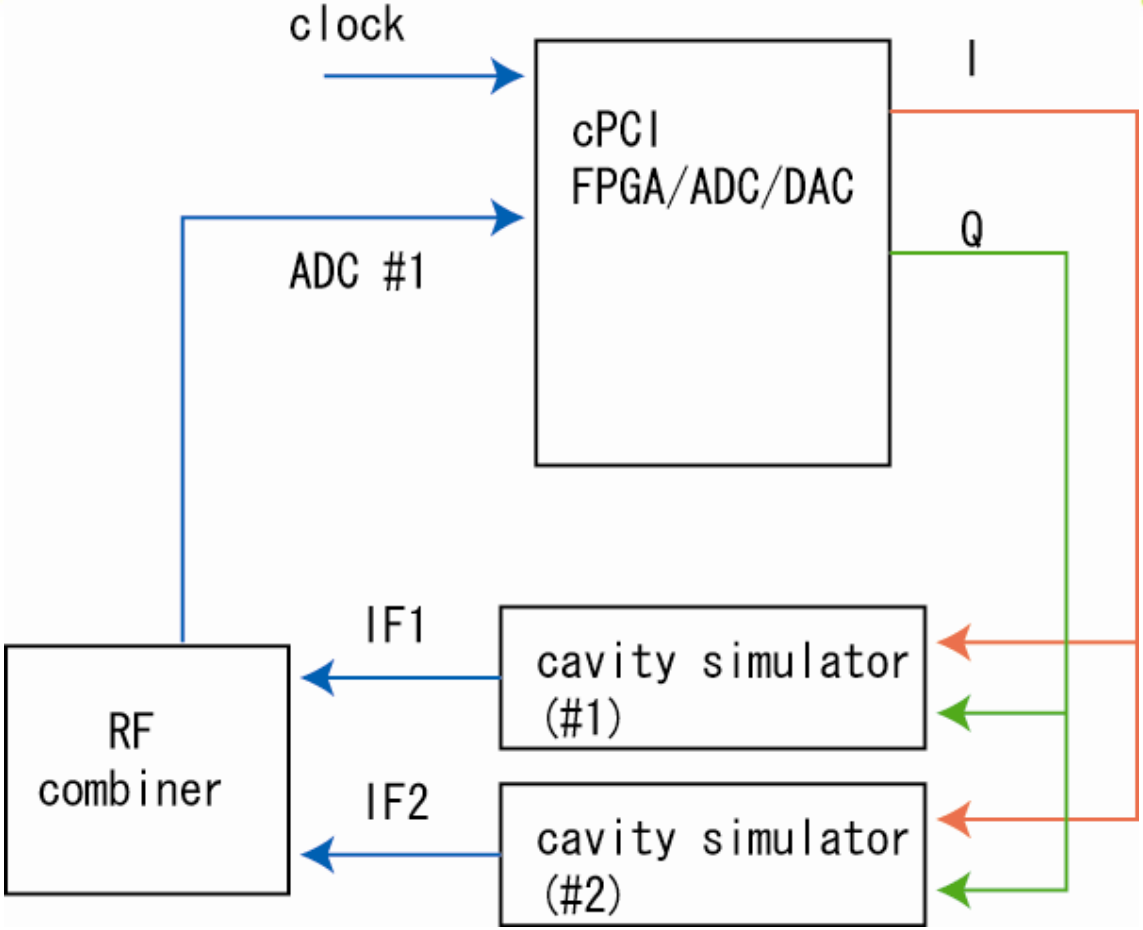


- Concept is like “digital receiver”
- Reduce the number of ADCs half or 1/3
- Two IF are mixed in analog.
- Two signals are separated by digital processing.



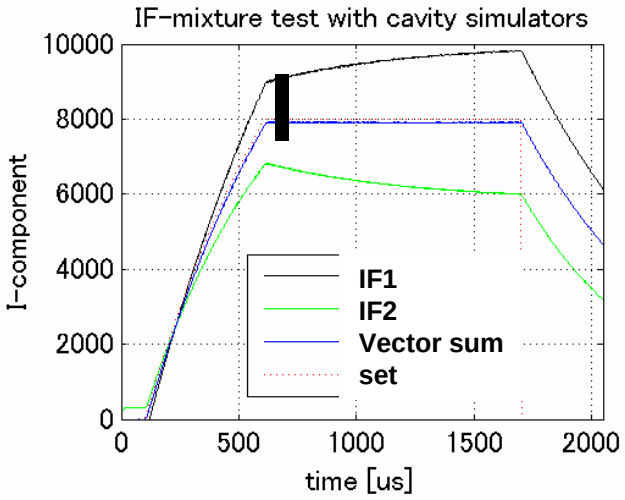
Possible IF selection @sampling *n* MHz
IF1: (n/6+nxk) MHz -> 8 MHz,56 MHz,104 MHz …(@48 MHz sampling)
IF2: (n/4+nxk’) MHz -> 12 MHz, 60 MHz, 108 MHz … (@48 MHz sampling)
Low IF will be durable for aperture jitter (@ same sampling rate)
but higher IF will be easier for clean LO generation

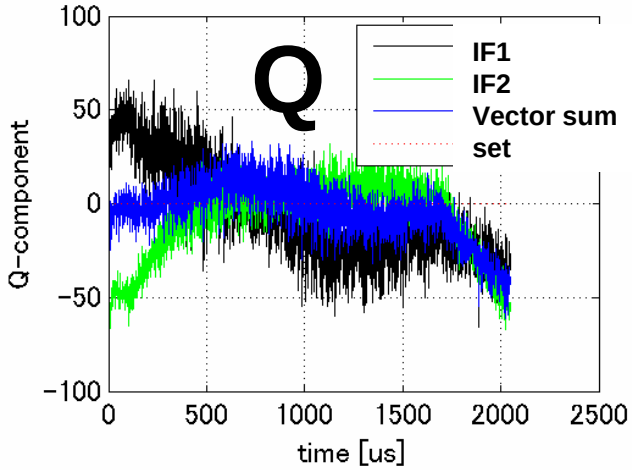
Experiments

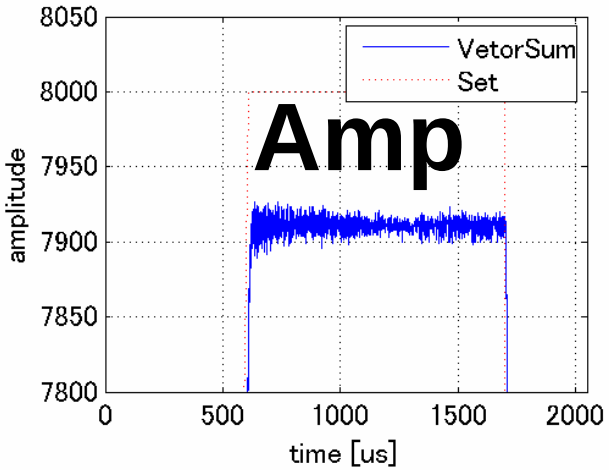


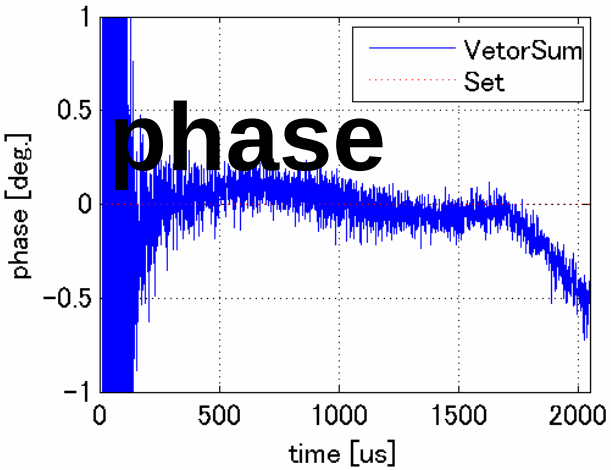
- Evaluation with two cavity simulators.
- Simple algorithm to remove other IF by averaging.

IF-mix performance (preliminary)









- Amplitude stability:<+/-0.2%
- Phase stability: <+/-0.2deg.
- @P-control (gain=100) without FF

JFY07 (Apr.07-Mar.08) plan

- Installation to #2 klystron test-station
- EPICS installation to cPCI (llrf station)
- Llrf data acquisitions to EPICS server

- Continued R&D works
  - **FPGA interlock system**
  - **Arc detector**
  - **IF-mixture**

Thank you