SCIPP R&D on Time-Over-Threshold Electronics and Long-Ladder Readout

LCWS 07 DESY

May 30 – June 3 2007

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Santa Cruz Institute for Particle Physics

The SCIPP/UCSC SiLC/SiD GROUP
(Harwdare R&D Participants)

Faculty/Senior	Post-Docs	Undergrads
Vitaliy Fadeyev	Jurgen Kroseberg	Greg Horn
Alex Grillo	Lei Wang	Luke Kelley
Bruce Schumm		Ian Horn
		Sean Crosby

Lead Engineer: Ned Spencer

Technical Staff: Max Wilder, Forest Martinez-McKinney

All participants are mostly working on other things (BaBar, ATLAS, biophysics…)

Students are undergraduate physics majors at UCSC

FOCUS AND MILESTONES

Goal: To develop readout generically suited to any ILC application (long or short strips, central or forward layers)

Current work focused on long ladders (more challenging!):

- Front-end electronics for long (~1 meter) ladders
- Exploration of sensor requirements for long ladders
- Demonstration (test-beam) of < 10 μm resolution mid-2008

After long-ladder proof-of-principle, will re-optimize (modest changes) for short-ladder, fast-rate application

We also hope to play an increasing role in overall system development (grounding/shielding, data transmission, module design and testing) as we have on ATLAS and GLAST

BRIEF SUMMARY OF STATUS

Testing of 8-channel (LSTFE-1) prototype fairly advanced:

- Reproducible operation (4 operating boards)
- Most features working, with needed refinements understood
- A number of "subtleties" (e.g. channel matching, environmental sensitivity) under control
- Starting to make progress on fundamental issues confronting long-ladder/high-resolution limit.

Design of 128-channel prototype (LSTFE-2) well underway (July submission)

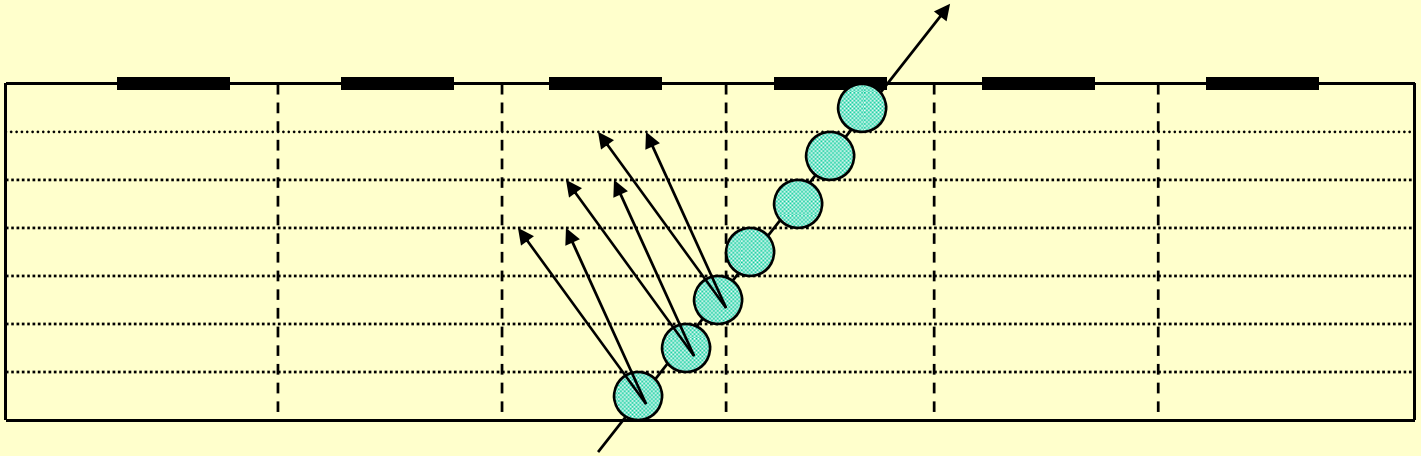
Now for the details…

Pulse Development Simulation

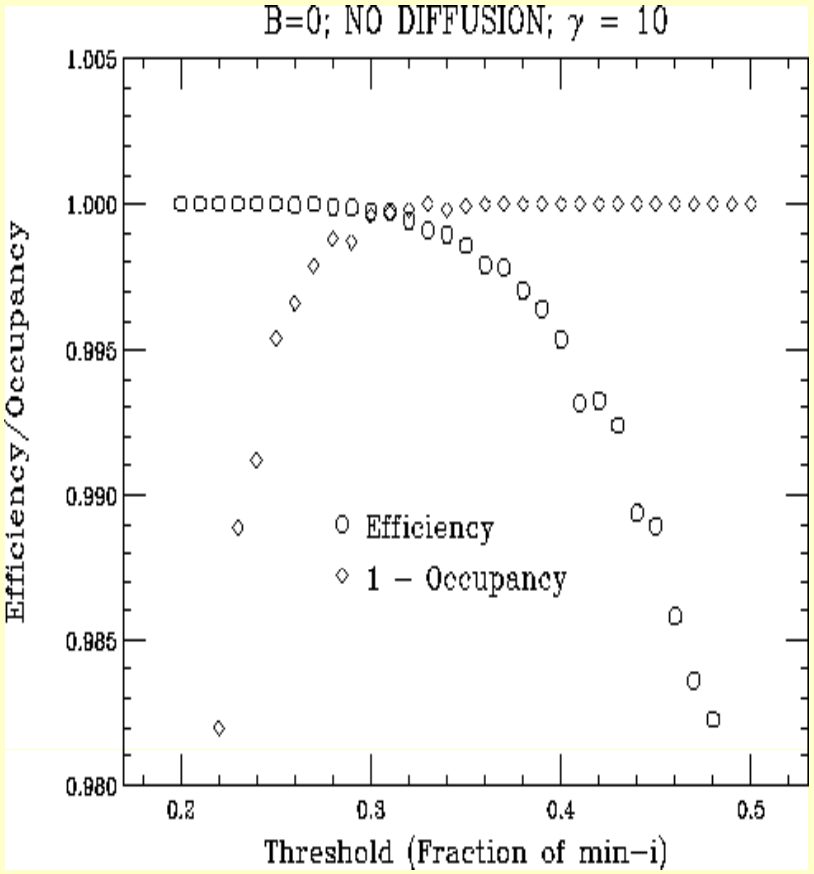
Christian Flacco & Michael Young (Grads); John Mikelich and Luke Kelley (Undergrads)

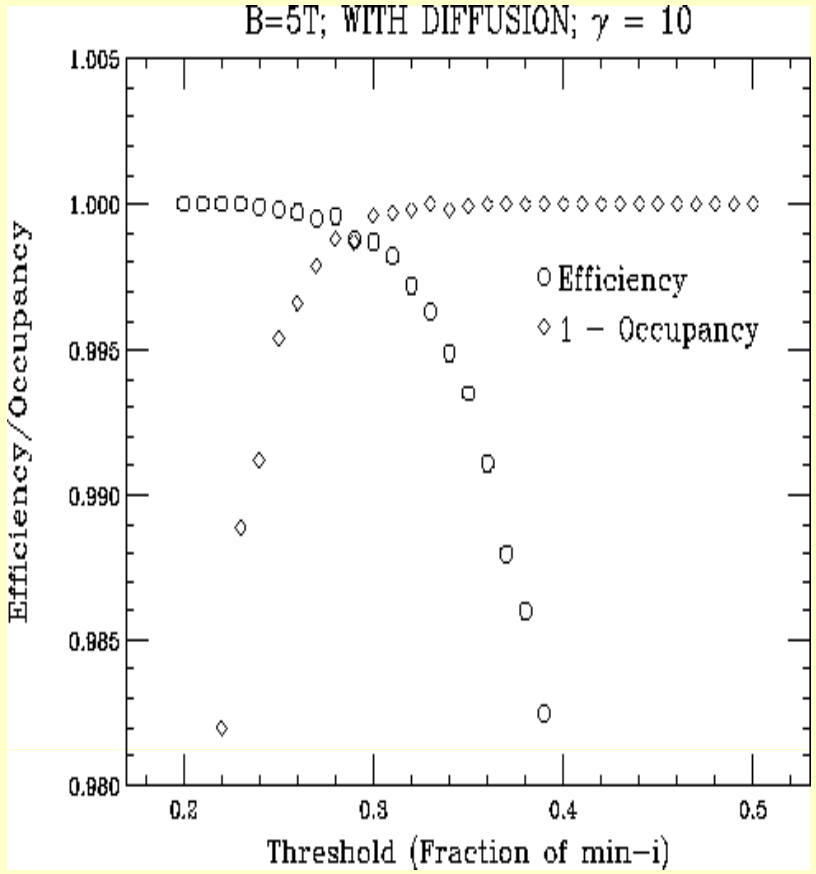
Long Shaping-Time Limit: strip sees signal if and only if hole is collected onto strip (no electrostatic coupling to neighboring strips)

Include: Landau deposition (SSSimSide; Gerry Lynch LBNL), variable geometry, Lorentz angle, carrier diffusion, electronic noise and digitization effects



Simulation Result: S/N for 167 cm Ladder (capacitive noise only)

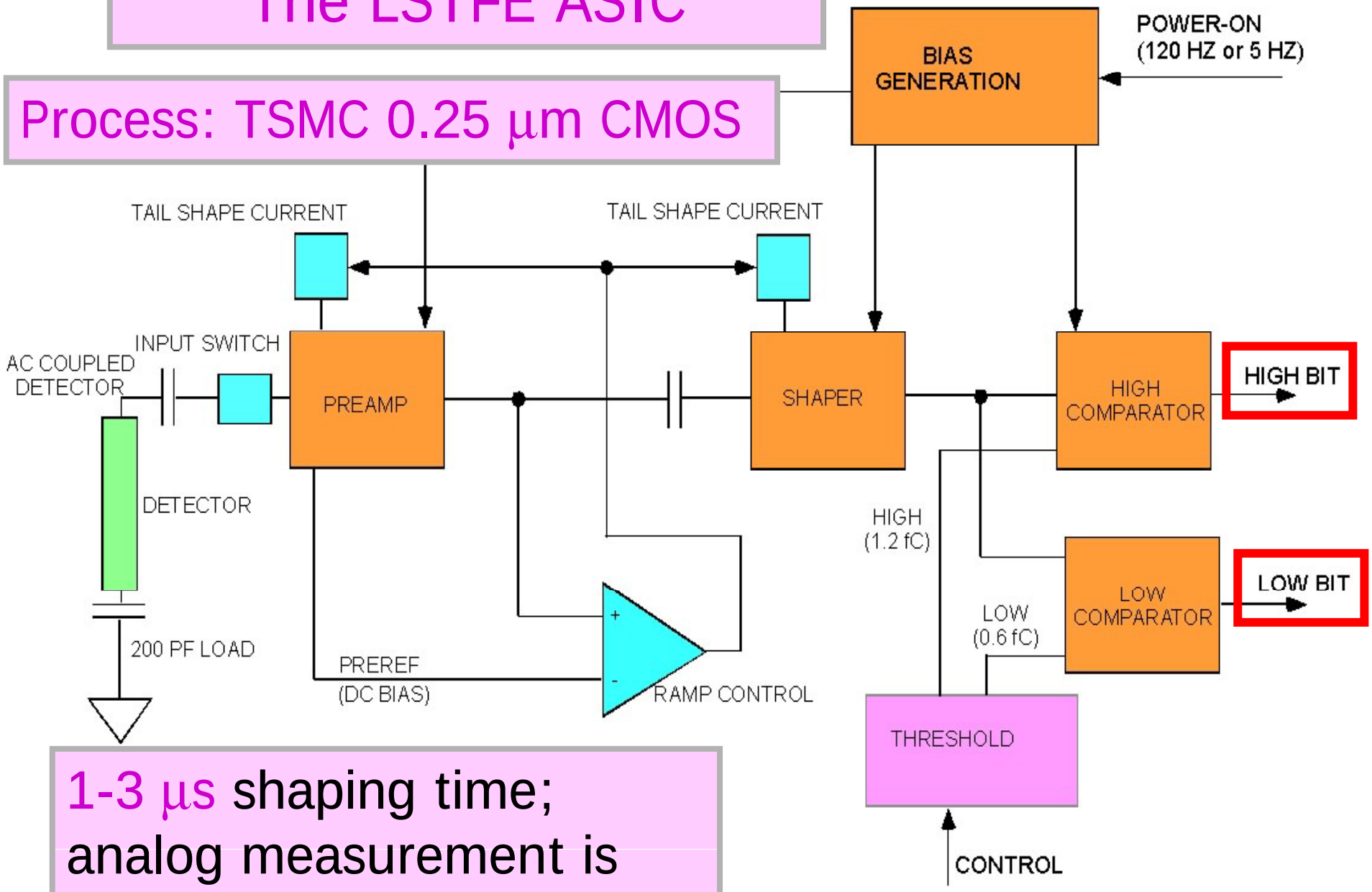




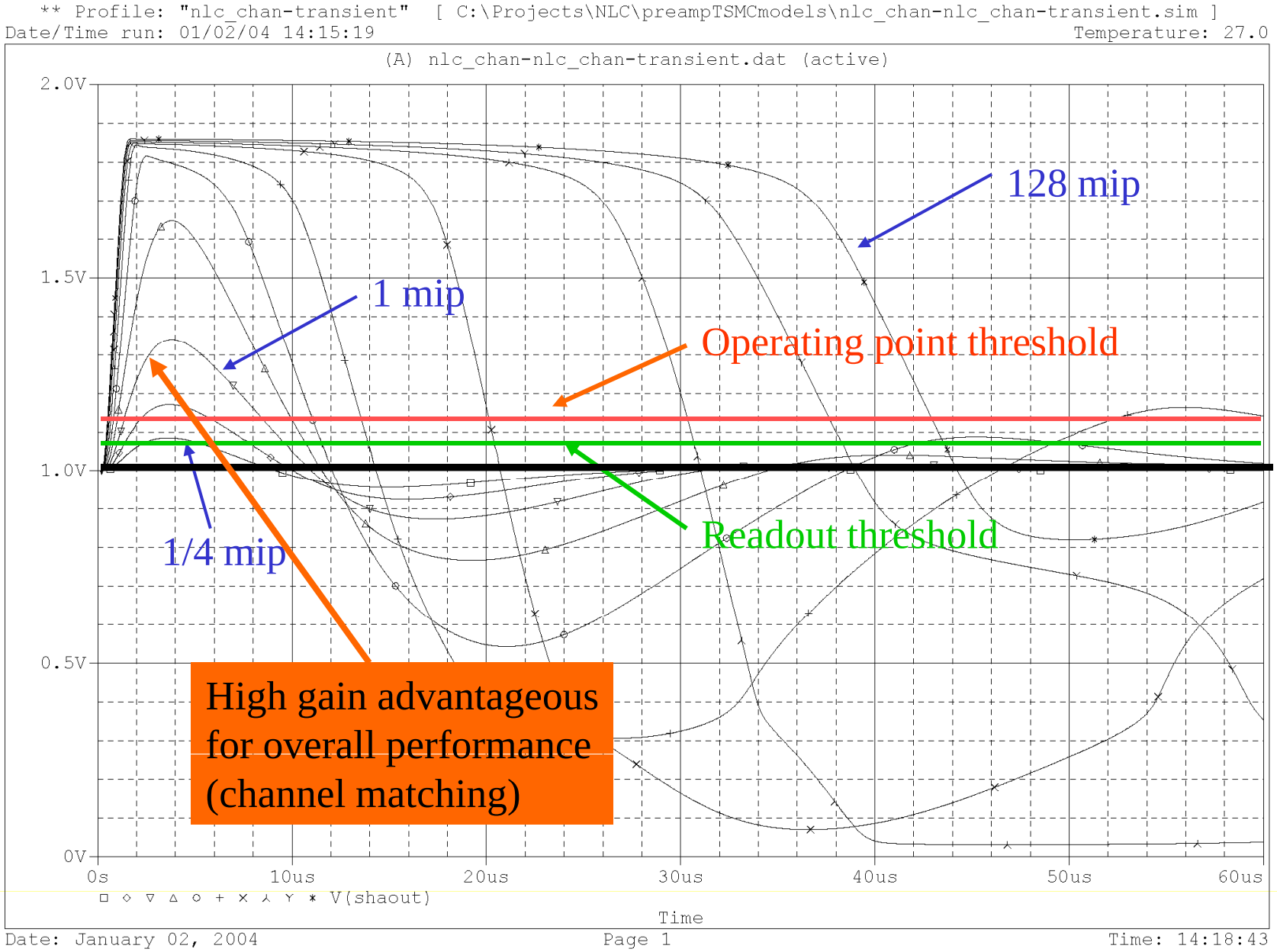
Simulation suggests that long-ladder operation is feasible

The LSTFE ASIC

Process: TSMC 0.25 μm CMOS



1-3 μs shaping time; analog measurement is Time-Over-Threshold


** Profile: "nlc_chan-transient" [C:\Projects\NLC\preampTSMCmodels\nlc_chan-nlc_chan-transient.sim]
Date/Time run: 01/02/04 14:15:19
Temperature: 27.0
(A) nlc_chan-nlc_chan-transient.dat (active)
2.0V
1.5V
1.0V
0.5V
0V
0s
10us
20us
30us
40us
50us
60us
Time
V(shaout)
128 mip
1 mip
1/4 mip
Operating point threshold
Readout threshold
High gain advantageous for overall performance (channel matching)
Date: January 02, 2004
Page 1
Time: 14:18:43

Electronics Simulation: Resolution

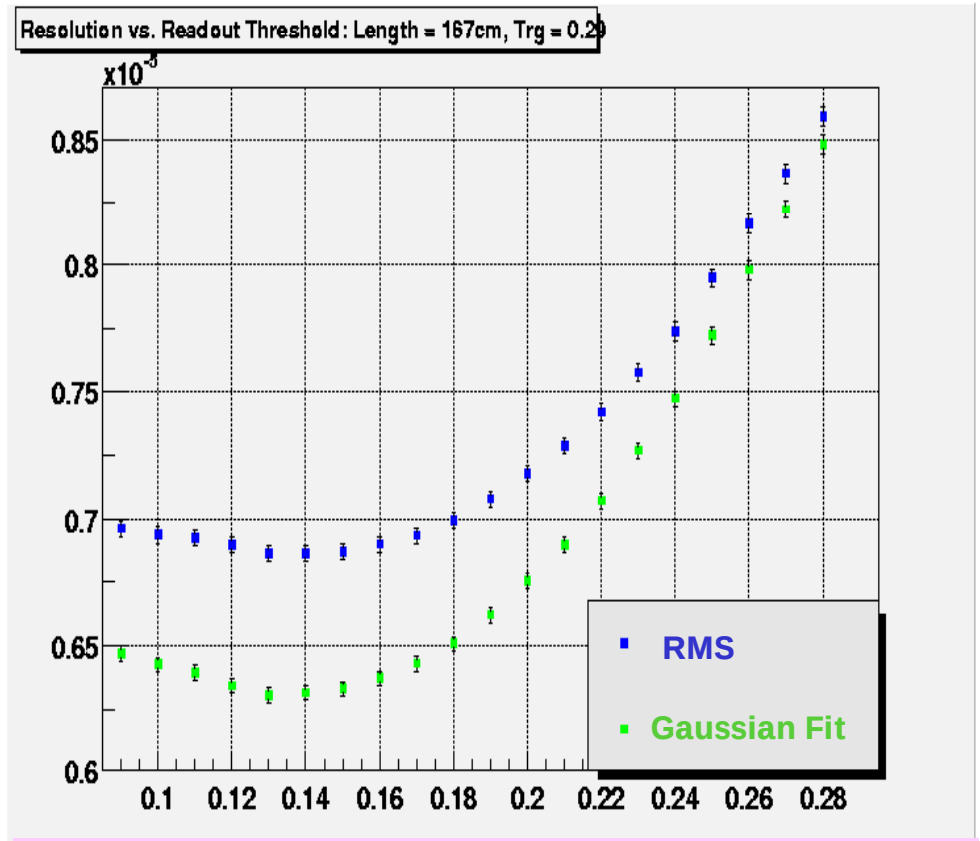
Detector Noise:

Capacitive contribution; from SPICE simulation normalized to bench tests with GLAST electronics

Analog Measurement:

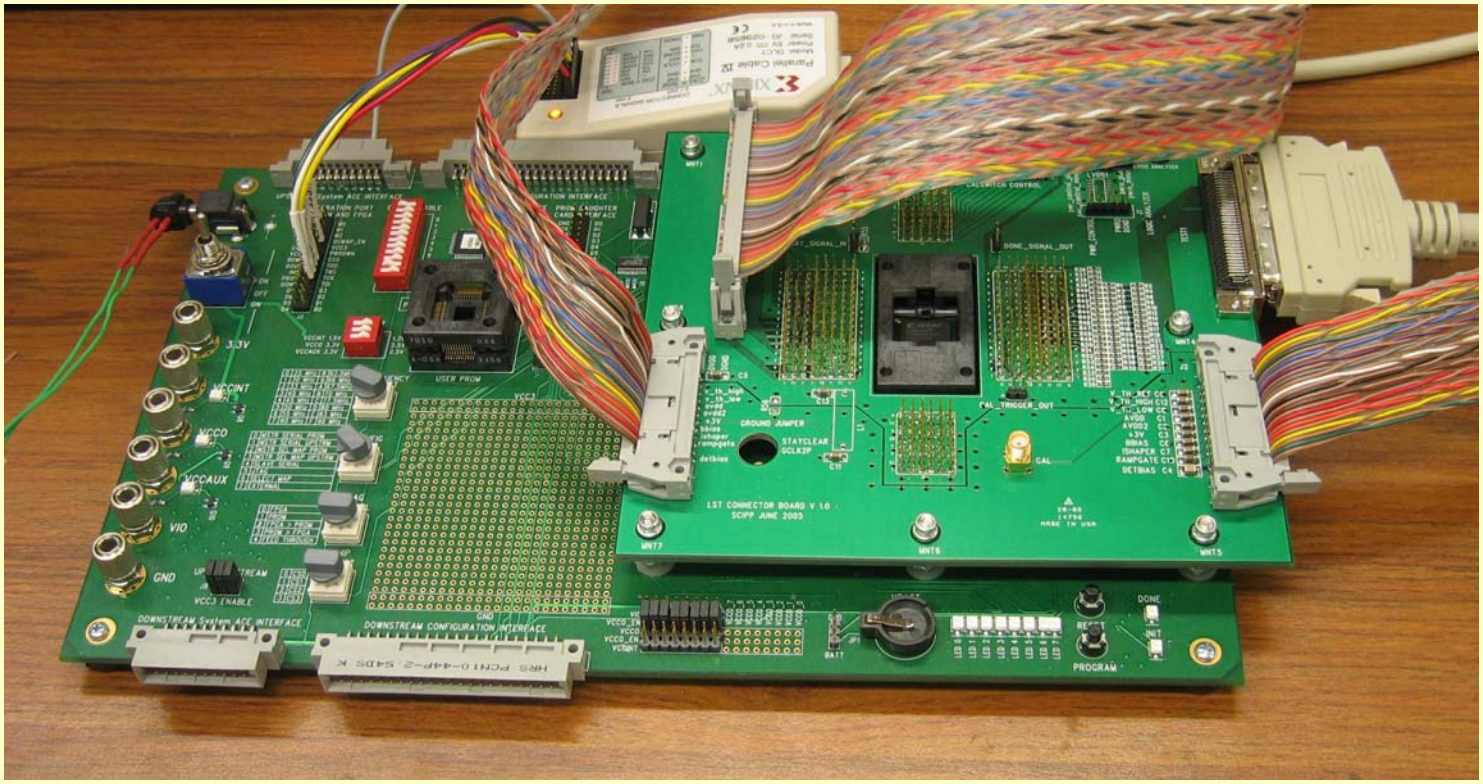
Provided by time-over-threshold; lookup table provides conversions back into analog pulse height (as for actual data)

Detector Resolution (units of 10μm)



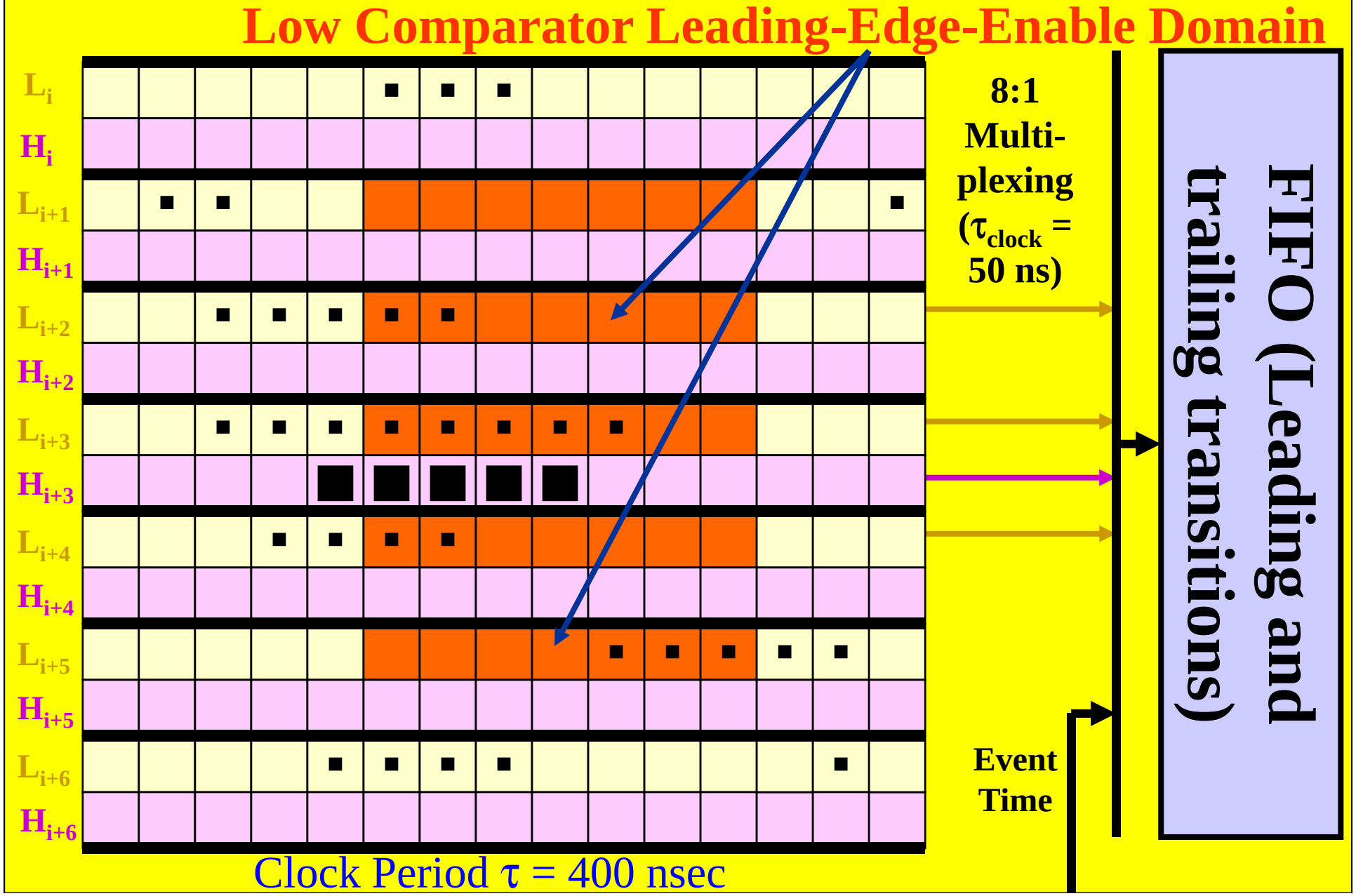
Lower (read) threshold in fraction of min-i
(High threshold is at 0.29 times min-i)

DIGITAL ARCHITECTURE: FPGA DEVELOPMENT



Digital logic under development on FPGA (Wang, Kroseberg), will be included on front-end ASIC after performance verified on test bench and in test beam.

Proposed LSTFE Back-End Architecture



Note on LSTFE Digital Architecture

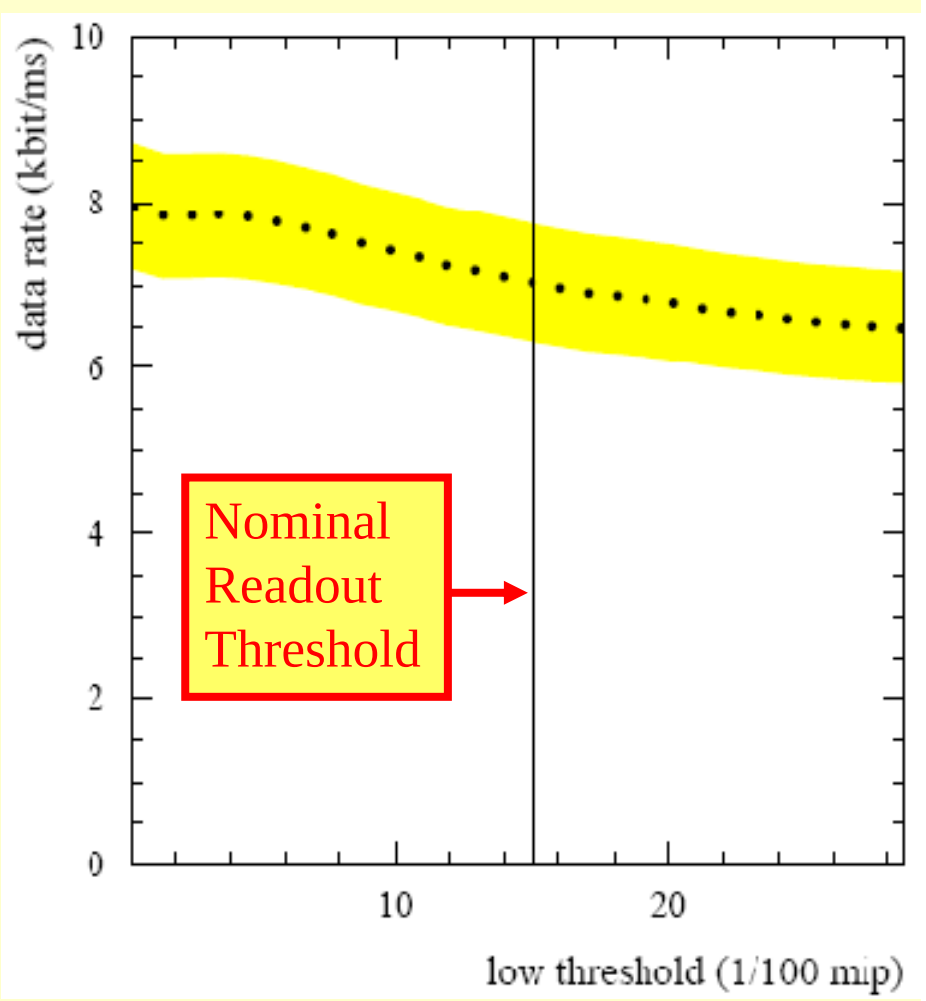
Use of time-over-threshold (vs. analog-to-digital conversion) permits real-time storage of pulse-height information.

➔ No concern about buffering

➔ LSTFE system can operate in arbitrarily high-rate environment; is ideal for (short ladder) forward tracking systems as well as long-ladder central tracking applications.

DIGITAL ARCHITECTURE SIMULATION

ModelSim package permits realistic simulation of FPGA code (signal propagation not yet simulated)

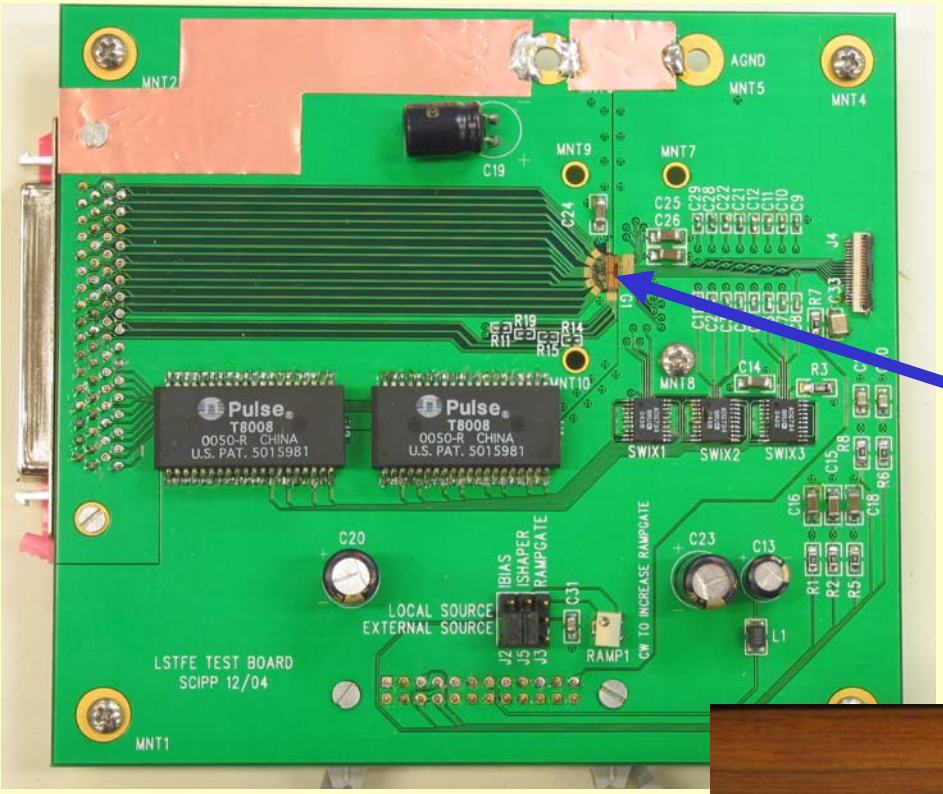


Simulate detector background (innermost SiD layer) and noise rates for 500 GeV running, as a function of read-out threshold.

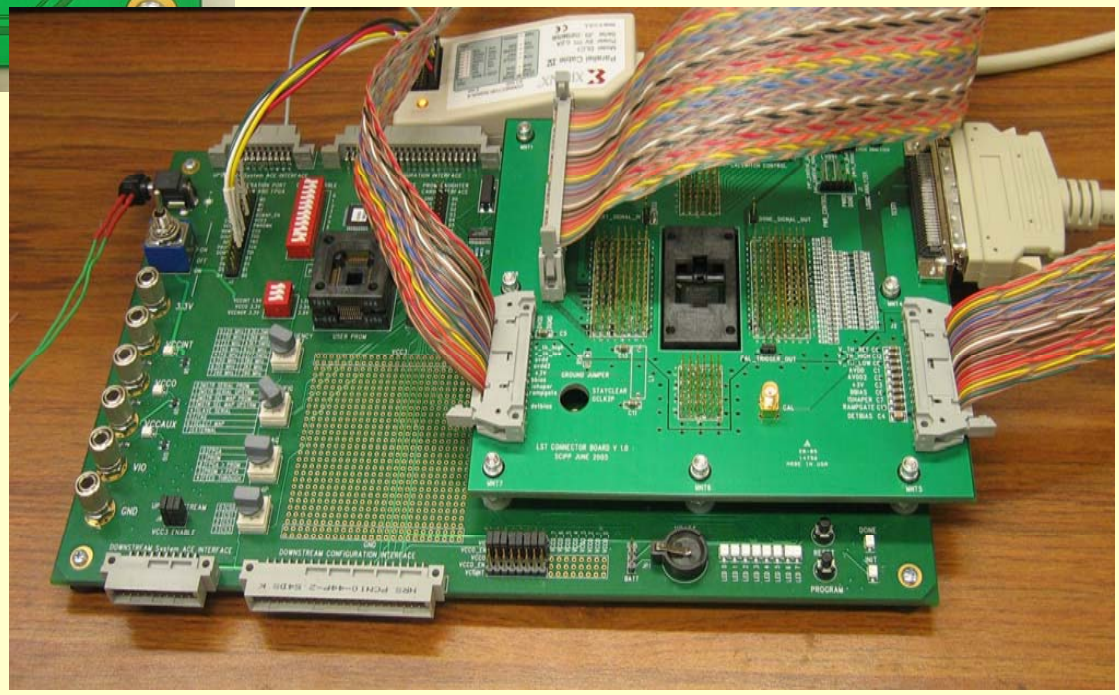
Per 128 channel chip ~ 7 kbit per spill ➔ 35 kbit/second

For entire SiD tracker ~ 0.5-5 GHz data rate, depending on ladder length (x100 data rate suppression)

INITIAL RESULTS



LSTFE chip mounted on readout board



FPGA-based control and data-acquisition system

Note About LSTFE Shaping Time

Original target: τ_{shape} = 3 μsec, with some controlled variability ("ISHAPR")
➔ Appropriate for long (2m) ladders

In actuality, τ_{shape} ~ 1.5 μsec; tests are done at 1.2 μsec, closer to optimum for SLAC short-ladder approach

Difference between target and actual shaping time understood in terms of simulation (full layout)

LSTFE-2 will have ~3 μsec shaping time

Comparator S Curves

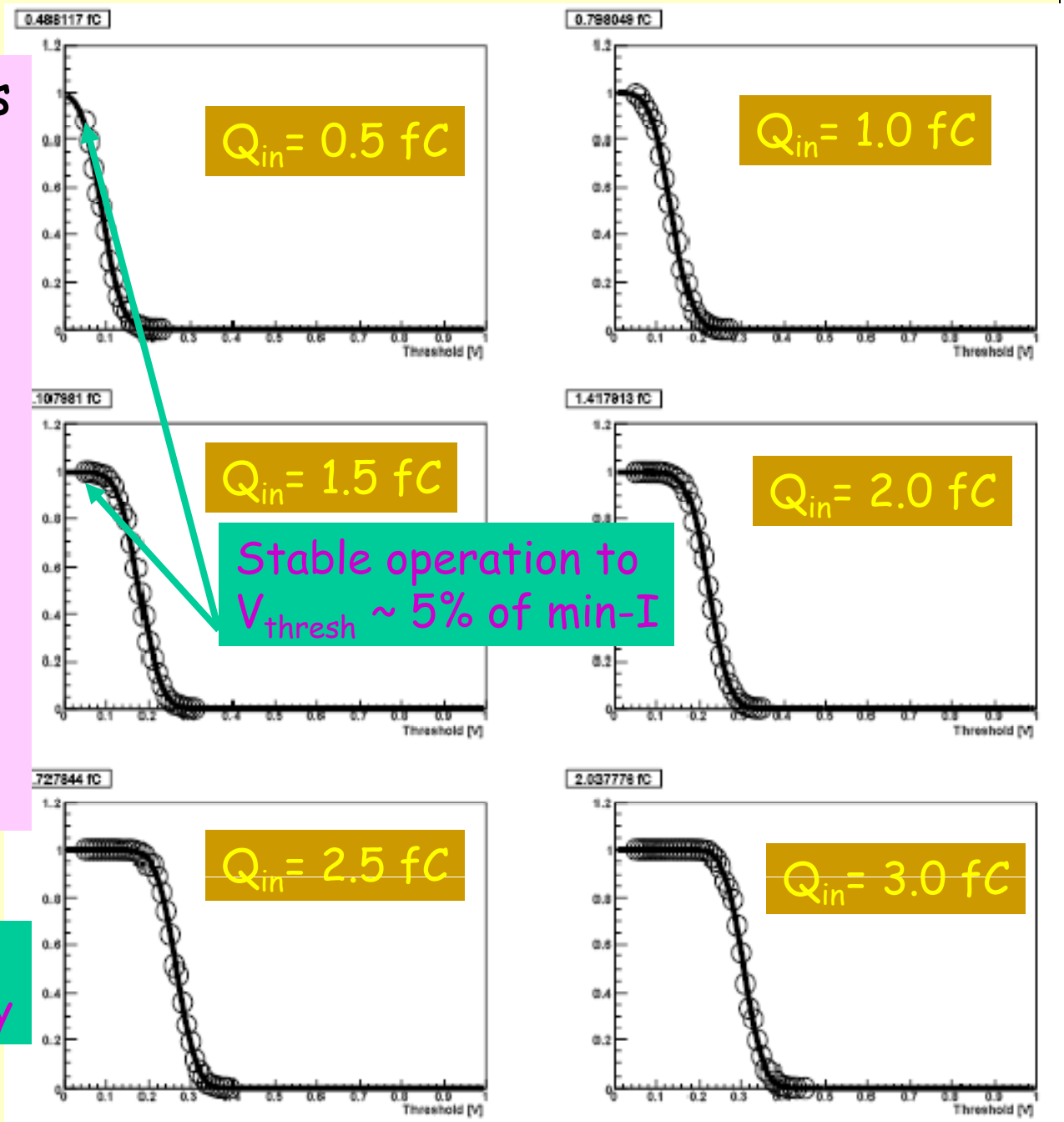
Vary threshold for given input charge

Read out system with FPG-based DAQ

Get

```
1-erf(threshold)
```

with 50% point giving response, and width giving noise



Stable operation to V_{thresh} ~ 5% of min-I

Hi/Lo comparators function independently

EQUIVALENT CAPACITANCE STUDY

Noise vs. Capacitance
(at τ_{shape} = 1.2 μs)

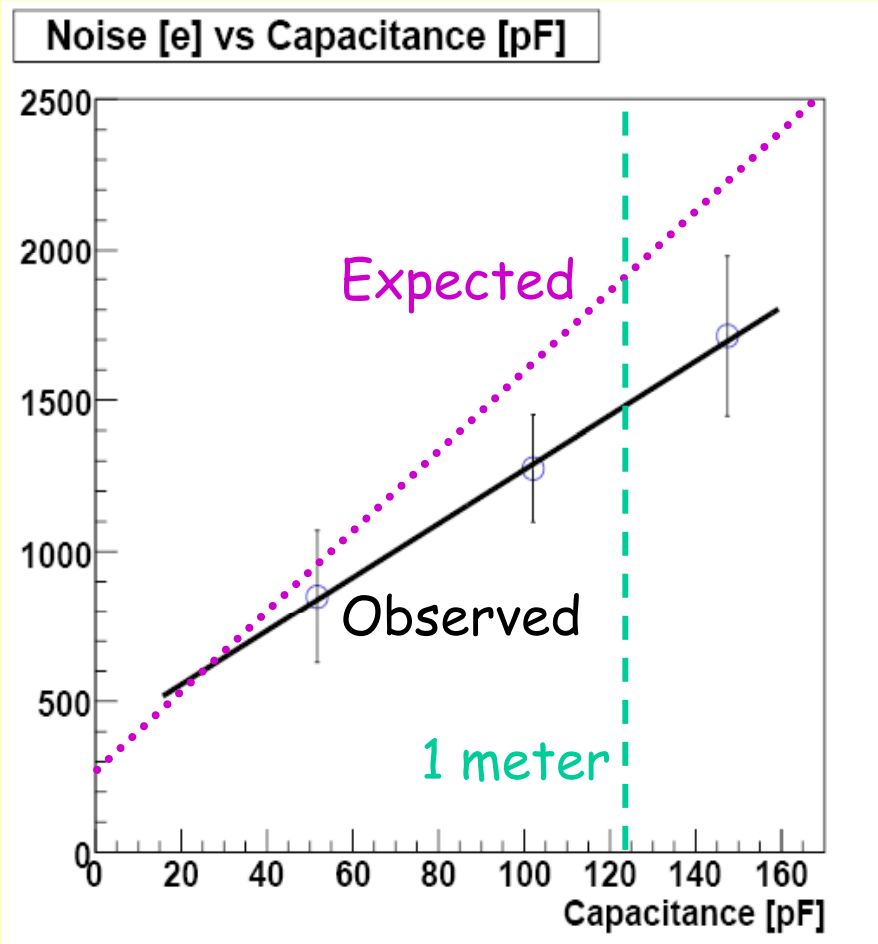
Measured dependence is roughly (noise in equivalent electrons)

$$\sigma_{noise} = 375 + 8.9*C$$

with C in pF.

Experience at 0.5 μm had suggested that model noise parameters needed to be boosted by 20% or so; these results suggest 0.25 μm model parameters are accurate

➔ Noise performance somewhat better than anticipated.



Timing Resolution Study (50 pF Load)

Nominal expectation:

$$\sigma_t = \frac{\tau}{SNR} \bullet \frac{1}{1 - \frac{\theta}{SNR}}$$

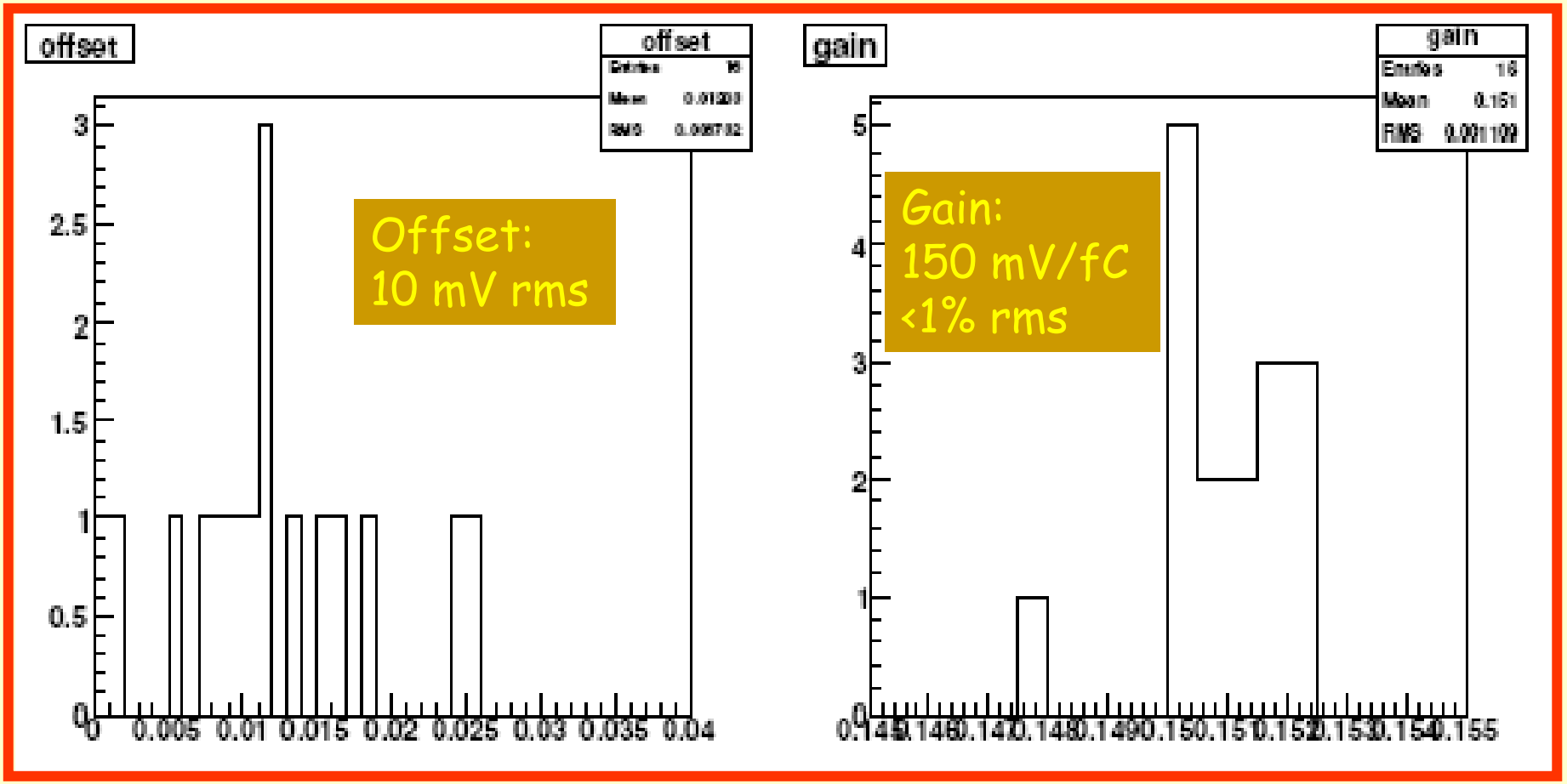
where τ = 1.5 μs is the shaping time, θ = 8.8 is the applied threshold in units of rms noise, and SNR = 28. This yields an expectation of

$\sigma_t \sim 75$ ns (expected)

σ_t was measured at a series of input charges, which were averaged together with weights from a Landau distributions, yielding

$\sigma_t \sim 50$ ns (measured)

Channel-to-Channel Matching



Occupancy threshold of 1.2 fC (1875 e^-) ➔ 180 mV

± 2 mV (20 e^-) from gain variation

± 10 mV (100 e^-) from offset variation

Power Cycling

Idea: Latch operating bias points and isolate chip from outside world.

- Per-channel power consumption reduces from ~0.5 mW to ~0.5 μW.
- Restoration to operating point should take ~ 1 msec.

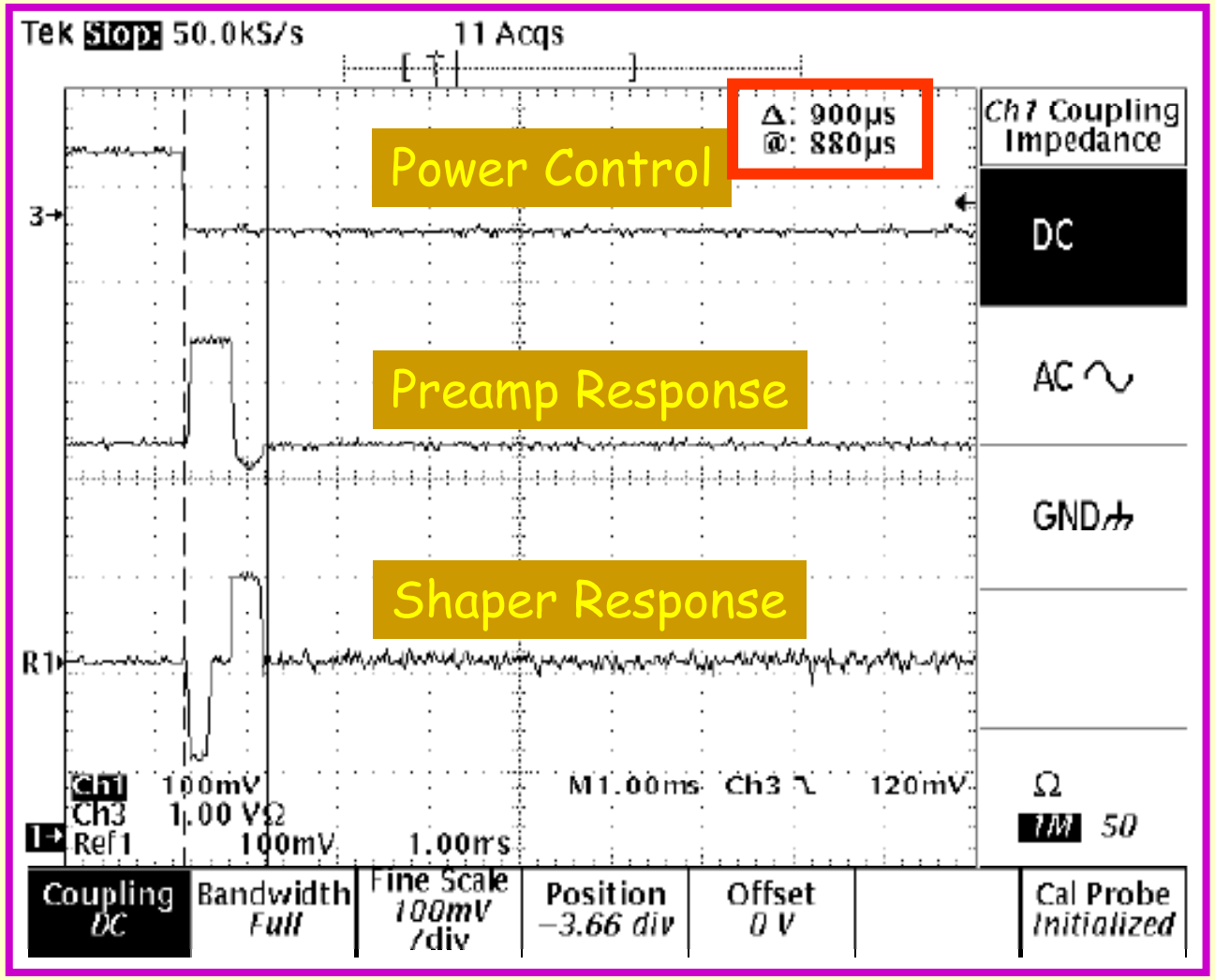
Current status:

- Internal leakage (protection diodes + ?) degrades latched operating point
- Restoration takes ~40 msec (x5 power savings)
- Injection of small current (< 1 nA) to counter leakage allows for 1 msec restoration.

Future (LSTFE-2)

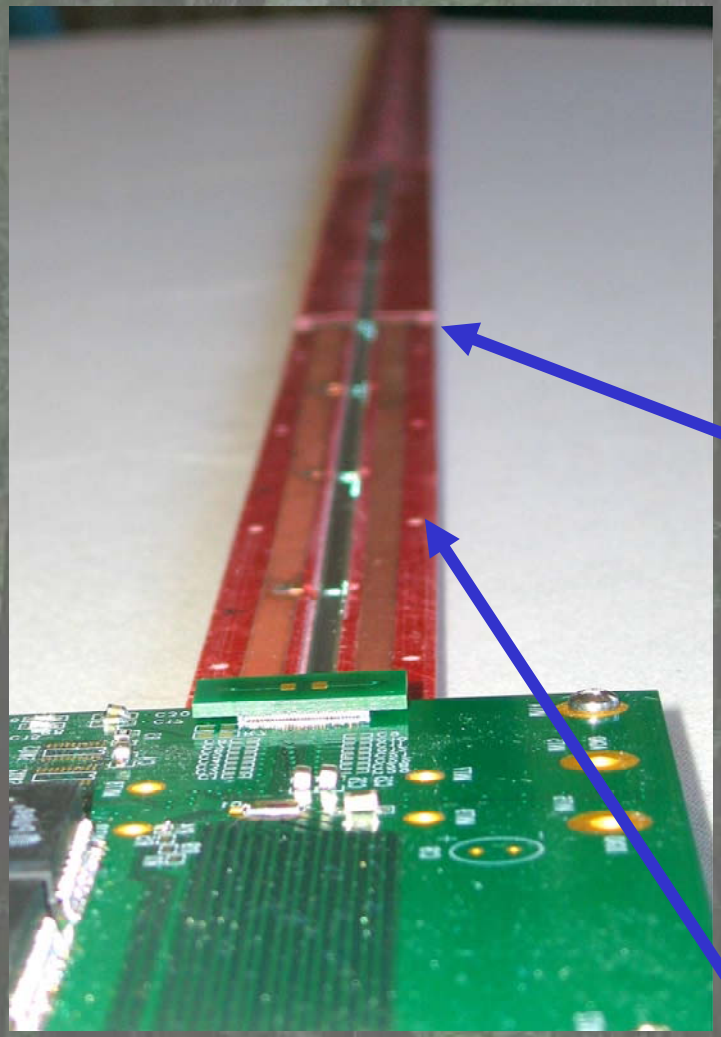
- Low-current feedback will maintain bias points; solution already incorporated in LSTFE-2 design

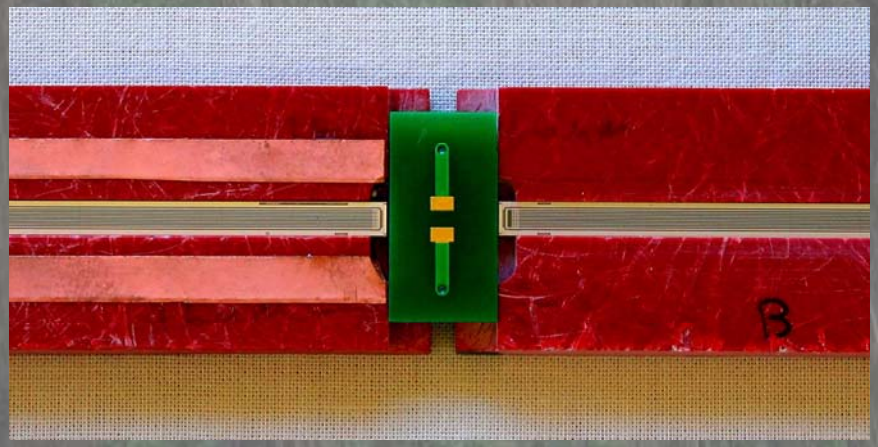
Power Cycling with Small Injected Current

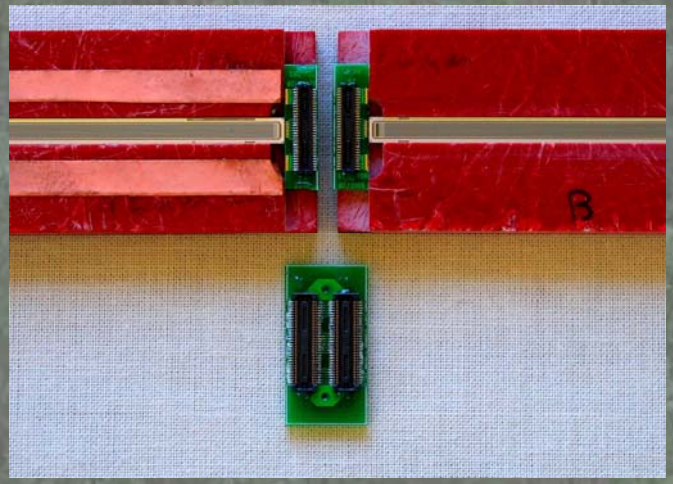


Solution in hand to maintain bias levels in "off" state with low-power feedback; will eliminate need for external trickle current

LONG LADDER CONSTRUCTION







LONG LADDER EXPERIENCE

A current focus of SCIPP activity

Using GLAST "cut-off" (8 channel) sensors; 237 μm pitch with 65 μm strip width

Have now studied modules of varying length, between 9cm and 143cm.

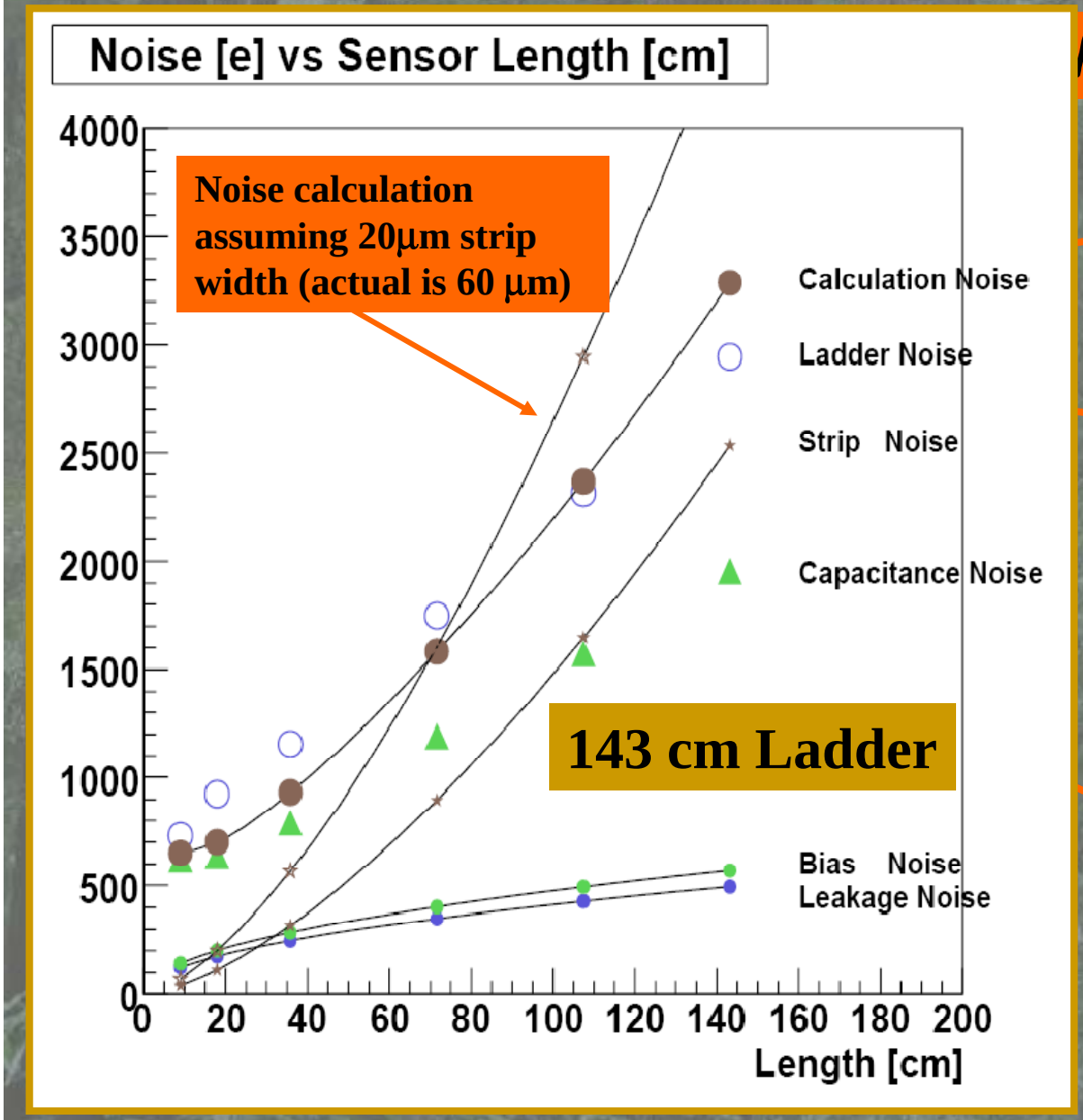
Measure inputs to estimate noise sources other than detector capacitance:

- Leakage current 1.0 nA/cm
- Strip resistance 3.1 Ω/cm
- Bias resistance 35 MΩ per sensor

All of these should be considered in module design!

Strip resistance for fine pitch could be an issue → are starting careful study and considering options → feedback to detector/module design.

Measured Noise vs. Sum of Estimated Contributions



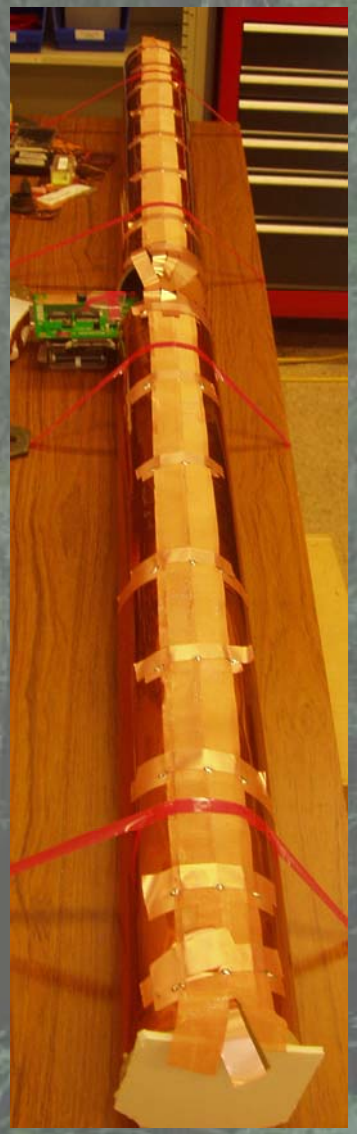
Measured noise

Sum of estimates

Projected Johnson noise for 20 µm strip (not part of estimate)

Estimated Johnson noise for actual 65 µm strip (part of estimate)

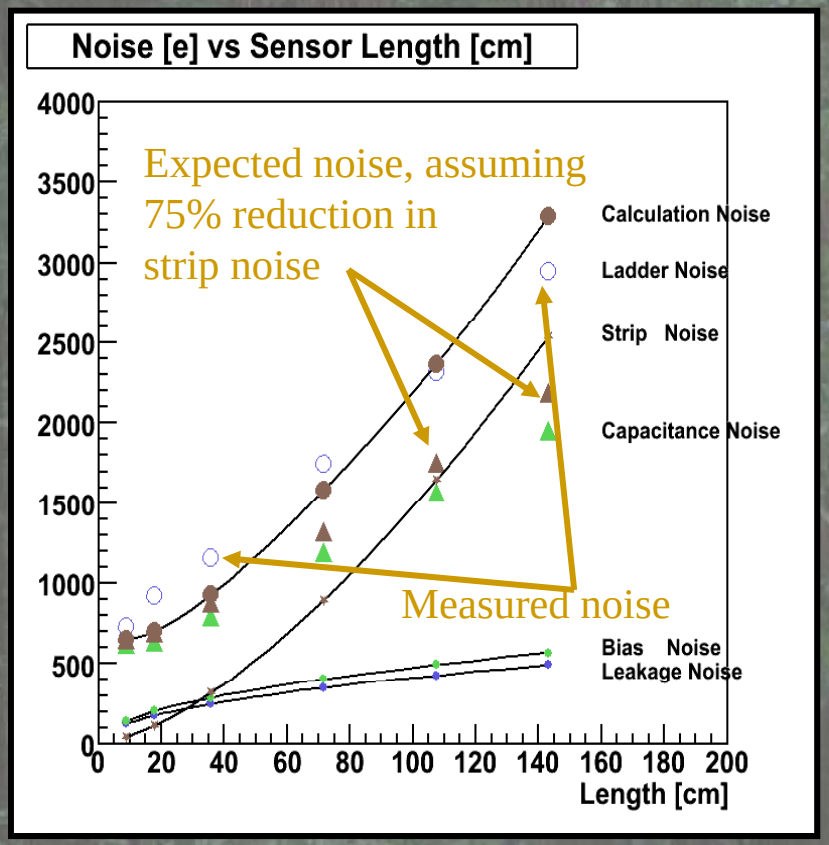
Strip Noise Idea: "Center Tapping" – half the capacitance, half the resistance?



Result: no significant change in measured noise

However, sensors have 237 μm pitch

➔ Currently characterizing CDF L00 sensors



TIME-OVER-THRESHOLD READOUT SUMMARY

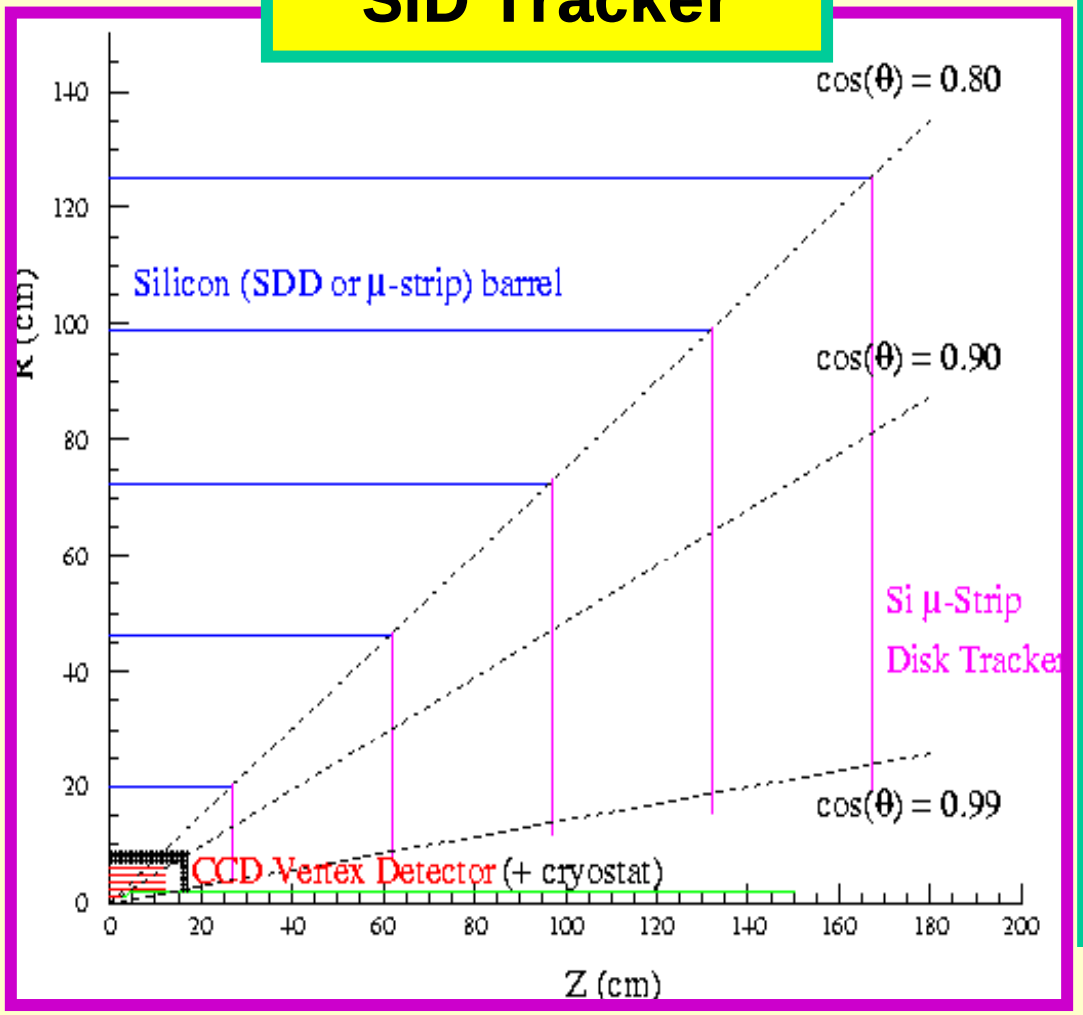
The LSTFE readout system is:

- Universally applicable (long strips, short strips, central, forward, SiD, LDC, GLD, 4th…)
- Rigorously optimized for ILC tracking
- Relative simple (reliability, yield)
- In a relatively advanced stage of development
- Is now being used as an instrument to understand fundamental principles of long ladder operation, particularly for narrow strips (CDF Layer00 sensors available, being qualified)

RANDOM BACK-UP SLIDES

Silicon Microstrip Readout R&D

SiD Tracker



Initial Motivation

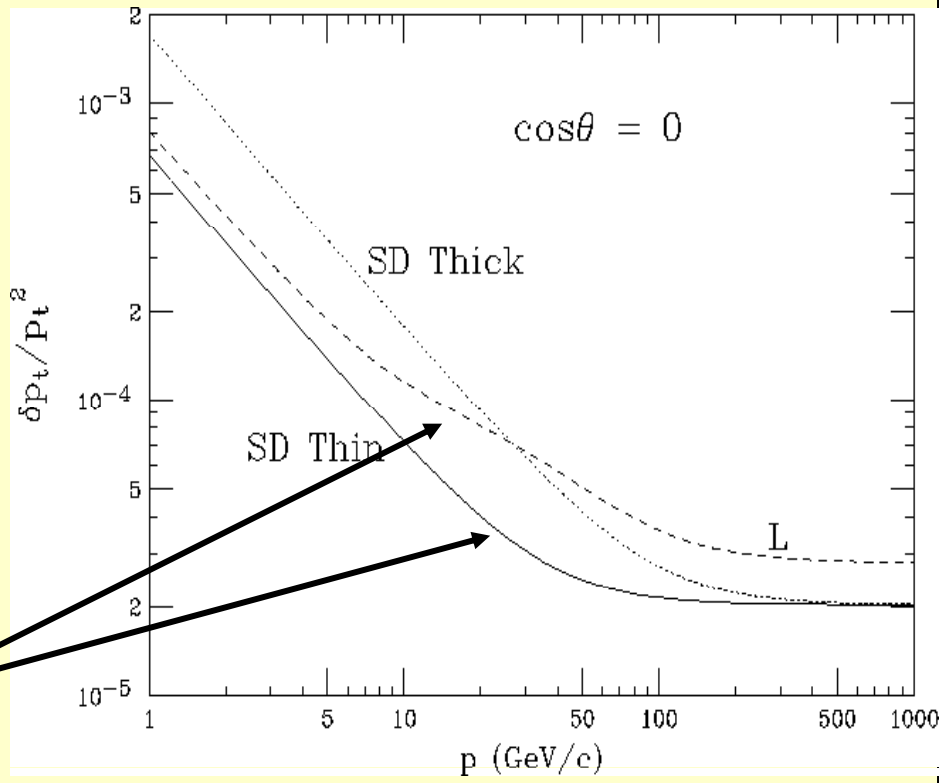
Exploit long shaping time (low noise) and power cycling to:

- Remove electronics and cabling from active area (long ladders)
- Eliminate need for active cooling

The Gossamer Tracker

Ideas:

- Low noise readout ➔ Long ladders ➔ substantially limit electronics readout and support
- Thin inner detector layers
- Exploit duty cycle ➔ eliminate need for active cooling



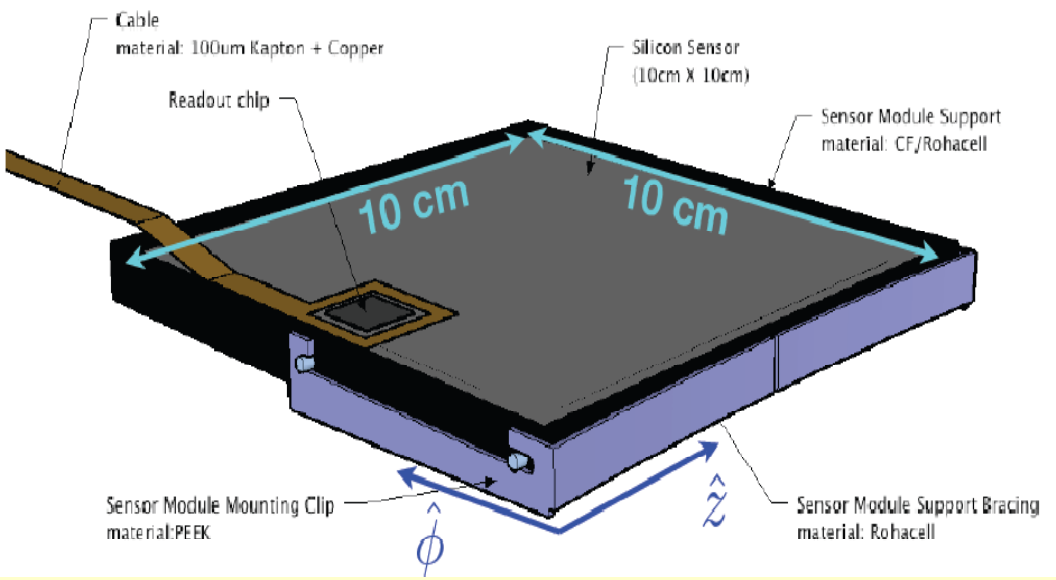
Competitive with gaseous tracking over full range of momentum (also: **forward region**)

Alternative: shorter ladders, but better point resolution

Alternative: shorter ladders, but better point resolution

The LSTFE approach would be well suited to use in short-strip applications, and would offer several potential advantages relative to other approaches

- Optimized for LC tracking (less complex)
- More efficient data flow
- No need for buffering



Would require development of 2000 channel chip w/ bump bonding (should be solved by KPiX development)

LSTFE-2 DESIGN

LSTFE-1 gain rolls off at ~10 mip; are instituting log-amp design (50 mip dynamic range)

Power cycling sol'n that cancels (on-chip) leakage currents

Improved environmental isolation

Additional amplification stage (noise, shaping time, matching

Improved control of return-to-baseline for < 4 mip signals

Multi-channel (64? 128? 256?) w/ 8:1 multiplexing of output

Must still establish pad geometry (sensor choice!)