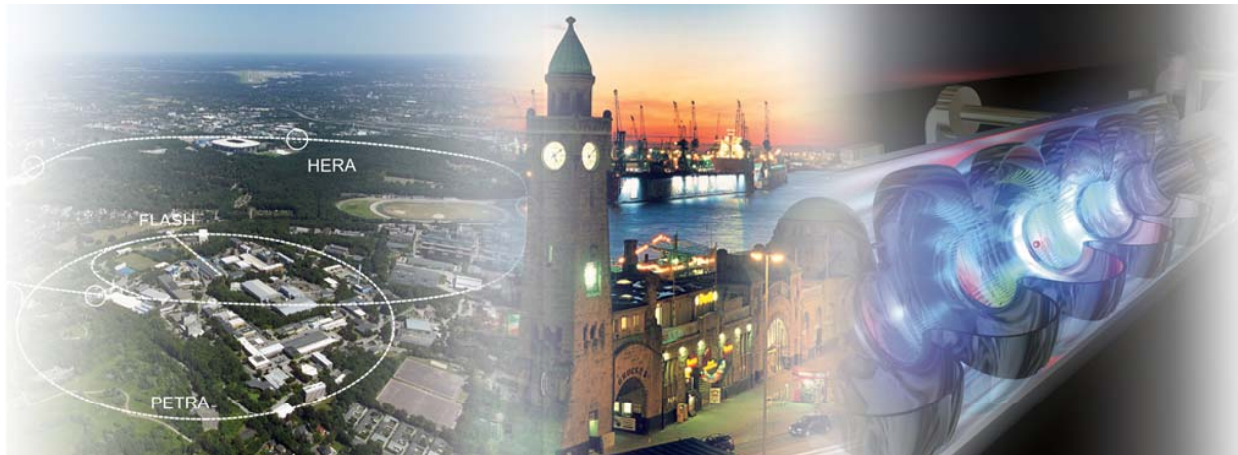




# Fast Kicker R&D in the Americas Region

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ILC2007

Global Design Effort





# Outline

- Fast kicker and pulser priorities for the Americas region
- Americas R&D Effort
  - **High Availability kicker development**
  - **Update from FID Technologies**
  - **Other efforts and possibilities in the Americas**
- Conclusion



# Focus of the ART Program

- Primary focus of US program
  - **Pursue a high availability pulsed power supply design**
    - Ensure that we have a route to meet system level requirements of the DR injection/extraction kicker systems
    - Continue to develop a well-understood system design that complements the pursuit of other proprietary off-the-shelf options
  - **Modest support for kicker structure development**
    - LBNL support of ATF kicker design
    - Expect small supporting effort for ILC design
      - Program assumes that major structure development will take place in the other regions

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# High Availability ILC Kicker with ATF

- Motivation
  - Fast precise pulses  $<5\text{nsec}$  needed to reduce DR size to 6 km.
  - Reliability/Availability of system of  $\sim 10\text{-}20$  or more pulsers in series critical.
- Program
  - **Phase I (FY06-08): Demonstrate HA pulsers, HA architecture**
    - Currently pursuing both Induction Adder MOSFET and DSRD\* pulser technologies (\*Delayed Step Recovery Diode used as pulse sharpener)
    - Final design may use Inductive Adder to pump DSRD circuits
  - **Phase II (FY08-09): Demonstrate 3 MHz,  $<5\text{ nsec}$  width, 1 nsec Tr Tf,  $\pm 10\text{kV}$  to  $\pm 0.1\%$  stability, DR pulser & kicker magnet performance**
  - **Phase III: Demonstrate, timing control, calibration, fast diagnostics, reliability, HA features for one, more than one pulser & magnet (FY09-10).**
  - Actual schedules determined by funding & resources.
- Involvement
  - SLAC, LLNL/Bechtel for pulser development
  - KEK testing/use at ATF

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# HA Kicker Systems

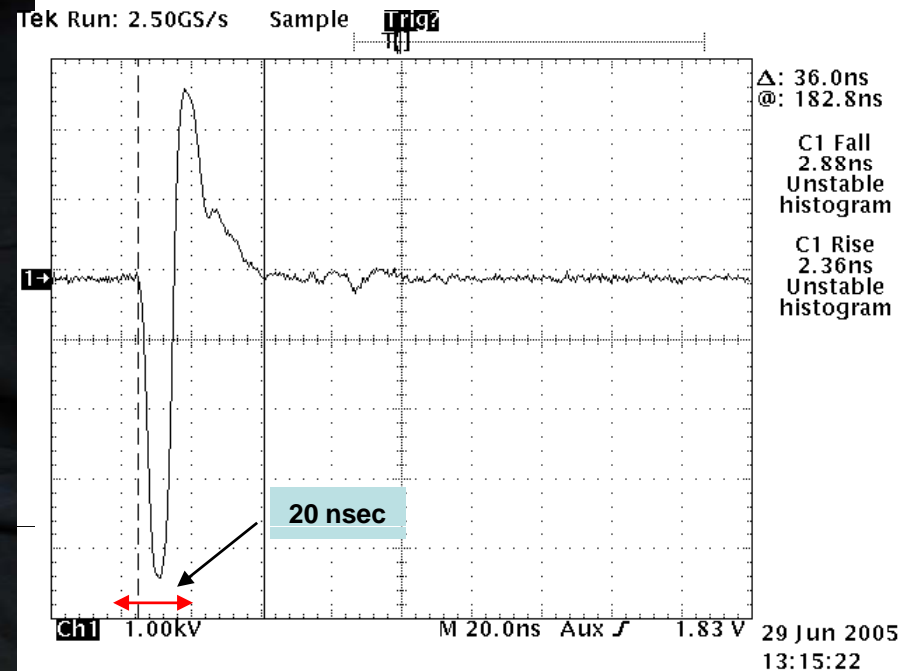
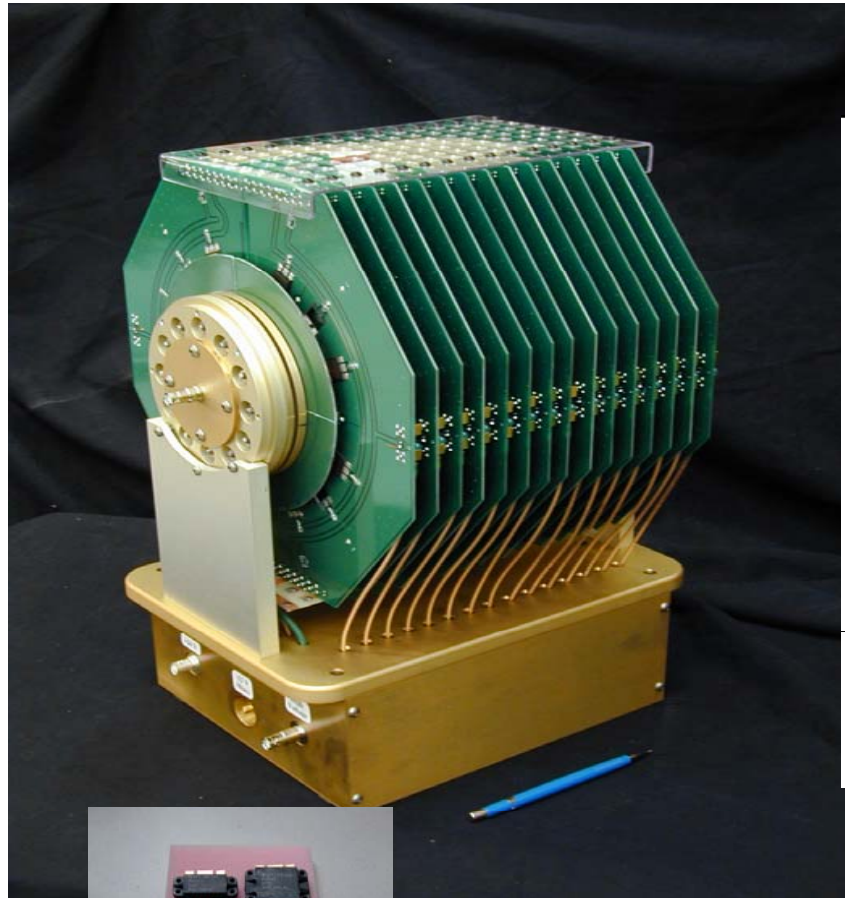
- Planning targets being ready for a technology down-select in 2009

ART WBS	2006	2007	2008	2009	2010	2011	2012	2013	2019
	RDR	EDR			Approval		Construction		Commiss.
<b>3.2.2</b>	<b>HA Kicker System</b>								
3.2.2.1	<i>Induction Adder</i>								
	Develop cascode pulser								
	Develop v2.MOSFET w/driver hybrid								
	Construct v2 complete adder								
	Test v2 Adder by mid FY 09								
	Test v3 Adder by end FY 09								
	Build & test 2 units w/cntrl								
3.2.2.2	<i>DSRD Pulser</i>								
	Develop diagnostic tools								
	Develop low gain DSRD prototype pulser								
	Drive w/ Induction Adder								
	Develop low gain DSRD prototype pulser								
3.2.2.3	<i>Kicker Magnet (no DR funding planned for 08-09)</i>								
	Model, simulate matching of structure								
	Build prototype								
	Test at ATF2								
3.2.2.4	<i>Kicker Systems</i>								
	Build & test 2 units w/cntrl								

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# Original Prototype Tested at KEK



Integrated Driver & Power MOSFET

Pulse needs faster  $T_r$ ,  $T_f$ , tail compensation

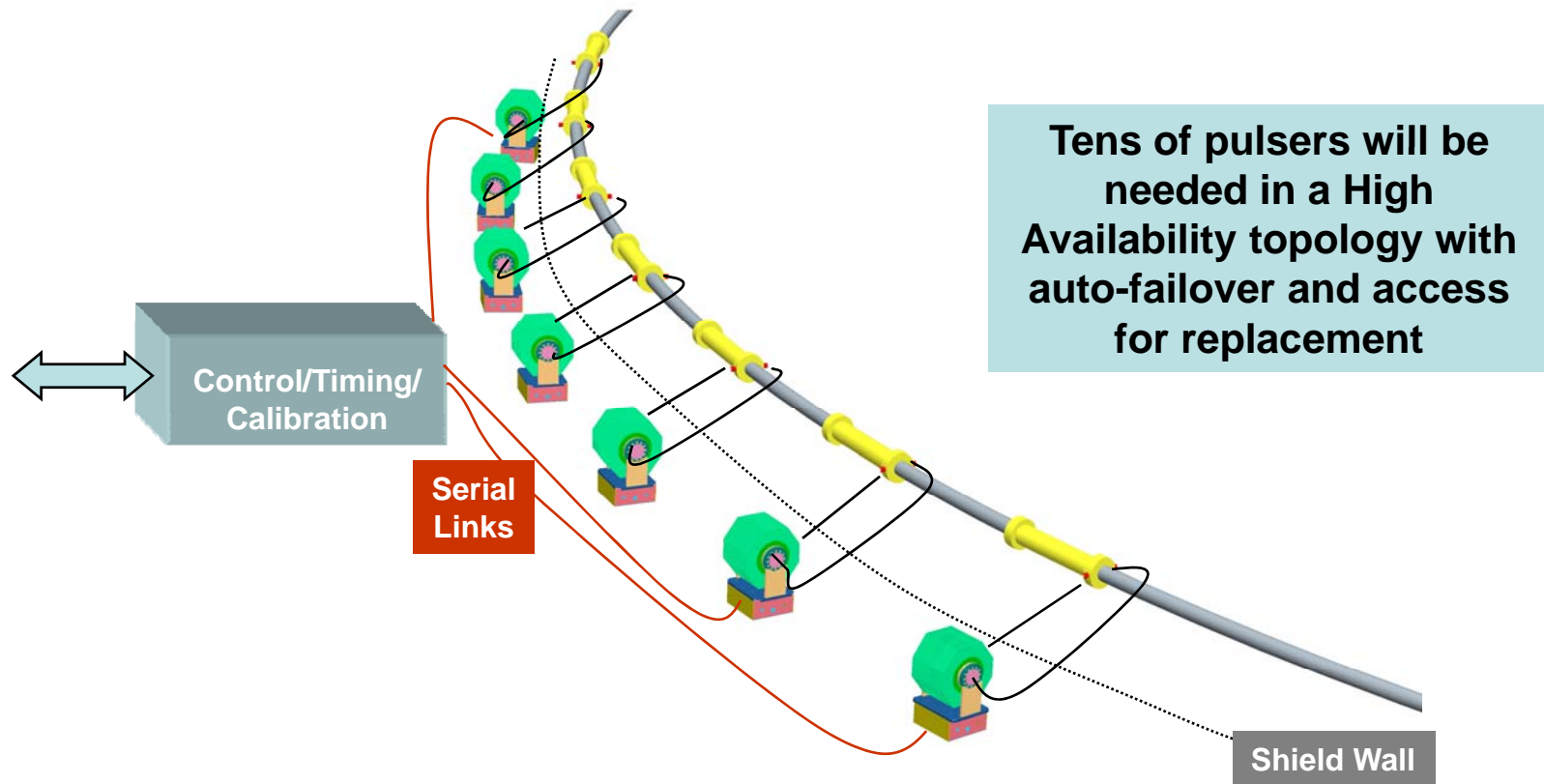
E. Cook LLNL

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# HA Kicker System Topology

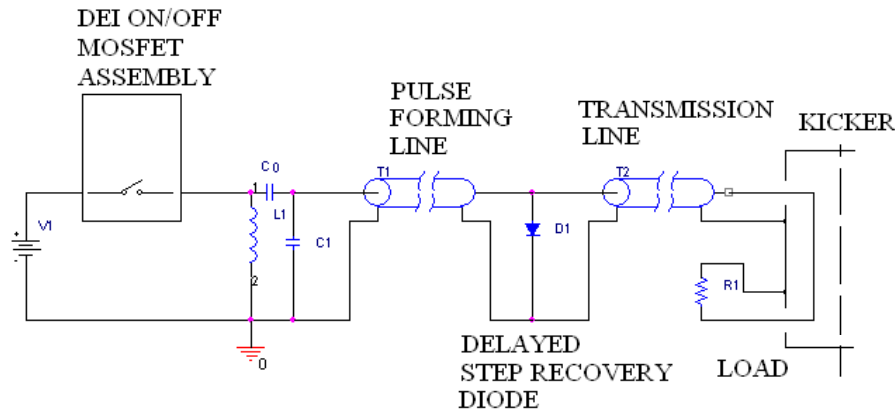


C. Brooksby BN/LLNL

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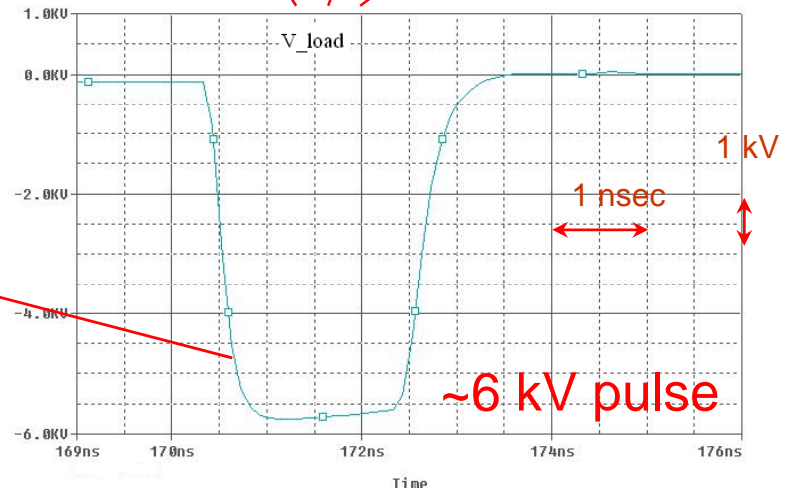
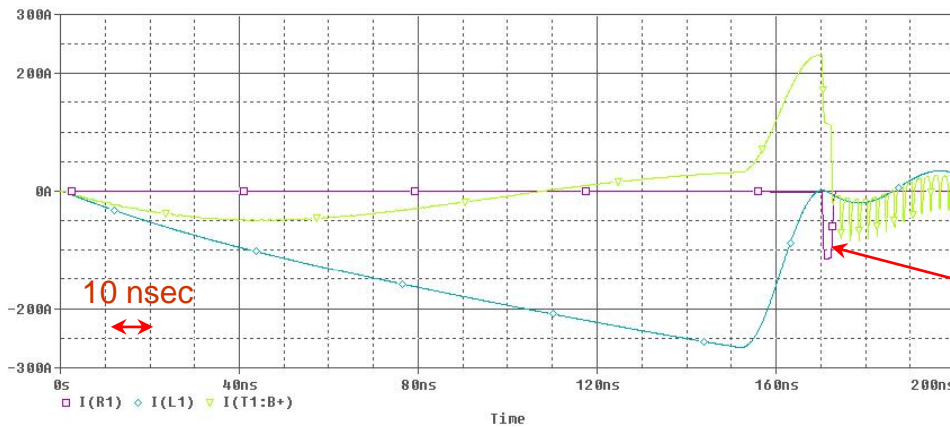
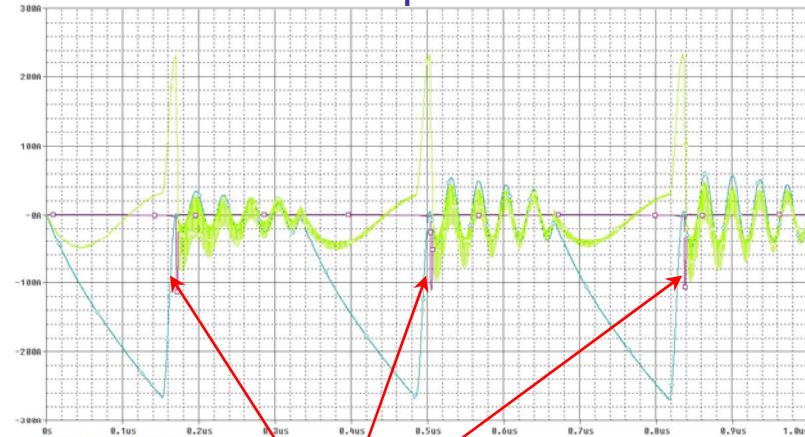


# DSRD Detailed Circuit Behavior



$L=40\text{ nH}$ ,  $C_0=30\text{ nF}$ ,  $C_1=1.5\text{ nF}$ ,  
 $t_{on}=150\text{ nsec}$ ,  $t = 1\text{ nsec}$

### 3 MHz Rep Rate



Currents vs. time for one cycle

Output Voltage, Residual Voltage is ~ 2%

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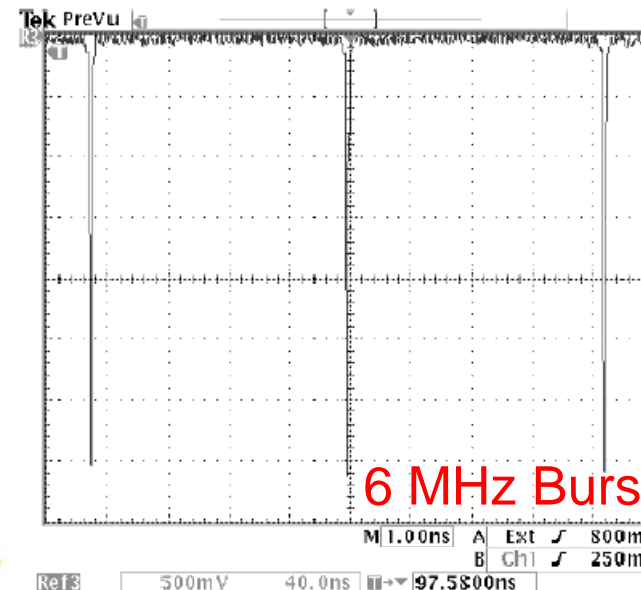
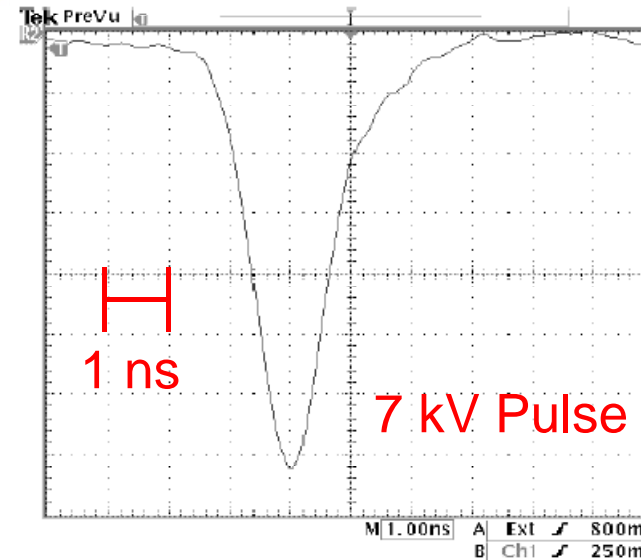
## HA Kicker Progress Summary

- Progress in FY07:
  - **Cascode driver promising; started development of new integrated driver chip with MOSFET to speed risetimes**
  - **DSRD single diode pulser achieved best waveform to date; but 07 SLAC effort barely started due to lack of initial funding**
  - **Startup funding now allocated for nanosecond pulse circuit diagnostics development in 07**
  - **Submitted comprehensive program plan, funding request for FY 08-09 to DR Area Group**
  - **Note: Kicker magnet development proposed but no funding for in FY 07-09 plans**



# Ongoing Contacts with FID Technologies

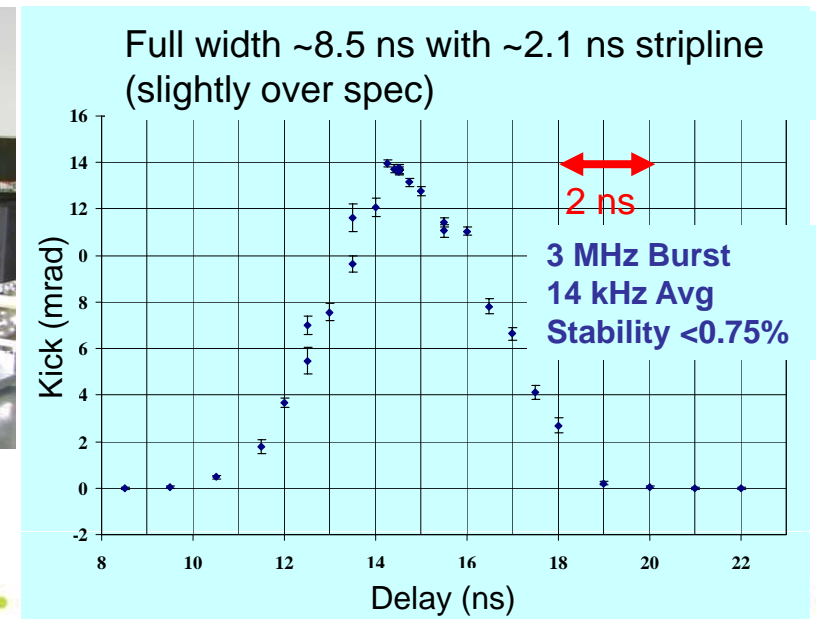
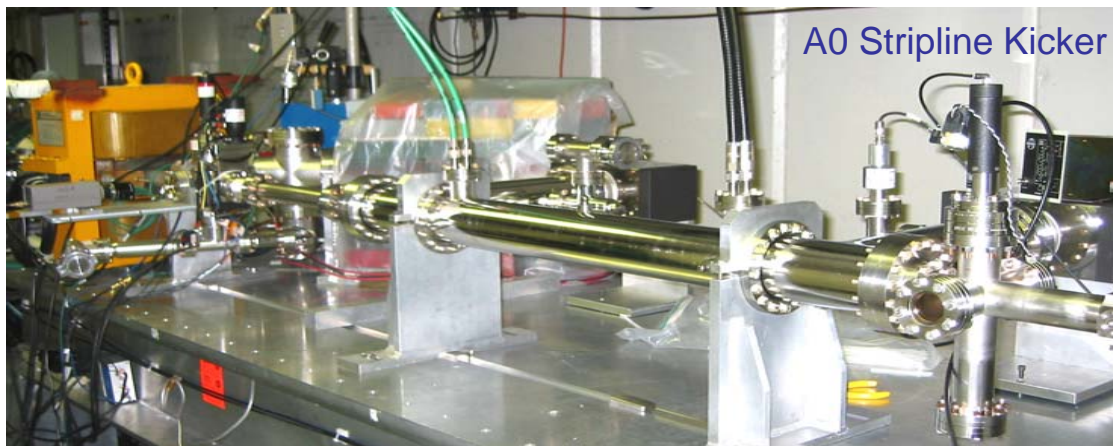
- FPG 10-6000NK
  - Pulse height in the 5-10 kV range
  - 1-2 ns full width
  - 6 MHz burst rate
  - 1 ns rise time
- Does *not* use a combiner to obtain burst rate from multiple internal channels
- No funding available to pursue this option in the Americas





# Other Efforts in the Americas (1)

- A0 kicker
  - Measurement of timing and pulse height stability of  $\pm 1$  kV pulser from FID technologies last year (Cornell/UIUC)
  - See presentation by George Gollin for A0 status and plans



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## Other Efforts (2)

- Proposal by Tom Mattison (Univ. of British Columbia) for work on ferrite pulse sharpeners
- NML beam facility at FNAL
  - Propose to use an ILC DR-style kicker to separate dark current and beam trajectories
  - Can potentially serve as a test bed for DR pulsers
  - Specifications:
    - 1 ns rise time
    - 3 MHz burst rate
    - Need *better* pulse stability than the DR specification ~0.1%
    - $\pm 3$  kV pulse height



## Conclusion

- Americas program primary goal is to have the HA architecture ready for a downselect decision before the end of 2009
  - **Determines the distribution of funding**
- Modest support for other R&D will be available
  - **Other pulser tests**
  - **Kicker structures**
- Plans appear consistent with EDR needs, S3 priorities and ongoing efforts in the other regions