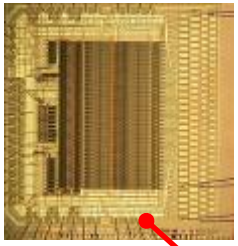
Status Report on DEPFET Active Pixel Sensors for the ILC VTX

Laci Andricek

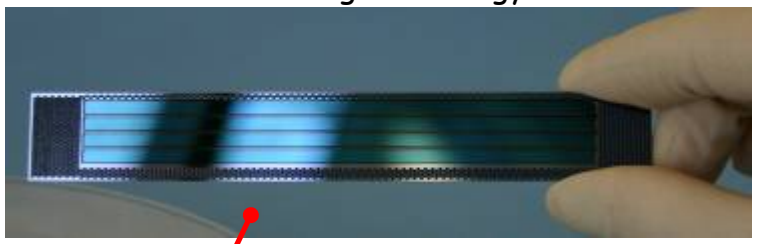
for the DEPFET Collaboration
(www.depfet.org)

The DEPFET ILC VTX Project

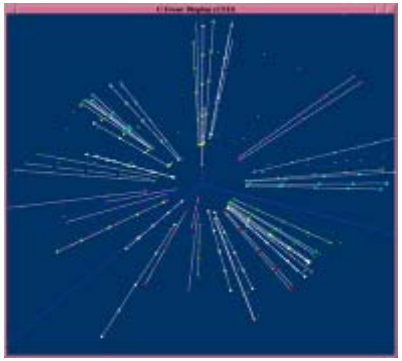
✓ steering chips Switcher



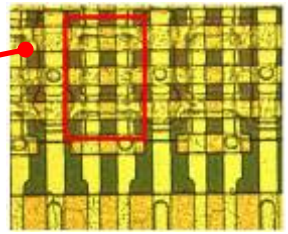
✓ thinning technology

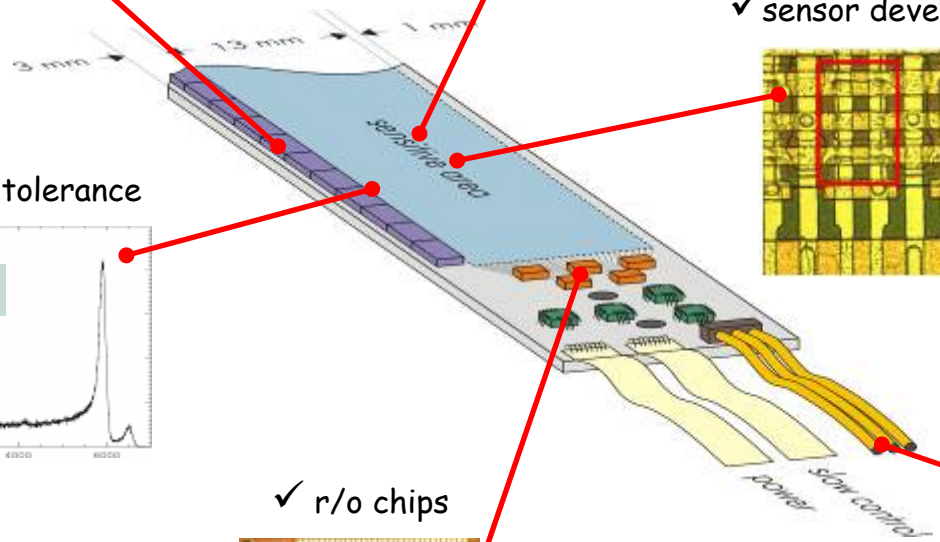


✓ Simulation

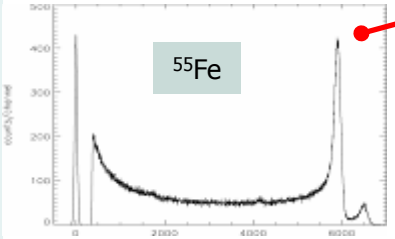


✓ sensor development

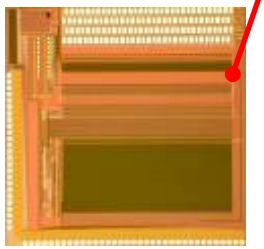




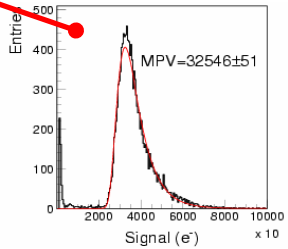
✓ radiation tolerance



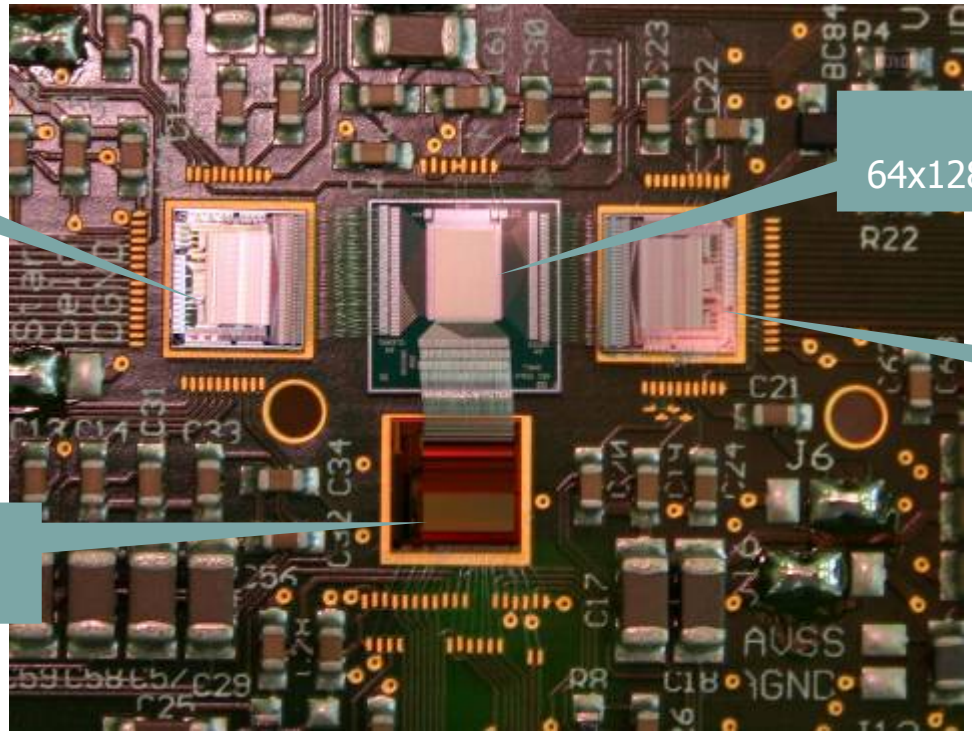
✓ r/o chips



✓ beam test



ILC Prototype System



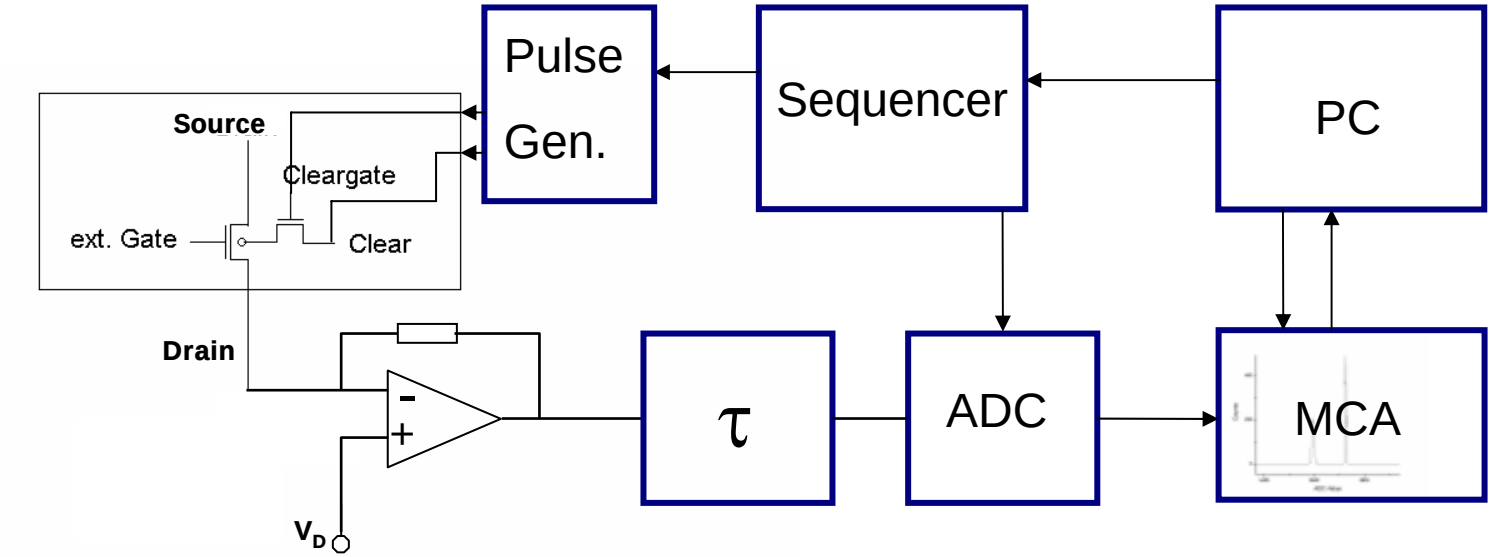
Outline of this talk

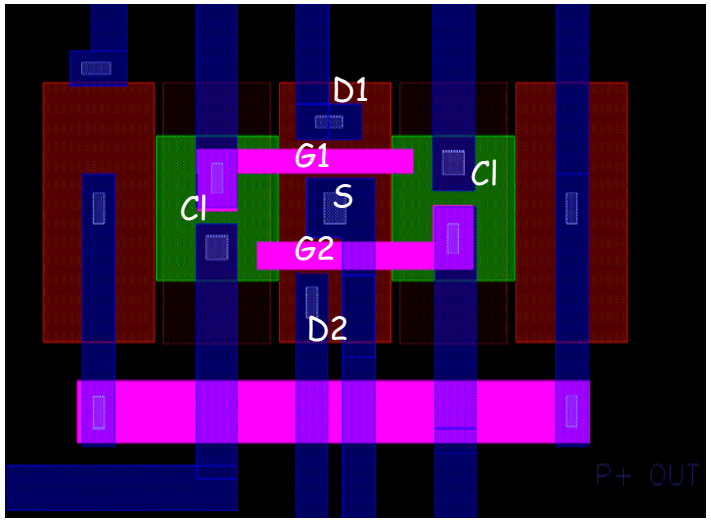
-: New Single Pixel Results
-: Radiation tolerance
-: New Switcher, new r/o chip DCD
-: News from thinning
-: Simulation results

Lars Reuen in the next talk

-: System Tests
-: Beam Test Results

Single Pixel Test Setup



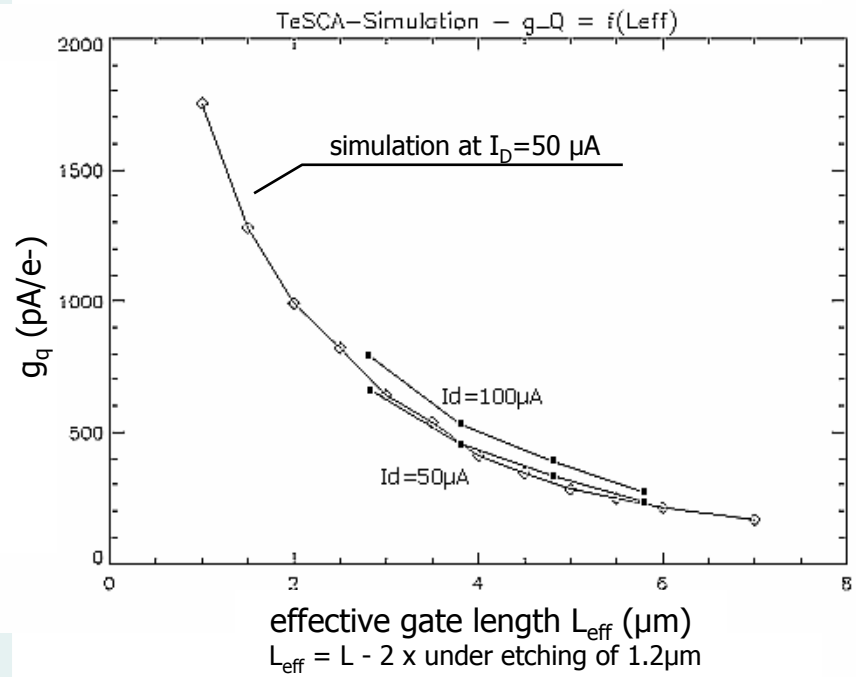


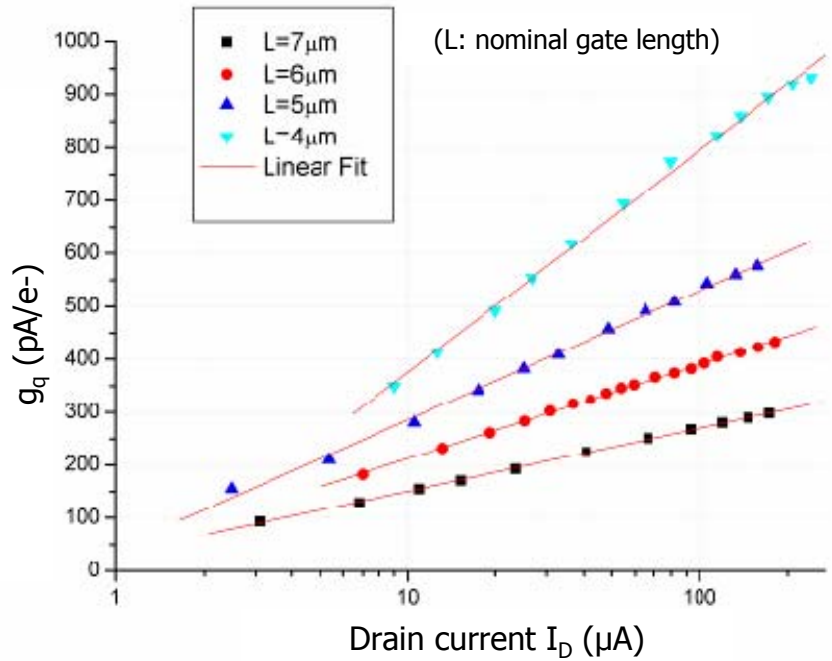
- Spectroscopic measurements
- Noise evaluation
- internal amplification (g_q)
- Leakage current

… before and after irradiation!

Internal amplification g_q

$$g_q = \frac{dI_D}{dQ} = -\frac{\mu_p}{L^2}(V_{GS} - V_{th})$$ (neglecting short channel effects)





As long as noise is dominated by r/o chip → S/N linear with g_q

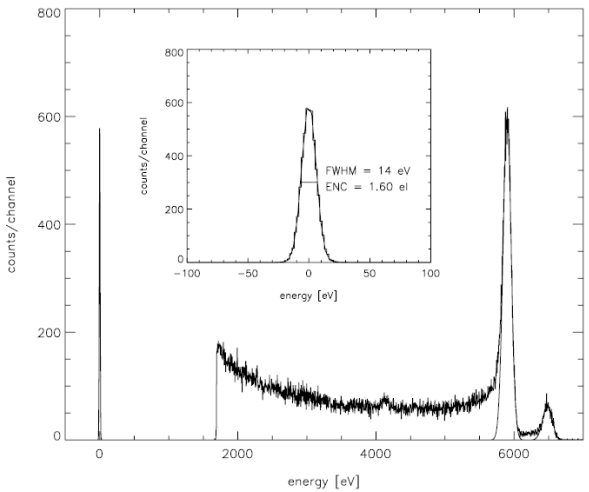
PXD4 has L=6µm, some matrices in PXD5 have now L=4µm → expect factor 2 better S/N

Bandwidth and Noise

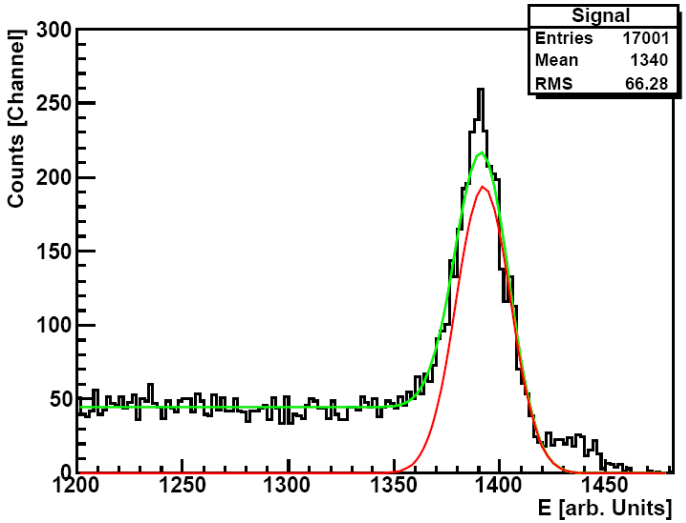
High readout speed → high bandwidth → short shaping times

$$ENC = \sqrt{\alpha \frac{8kT g_m}{3g_q^2}\frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau}$$

Measurements of a single pixel with an external high bandwidth amplifier



1.6 e ENC at t=10 µs



40 e ENC at t=20ns (50MHz)

Intrinsic DEPFET noise sufficiently low for high speed operation at ILC

Irradiations - Overview

-: New irradiations (protons and neutrons) done by Devis Contarato et al., LBNL

-: Single pixel structures with 6 and 7 µm gate length

-: Using the single-pixel setup, with current based readout

-: Look for degradation in:

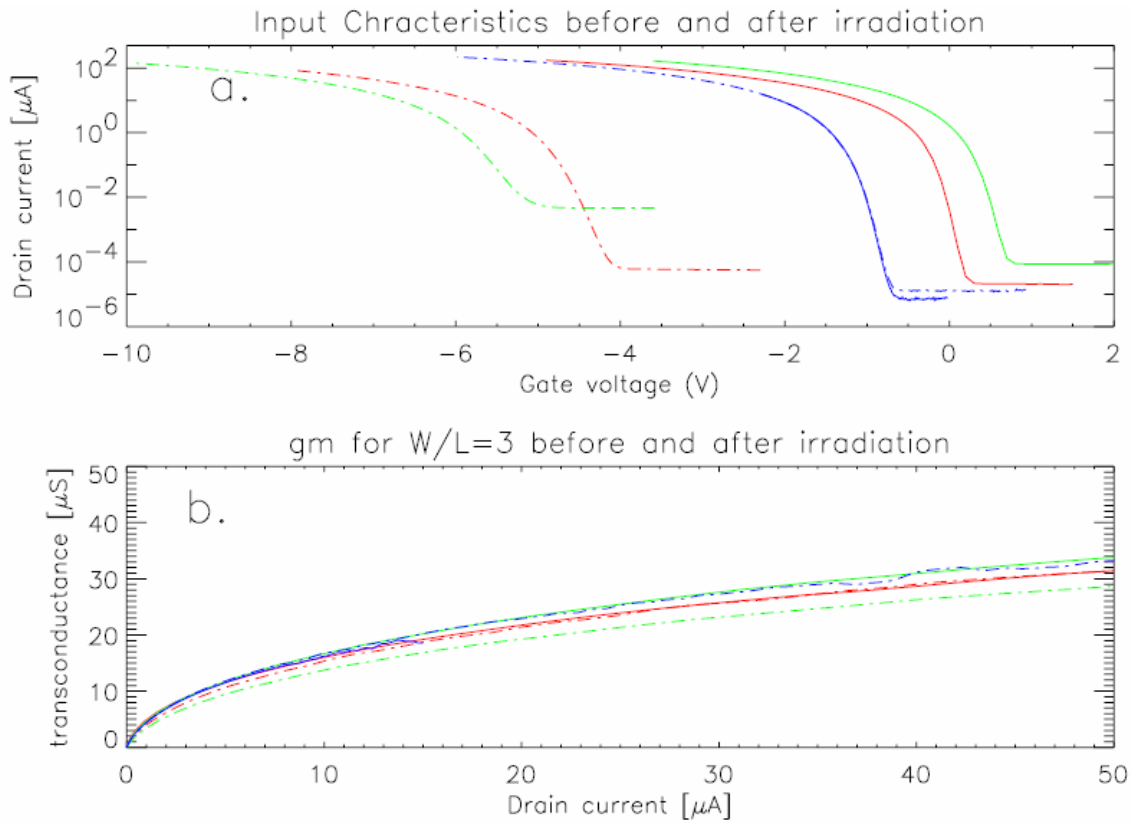
- Electric characteristics (V_{th} shifts, g_m and g_q)
- Leakage current (NIEL)
- Spectroscopic performance
- noise spectrum (1/f noise)

	PXD4-10 MO2	PXD4-5 M05	PXD4-2 J14
Type	Protons, 30MeV	Neutrons, 1-20MeV	Gammas - ^{60}Co
Fluence / Dose	$1.2 \cdot 10^{12}$ p/cm²	$1.6 \cdot 10^{11}$ n/cm²	913kRad
1MeV n equivalent	$3 \cdot 10^{12}$ n_{eq}/cm²	$2.4 \cdot 10^{11}$ n_{eq}/cm²	n/a

LBNL Cyclotron

GSF Munich

Basic Characteristics

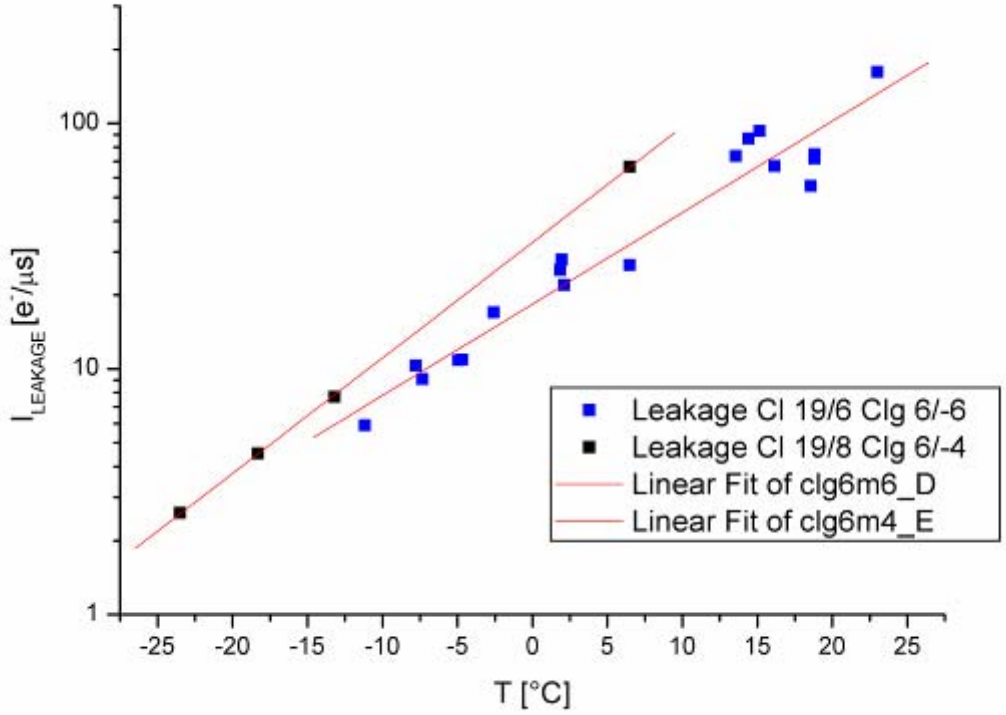


irradiation	TID / NIEL fluence	ΔV_{th}	g_m	I_{Leak} in int. gate at RT(*)
gamma ^{60}Co	913 krad / ~ 0	~-4V	unchanged	156 fA
neutron	~ 0 / 2.4x10^{11} n/cm^2	~ 0	unchanged	1.4 pA
proton	283krad / 3x10^{12} n/cm^2	~-5V	~ -15%	26 pA

(*) 5..22 fA non irrad.

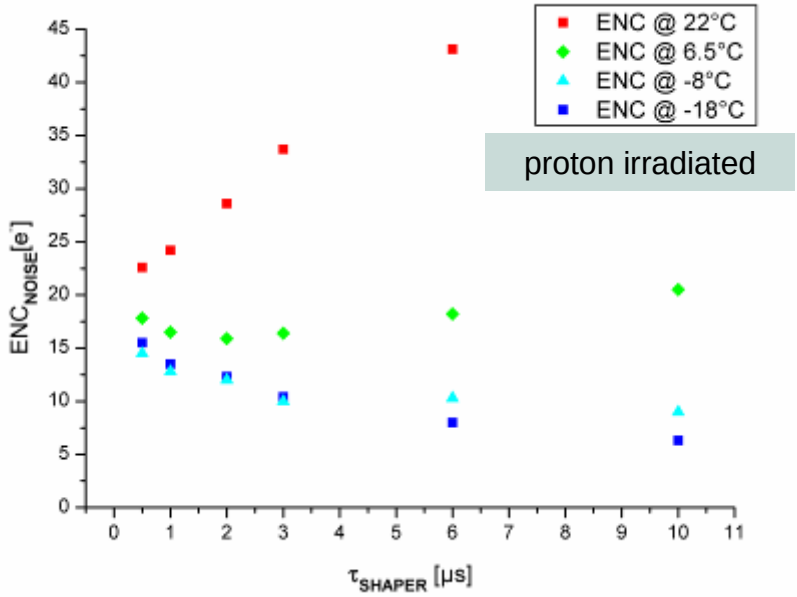
Bulk Leakage Current- Temperature dependence

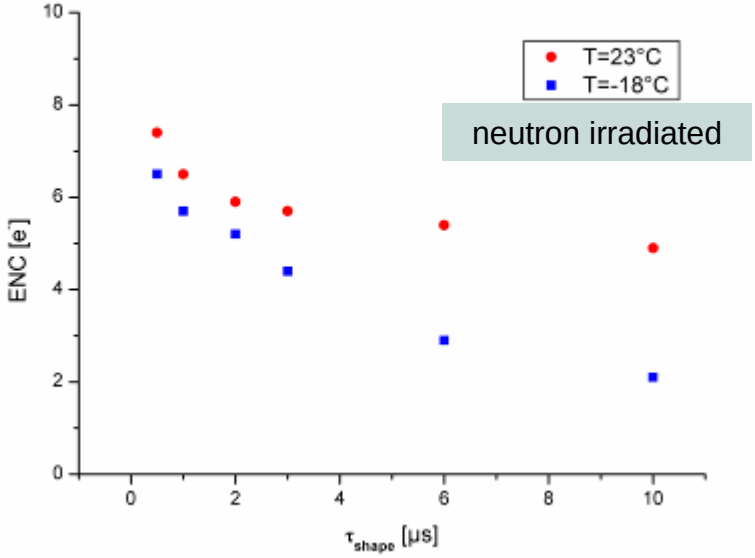
... almost as expected: exponential decrease by factor 2 every 7 K

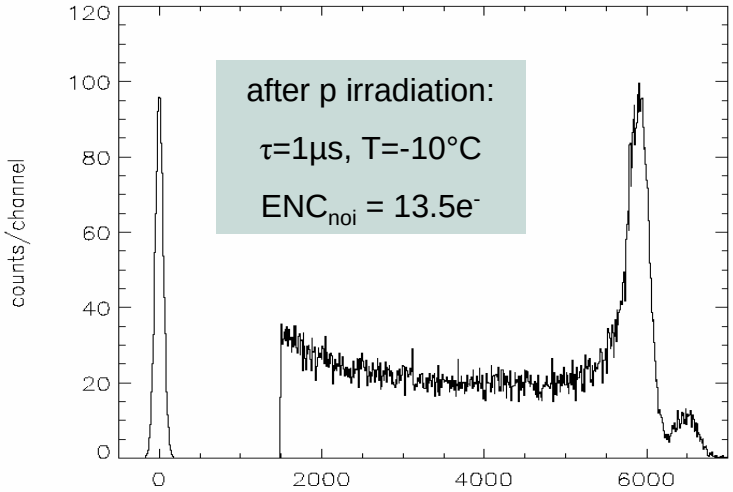


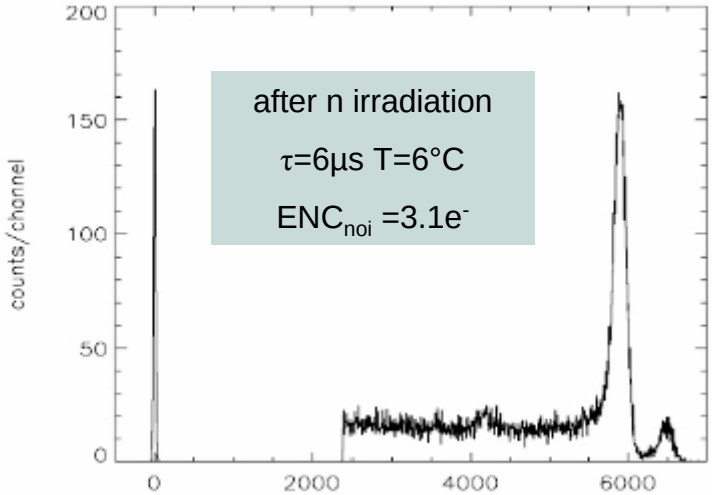
- Some dependence on operation voltages → other contributions than bulk?
- At 0 degC about 10 - 20 e-/µs into internal gate (after 10^{12} p/cm^2)
- expected noise contribution for the first layer (50µs int. time): 20-30 e^- ENC

Spectroscopic Performance





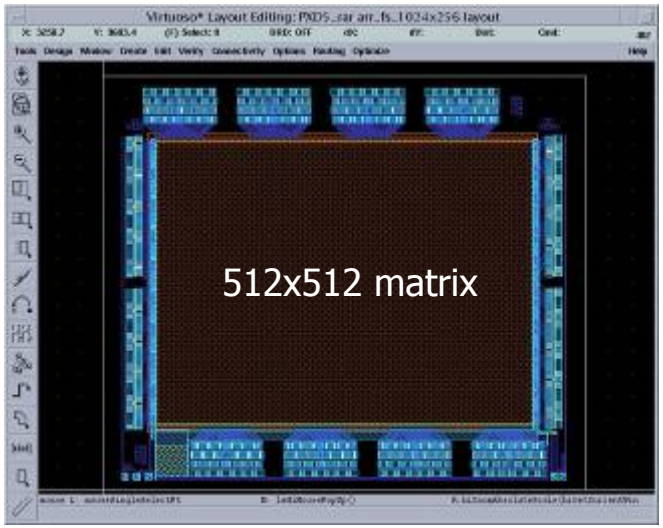


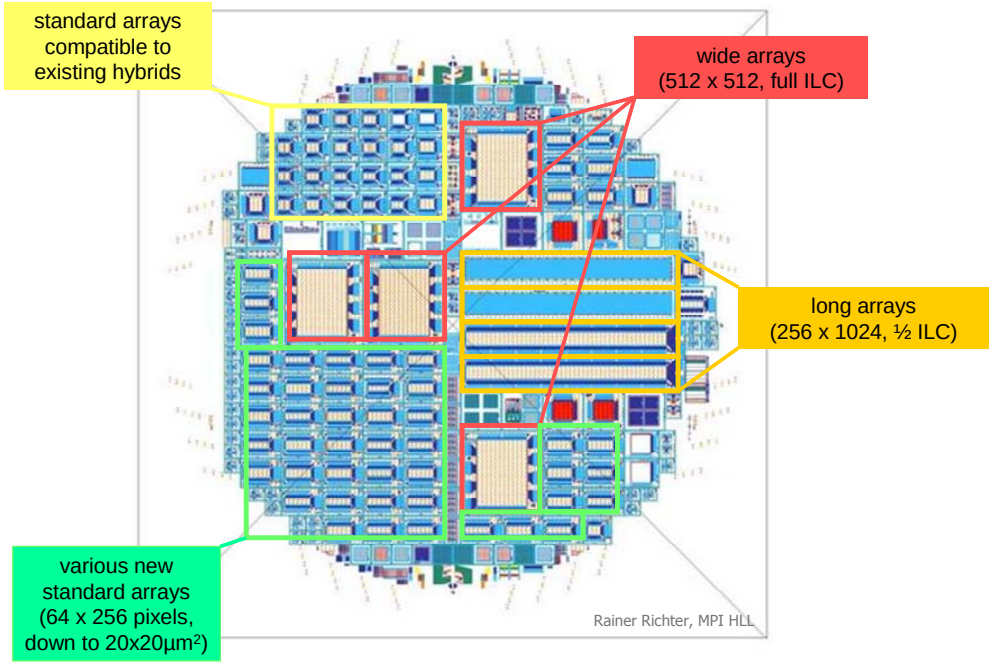


New DEPFET Generation 'PXD5'

- Mostly use 'baseline' linear DEPFET geometry
- Build **larger matrices**
  Long matrices (full ILC drain length)
  Wide matrices (full Load for Switcher Gate / Clear chips)
- Try new DEPFET variants:
  reduce **clear voltages** (modified implantations, modified geometry)
  Very **small** pixels (20µm x 20µm)
  - Increase internal **amplification** (g_q)
- Add some bump bonding test structures

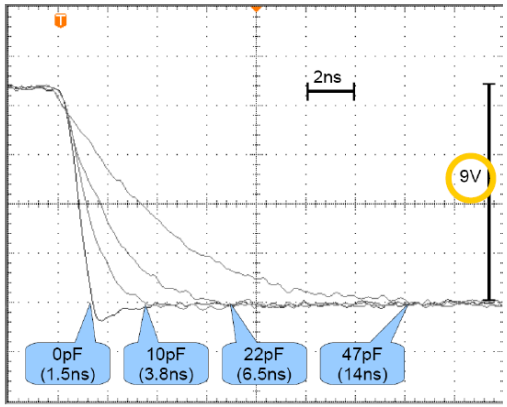
Production almost done!
→ June 2007



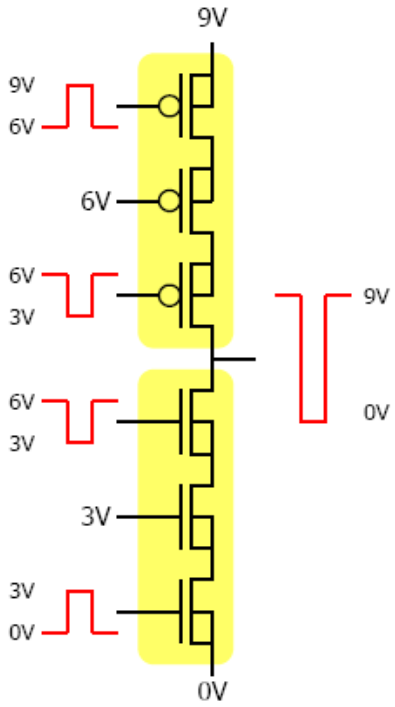


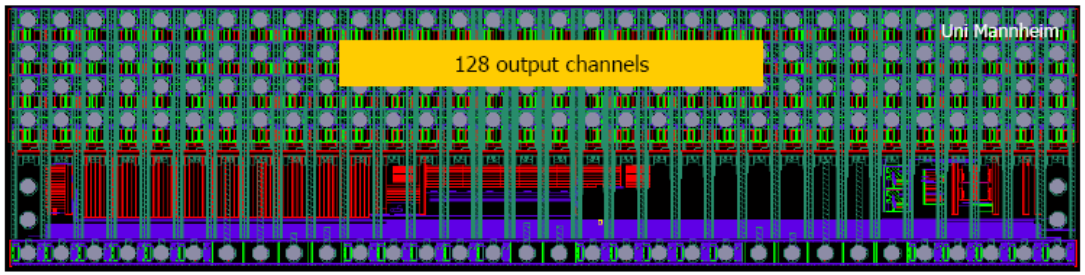
Switcher III

-: Radiation hard (AMS 0.35 mm, layout)
-: up to 10V swing (-> stacked transistors)
-: Low power ("0" standby current)
-: Fast settling (<4ns at 10 pF)
-: Compact layout (1.24 x 5.8 mm^2)
-: Test chip produced → rad. tolerance tested > 600kRad!
-: Full chip produced and tested



9V distributed over 3 transistors with 3V -> rad hard. technology possible

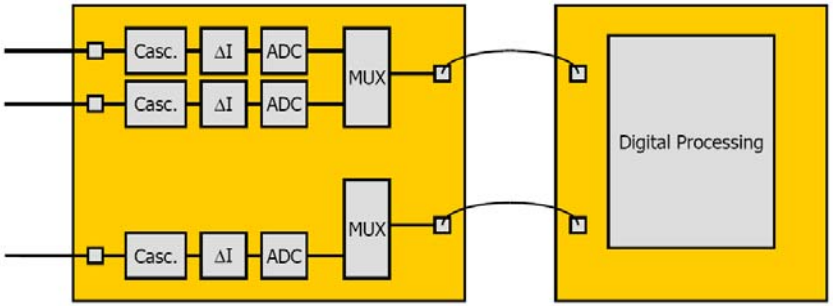




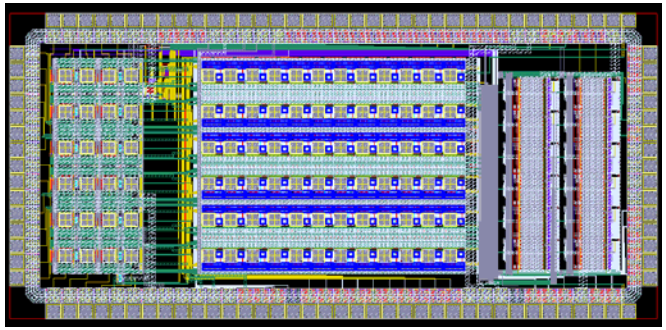
(Uni Mannheim)

A new r/o chip - DCD1

DCD: **D**rain **C**urrent **D**igitizer



Test chip: 6X12 channels (pixels)



submitted (UMC 0.18), April 2007

what is new?

-: improved input cascode (regulated) and current memory cells

-: digital hit processing done with 2nd chip/FPGA

-: designed for 40 pF load at the input (1st layer ILC VTX)

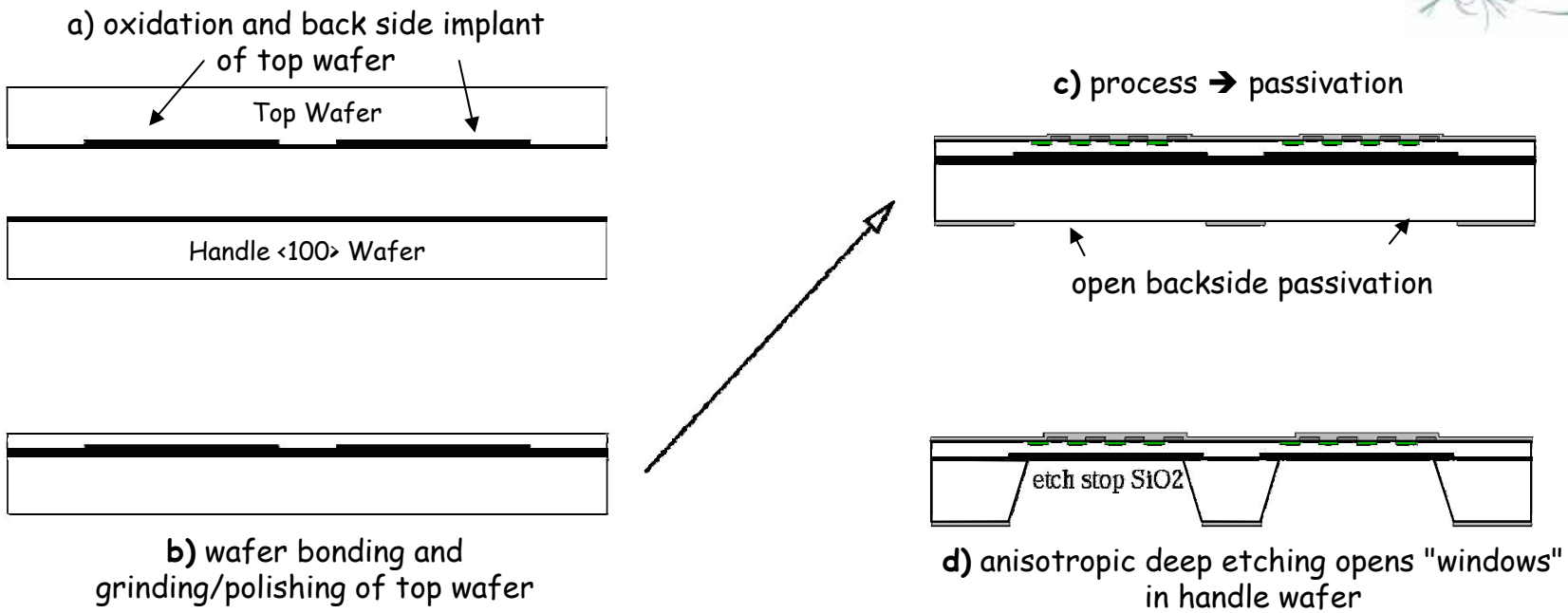
-: f/e noise: 34nA@40pF, 17nA@10pF, add 37nA for memory cells→ **50nA@40pF**
→ at 40pF with g_q=500pA/e → **100 e- ENC in total**

-: 2 current based ADCs per pixel, 8 bit

-: layout for bump bonding, rad. hard design

(Uni Mannheim)

Thinning Technology



New: **150mm** Ø wafers!

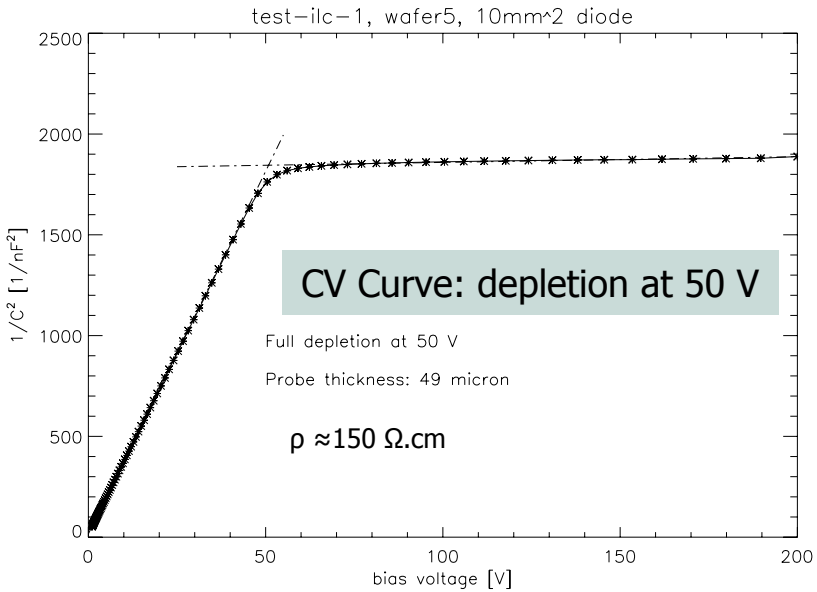
New: Wafer bonding and thinning in **industry**

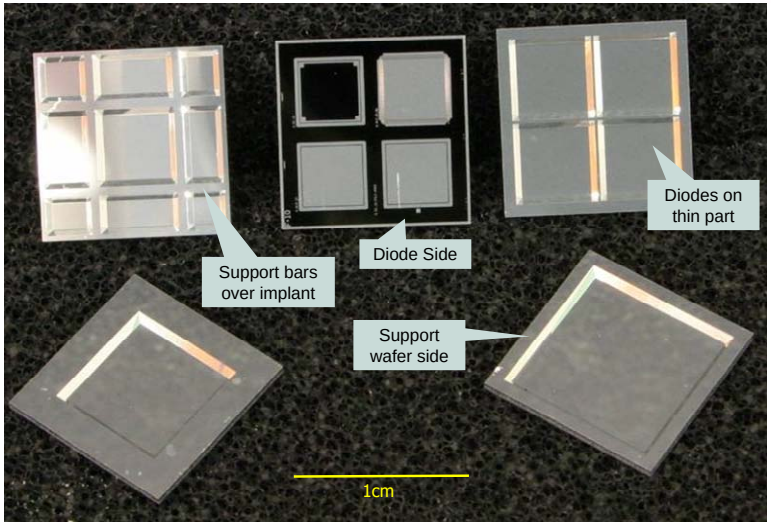
New: Compatibility with the main production line tested

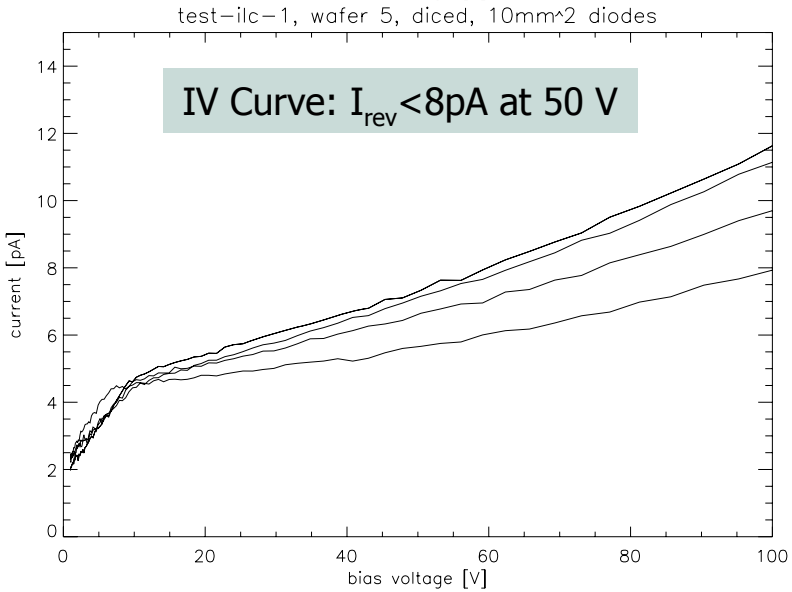
So far: mechanical samples & test structures on SOI wafers

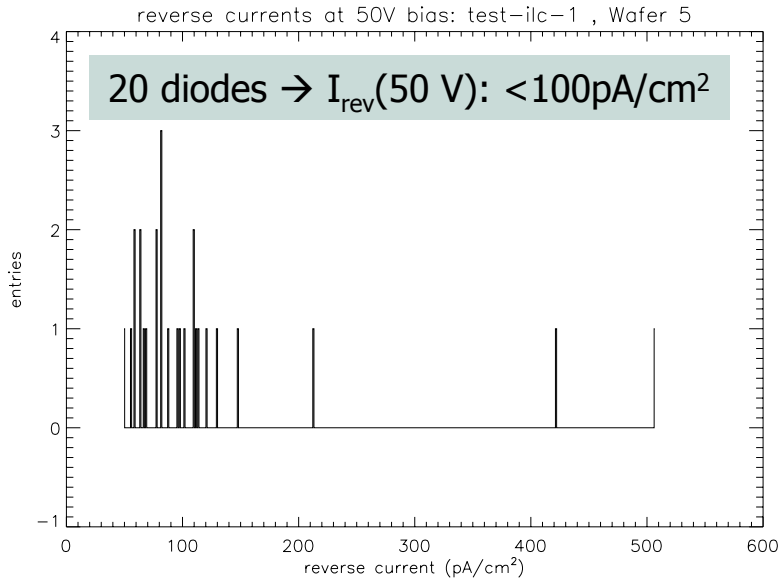
Plans 2007: production of thin (50, 100, and 150 µm) ATLAS pixel sensors for sLHC upgrade

PiN Diodes on thin Silicon

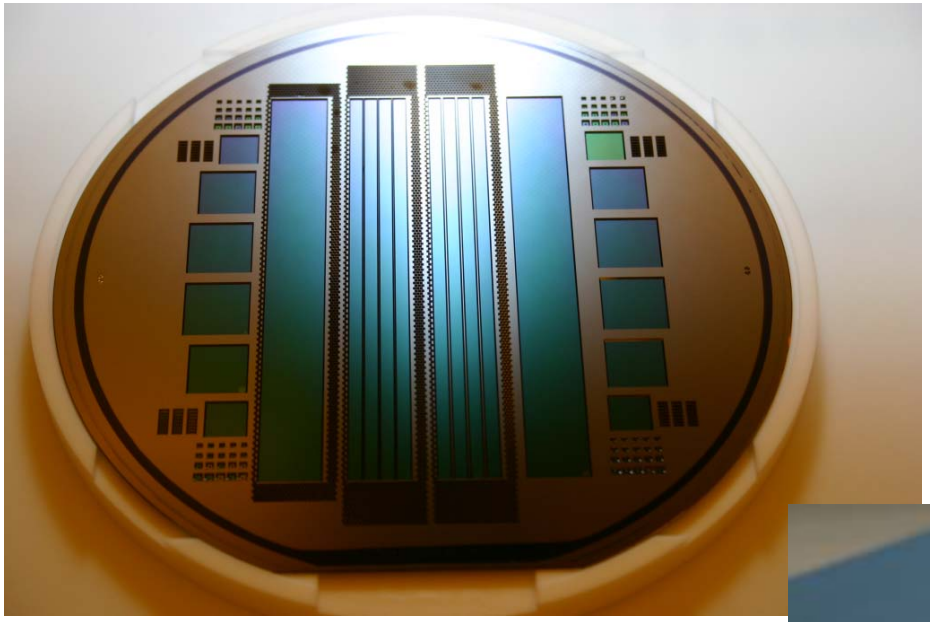


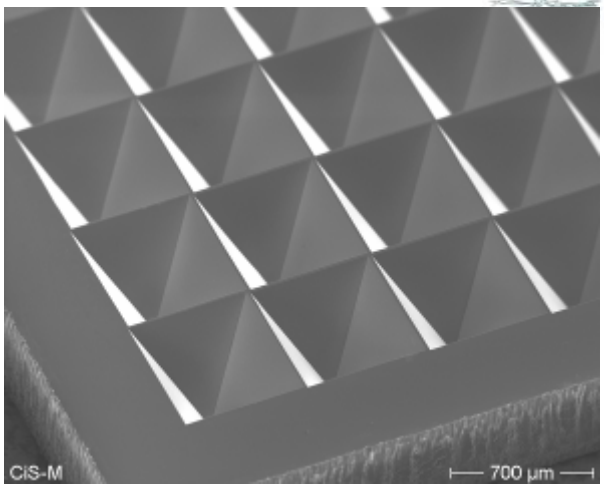


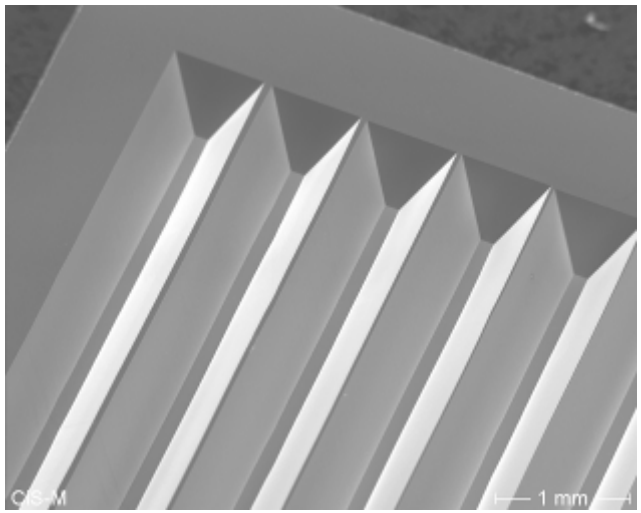


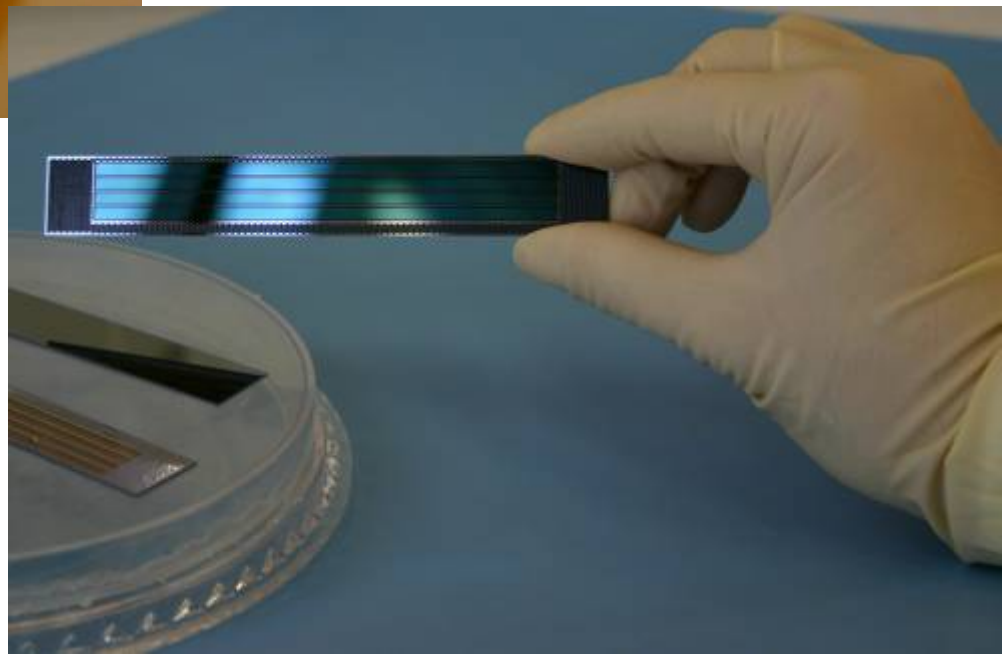


Thinning : mechanical samples

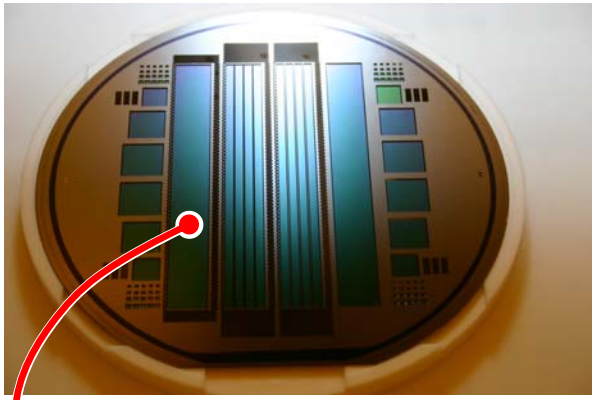


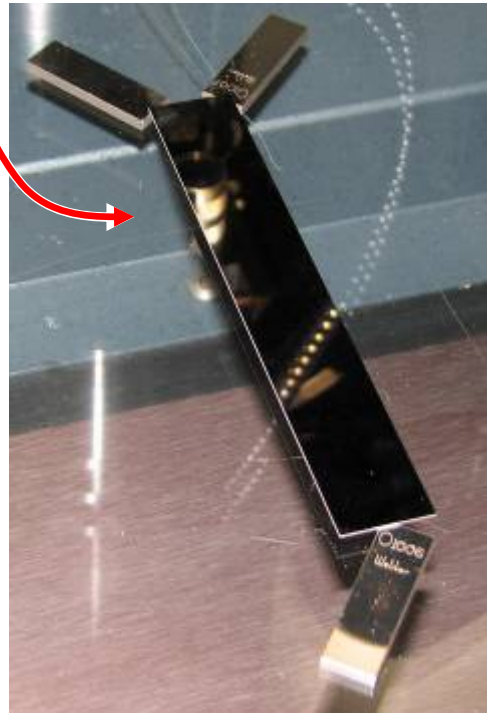






Thinning : mechanical samples

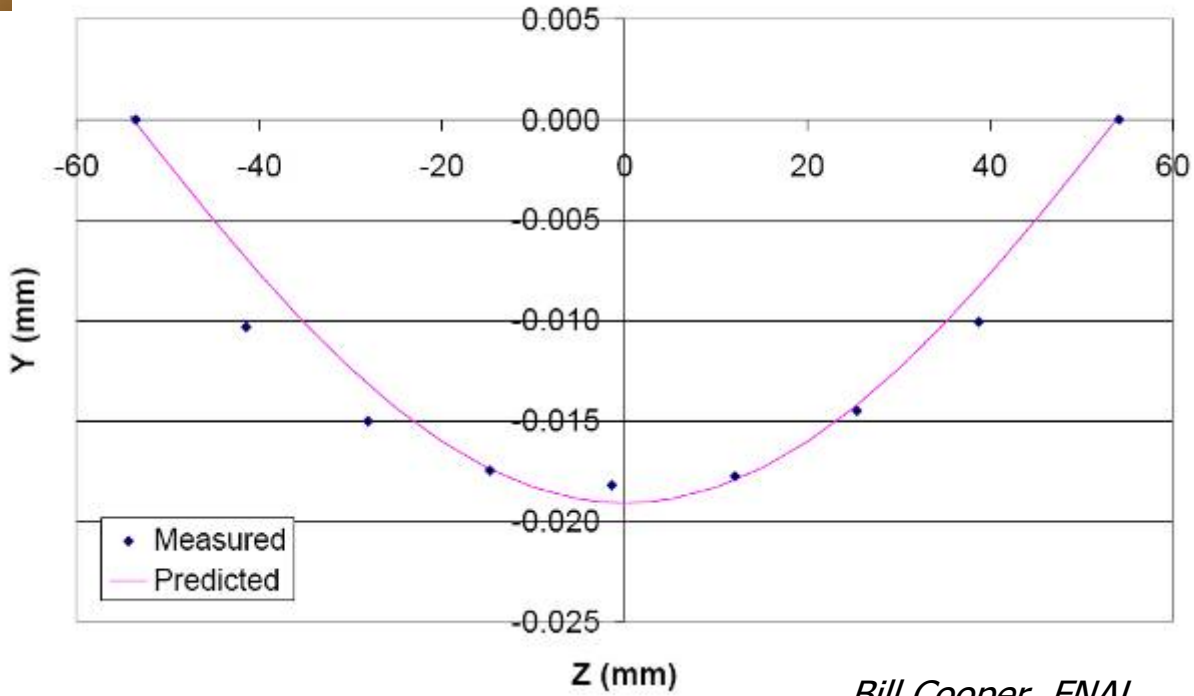




full size 1st layer module:

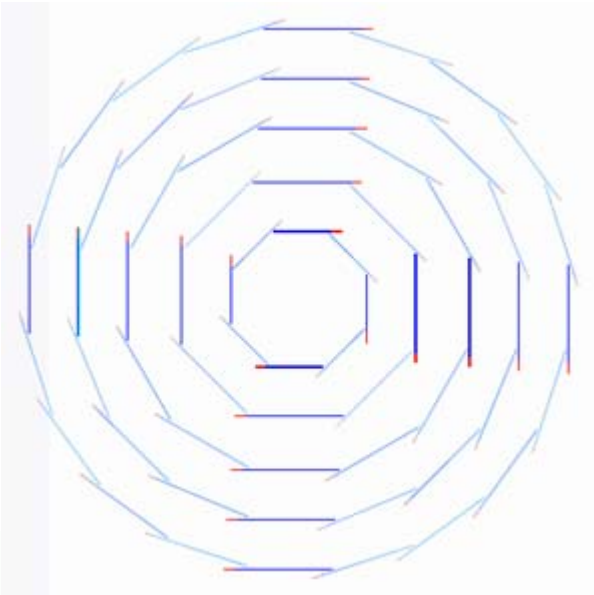
100x13 mm² sensitive area, 50 µm thin, 400 µm frame, no support bars

→ 20 µm deflection due to gravity



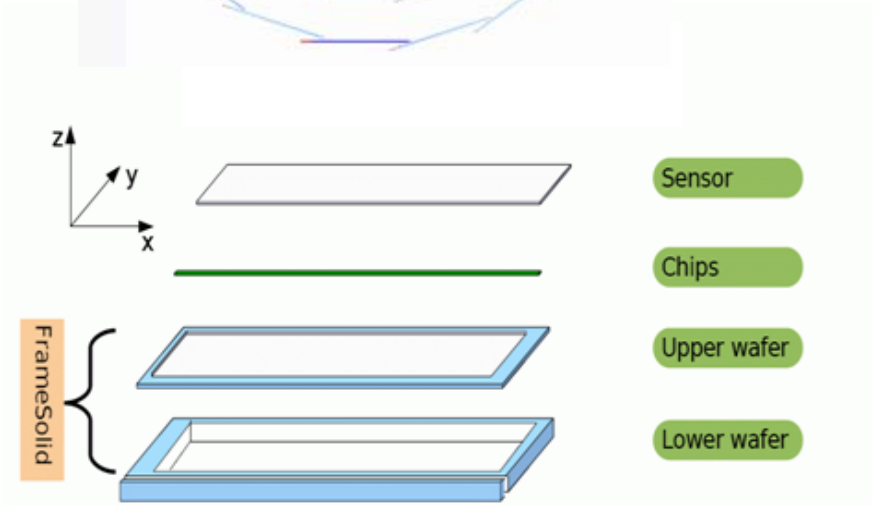
Bill Cooper, FNAL

Simulation: LDC Geometry description

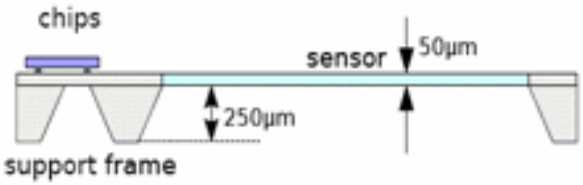


Sensitive layer thickness = 50 μm
Pixel size = 25×25 μm^2

	Radius (cm)	Ladders	Length (cm)
1	1.5	8	10.0
2	2.6	8	2 × 12.5
3	3.8	12	2 × 12.5
4	4.9	16	2 × 12.5
5	6.0	20	2 × 12.5



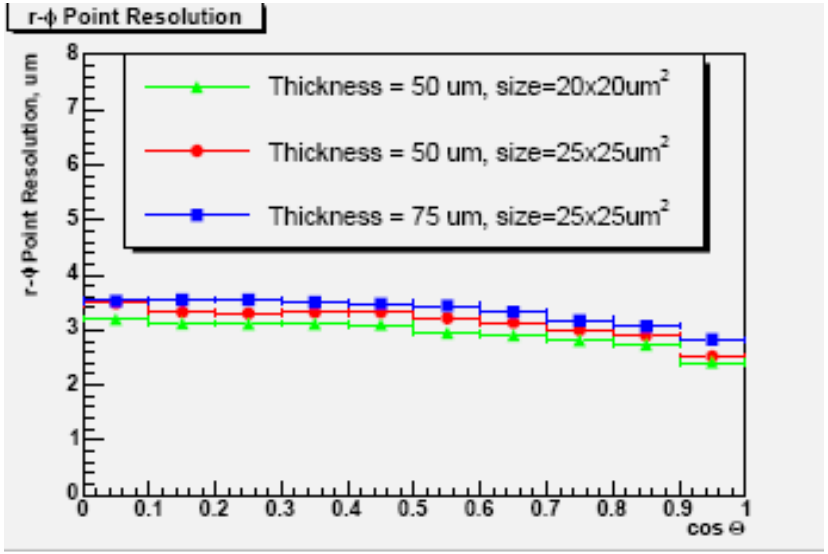
→ LDC ladders with support frames

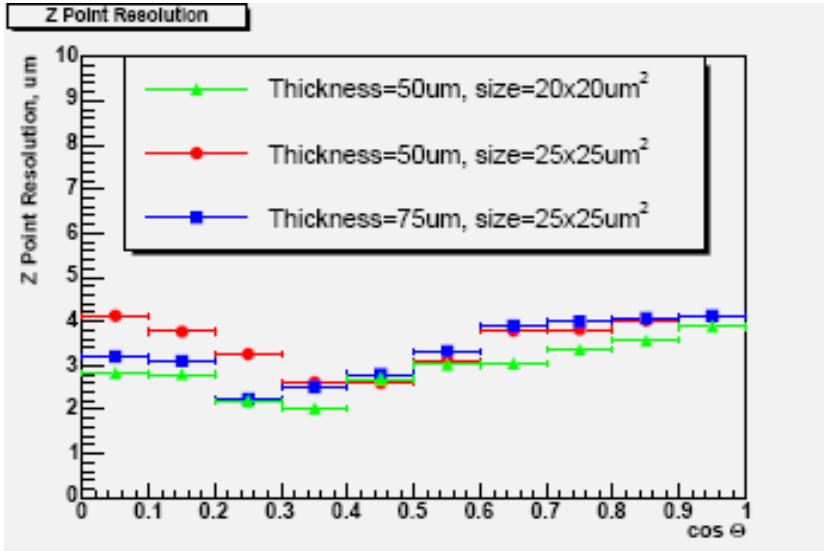


Material up to first layer : beam pipe (500 μm beryllium)

MC Studies

Spatial resolution for 50 mm thick 25 x 25 mm^2 pixels: <3.5 mm (r-φ), <4.0 mm (z)

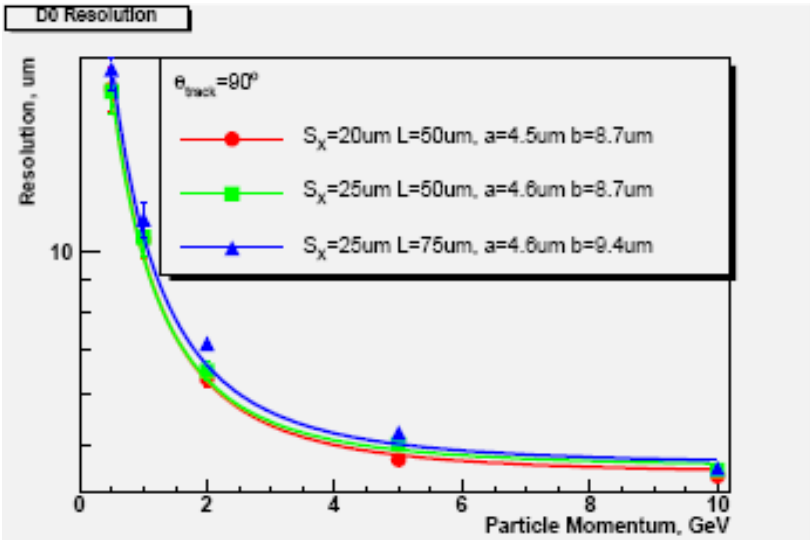




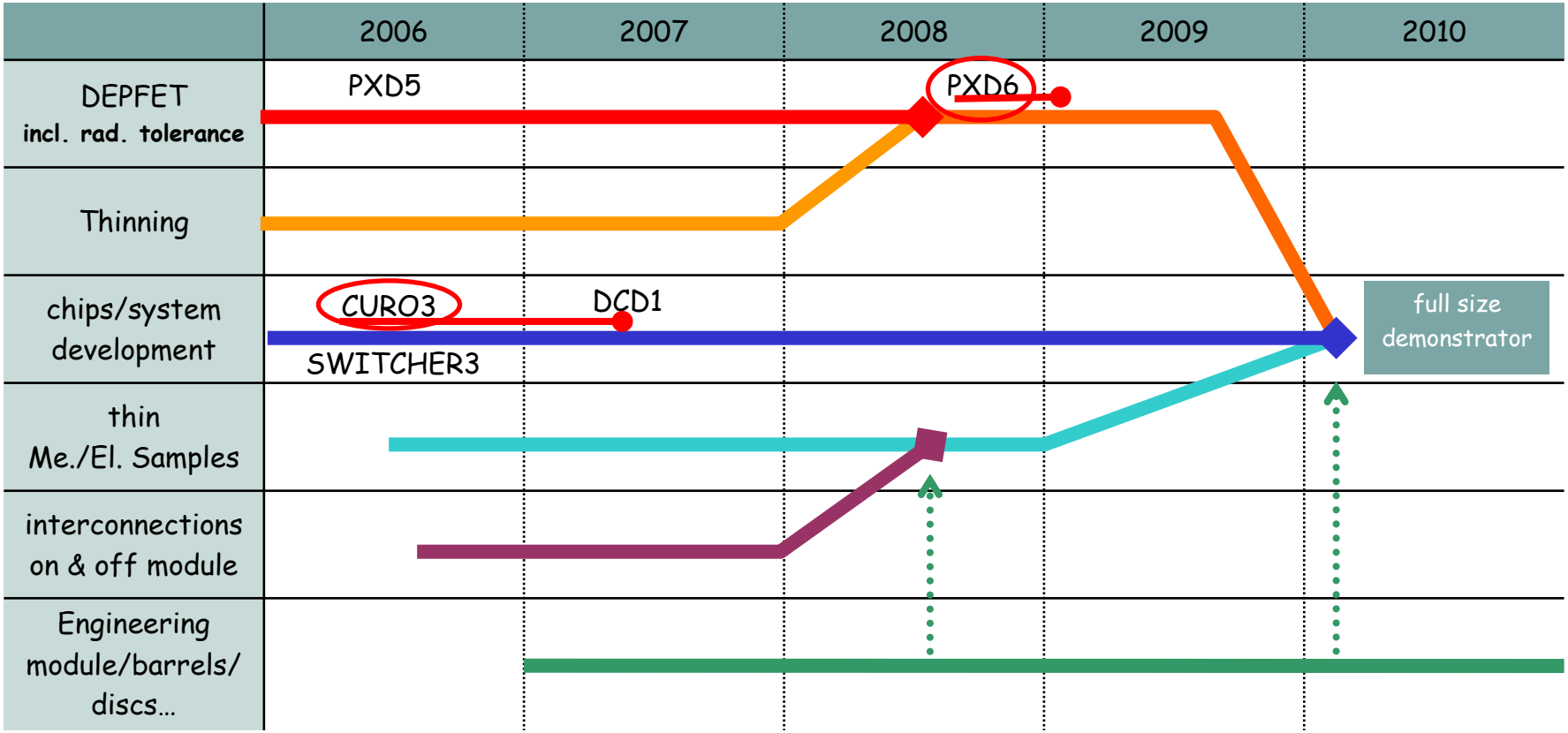
Impact parameter resolution
(5 layers, frames, 500 mm Be beam pipe)

$$\sigma(IP)_{r\text{-}\phi} = 4.5\ \mu m \oplus \frac{8.7\ \mu m}{p(GeV/c)\ \sin^{3/2}\theta}$$

ILC requirements fulfilled



~~Roadmap~~ Subway map towards a thin demonstrator



Summary

- ✓ Preparations for the **new DEPFET generation** are in full swing:
  - ✓ New Sensors, larger matrices, with improved gain expected end of June 2007
  - ✓ Steering chip Switcher operational and rad. hard
  - ✓ New r/o chip submitted
- ✓ **Radiation tolerance** of basic pixel cell **proven** for fluences far beyond the ones expected at the ILC .
- ✓ **Thinning** technology at the door step to migrate to the **production line**. Excellent results using a commercial supplier for the engineered SOI wafers.
- ✓ **MC Studies** show the feasibility of the current module concept and pixel size.

It remains a challenging task but we don't see any show stoppers and are on schedule for a thin "full size" demonstrator by ~2010!