LumiCal & BeamCal

Readout Electronics

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Outline

- Introduction
- Front-end electronics challenges
- LumiCal : readout architecture, front-end design & simulations, ADC design & simulations, layout
- BeamCal: readout architecture, front-end design, fast feedback, ADC and memory issues, radiation hardness, power consumption
- Summary & milestones

Detector specs

- Wide signal range: from ~2 fC in calibration mode up to ~15 pC for LumiCal and ~40 pC for BeamCal in physics mode, 10 bit resolution
- High speed operation: short inter bunch time of ~300 ns and high particle occupancy
- Wide range of sensor capacitance: 10-100 pF for LumiCal, rather constant ~20 pF plus fanout for BeamCal
- Low average power dissipation
- Radiation hardness: an issue for BeamCal, less for LumiCal
- Fast feedback: needed for BeamCal for beam diagnosis

Challenges of front-end

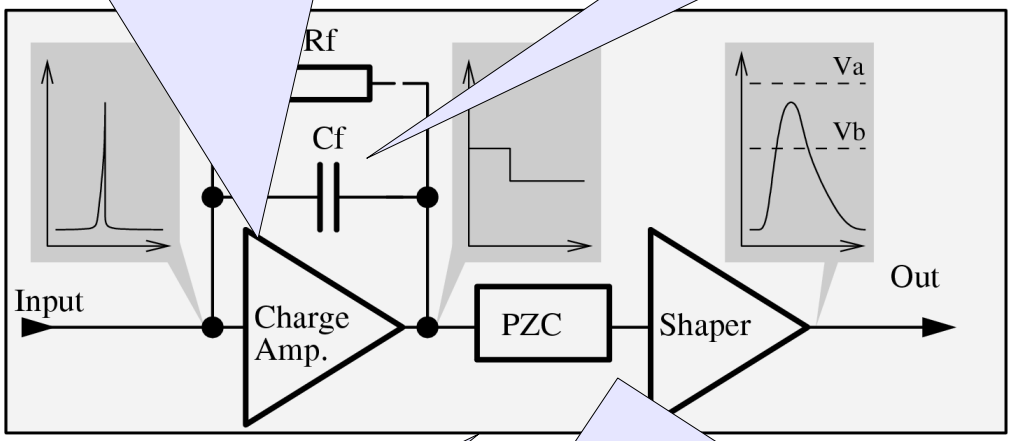
Large C_{det} range 10-100 pF

Calibration mode S/N~10 for MIP

Charge sensitive amplifier

Q_{max} ~ 15 pC (40 pC)

Cf ~ 10 pF (40 pF)



Calibration & Physics mode

Variable gain

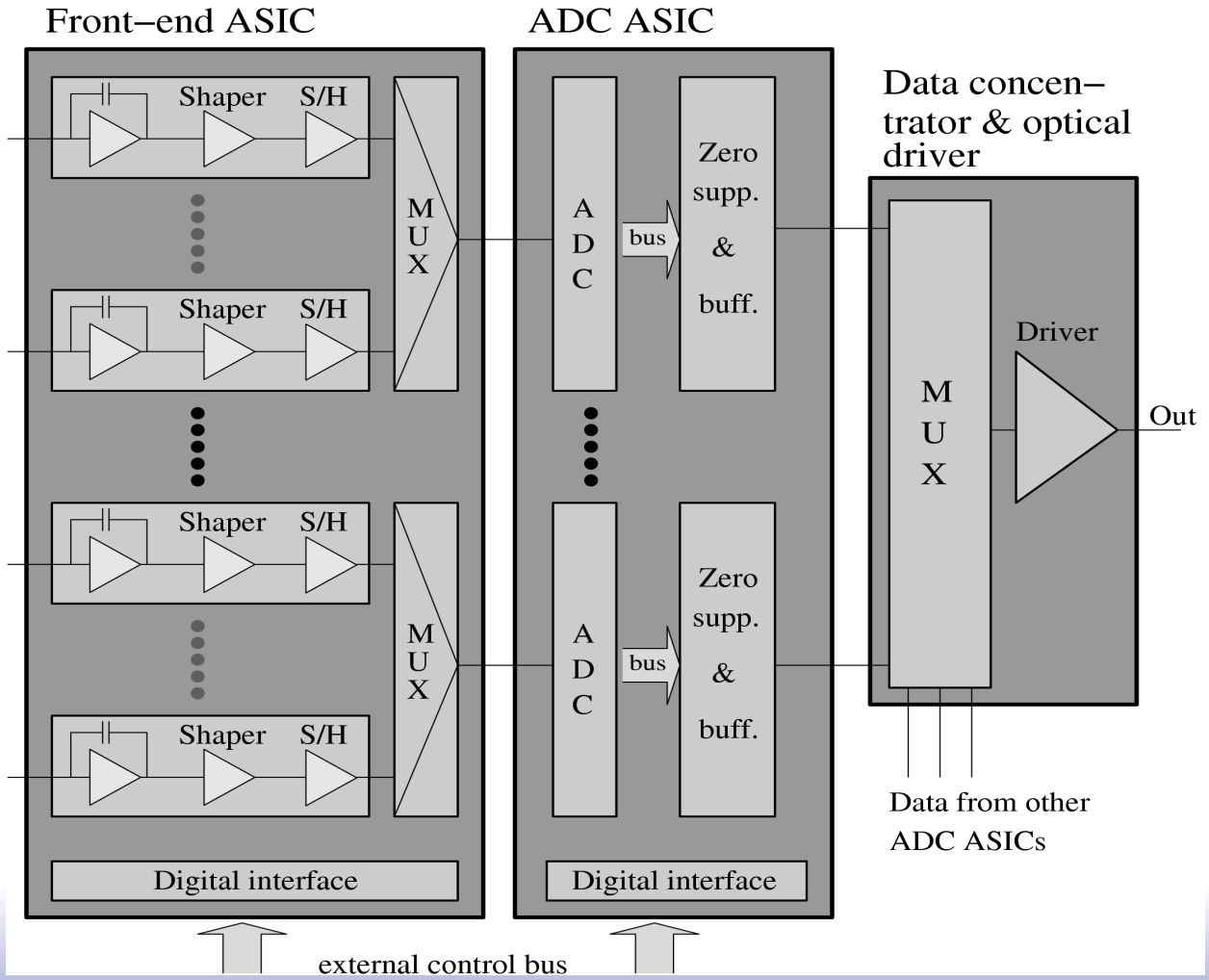
$\Delta t \simeq 300$ ns, high occupancy

LumiCal: PZC +Shaper T_{peak} ~ 60ns

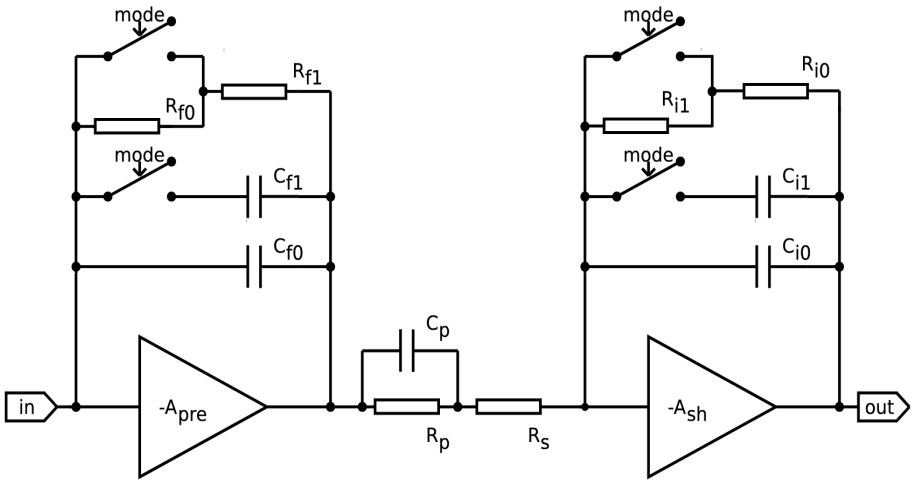
BeamCal: under study

LumiCal readout architecture

- Front-end ASIC with 32-64 channels
- An ADC serving 1-8 front-end channels
- Direct readout
- First prototypes in AMS 0.35 μm

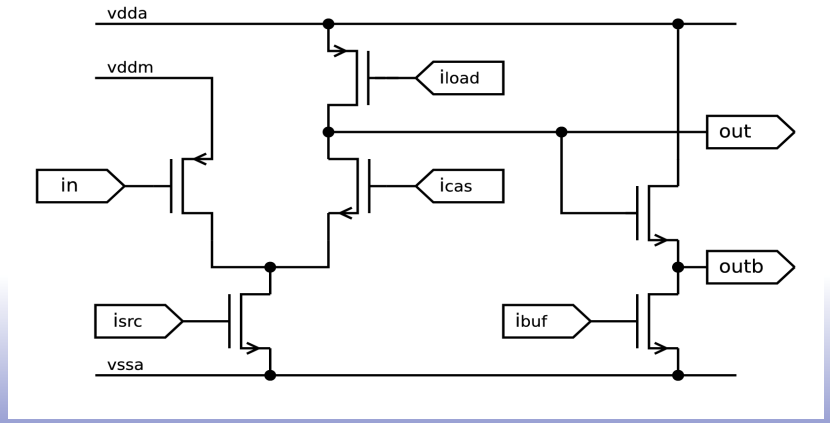


LumiCal front-end electronics architecture

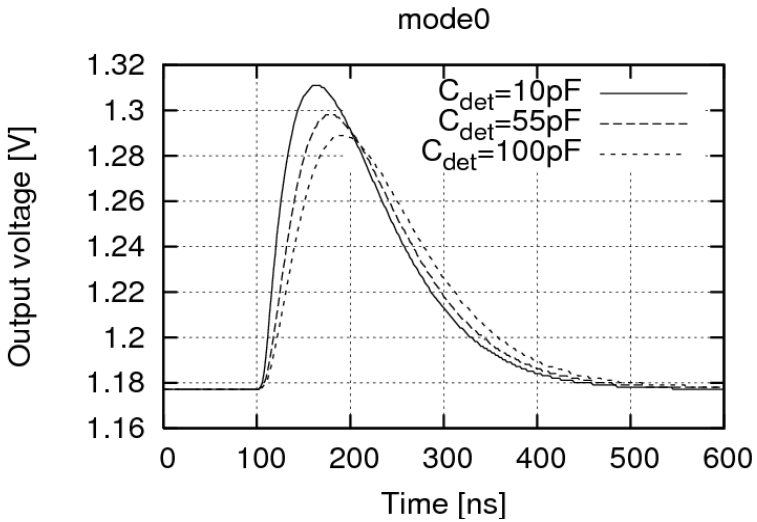


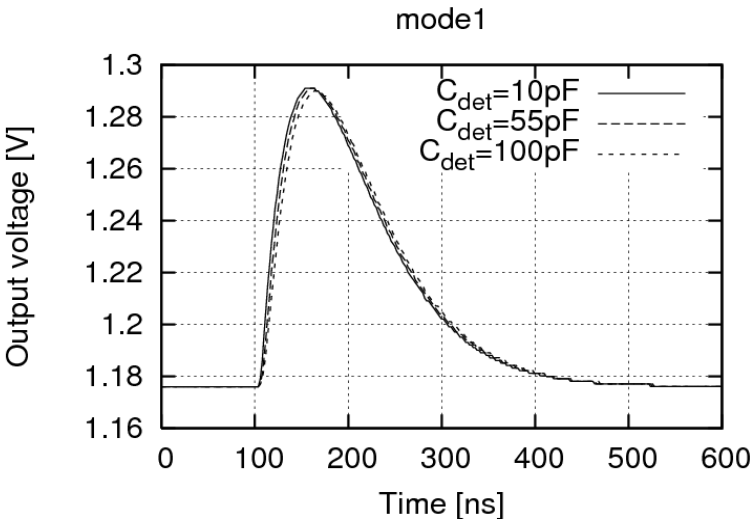
- Preamplifier: Cf~10pF (physics), Cf~0.5pF (calibration), I_{pre}~2.5mA,
- Shaper: 1st order, T_{peak}~60ns, variable gain, I_{sh}~0.5mA

- Both Preamplifier and Shaper designed as folded cascode plus source follower



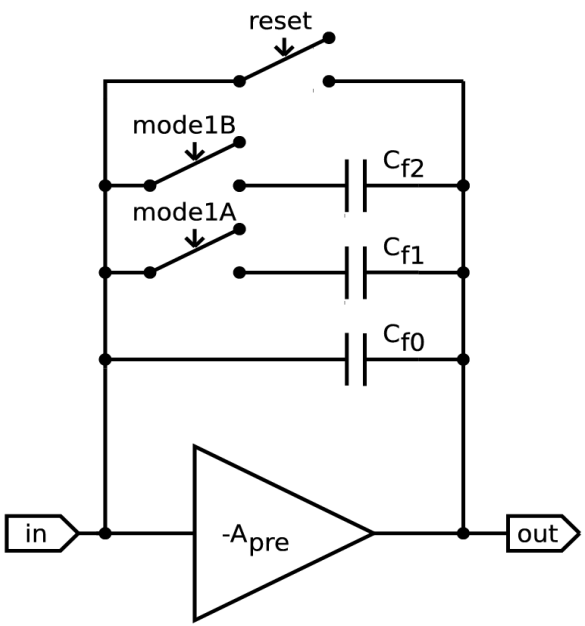
Front-end simulations





- Front-end response in calibration (mode0) and physics (mode1) mode for different C_{det}
- In physics mode the output vs Q_{in} is linear up to ~7 pC and saturates for ~12 pC

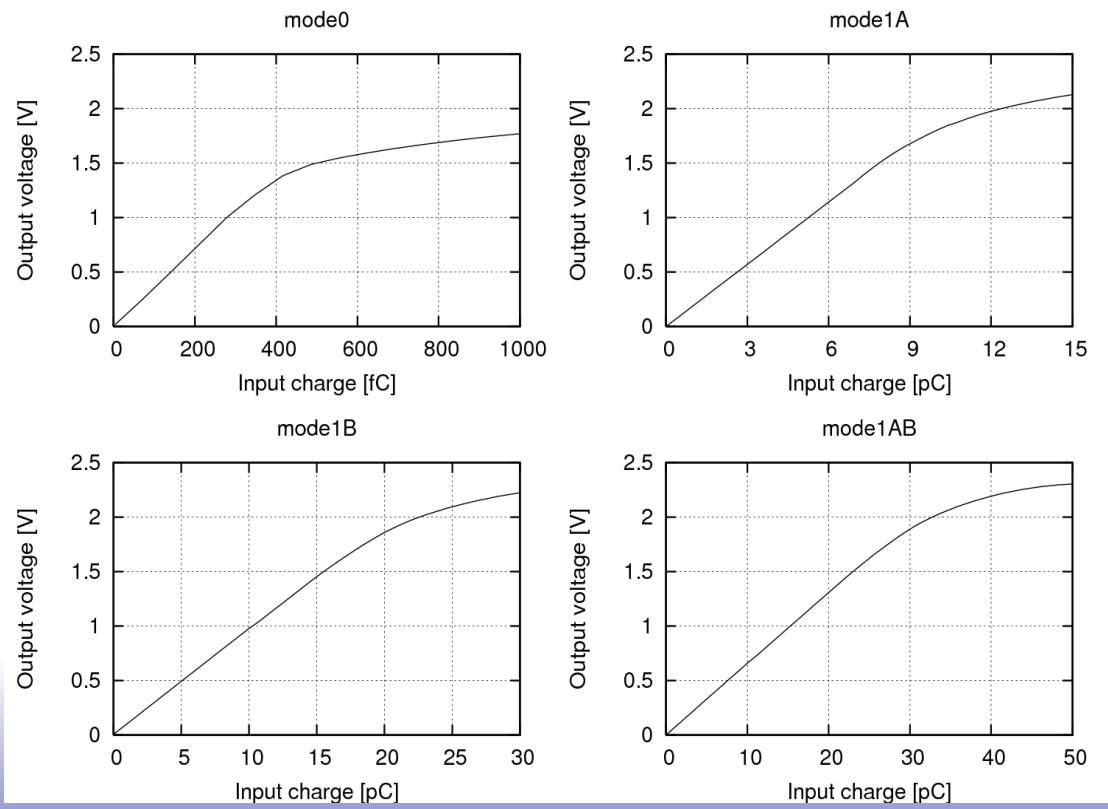
Alternative front-end
Switched-Reset configuration



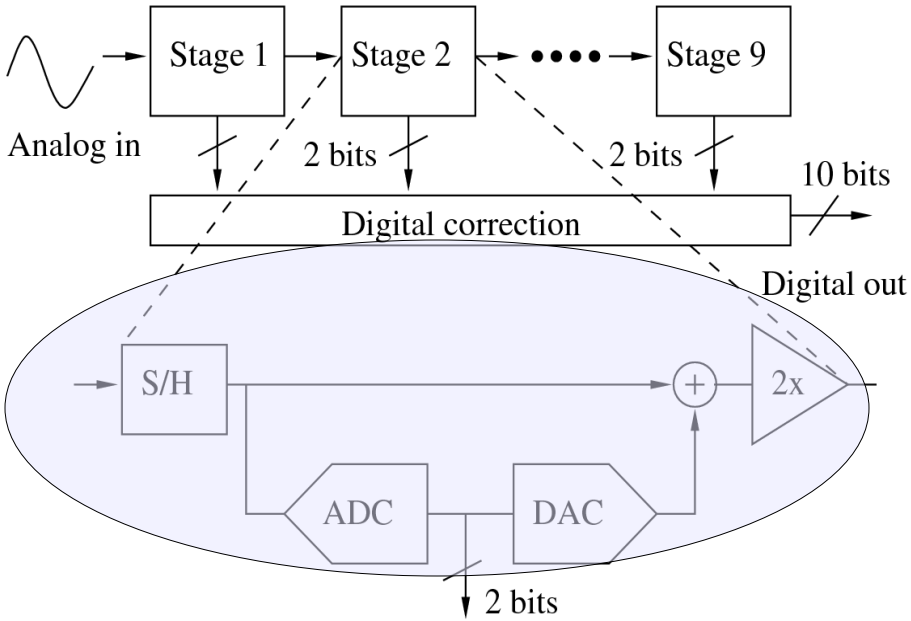
- Single stage
- Wide output range

Output amplitude vs Q_{in}

for different Cf



LumiCal ADC architecture

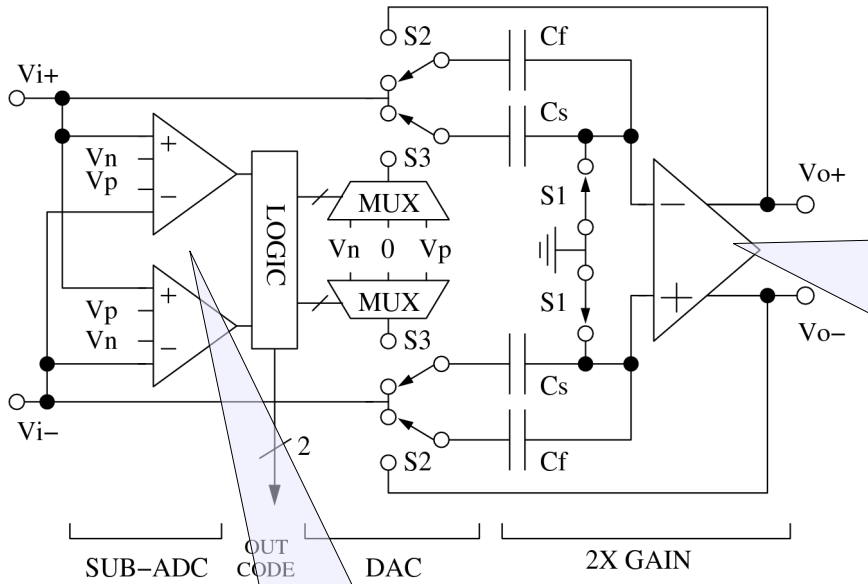


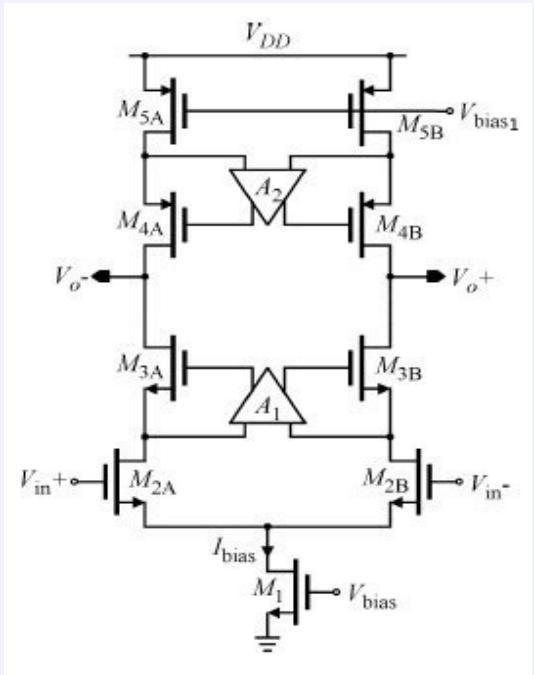
- 10 bit pipeline ADC
- 1.5 bit stage
- Fully differential architecture

Pipeline advantages

- High throughput
- Robustness
- Power efficient
- Reasonable area

1.5 bit stage architecture

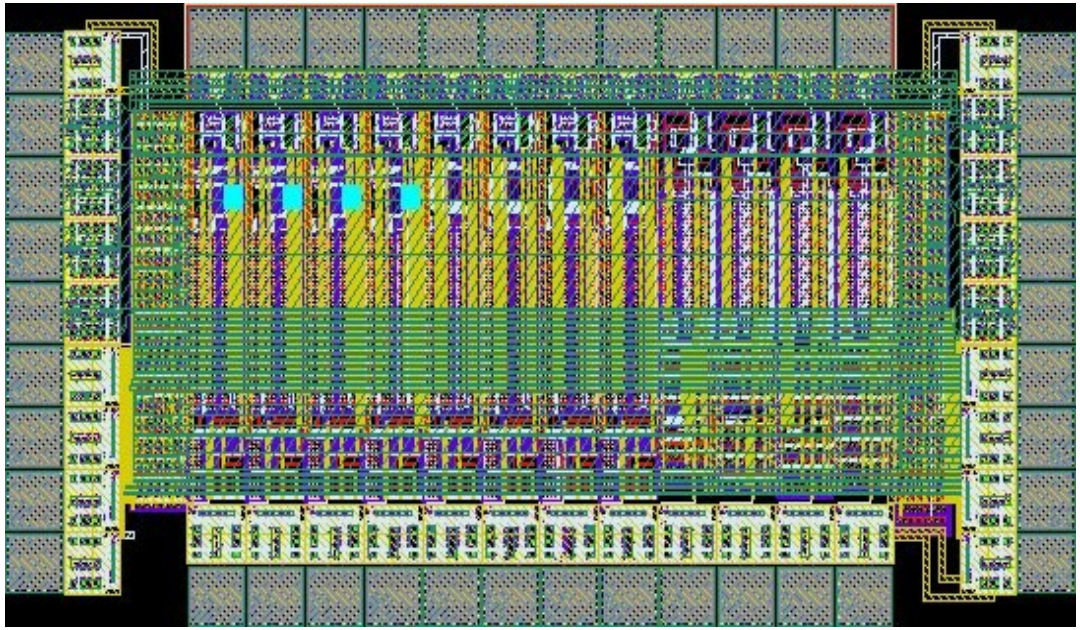




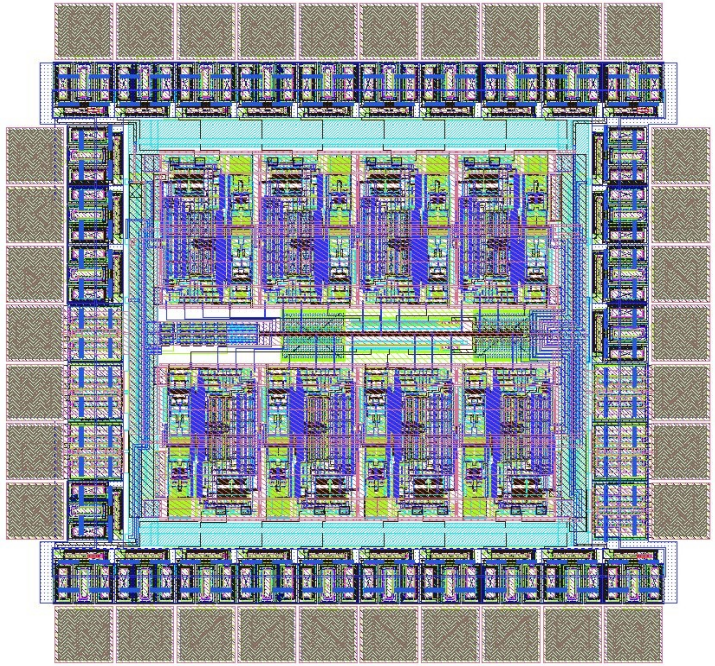
Dynamic latch comparators

Layout of LumiCal ASICs

We have just submitted the prototype ASICs containing front-end and ADC functional blocks

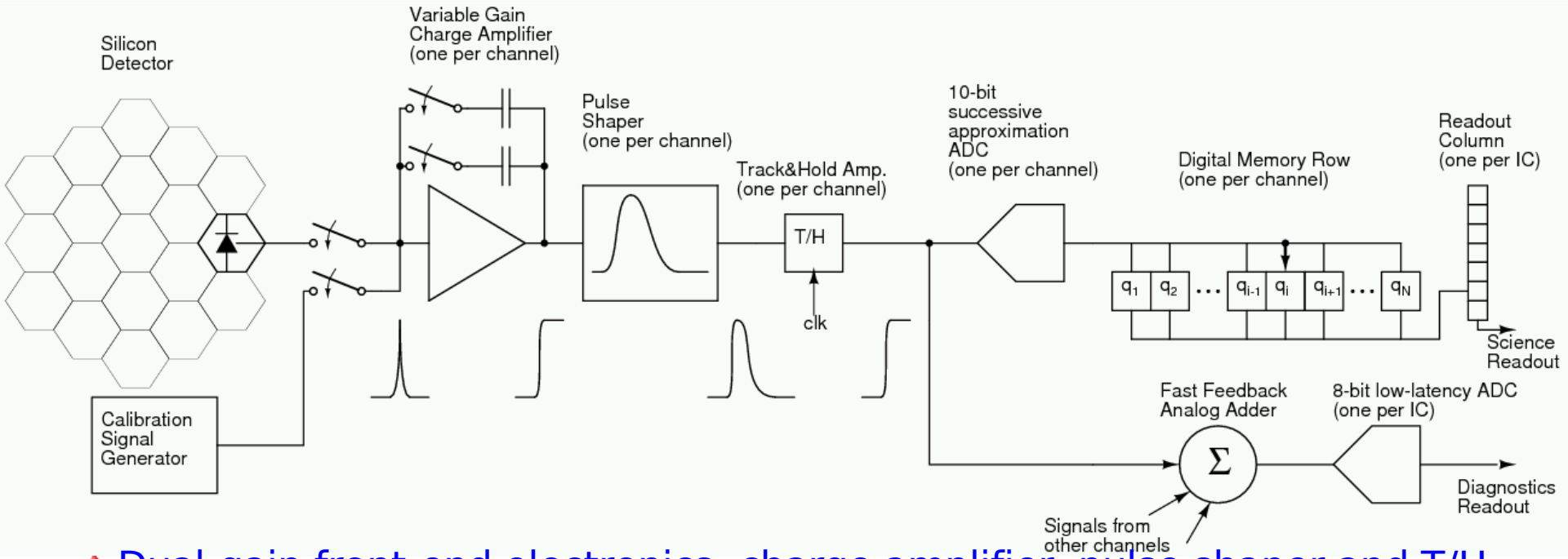


8 channels with continuous shaping and 4 channels with switched-reset



8 pipeline 1.5 bit stages

BeamCal readout architecture



- Dual-gain front-end electronics: charge amplifier, pulse shaper and T/H circuit, 32 channels per ASIC
- Successive approximation ADC, one per channel
- Digital memory, 2820 (10 bits + parity) words per channel
- Analog addition of 32 outputs for fast feedback; low-latency ADC
- Prototype in 0.18-μm TSMC CMOS technology

ADC and memory issues

- ADC power consumption depends lightly on the number of ADCs
  - one channel per ADC is simple in terms of operation
  - many channels per ADC are efficient in terms of area
  - successive approximation ADCs present a balanced tradeoff, could eventually assign a single channel per ADC without a significant increase in area; currently under study
- Memory choice: analog or digital?
  - Analog memory problems:
    - high droop rate due to switch leakage, especially after irradiation
    - radiation-tolerance techniques are not simple nor flexible
  - Digital memory problems:
    - more area
  - Digital memory will be used mainly due to flexibility

Radiation hardness requirements

- Chip must be able to tolerate 1Mrad(SiO_2) total ionizing dose (TID)
- TSMC018 is naturally tolerant to TID, but some sensitive circuits in the chip require additional protection
- This can be done by using mitigation techniques:
  - Enclosed-layout transistors
  - Guard rings
- Consequences in circuit design:
  - Power consumption increases by 2× or more, depending on the circuit
  - Chip area increases by 2.5× in some circuits
- First prototype will not be radiation-tolerant, but will allow to:
  - assess the technology tolerance to radiation
  - detect the most radiation sensitive circuits

Power consumption estimation per IC

- Front-end circuits: 1.8mW
- ADC: 0.9mW
- Memory: 0.03mW
- LVDS drivers: 1.8mW

- Average power consumption per IC: 4.5 mW

Milestones

- Now - first prototypes submitted
- ~March 2008 – tests finished, submission of ADC prototypes and front-end prototypes including S/H
- ~December 2008 – tests finished, submission of complete front-end and ADC prototypes
- ~June 2009 - tests of prototypes completed

- August 2007-July 2008: Front-end designed, ADC designed, Memory designed, Fast feedback designed, Bias and supporting circuits, Circuit layout complete,Verification complete
- Sept.-December 2008: Prototype ready, Prototype tests complete