Readout electronics for LumiCal detector

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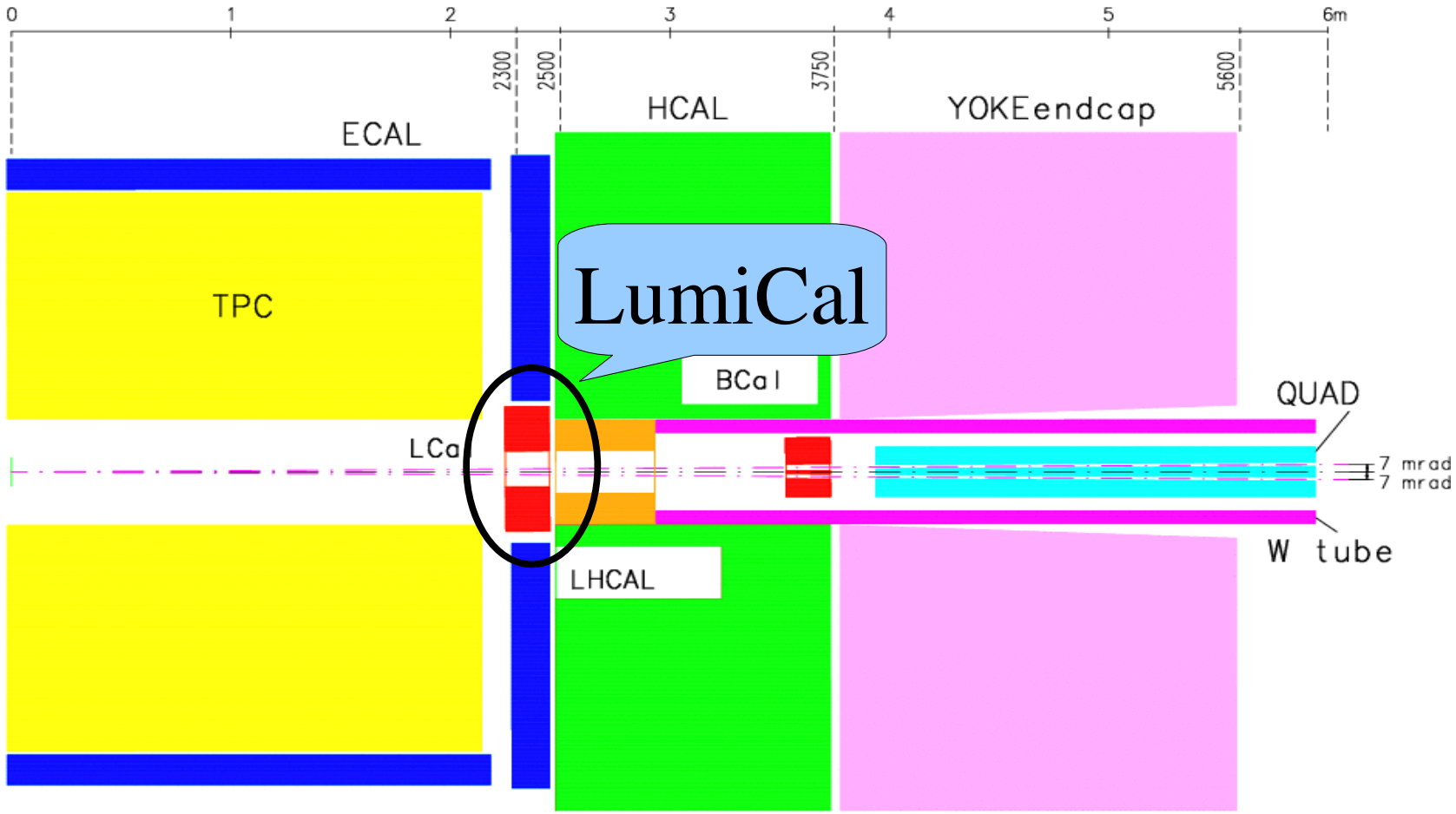
Outline

- Introduction
- Challanges for LumiCal electronics
- Readout architecture
- Front-end design & simulations
- ADC design & simulations
- Summary & milestones

FCAL architecture

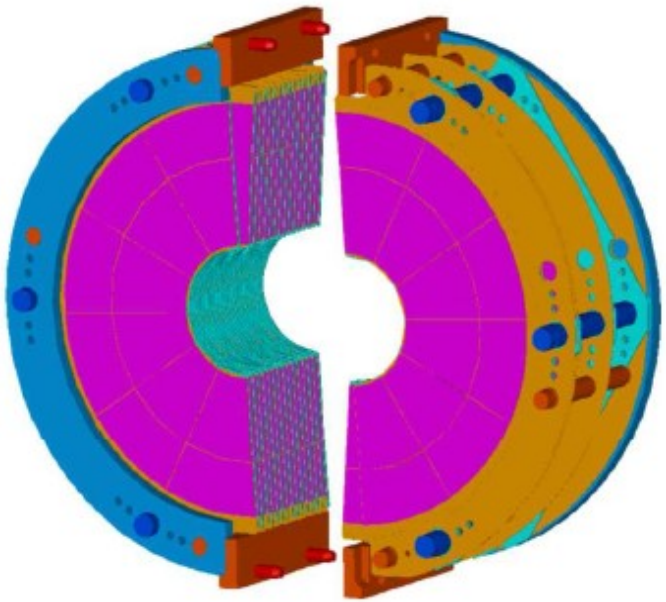


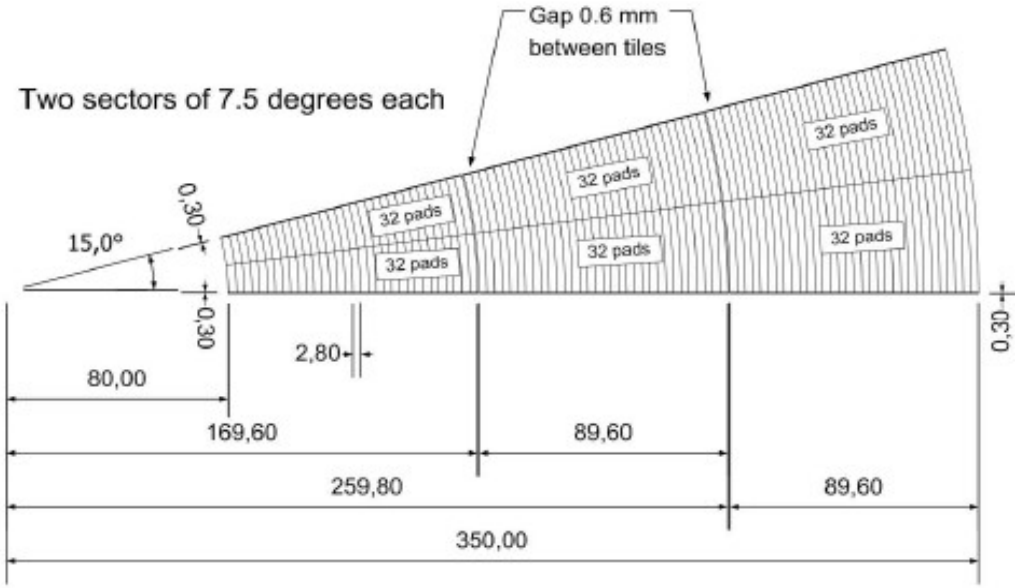
LCal R_i = 100 mm, R_o = 350 mm, z_1 = 2270 mm, z_2 = 2470 mm

LHCAL R_i = 120 mm, R_o = 290 mm, z_1 = 2500 mm, z_2 = 2950 mm

BCal R_i = 20 mm / 15 mm, R_o = 165 mm, z_1 = 3550 mm, z_2 = 3750 mm

LumiCal architecture





- LumiCal ⇔ 30-40 discs of silicon detectors
- Disc ⇔ 48 azimuthal (7.5°) sectors
- Sector ⇔ $R_{in\text{-}out}$ = 8-35 cm, built of ~100 radial pads
- Channel number estimation 2*30*48*100~300000

Detector specifications

- Wide sensor signal range: from ~2 fC in calibration mode up to ~15 pC in physics mode
- High speed operation: ~300 ns between bunches and high occupancy
- Wide range of sensor capacitance: 10-100 pF
- Low average power dissipation requested

Challanges of LumiCal front-end

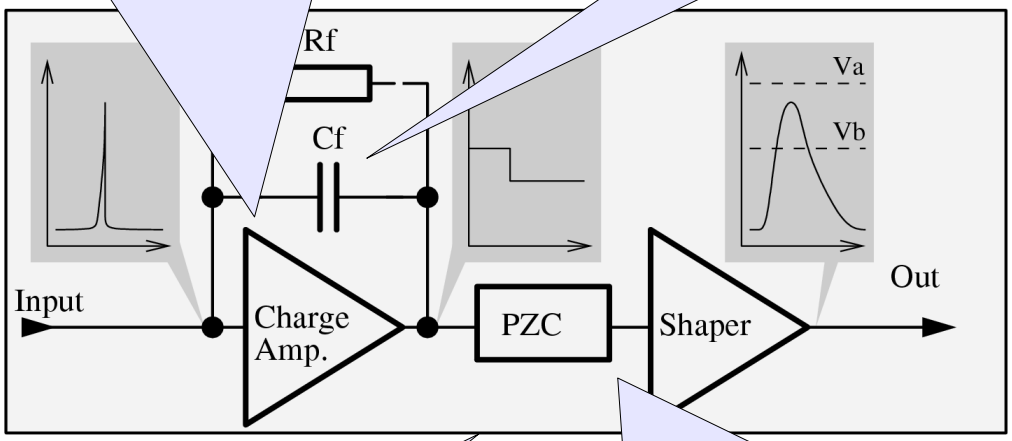
Large C_{det} range 10-100 pF

Calibration mode S/N~10 for MIP

Charge sensitive amplifier

Q_{max} ~ 15 pC

Cf ~ 10 pF



Calibration & Physics mode

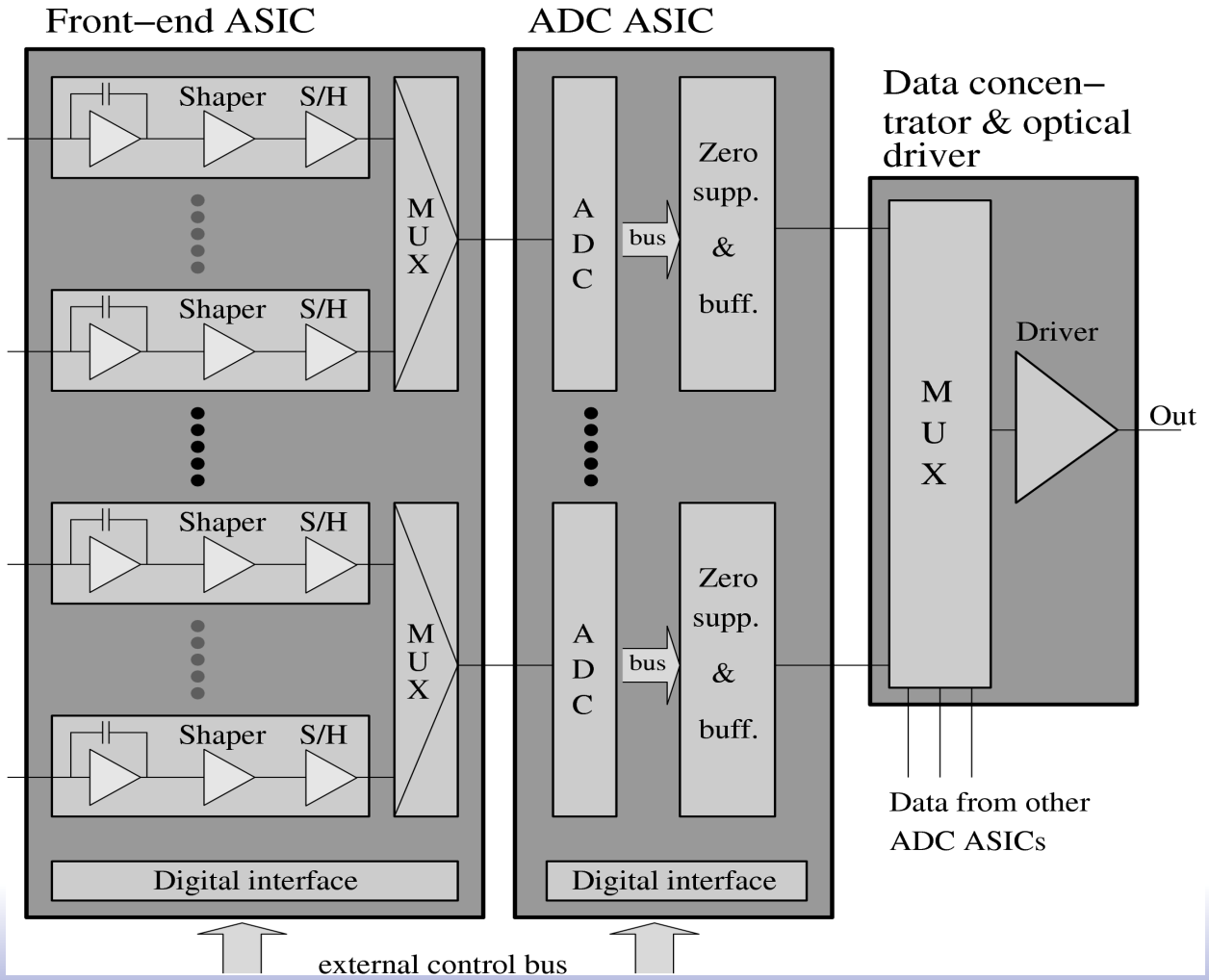
Variable gain

$\Delta t \simeq 300$ ns, high occupancy

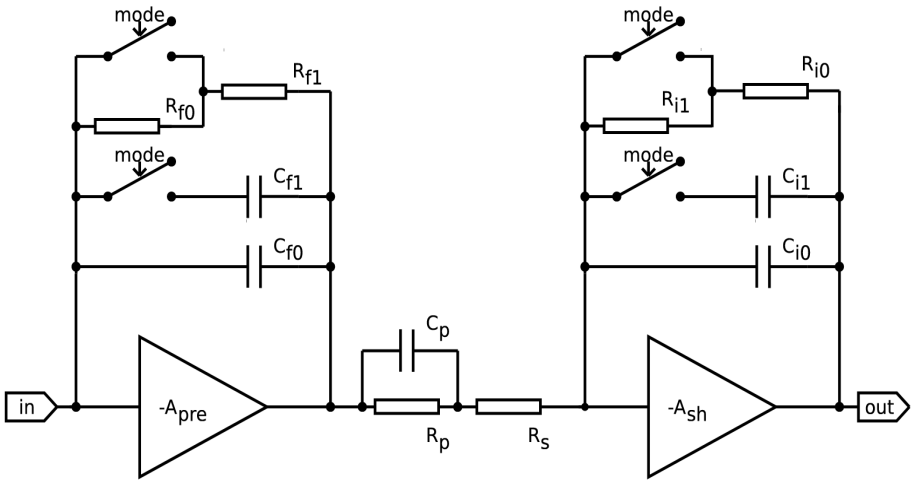
PZC +Shaper T_{peak} ~ 60ns

LumiCal readout architecture

- Front-end ASIC with ~32 channels
- One ADC serving 1-8 front-end channels
- No memory, direct transmission
- First prototypes in AMS 0.35 µm

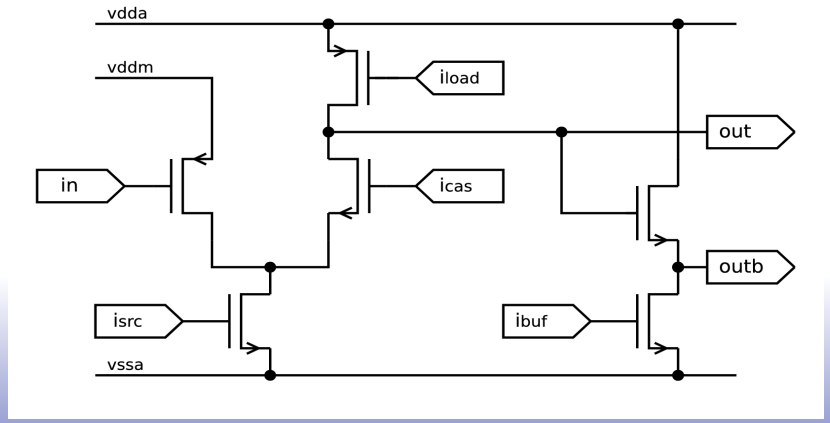


LumiCal front-end electronics architecture

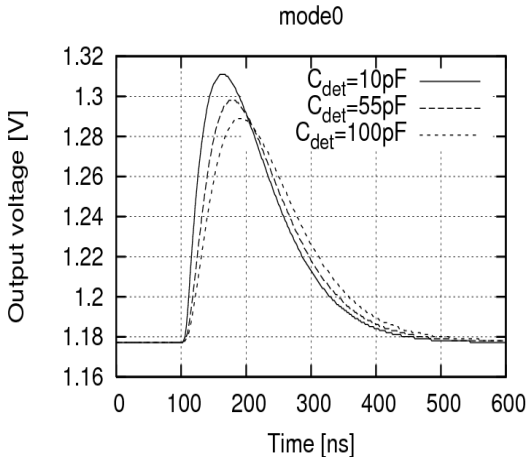


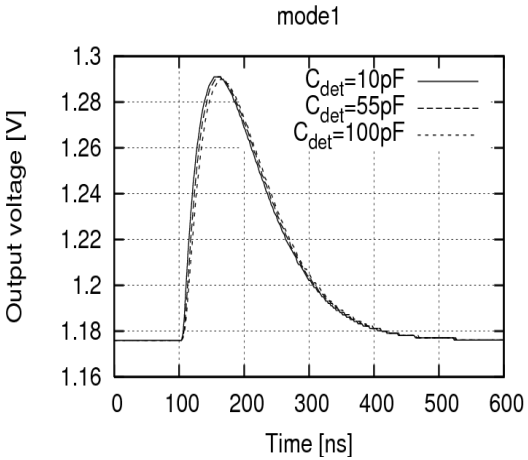
- Preamplifier: Cf~10pF (physics), Cf~0.5pF (calibration), I_{pre}~2.5mA,
- Shaper: 1st order, T_{peak}~60ns, variable gain, I_{sh}~0.5mA

- Both Preamplifier and Shaper designed as folded cascode plus source follower



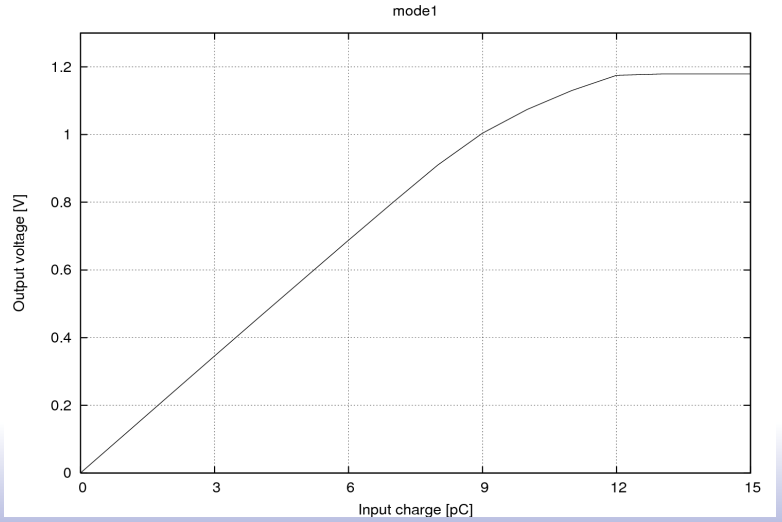
Front-end simulations



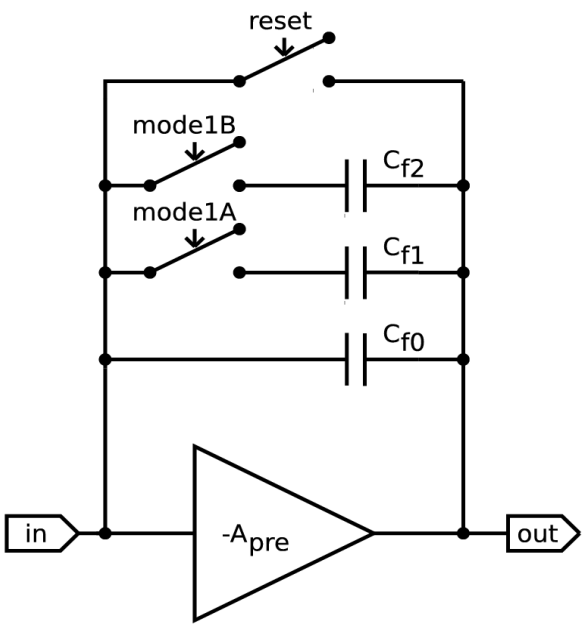


- Front-end response in calibration (mode0) and physics (mode1) mode for different C_{det}

- Output amplitude versus injected charge in physics mode

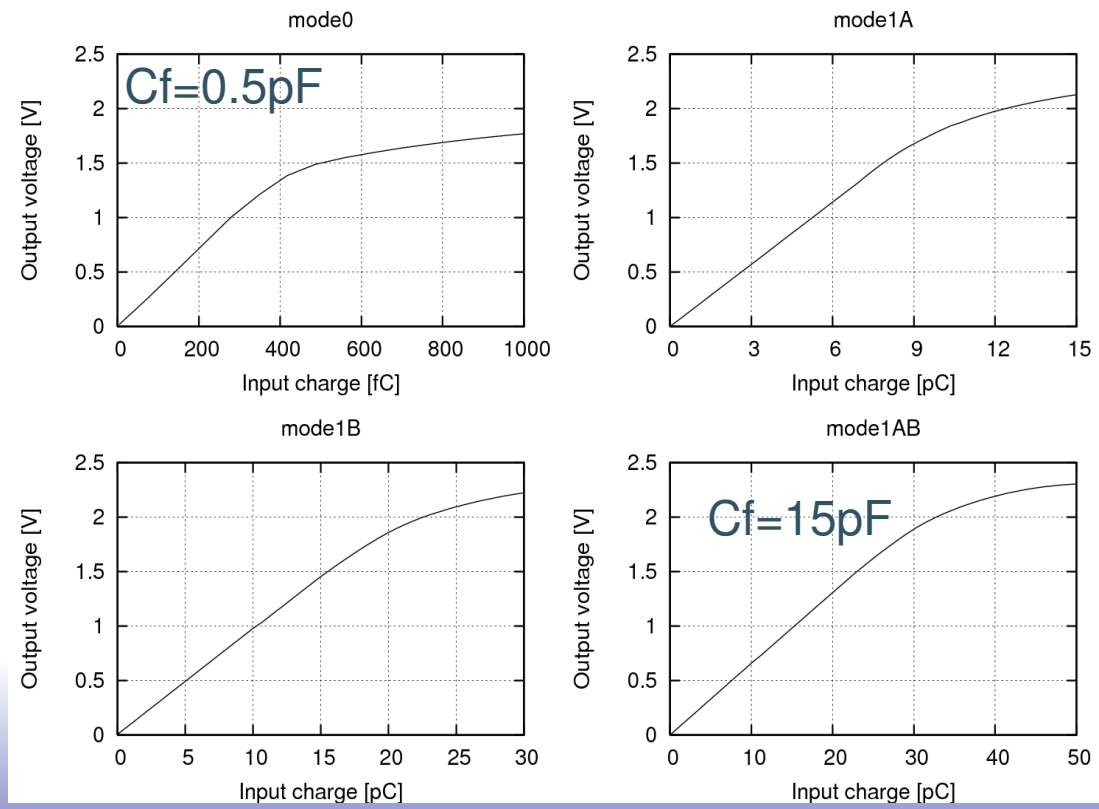


Alternative front-end
Switched-Reset configuration



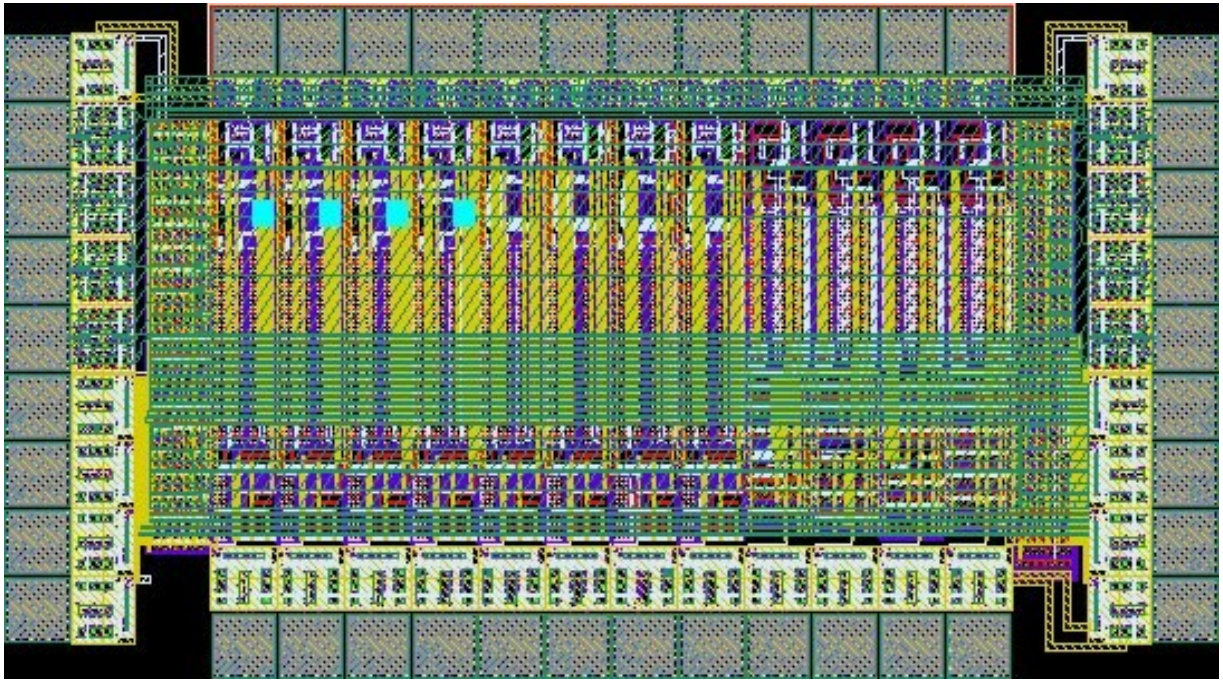
Output amplitude vs Q_{in}

for different Cf



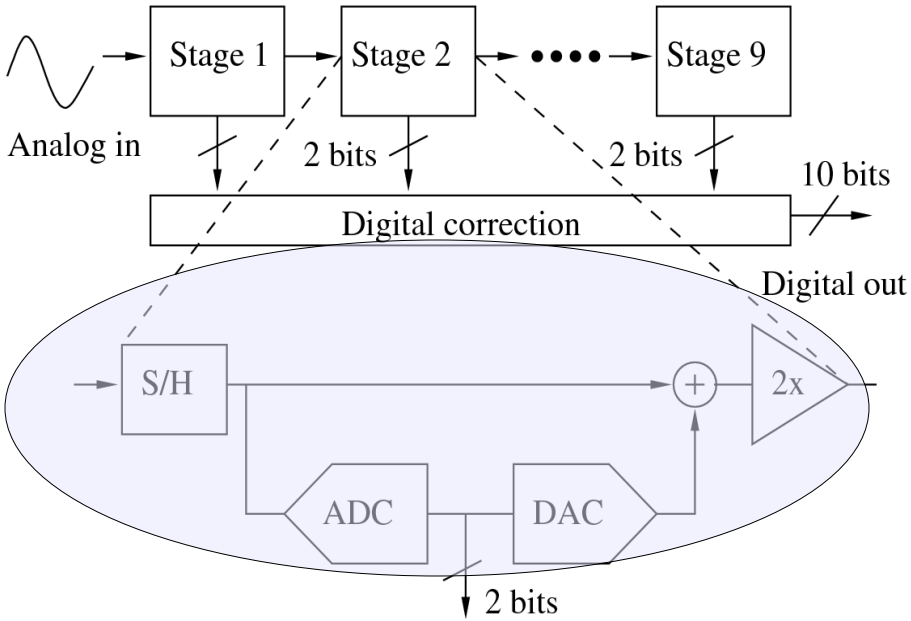
- Single stage
- Wide output range

Layout of prototype front-end



We have just submitted prototype ASIC containing 8 channels (preamp+shaper) with continuous shaping and 4 channels with switched-reset

ADC architecture

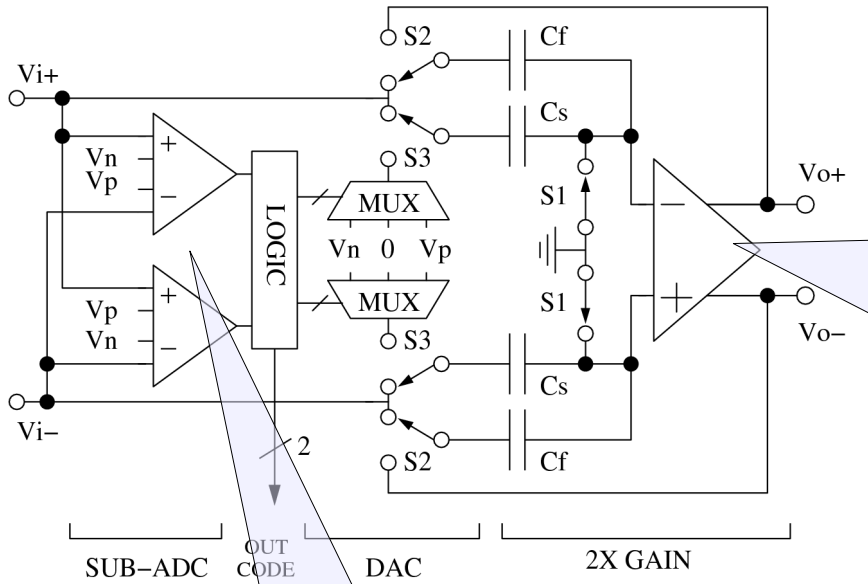


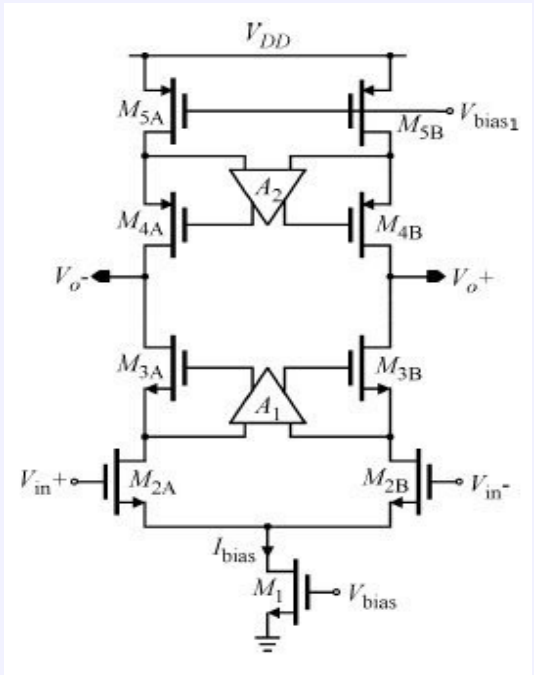
- 10 bit pipeline ADC
- 1.5 bit stage configuration
- Fully differential architecture

Pipeline advantages

- High throughput
- Robust
- Power efficient
- Reasonable area

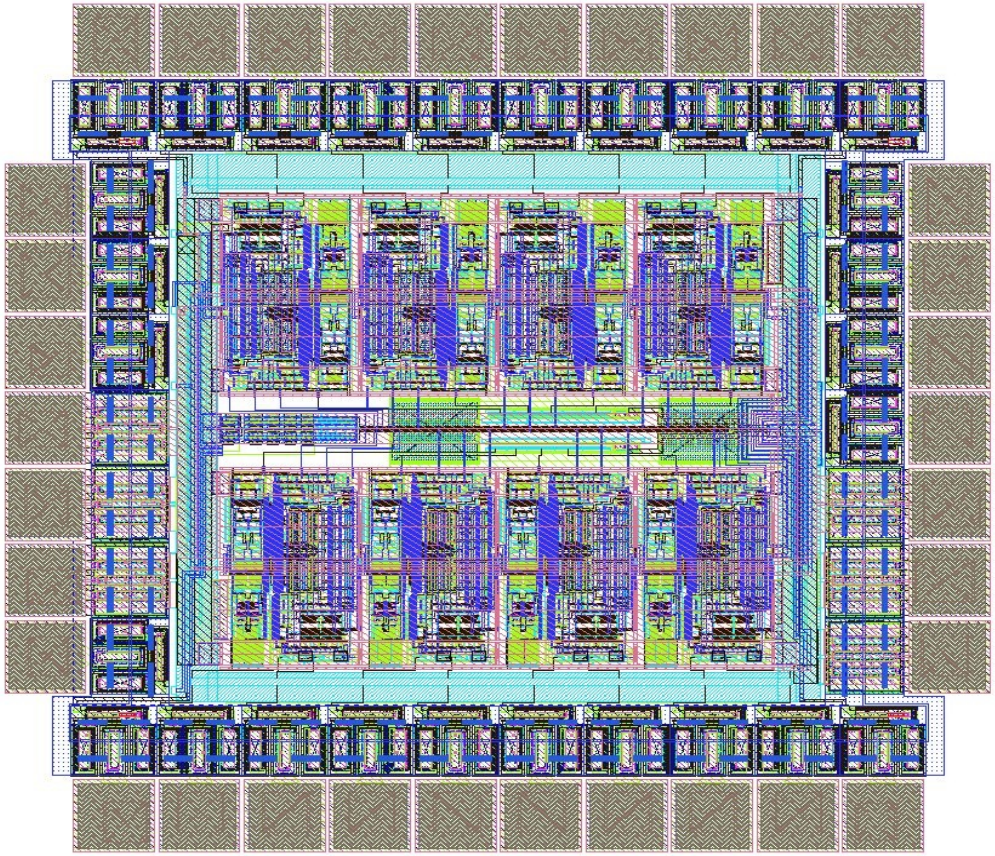
1.5 bit stage architecture





Dynamic latch comparators

Layout of ADC blocks



We have just submitted prototype ASIC

containing 8 pipeline 1.5 bit stages

Summary & milestones

- The work on LumiCal readout has only started
- Now - first prototypes of the front-end and ADC functional blocks are being submitted
- Our goal – prototypes of complete front-end and ADC ASICs in 2009