Second generation Front-end chip for H-Cal SiPM readout : SPIROC

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First generation chip for SiPM : short reminder

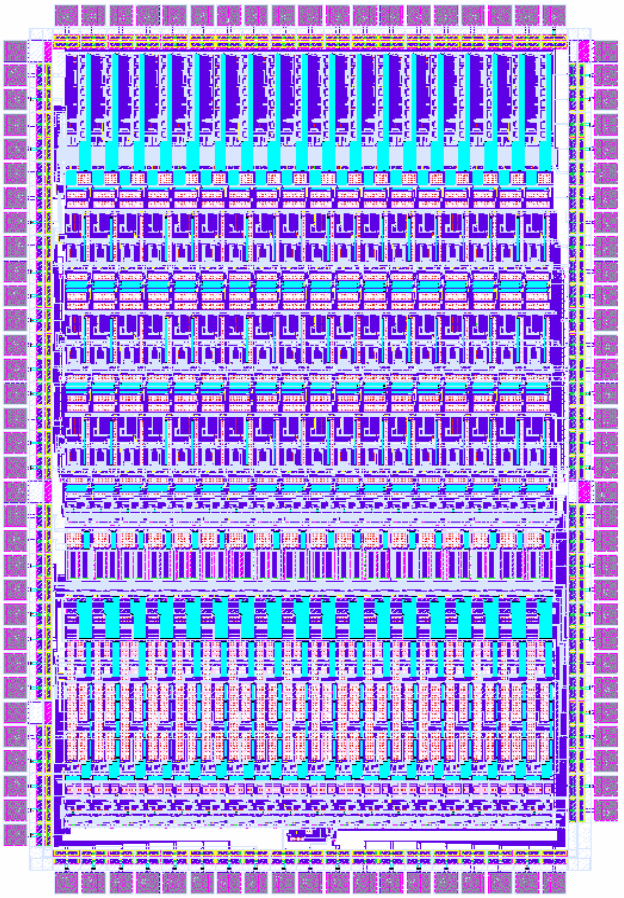
18-channel 8-bit DAC (0-5V)

18-channel front-end readout :

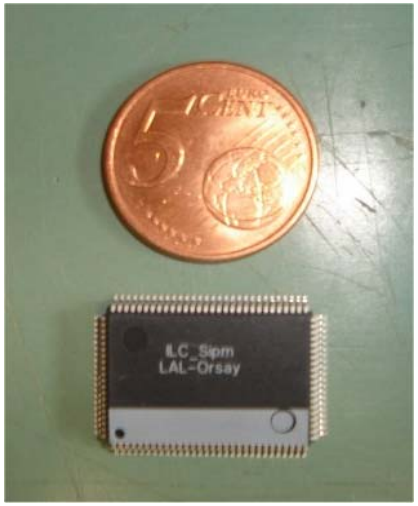
- Variable gain charge preamplifier (0.67 to 10 V/pC)

  Variable tine constant CRRC^2 shaper (12 to 180 ns)

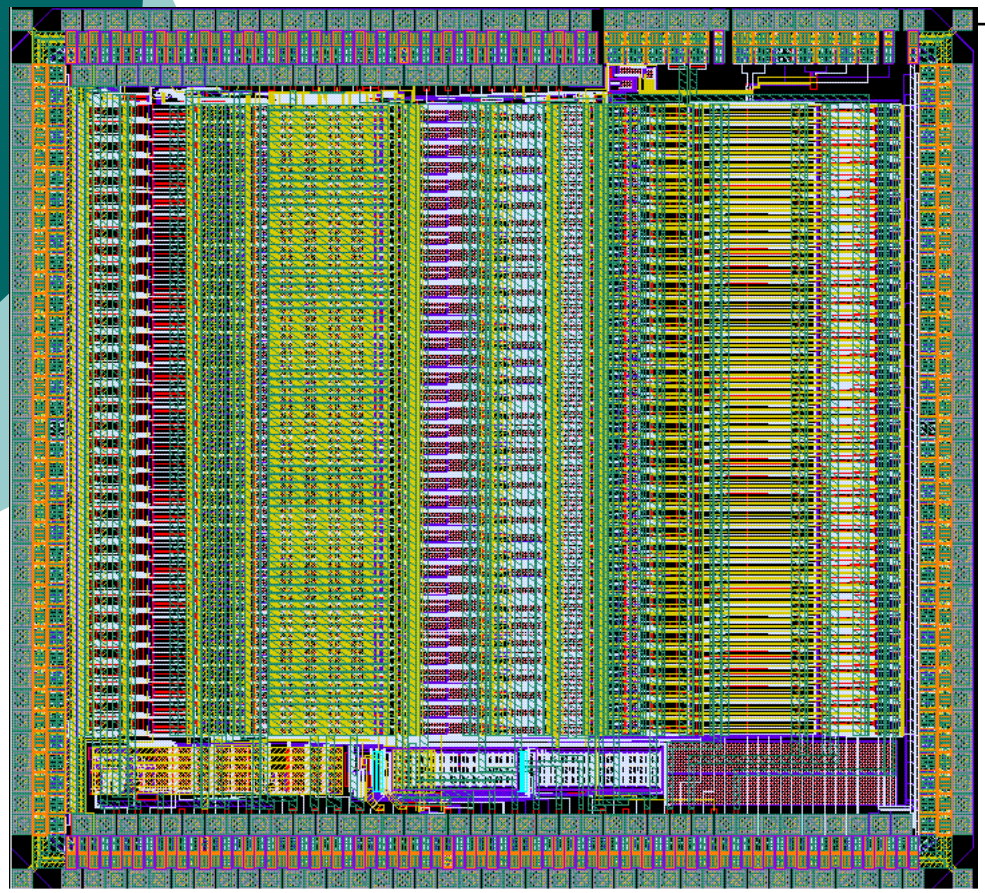
- Track and hold → 1 multiplexed output
- Power consumption : **~200mW (supply : 0-5V)**



- Technology : **AMS 0.8 µm CMOS**
- Chip area : **~10mm²**
- Package : **QFP-100**



Second generation chip for SiPM : SPIROC



- A-HCAL read out
- Silicon PM detector
- 36 channels
- Compatible with new DAQ
- Many SKIROC, HARDROC, and MAROC features re-used

Technology : AMS 0.35 µm SiGe

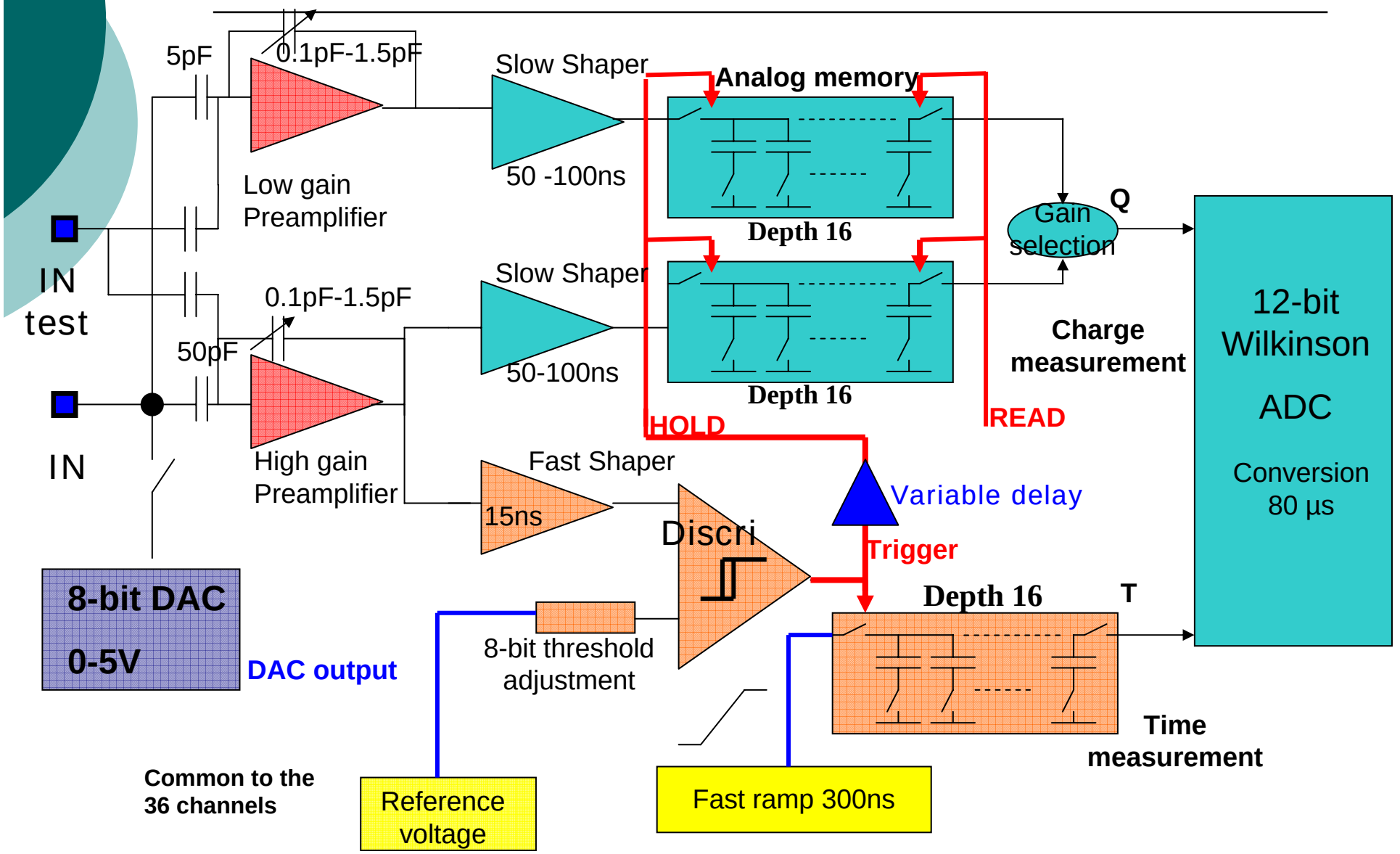
Skiroc layout :
~20mm²

SPIROC submission expected on 11th june

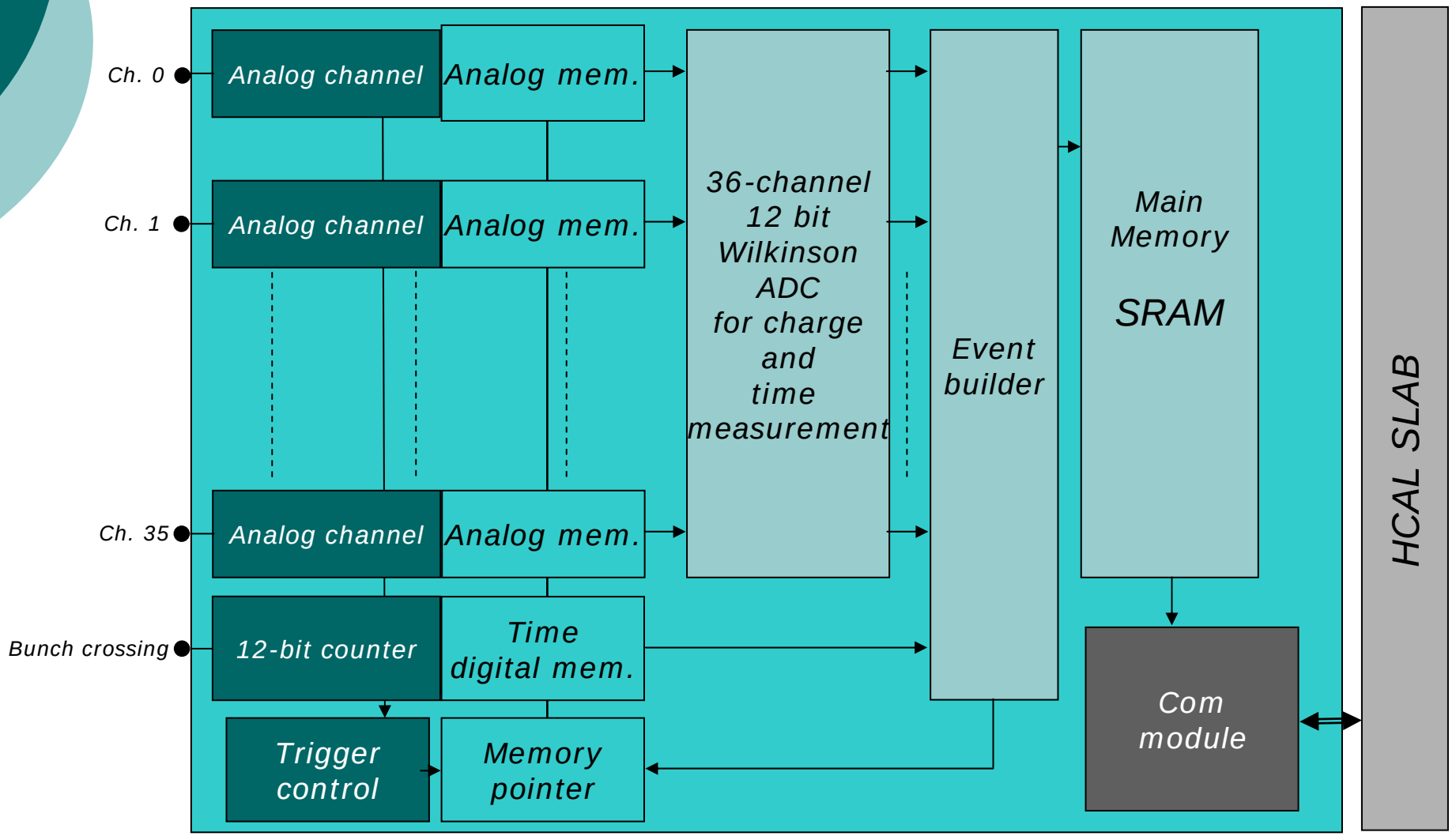
SPIROC main features

- 36-channel readout chip
- Internal input 8-bit DAC (0-5V) for SiPM gain adjustment
- Energy measurement :
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- Time measurement :
  - 1 TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on ½ pe
- Analog memory for time and charge measurement : depth 16
- Power pulsing integrated
- Low consumption : ~25µW per channel (in power pulsing mode)
- Calibration injection capacitance
- Embedded bandgap for voltage references
- Embedded DAC for trigger threshold
- Compatible with physic prototype DAQ
  - Serial analogue output
  - External “force trigger”
- Probe bus for debug
- 12-bit Bunch Crossing ID
- SRAM with data formatting 2 x 2kbytes = 4kbytes
- Output & control with daisy-chain

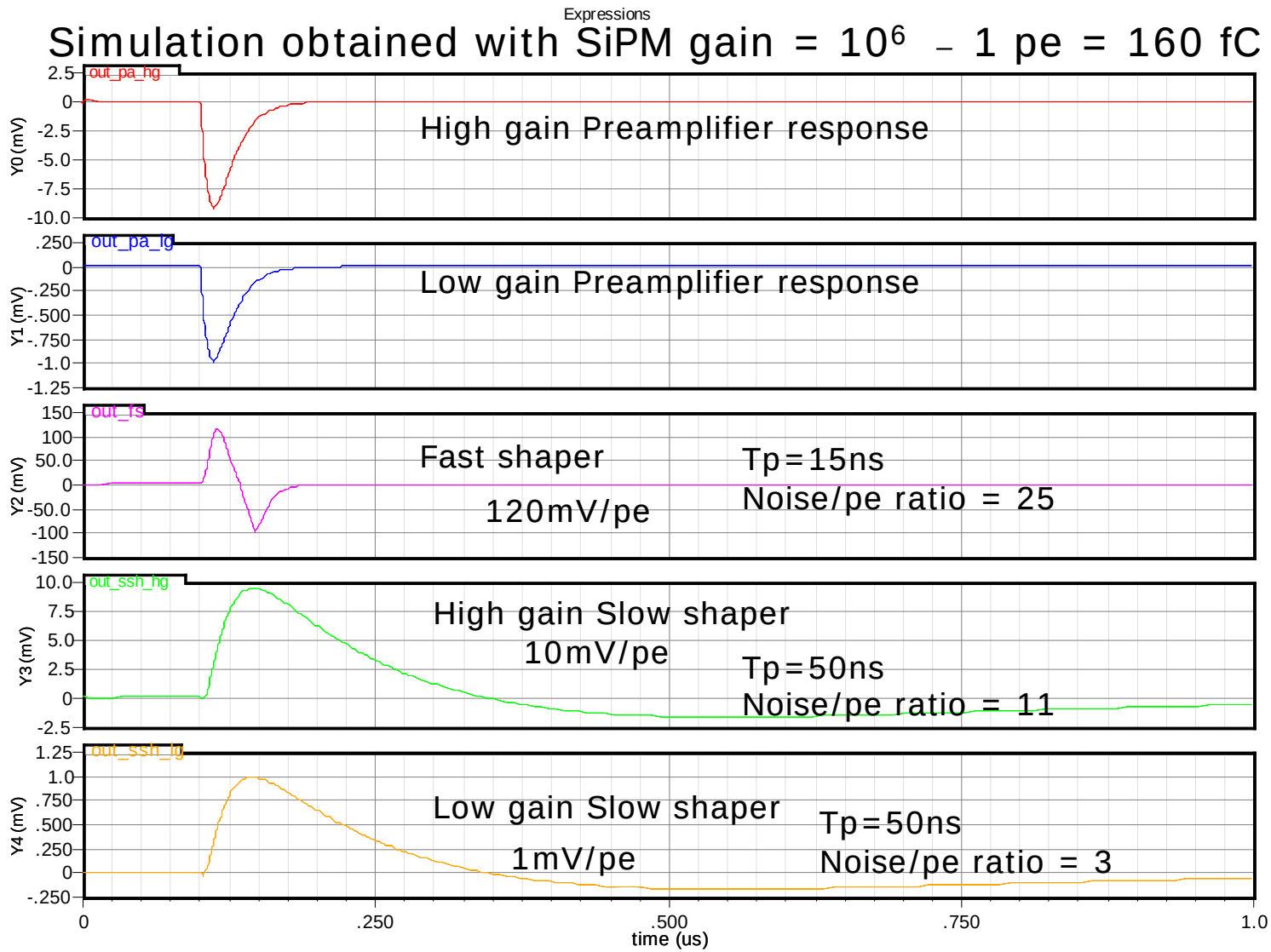
SPIROC: One channel schematic



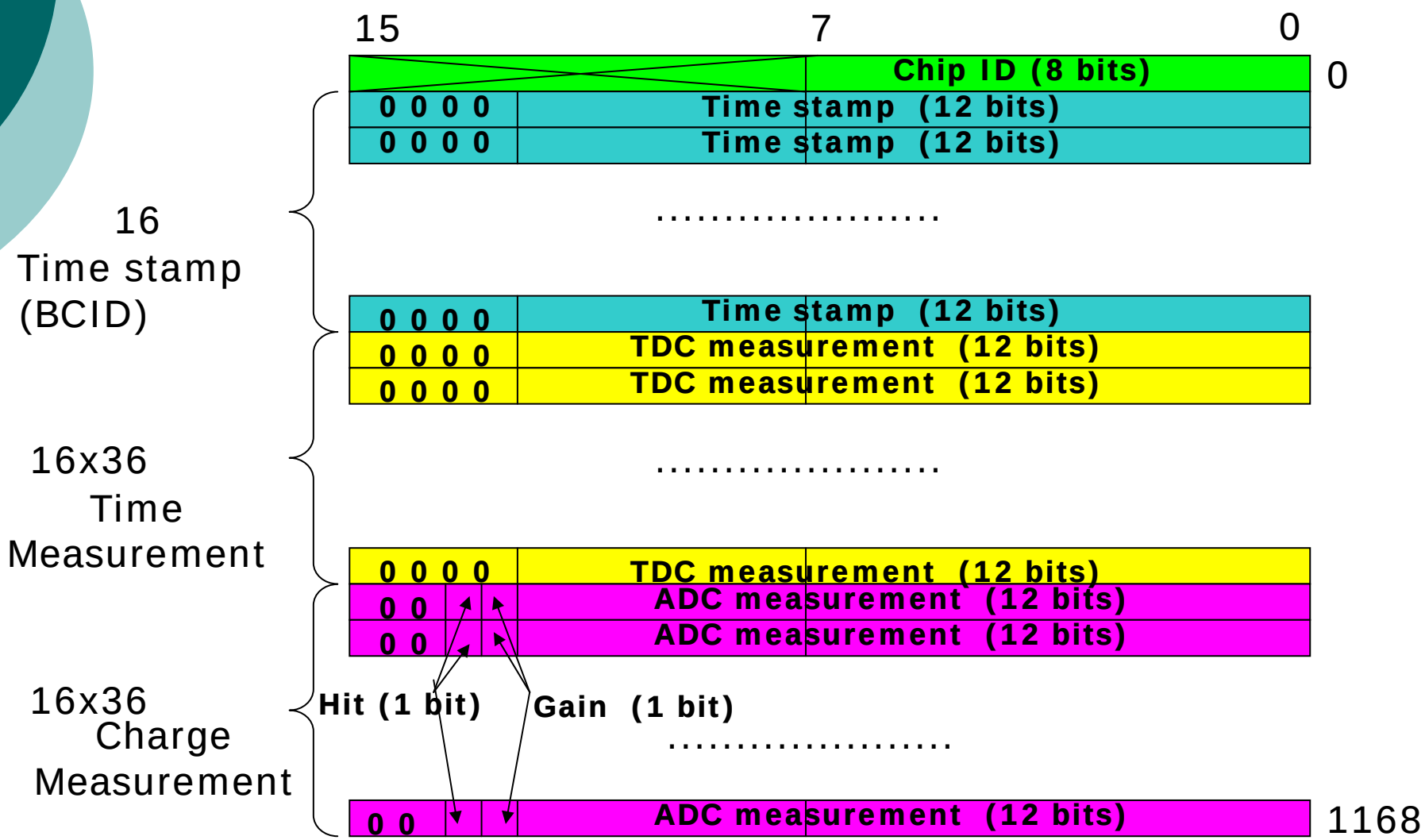
Block scheme of SPIROC



SPIROC : Photoelectron response simulation

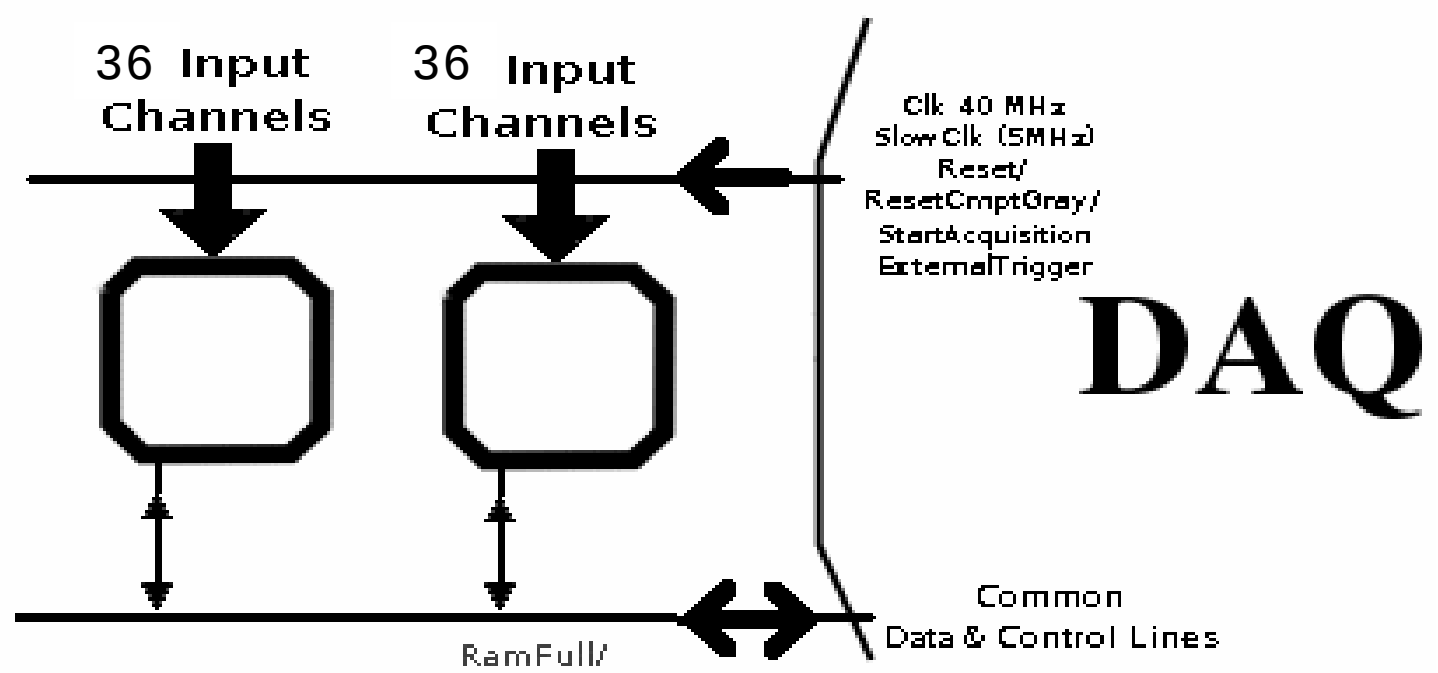


SPIROC : RAM Mapping



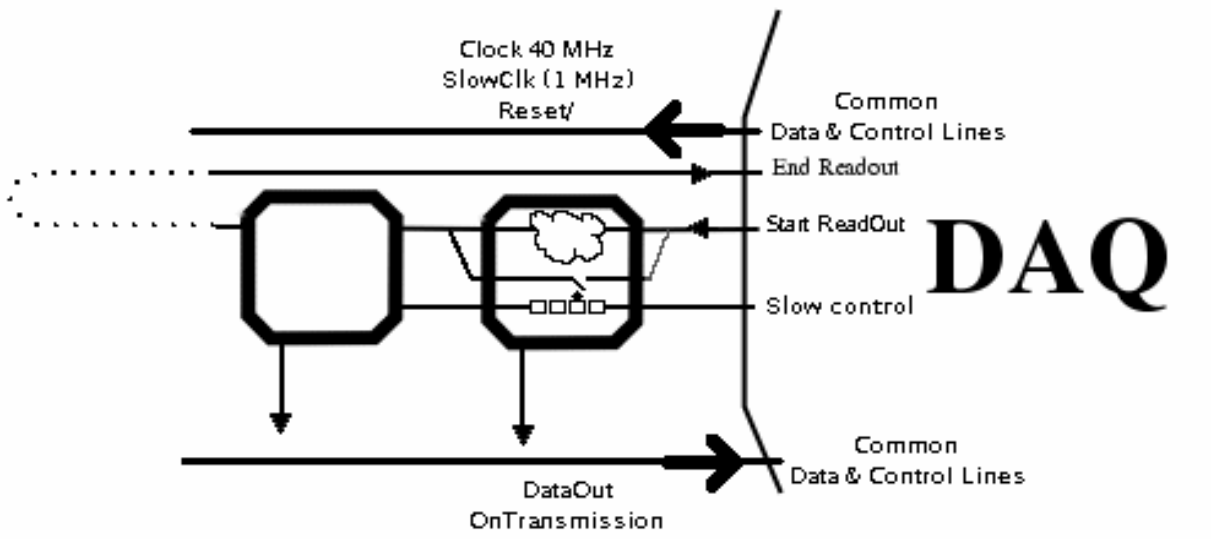
SPIROC : Acquisition mode

- Store up to 16 events in RAM
- Stop acquisition when ram_full signal asserted
  - Common collector bus for ram_full signal

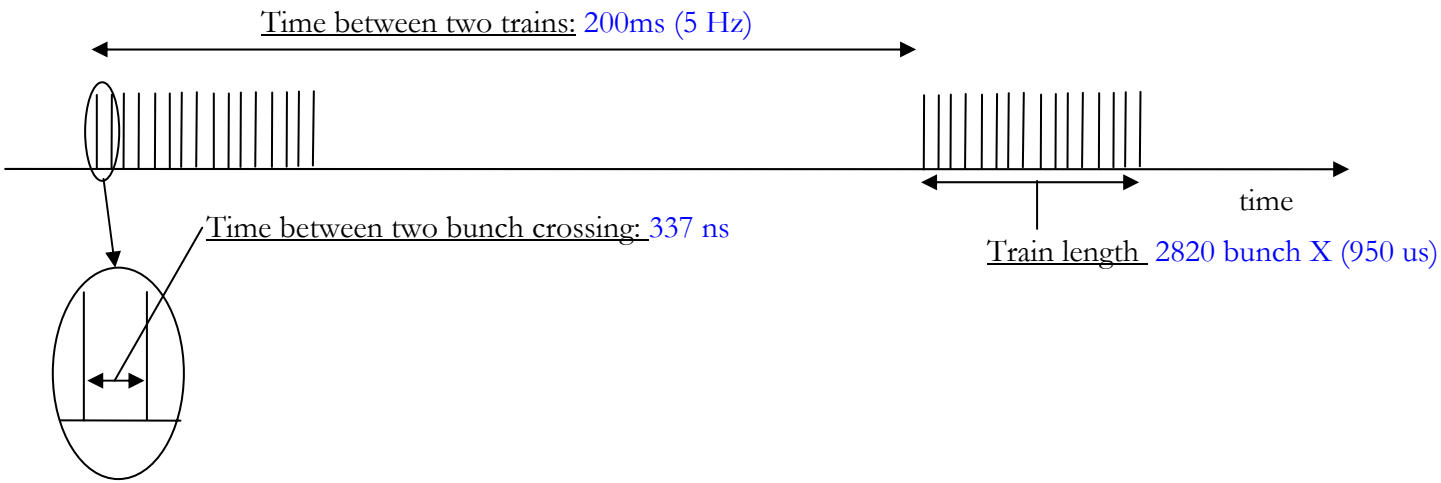


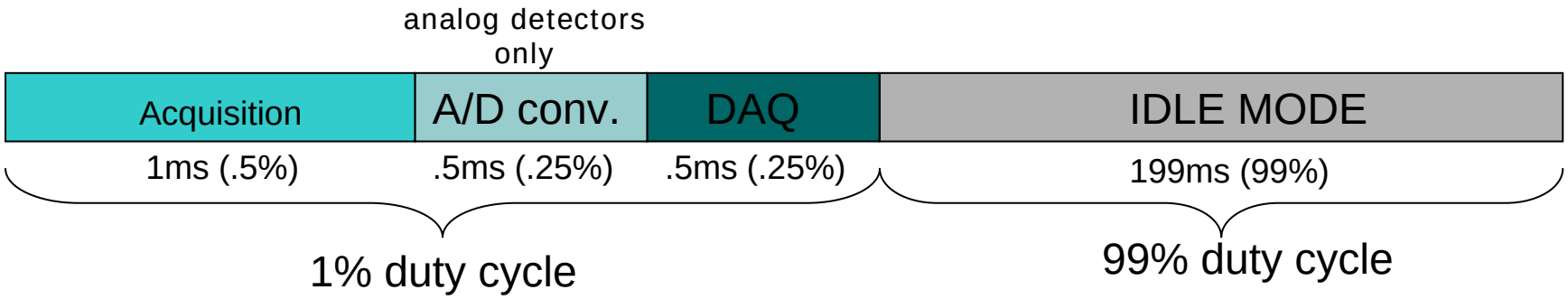
SPIROC : Readout mode

- Based on daisy chain mechanism initiated by DAQ
  - Possibility to bypass a chip by slow control
- One data line activated by each chip sequentially
  - Readout rate few MHz to minimize power dissipation
  - With 500 pF bus capacitance, power dissipation is ~10µW/chip
  - i=CdV/dt = 1 mA => 1 mW for up to 100 chips on bus
  - Readout time max (ram full) 20kbits x 1 µs = 20 ms/chip



Time considerations





Schedule

- First Prototype submission : 11th june 2007
- Expected delivery : September 2007
- SPIROC Characterization : End of Year

Conclusion

- SPIROC designed for SiPM A-HCAL : second generation ASICs
- Many SKIROC, HARDROC, and MAROC features re-used for SPIROC : power pulsing, bandgap, daisy chain mechanism, etc.
- New features embedded : Time measurement, low consumption input DAC, etc.
- Compatible with new DAQ
- Complexity is increasing
- Submission in june 2007 and first prototype expected in September 2007