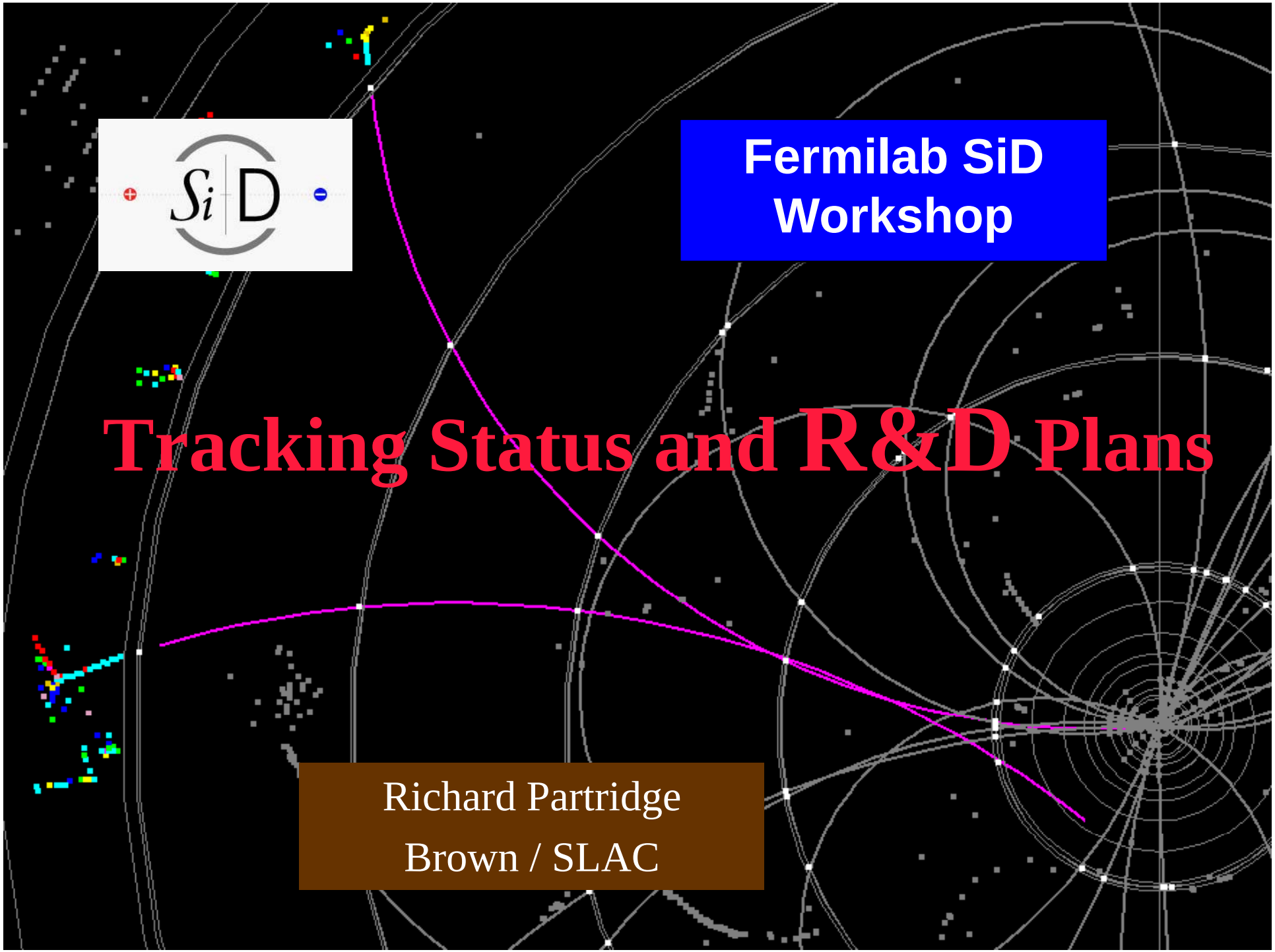


Fermilab SiD Workshop

Tracking Status and R&D Plans

Richard Partridge
Brown / SLAC

Overview

- A fairly detailed and reasonably current report was prepared for the Beijing Review:

http://www-sid.slac.stanford.edu/Documents/Tracking_review.pdf

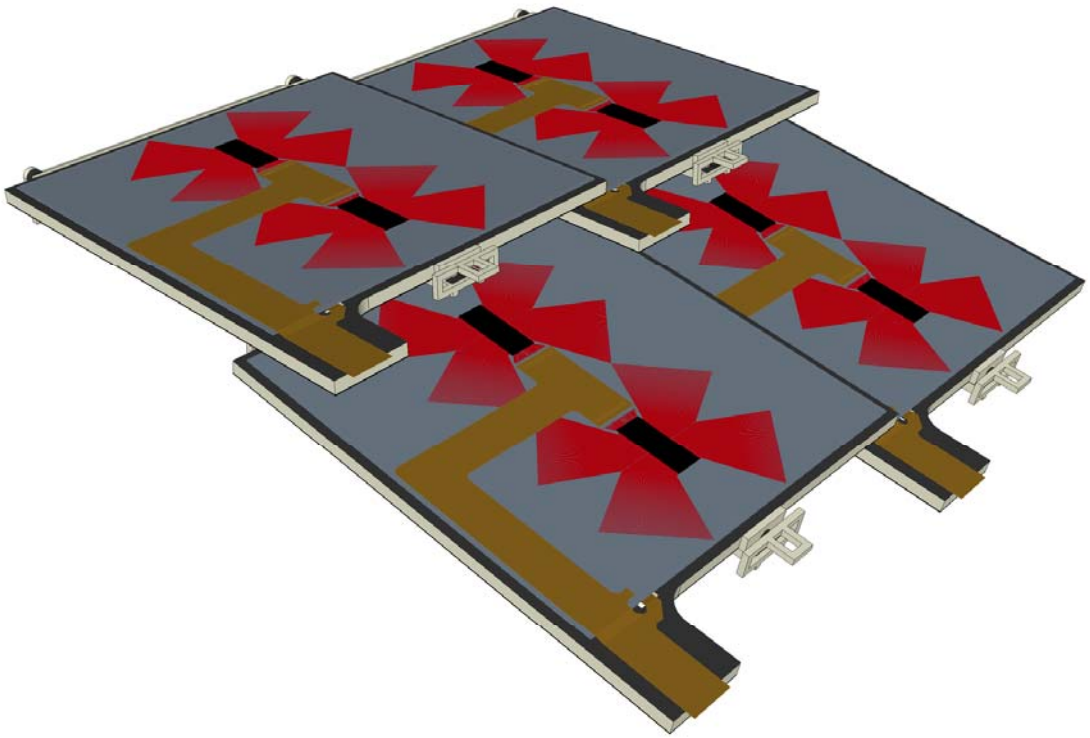
- Only a small fraction of the material in this report will be found in this talk
- Rather, this talk will focus on recent developments and major issues that need to be resolved for the CDR / EDR

Tracker Design Strategy

- Goal is to produce a robust, precise, tracker with full coverage and a minimum amount of material
- We are exploring multiple paths to meet this goal
- Greatest focus is on our "baseline design"
  - Short (~92mm) AC coupled strips on single-sided sensors
  - Double metal routing of strips to bump-bonded KPiX readout chip
  - 5 Layers of axial strips in barrel, 4 disks with stereo readout forward
- We have not yet proven that the baseline design meets the goals listed above
- A number of alternatives are under consideration within SiD:
  - Wirebonding readout chip to sensor
  - LSFE readout chip under development at UCSC
  - Thinned silicon to reduce sensor material
  - Charge division readout to measure coordinate parallel to strip direction
  - Stereo readout in barrel is possible if warranted by simulation studies

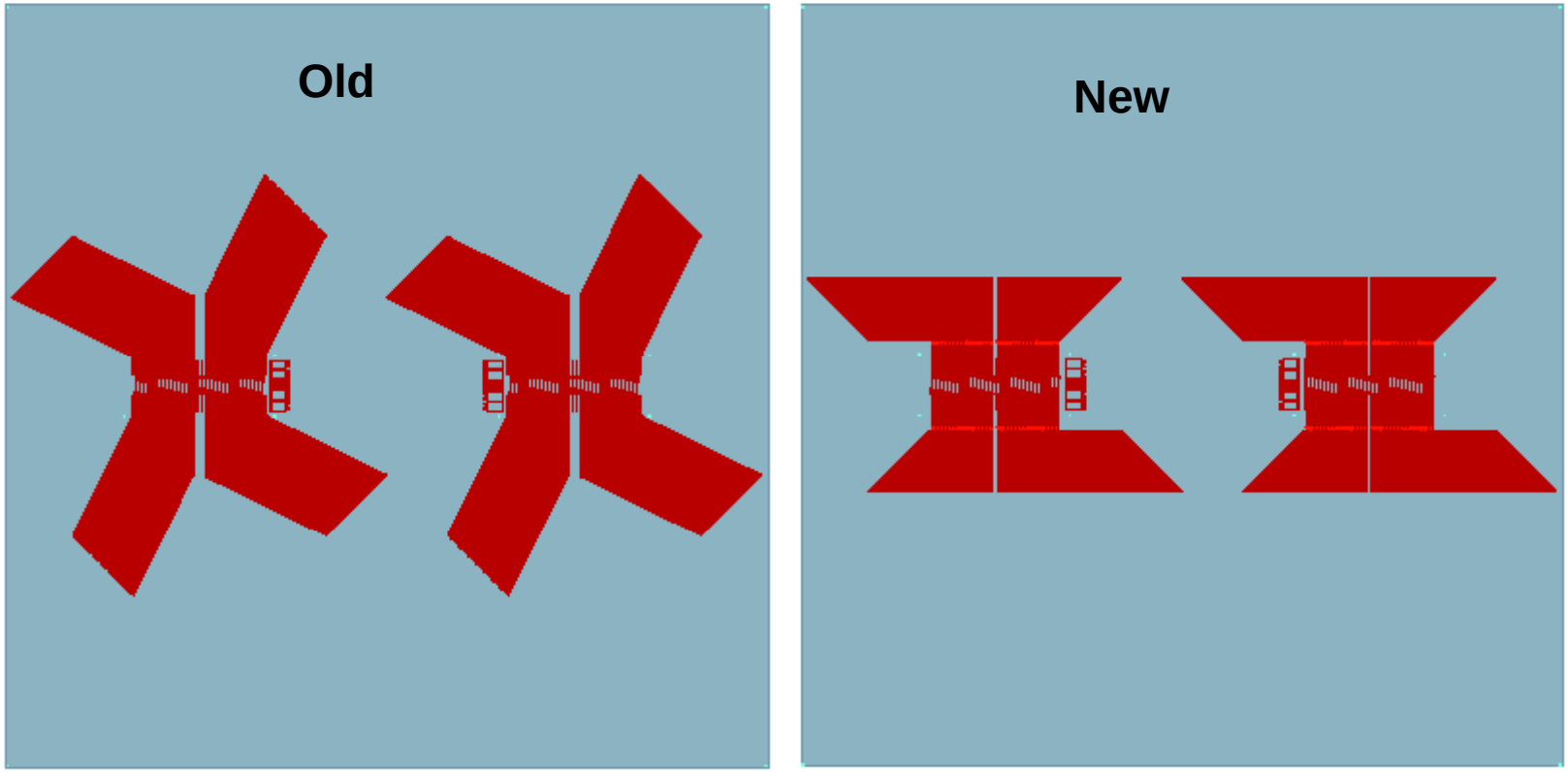
Baseline Module Design

- No real changes
- 1 or 2 sensors per module
- Sensors are ~92mm on a side
- Each sensor has is readout independently
- Modules overlap to eliminate projective cracks
- Modules clip into holders mounted on support structure



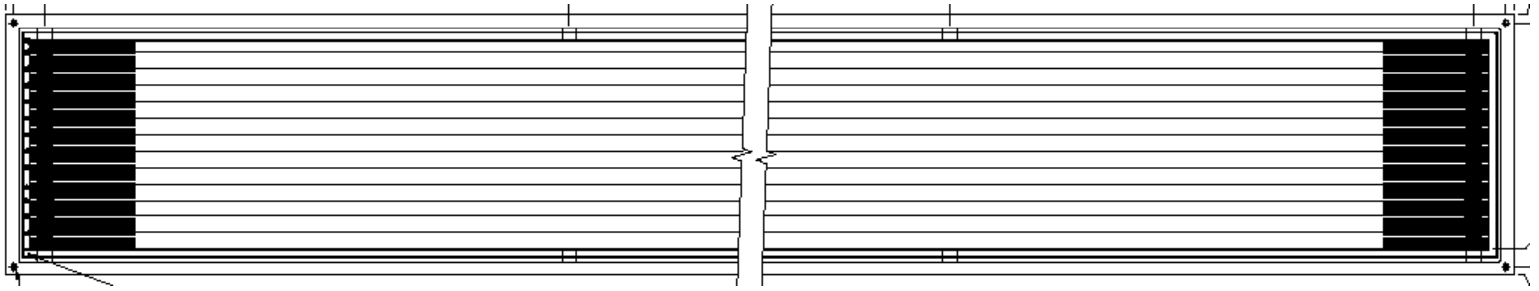
Baseline Sensor Design

- Double metal traces (red) connect strips to readout chips
- Ansys capacitance calculations ⇒ new double metal layout proposed to reduce capacitance spread (95% have 14-18 pF)
- Wire bond pads added for strips that do not run under chips



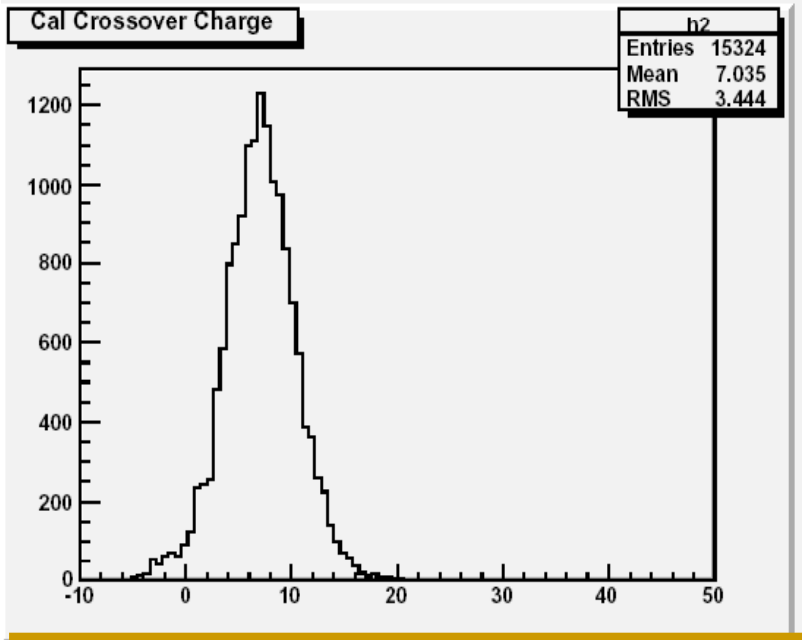
Sensor Submission

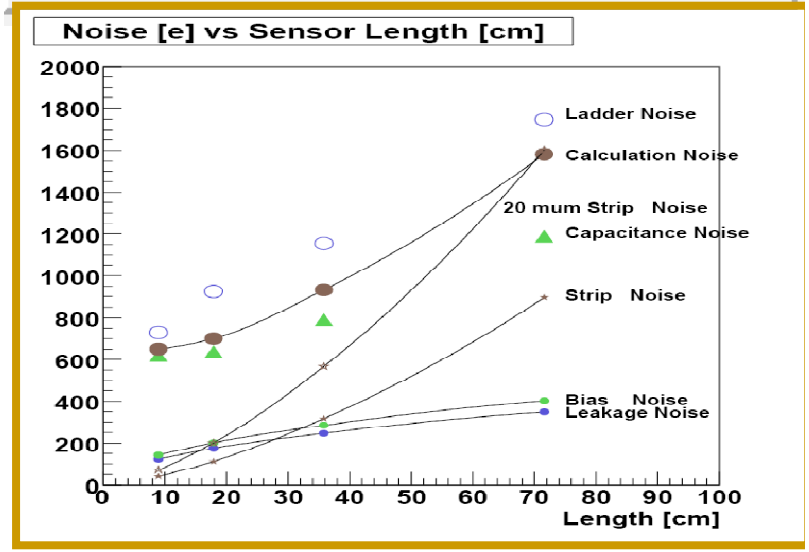
- Tracking group conducted sensor design review in November
  - Reviewers: Gino Bolla, Hartmut Sadrozinski, Sally Seidel, Hiro Tajima
- Also received some comments at the Beijing tracking review
- Design has been updated to reflect comments from sensor review, Beijing tracking review, and input from Hamamatsu
  - See Tim Nelson's talk in the tracking parallel session
- Several small R&D detectors proposed to fit in unused silicon along sides of the prototype sensor
  - DC coupled sensor for charge division testing
  - Non-ILC test sensors for Hiro Tajima of SLAC
- Goal is to finalize drawings, submit to Hamamatsu ASAP



Readout Chip

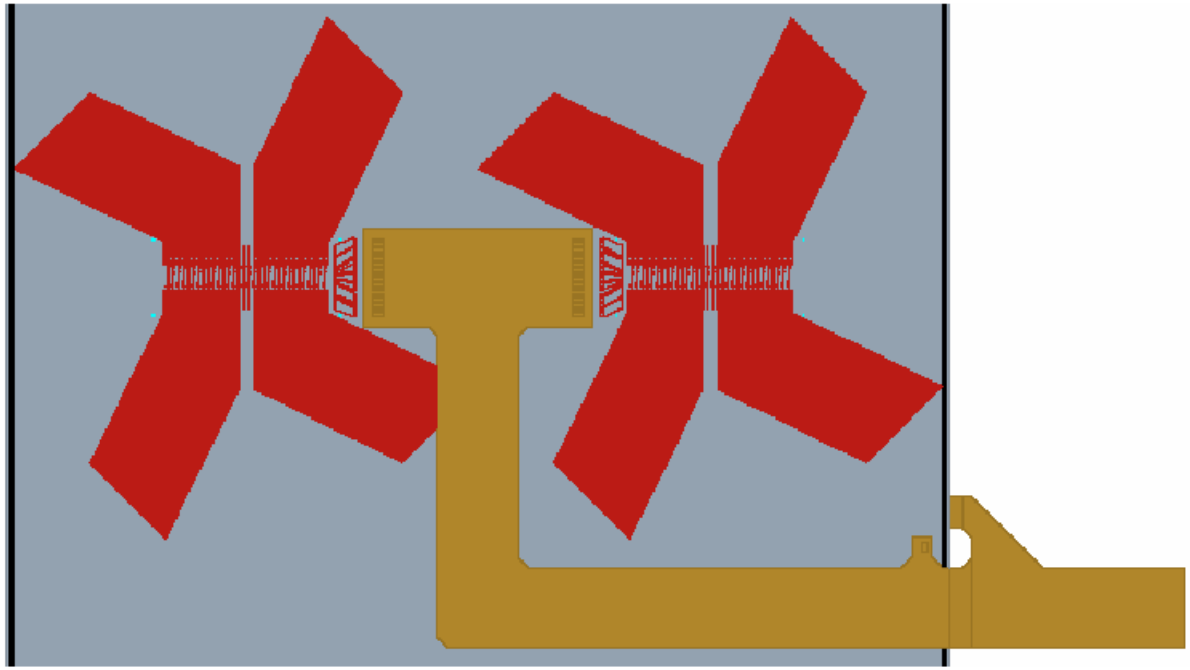
- Baseline readout chip is KPiX
  - 1024 channel chip planned
  - 4 analog buffers./ channel
  - Same chip as calorimeter readout?
- Recent KPiX source results!
  - KPiX wire bonded to CDF L00 Sensor
  - Exposed to Sr 90 beta source
  - Still many issues to be resolved
- LSTFE-2 is close to submission
  - First version showed good noise performance
  - Time over threshold readout chip
- New idea: charge division
  - Readout both ends of a DC coupled strip
  - Expect σ_z ~5.5mm





Cable Design

- New effort by New Mexico to design tracker cable
- Preliminary design presented on Monday for pig-tail cable
  - See Martin Hoeferkamp's talk in the tracking parallel session
- 4 layer Cu / kapton cable that carries power, signals, and bias
- Wire bond from cable to double metal traces that connect to bump bond pads

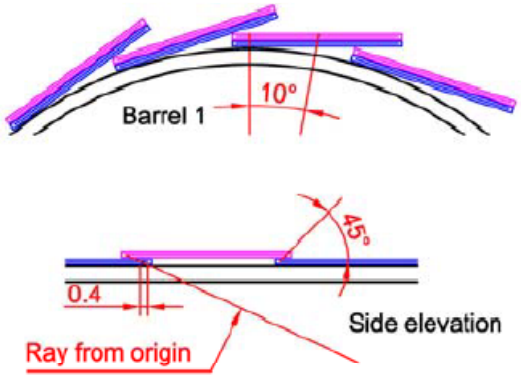


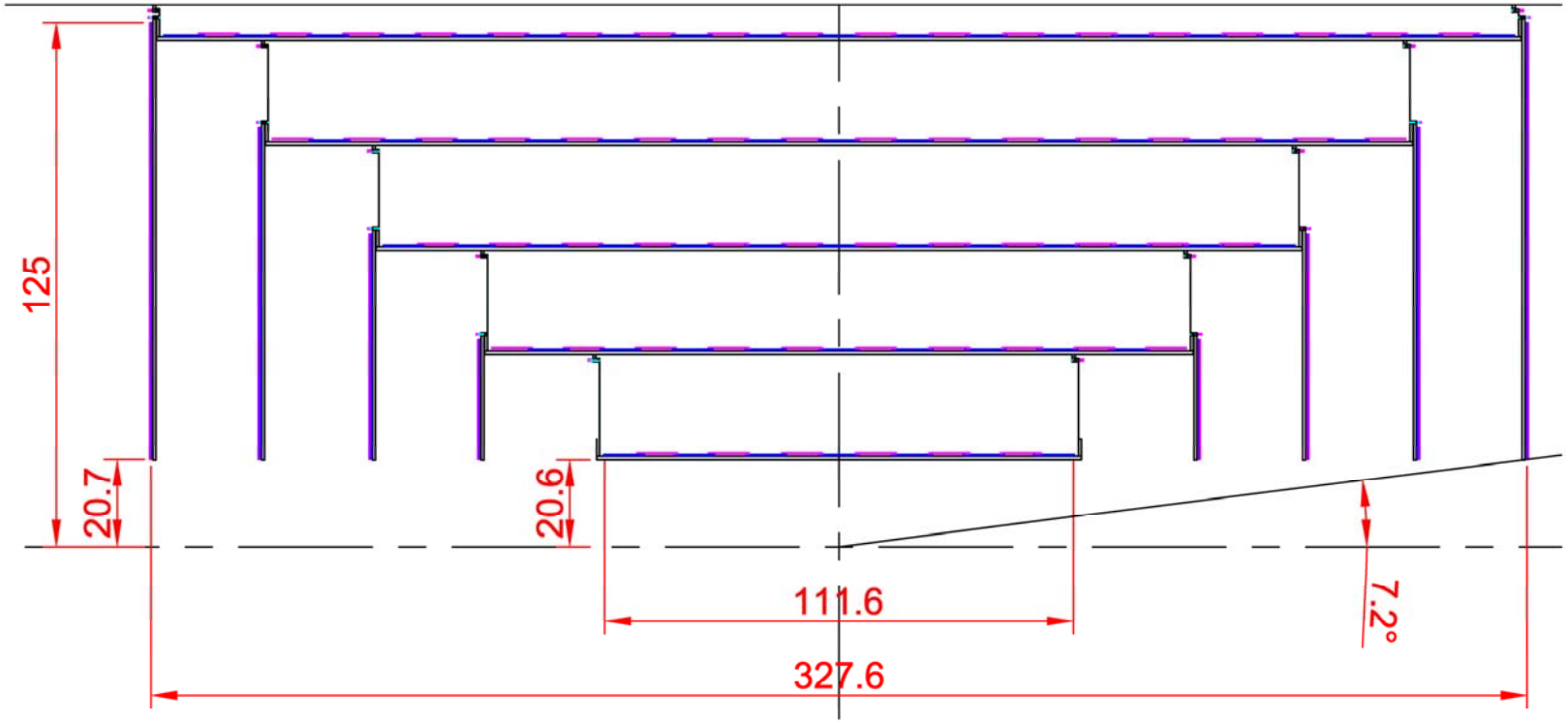
Power Delivery Issues

- These need to be investigated!!
- Need to switch ~10kA on / off @ 5 Hz for power cycling
- Large Lorentz forces on conductors
- Net force on tracker must be 0, but potential for substantial internal forces and torques
  - Forces are not static – power cycling will generate impulses at 5 Hz
  - Will these forces / torques cause the tracker to vibrate?
- How do we bring power in?
  - Probably don't want to bring in 10kA at 2.5 V
  - Serial powering of multiple readout chips?
  - Capacitive DC-DC converter for each readout chip?
- These issues need to be investigated!!
  - Good opportunity for someone who wants to take on a SiD tracking project

Mechanical Design

- No real changes since R&D report
- 5 barrel layers of axial strips
- 4 forward disks / end with stereo strips
- Pin-wheel design with z overlaps



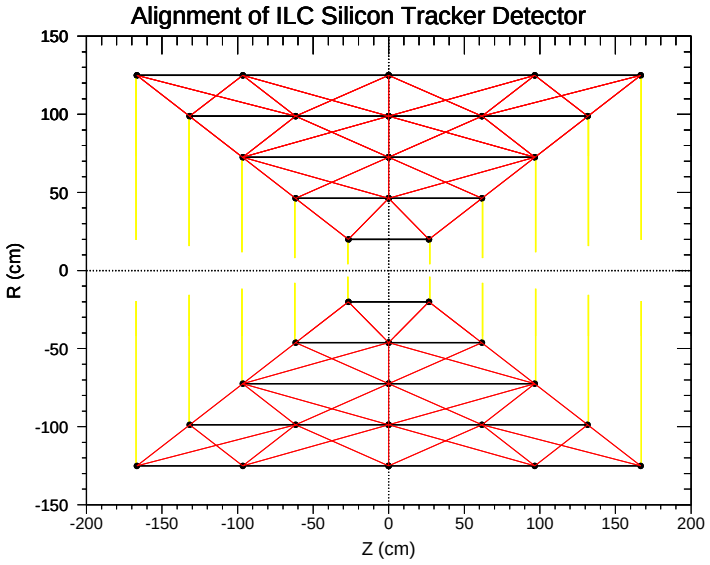


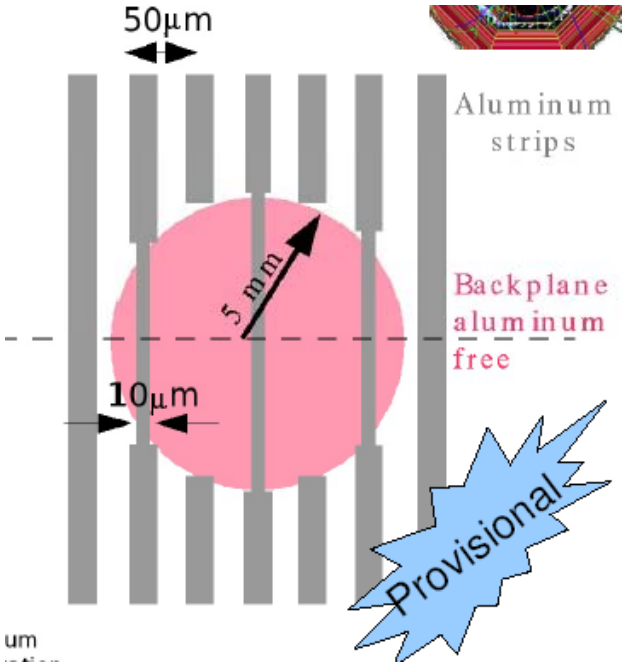
Alignment and Position Monitoring

- For ~10,000 sensors, there are ~60,000 alignment constants
  - Track based alignment is probably the only method that will meet our goal of 7 μm hit position resolution
  - Scale of problem overwhelms usual matrix inversion algorithms
  - New algorithms have been developed for CMS – need to learn about this!
- Track-based alignment requires detector positions to be stable or well monitored over long intervals
- Problem has a number of different aspects
  - Relative alignment of sensors in a tracker barrels / disks
  - Relative position between barrel / disk layers
  - Relative position between tracker and vertex detector
  - Relative position of tracking systems relative to beam spot
  - Reproducibility of positioning during push-pull operation
- Likely there is not a single solution to all problems

Laser Alignment Systems

- Frequency scanned interferometry can measure point-point distances to ~0.2 μm accuracy
  - See talk by Haijun Yang in the tracker parallel session
- IR laser can shine through detectors while also depositing charge along the laser path
  - See talk by Marcos Fernandez Garcia in the tracker parallel session
- Both techniques look promising – but what is really required?



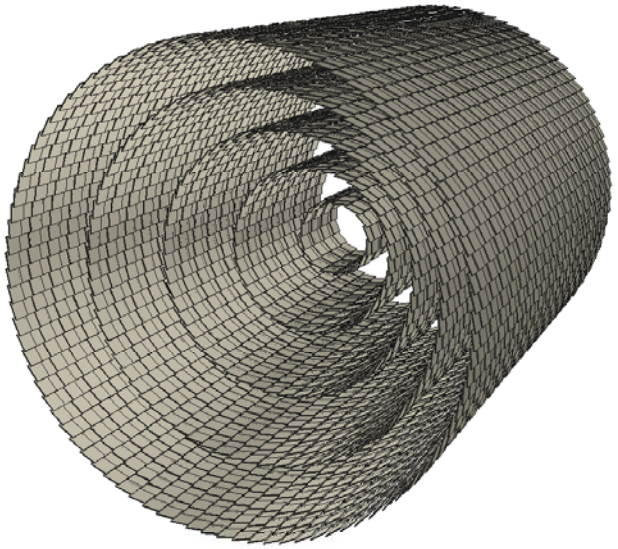


Beam and non-Beam Testing

- Need to test critical aspects of SiD tracker design
- Some expected tests include:
  - Noise / cross-talk / performance of double metal design
  - Verification of hit position resolution
  - Electrical and mechanical aspects of power pulsing in 5T field
  - Mechanical properties of prototype support structures
- Beijing tracking review recommended a large bore solenoid for beam testing to be shared between the silicon and TPC groups
  - If this was free, that would be great!
  - If expensive, then we need to identify our true magnet needs
    - Do we really need a big bore?
    - What tests are best done in beam? What are best done optically?
- What sort of system/slice tests are needed for the detector EDR?
- What tests are needed to make technology choices?

Simulations

- Dmitri provided an excellent description of the tracking software infrastructure and algorithms
- This work is expected to converge into a set of powerful tools for studying tracker performance in the next 1-2 months
- Goal of this work is to optimize tracker design based on tracker performance and ultimately physics benchmarks
  - How many layers are needed?
  - Where are they located?
  - What is the impact of K_S, Λ decays?
  - What is the impact of long lived b decays?
  - Do we benefit from >0 barrel stereo layers?
  - Does charge division readout help?
  - What is the optimum forward design?
  - What is the impact of tracker material?
  - Do we meet our physics goals?



Tracking R&D Summary

System	Work Package	Institutions
Mechanical	Mechanical Support Design	Fermilab, SLAC, Washington
	Module Design	Fermilab, SLAC
	Frequency Scanning Interferometry	Michigan
Sensor	Double Metal Sensor	Fermilab, SLAC, Tokyo
	Thin Silicon	Purdue
	Sensor Characterization and Testing	New Mexico, SLAC
Readout	KPiX Readout	Davis, Oregon, SLAC
	Time Over Threshold Readout	Santa Cruz
	Charge Division Readout	Brown, Santa Cruz
Cable	Tracker KPiX Cable	New Mexico, SLAC
Simulation	Simulation Infrastructure	Fermilab, Oregon, SLAC
	Vertex Seeded Tracking	Brown, Colorado, Fermilab, Oregon, Santa Cruz
	Stand Alone Tracking	Fermilab, Santa Cruz, SLAC
	Calorimeter Assisted Tracking	Kansas State (Bonn)
	Fitting and Resolution	Oregon, Santa Cruz, SLAC

Conclusions

From Beijing Tracking Review:

- The SiD Tracking effort is founded on a few key principles
  - Take full advantage of the superb hit resolution, two-track separation, design flexibility, and timing properties offered by silicon strip detectors to provide robust tracking capability that meets the ILC physics goals
  - Aggressively work to minimize the material in the tracking volume
  - Optimize the tracker as one element of an integrated detector design
- A comprehensive R&D program has been put in place to perform the R&D required to succeed in this effort
  - This program is unlikely to be static, as historically we have benefited by the rapid pace of advances in semiconductor manufacturing technology
- During these talks, we have tried to highlight our R&D plans and the status of our R&D efforts – further details can be found in our written report