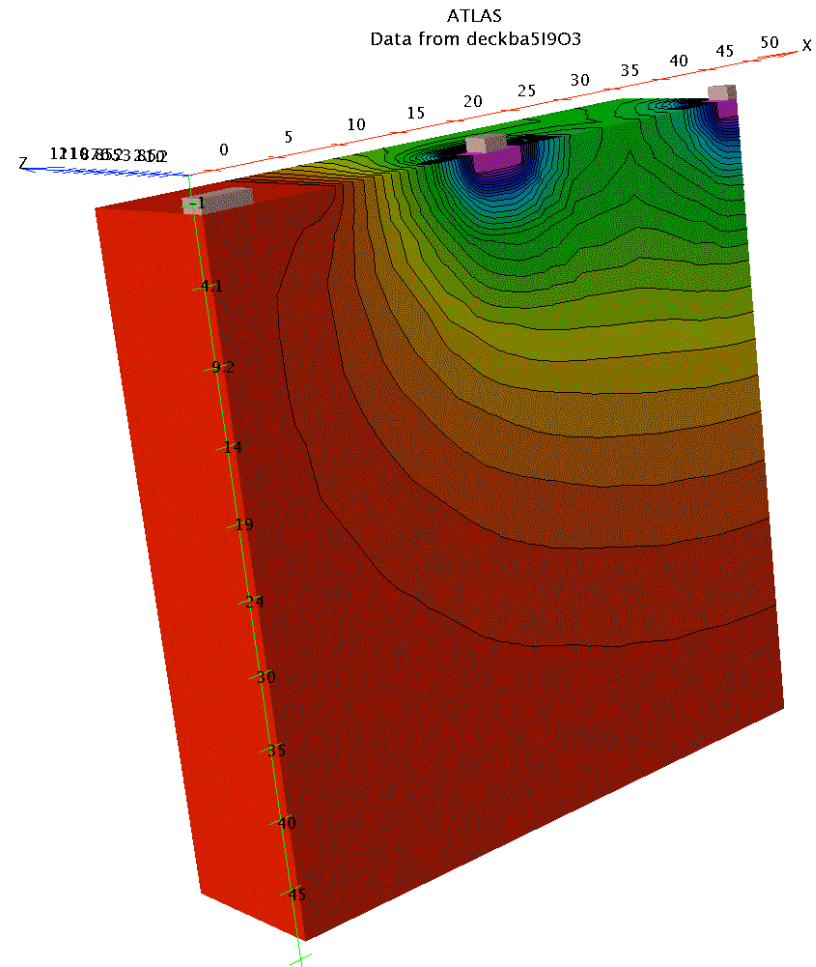# Vertex R&D Summary

Contents:

- Requirements
- Candidate technologies
- R&D Reports
- Mechanical Studies
- Simulation
- EMI and Power
- Future Plans

Mostly a summary of the parallel session, with additions and editorial comments

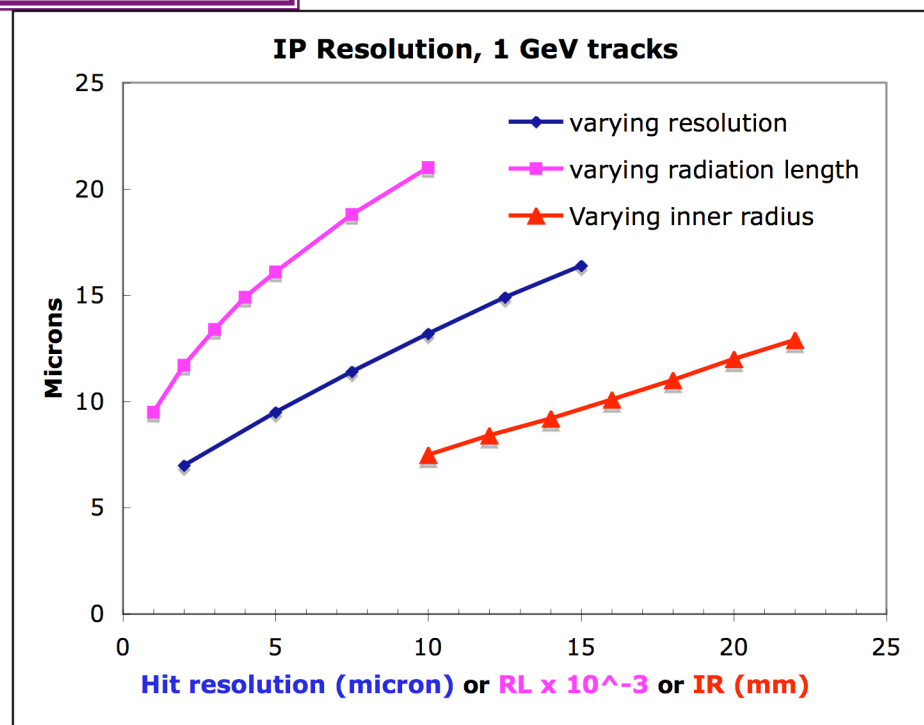# Why is it so hard?

Detector Requirements(Sinev)

- **Good angular coverage with many layers close to vertex**
- **Excellent spacepoint precision (** < 4 microns **)**
- **Superb impact parameter resolution (** $5\mu m \oplus 10\mu m/(p\ sin^{3/2}\theta)$ **)**
- **Transparency (** ~0.1% X_0 per layer **)**
- **Track reconstruction (** find tracks in VXD alone **)**
- **Sensitive to acceptable number of bunch crossings (** <150 = 45 sec **)**
- **EMI immunity**
- **Power Constraint** (< 100 Watts)

Difficult to satisfy all of the constraints, especially power and time resolution

Performance Factors

- Inner radius
- Material
- Position resolution (<5 microns)
  - Binary or analog
  - Charge collection diffusion (MAPS) or drift (3D, SOI)
- Power dissipation (related to material)
- Time resolution (optimize pattern recognition)
- Cost - small area so sensors can be rather costly/mm^2
- Integration with tracker (especially disks)

IP Resolution, 1 GeV tracks

Legend:
- varying resolution
- varying radiation length
- Varying inner radius

Y-axis: Microns (0, 5, 10, 15, 20, 25)

X-axis: 0, 5, 10, 15, 20, 25
Hit resolution (micron) or RL x 10^-3 or IR (mm)

Parametric simulation assuming:
- 0.1% RL per layer
- 5 micron resoluton
- 1.4 cm inner radius

Varying each parameter

Candidate Technologies

- CCDs
  - Column Parallel (LCFI)
  - ISIS (LCFI)
  - Split Column (SLAC/Oregon)
- CMOS Active Pixels
  - Chronopixel (Oregon/Yale/Sarnoff)
  - Mimosa + LCRD 1-3 (LBL)
- SOI
  - Mambo (FNAL)
  - American Semiconductor (FNAL)
  - LCRD-SOI (LBL)
- 3D
  - 3DIC (FNAL)
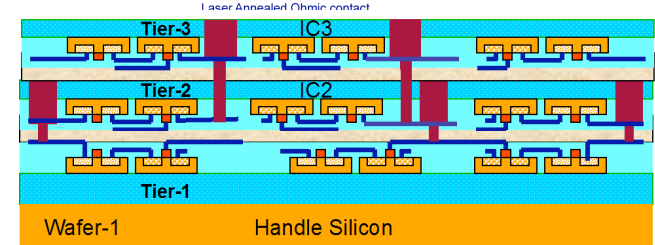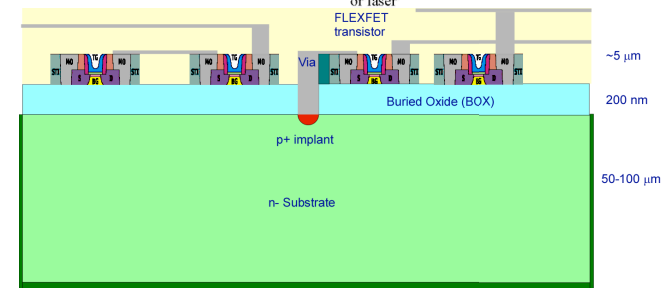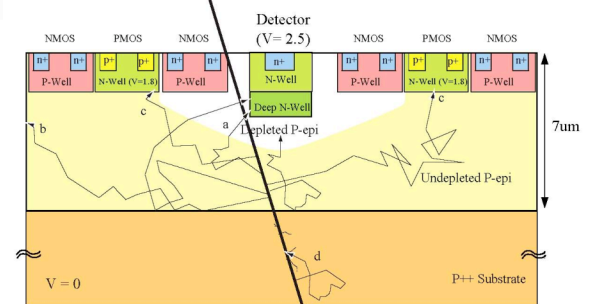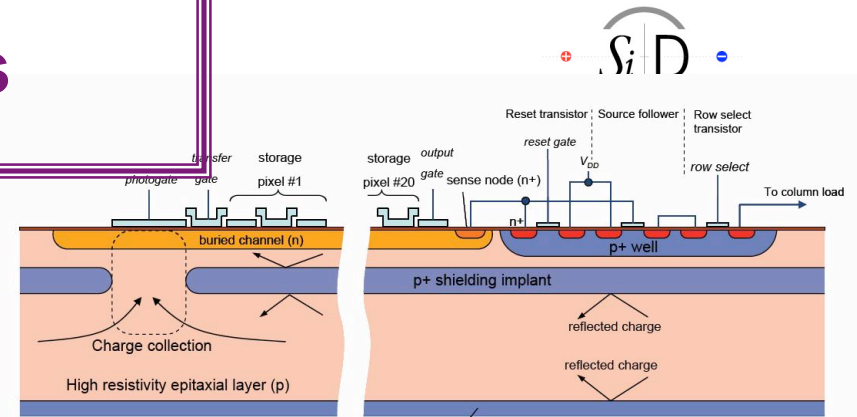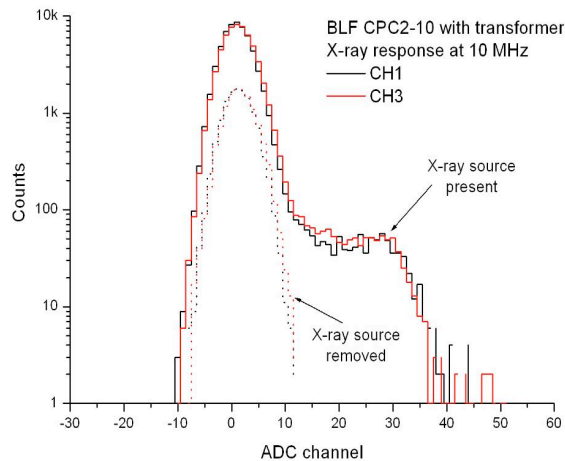
LCFI (Nomerotski)

Basic issue for CCD - time resolution

- Column-parallel CCD (LCFI)
  - Fast, parallel readout of columns
  - Achieved 45 Mhz (goal 50)
  - Requires ~20A of current/device
  - R&D on drivers, device capacitance, alternate structures

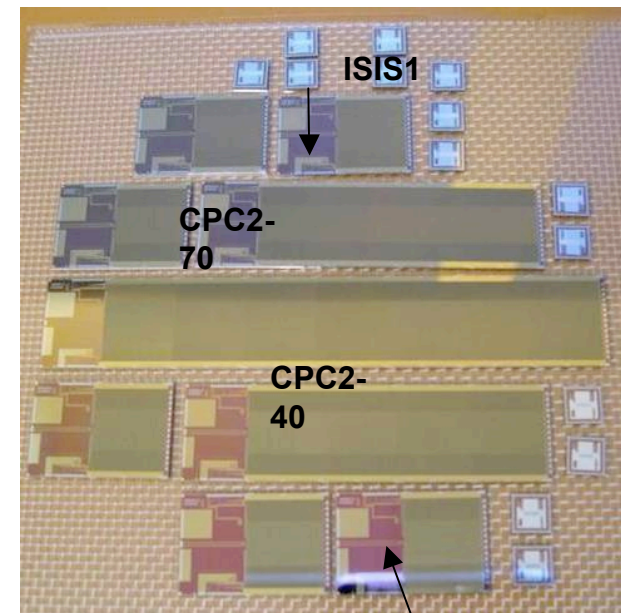Substantial chip and device development aimed at 50 Mhz

- CPC1/2 - sensors - low L, large area
- CPR1/2 - readout chips
- CPD1 - clock driver

- ^{55}Fe X-ray signals observed at up to 45 MHz!
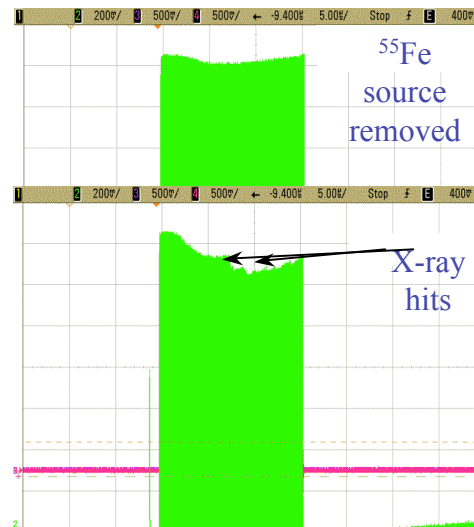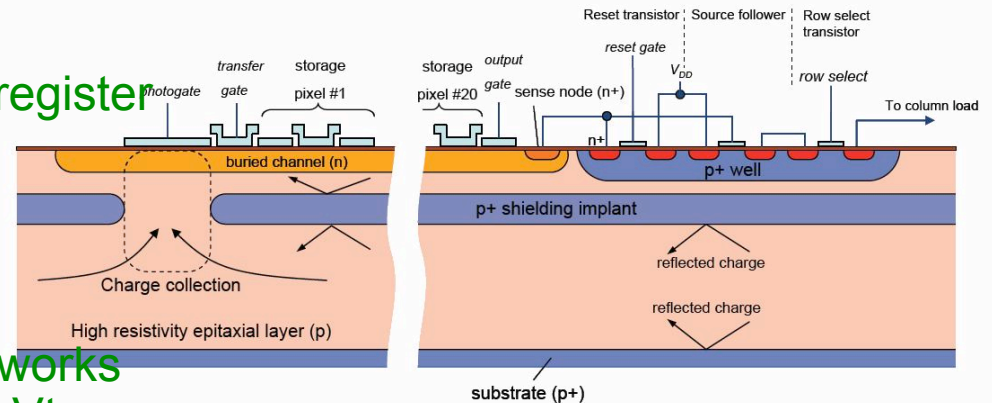

But noisy due to RF amp

LCFI II (Nomerotski)

ISIS

- Each pixel has its own 20-cell CCD register : store raw charge during collisions

- Increased resistance to EMI

- Column-parallel readout during quiet time at ~1 MHz

- ISIS1 without p-well tested first and works OK, ISIS1 with p-well has very large Vt, problem understood

Support structures

- Silicon-RVC foam sandwich (~3% density)

  – Foam (1.5mm thick), sandwiched between two 25 µm silicon pieces

  – Achieves 0.09% X0

- Silicon on SiC foam (~ 8% density)

  – Silicon (25 µm) on SiC foam

  – Achieves 0.16% X0

  – 0.09% X0 possible with lower density foams (< 5%)


RVC foam (foam thickness 1.5 mm)
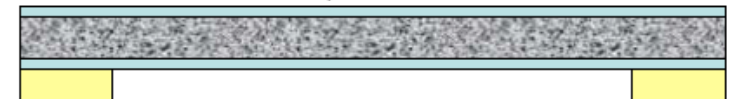
Silicon Carbide foam (foam thickness 1.5 mm)

Cluster Split CCD (Sinev)

- The most important effect is, that if physics event hit is limited to only one column, but some another hit (from background or electronics noise) appeared within timeframe consistent for combining hits in neighboring column, it will lead to wrong time assignment for our physics hit, so it will be thought as not belonging to given event, giving hit recognition inefficiency.
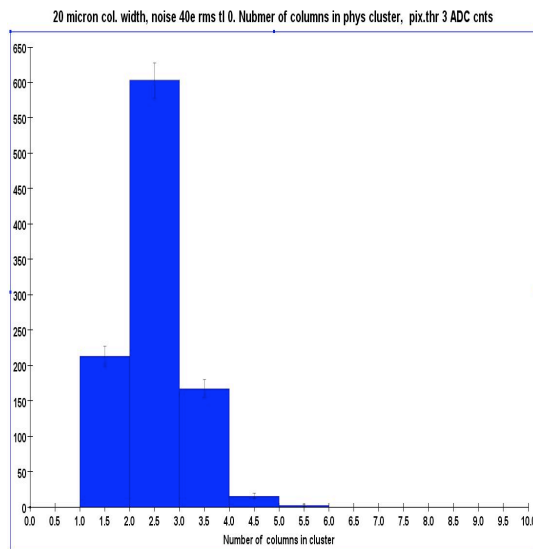
Example of number of column distribution. 20µ columns, but very low (3 ADC cnts) pixel thr.
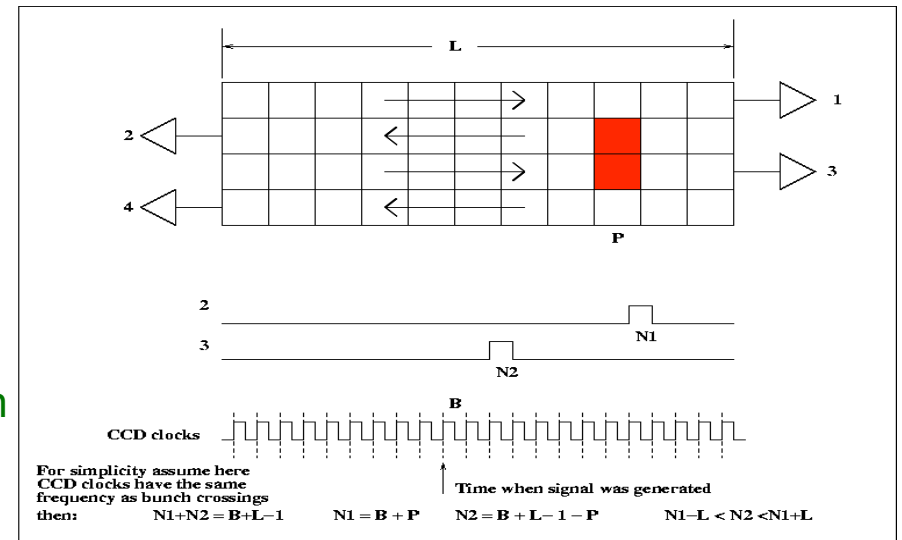
This is better at large dip angles, and can be improved by increasing epi thickness, but is the major issue with this technology

Chronopixel (Sinev)

- CMOS MAPS design
  - Single bunch (13 bit) digital time stamp
  - 4-deep hit buffers
  - 50x50 μm pixels
    - Scales to <20 microns in 45 nm
  - ~ 40 μW x f/channel
  - Depleted epi, binary readout
- Fabricate prototype in TSMC 180 nm process (if funded)
  - Thin (7 micron) epi layer
  - Lack of deep p-well limits sensitive area of depleted pixel to 5%
  - Test operation, unique features, understand charge collection, noise
- Depends on scaling to 45 nm
  - Deep p-well process with thick epi layer is necessary
  - Is digital gate leakage current important?
  - Does power/pixel (capacitance scaling) remain constant?
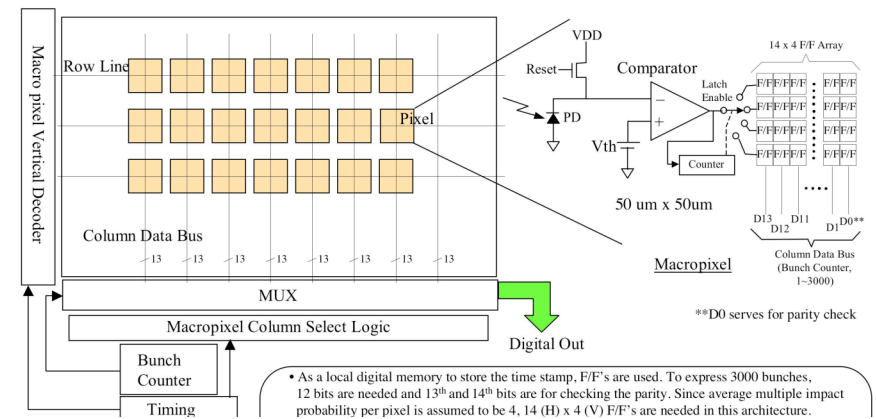
MAPS/SOI (Battaglia)
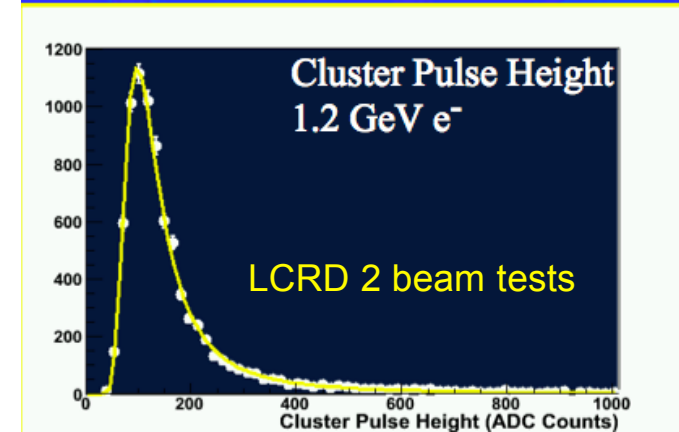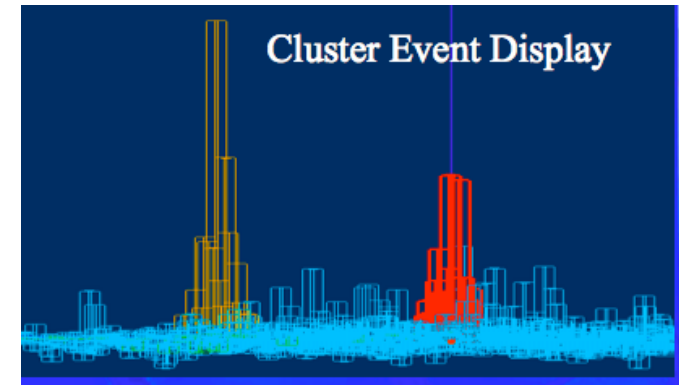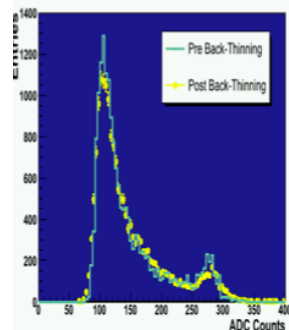
LBL is working in several areas:

- Analog MAPS - LDRD 1, 2, 3
    - 10-40 micron pixels
    - Progression in complexity (CDS, digitization)
- LCRD-SOI 10 micron analog and binary pixels
    - OKI/KEK SOI
- Backthinning studies
    - 90% yield @50 μm
- Test beams - Advanced Light Source
    - 3 layers thinned Mimosa 5
    - 8.5 μm extrapolation resolution
        - Consistent with ILC vertex requirements
- Test beams - FNAL
    - 4 layers of 50 μm Mimosa 5
    - 4 layers of LDRD 2
        - Study LDRD 1, 2, SOI

Cluster Event Display

Cluster Pulse Height 1.2 GeV e⁻

LCRD 2 beam tests

⁵⁵Fe Determine chip gain and S/N for 5.9 keV X rays

Collimated Laser Compare charge collection in Si at different depths
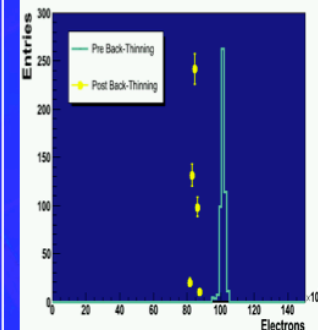
1.5 GeV e⁻ beam Determine S/N and cluster size for m.i.p.

Pre Back-Thinning
Post Back-Thinning

Response before/after thinning

SOI/3D (Lipton)

3D Concept

- Designs based on newly available technologies, separate circuit, detector layers
  - SOI - thin circuit layer on oxide on fully depleted substrate (OKI, ASI(Cypress))
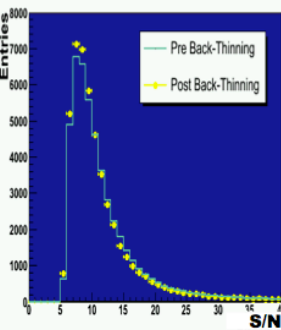   - 12 bit 26 micron x-ray counting chip OKI/KEK (due soon)
    - ILC pixel readout chip (designed)
  - 3D - multi-layered circuit assembly based on thinned, bonded silicon
    - Full time stamp/double correlated sample in 20 micron pixel, low power
    - Due back in August
  - Thinned sensors - MIT-LL
    - 50, 100 microns thick, 4-side abuttable
  - S/N ~100:1 in SOI/3D
  - Demonstrated laser annealing of backside
  - Demonstrated FPIX chip thinning to 15 microns
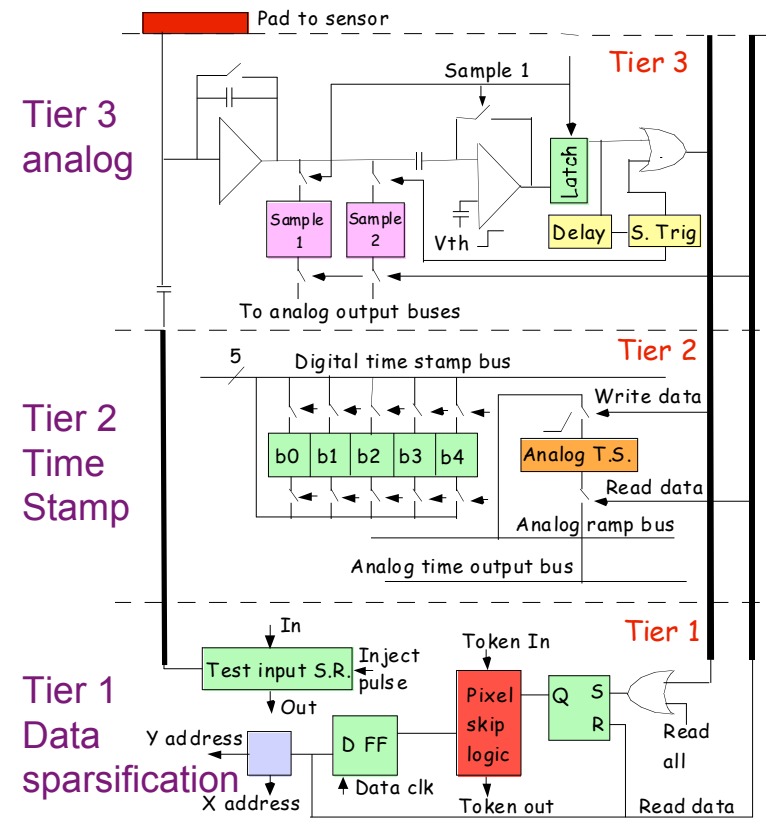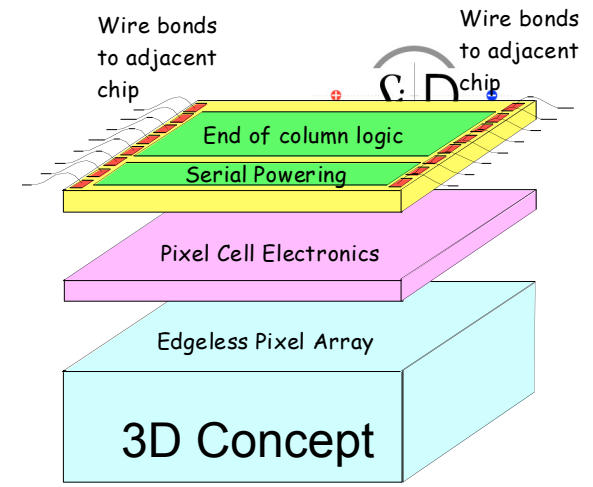
Mechanical (Cooper/Lubatti)

Vertex CF support structures

- Develop techniques for fabricating and handling thin-walled carbon fiber structures
  - Current design has cutouts to reduce material
- Develop assembly tooling/mandrels
- Prototypes of carbon-fiber support structures
  - Three delivered to FNAL
- FEA analysis of mechanical and thermal behavior
  - Deflection under gravity OK
  - Thermal deflections unacceptably large - assuming -10 deg C operation
    - Removing cutouts helps
    - Operating at RT would help more

Learn how to work with thinned silicon and goissimer supports
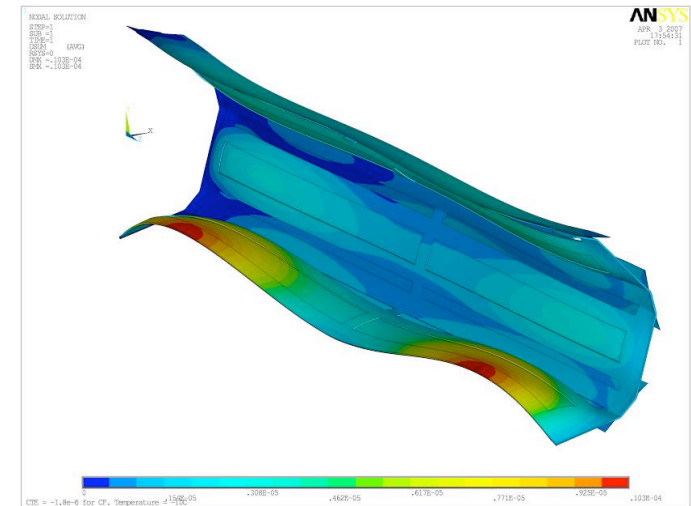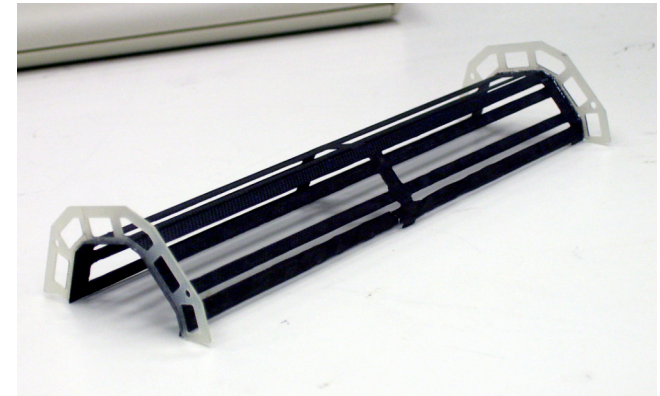
δ = 10.3 μm, Δt=10 deg

EMI (Sinev)

Results of a End Station A study of beam-induced EMI

- Based on problems experienced at SLD - VXD phase-lock loops failed during beam crossings

- Antennas placed near (~1 m) gaps observed pulses of EMI in the high MHz range with strengths up to ~20 V/m.

- The pulse shapes are very stable over widely varying beam conditions indicating they are determined by the geometry of the beam line elements.

- The pulse amplitudes varied in proportion to the bunch charge but were independent of the bunch length.
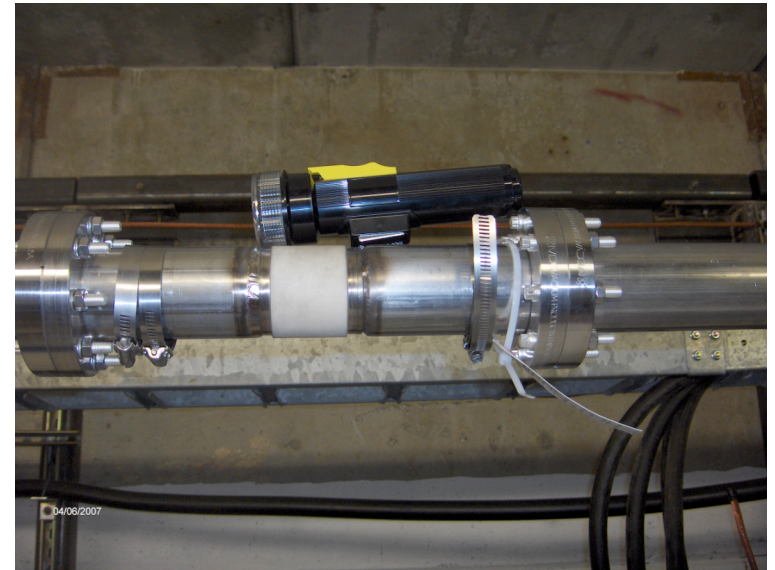
Recent Results

- A single layer of common 5mil aluminum foil was placed over the ceramic gap and clamped at both ends to provide an image current path.

- The signal amplitude was reduced by >x10 (eliminated?)

Is there any reason to have gaps in the pipe?

How close to the IR?

To what extent is this a design constraint on the vertex and tracking?

Other Technologies

- DEPFETs
  - Charge amplification internal to detector
  - Potentially low power
  - Needs ancillary circuitry
- Small pixel CCDs (Japan)
- CMOS MAPS
  - IRES-centered effort - mostly rolling shutter
  - INFN - a number of deep submicron prototypes
  - FAPs, CAPs - designs with internal buffers

Material

- Disipline and vigilence

LHC

VXD hit coverage

SiDMay06

VXD material summary

Readout & services
Mechanical Support
Beam pipe
Sensors
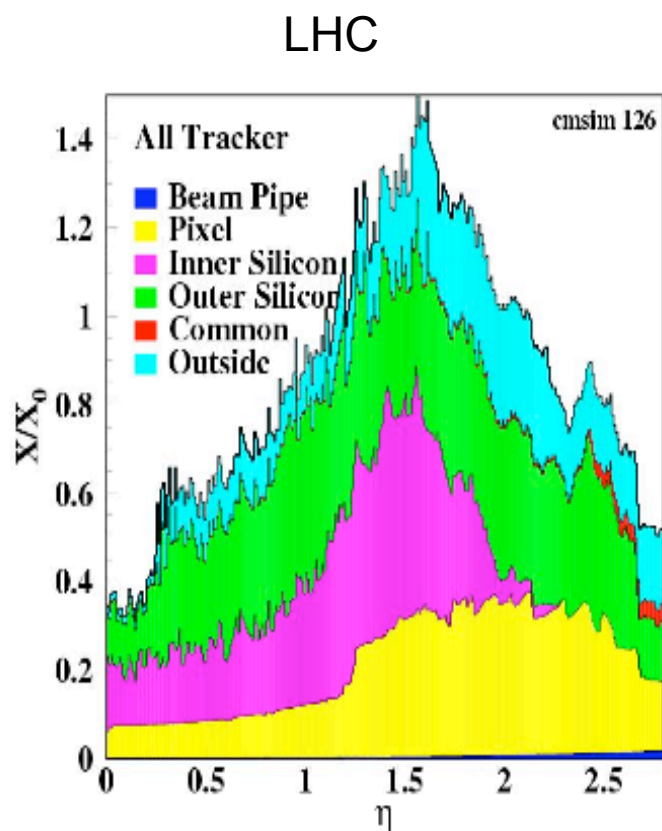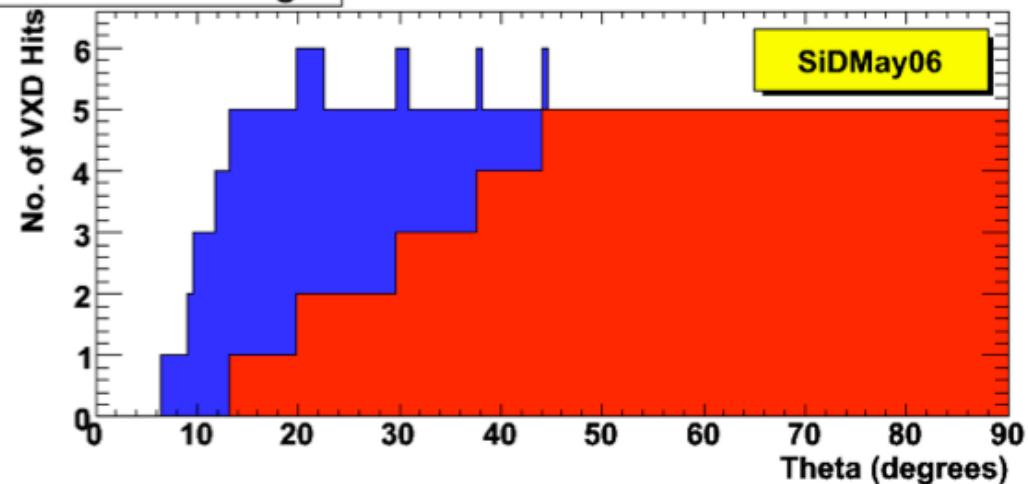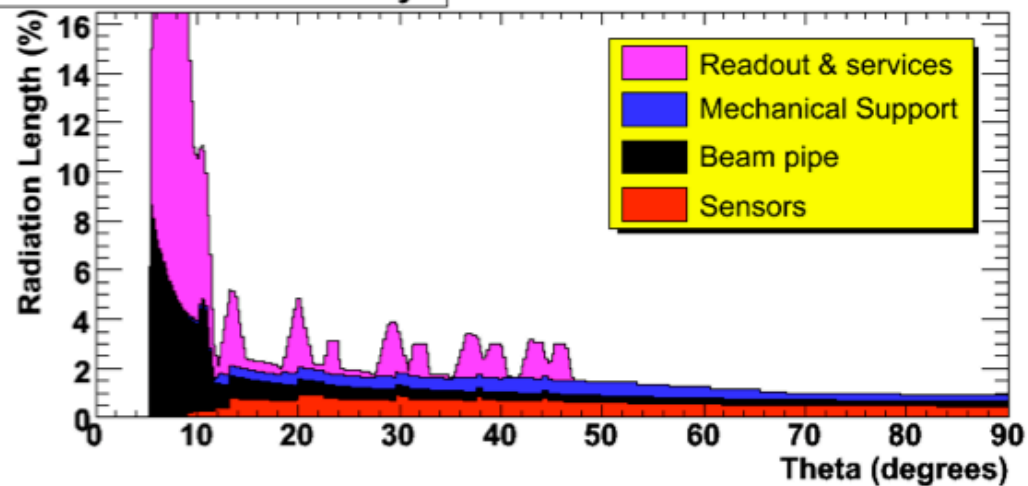
Figure 33 VXD hit pattern and material summary as a function of polar angle.

Simulation

- LBL (Battaglia)
  - 50 μm detector thickness ~optimal
  - Implemented sensor simulation and cluster analysis
    - CDF vertex fit
    - Jet flavor tagging/physics analysis of DM-SUSY scenarios
  - Validated simulation with test beam
  - Pair background simulation
- LCFI (Nomerotski)
  - Implementation of ZVTOP algorithm used at SLD
    - ZVKIN part (ghost track) is implemented as well
  - Flavour Tagging Package is using Neural Net based on inputs from the Vertexing Package
  - Both packages are fully interfaced to MarlinReco reconstruction framework
    - Marlin processes exist for all parts of the two packages
  - Plan to officially release in April

Technology R&D Issues

Technology	R&D Issues (my interpretation)
CP CCD	Operation at 50Mhz, clock power, cryogenic operation
ISIS	Pixel size, demonstrate performance with p-well, pixel readout design
SC CCD	Lack of charge sharing can mis-assign hits, more detailed conceptions of device geometry, proof of principle
Chronopixel	Proof of principle, device scaling to 45 nm - scaling of s/n, power
MAPS	Power, optimization of time resolution
SOI	Proof of principle, back gate effects (OKI), analog/digital shielding
3D	Proof of principle, manufacturability, yield

Forward Region

- Not addressed at this workshop
- Assuming pixels for the forward region
  - What are we asking of the forward disks
    - IP resolution - dominated by barrels
    - Pattern recognition
  - Integration with forward silicon design
  - Pixel size
    - Maximum size -> minimum power
    - Support and geometry

Vertex barrel ~ 150,000 mm^2
Vertex Disks ~ 120,000 mm^2

IP Resolution, Disks, 1 Gev Tracks

- varying resolution
- varying radiation length

Microns (y-axis, 0 to 25)

Hit resolution (micron) or RL x 10^-3 (x-axis, 0 to 25)
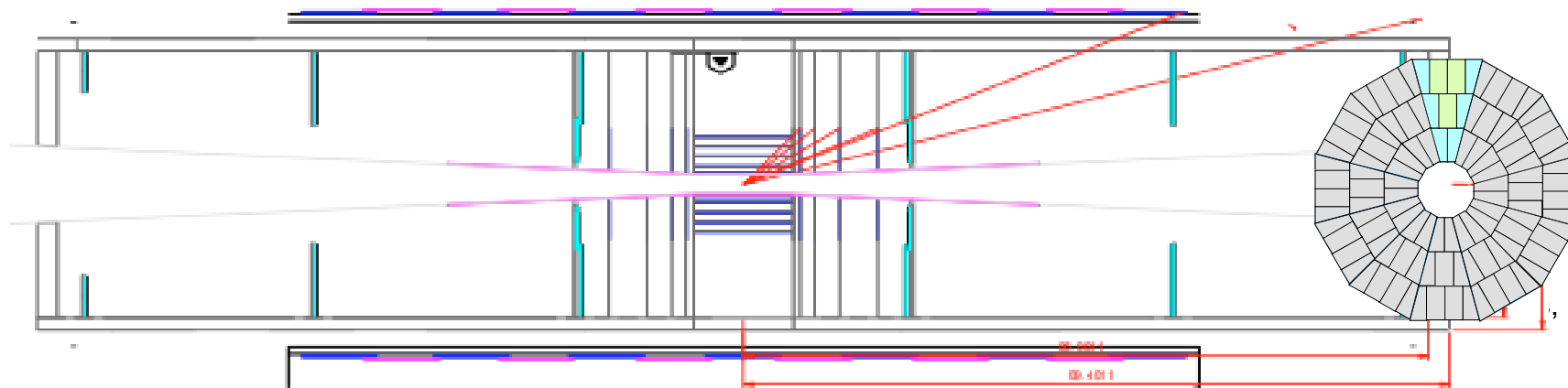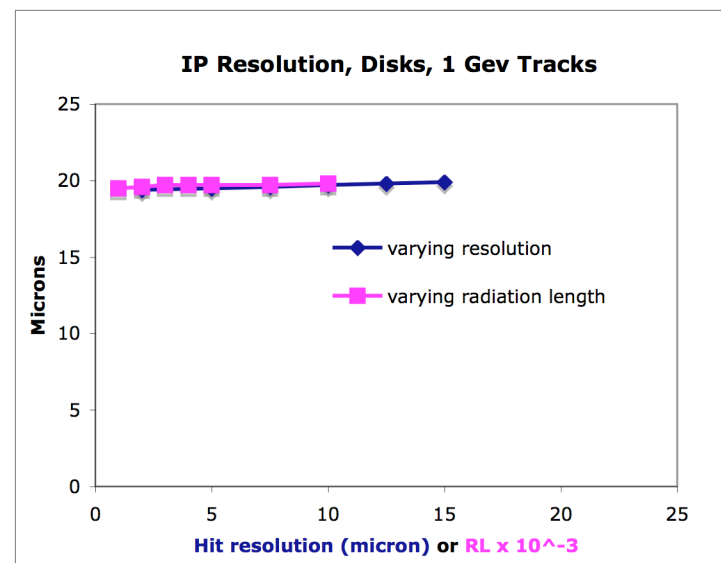
Noise and Power

- Last week Chris brought up the question of the relation between device scaling and noise/power - my interpretation of Helmudt Spieler's answers: series white noise:

$$ENC^2 = (C_{\text{det}} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

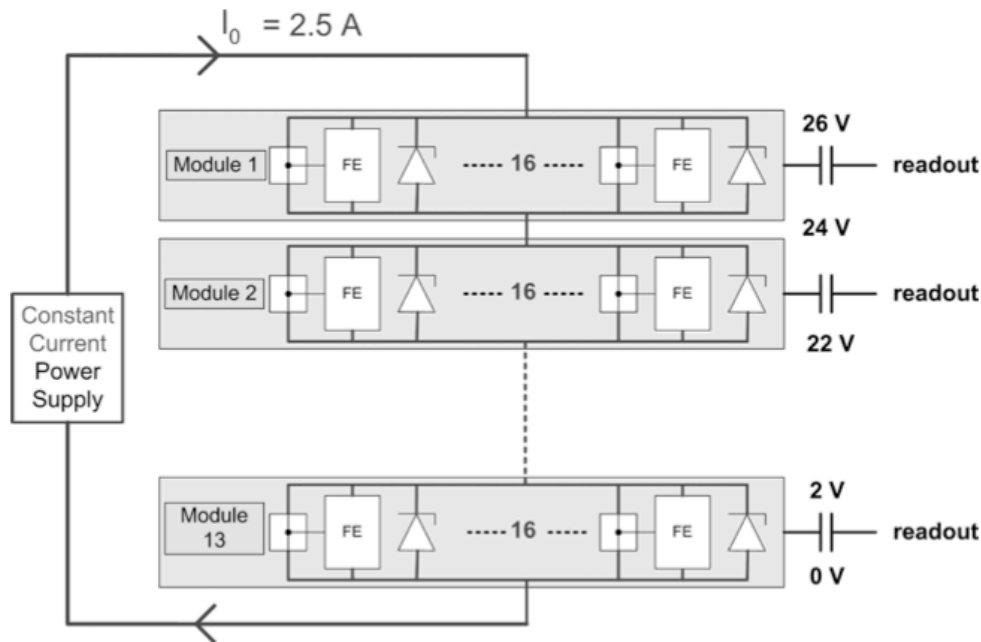- Noise scales as C and 1/sqrt[transductance (g_m)]
- Pixel front end transistors will operate in weak inversion - where g_m is independent of device geometry and $\sim(I_d q/kT)$.
- Acceptable low current operation (<1 μA) requires long shaping and/or low node capacitance
  - For 50e noise, t_s = 100ns, I_d=0.5 μA $C_d \sim 100\ ff$
  - ~10 ff should be achievable in SOI devices, 20-40 in MAPS

Power Distribution

- Power is a crucial issue for the vertex detector
  - CP CCD 20 amps x 200 modules = *4000 amps* of clock
  - MAPS or SOI 20-100W x 100(DF)@1V = *2000 - 10,000 amps*
- LHC detectors are seriously compromised because power was not a driver from the start
- Vertex detector technology is sexy - but power engineering is just as important
  - Serial powering (think Xmas lights) can lower instantaneous current
    - Understand noise, engineer regulators, understand interconnects
  - Lower CCD capacitance
  - Routing within SiD
    - Include something capable of providing 2-10kW during train in simulation

Serial Power

Fig. 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt regulator generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

Atlas SLHC design

Initial tests indicate good noise performance

- instantaneous power = average power x 50-100) (achievable rise/fall times). 20W=>2kW
- At 1.5 V peak current ~666 A, 3 cm diam. of copper/side needed for 50mV drop

- Serial powering can reduce peak currents
  - Individual ladder regulators
  - V*n, I/n, ΔV tolerances relaxed with local regulation
  - Being pursued for SLHC, primarily by ATLAS

Plans - Near Future

- Continue technology R&D on several fronts (~independent of SiD)
  - Chronopixel
    - first prototype - bench and laser tests
  - Detailed tests of CMOS APS chips
    - Beam tests, optimized design
  - CCD
    - continued refinement of designs, optimize for low power
  - SOI
    - demonstration devices soon, beam and laser tests
  - 3D
    - demonstration chip this summer
    - plan for integrated sensor fabrication (cost, multiproject opportunity?

Strawman Milestones
too aggressive? comments?

Si D

fall 2007	Ask proponents to provide conceptual designs of technologies which meet ILC goals including mass, power, position resolution, and time resolution (Vertex review)
fall 2008	Demonstrate detector performance of small-scale prototypes in test beams
spring 2009	Demonstrate workable mechanical/electrical design for candidate technologies
fall 2009	Choose one or two target technologies
fall 2010	Fabricate sample ladders and wedges for VXD with readout in target technologies

- The CDR would not specify a particular technology, but should address system issues that could affect physics.
  - Power distribution, including plans for serial or DC-DC powering
  - Interconnect issues, and additional mass
  - Support and mechanical issues, these could be quite different for various technologies (CCD, MAPS …)

Conclusions

- Vertex system is most sensitive to evolving technology
  - late decision will probably give best performance -like buying computers
  - Conflict with "milestones"
- Real progress in several areas - understanding EMI, CCD technology, mechanical supports first versions of 3D, SOI, Chronopix design
- Need more work on the guts
  - Forward region
  - Power distribution
  - Interconnections