ILC Vertex Tracker R&D at LBNL

From Sensors to Physics Benchmarking

M. Battaglia

UC Berkeley and LBNL

with J.M. Bussat, D. Contarato, K. Deck, P. Denes, L. Glesener,
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B. Nguyen, C. Nguyen, D. Shuman

SiD Meeting
Fermilab, April 11, 2007

LAWRENCE BERKELEY NATIONAL LABORATORY
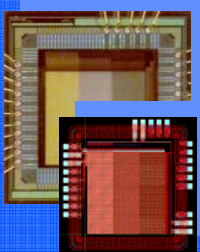
Probing the Architecture Matrix
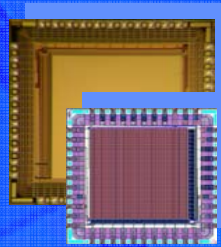
Analog Pixel Architecture

- Charge Interpolation $[\sigma \sim a/(S/N)]$
- In-pixel CDS & On-chip Digitisation
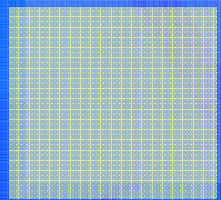- Fast Readout

Binary Pixel Architecture

- Small Pixels $[\sigma = \text{pitch}/\sqrt{12}]$
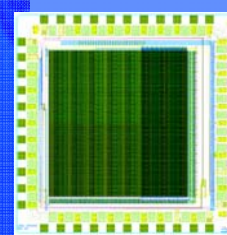- In-pixel Discr. & Time Stamping
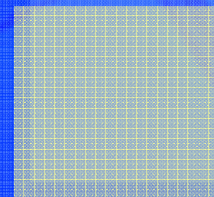- In-situ Charge Storage

LDRD-1 (2005):
10, 20, 40μm pixels

LDRD-2 (2006):
20μm pixels,
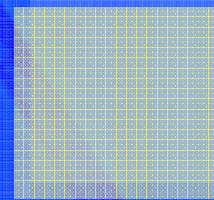in-pixel CDS
3-T and SB pixels

LDRD-3 (Summer 2007):
20μm pixels,
in-pixel CDS, 50 MHz r/o
on-chip 5-bit ADCs

LDRD-SOI (2007):
10μm pixels,
analog & binary pixels

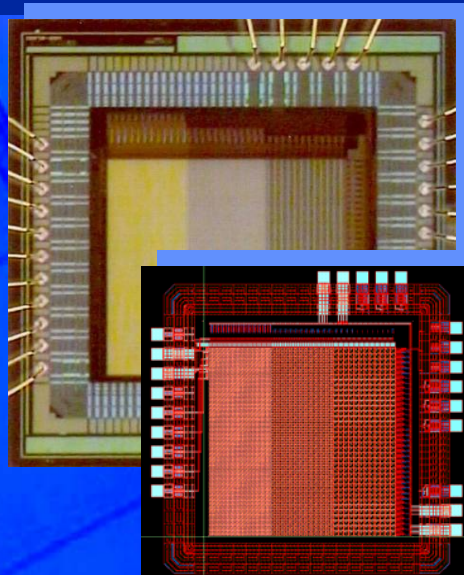**In progress** (2008):
10μm pixels,
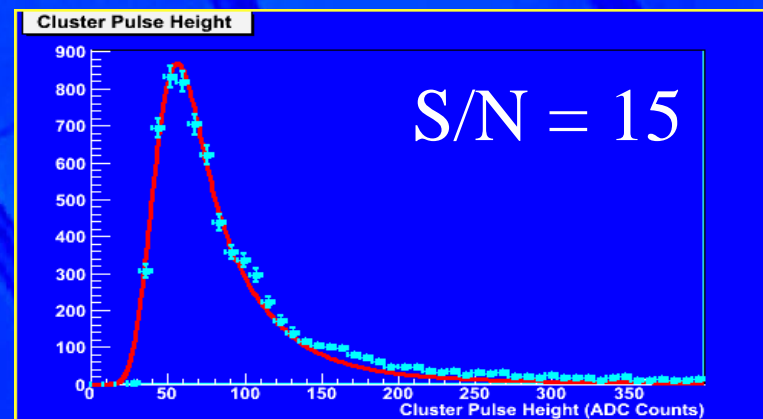binary pixels
in-pixel time stamp

. . .

LDRD-1 Chip

LDRD-1 Chip:

First LBNL test structure, simple 3T pixels, analog output, 3 matrices with 10x10 μm^2, 20x20 μm^2 and 40x40 μm^2 pixels;

AMS 0.35 OPTO process

m.i.p. response with 1.5 GeV e$^-$ beam at ALS

Cluster Pulse Height

$S/N = 15$

Cluster Pulse Height (ADC Counts)

Resolution Study (focused laser spot)

Pitch (µm)	Laser Scan	Pixel Sim
10	2.0	1.5
20	3.3	3.2
40	5.1	5.0

850 nm Laser Scan, 40×40 µm² Pixels

40 µm
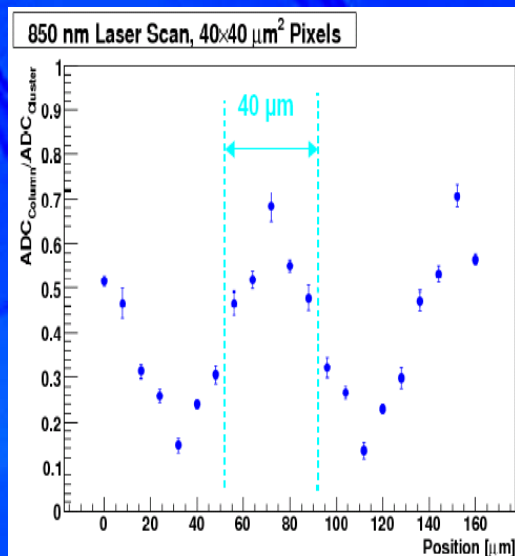
Radiation Hardness Test with 30 MeV p and n at 88" Cyclotron

Average Noise vs Fluence

- ▲ 10×10 µm
- ★ 20×20 µm
- ▼ 40×40 µm

1.5×10^{12} p cm^{-2}

Integrated Fluence [10^{12} p/cm²]
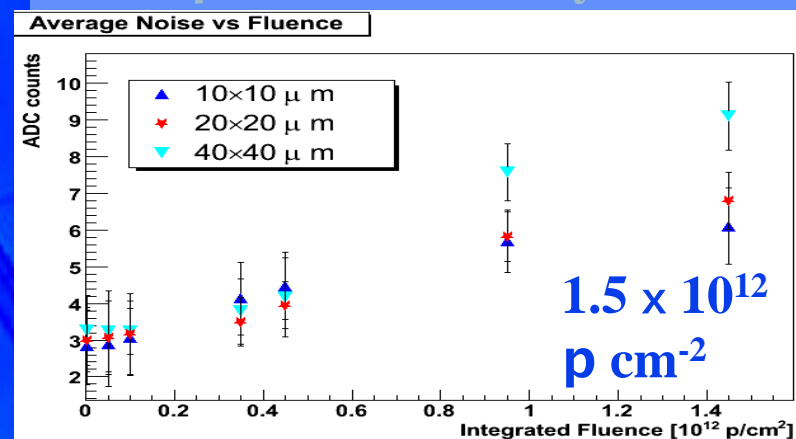
LDRD-1 Chip: Charge Collection Time
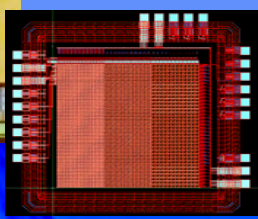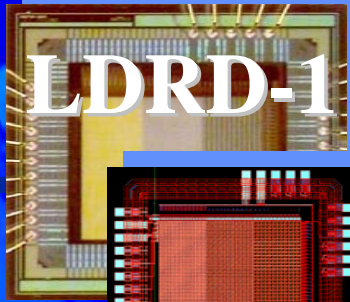
Charge carriers collected by diffusion in almost field-free epitaxial layer;

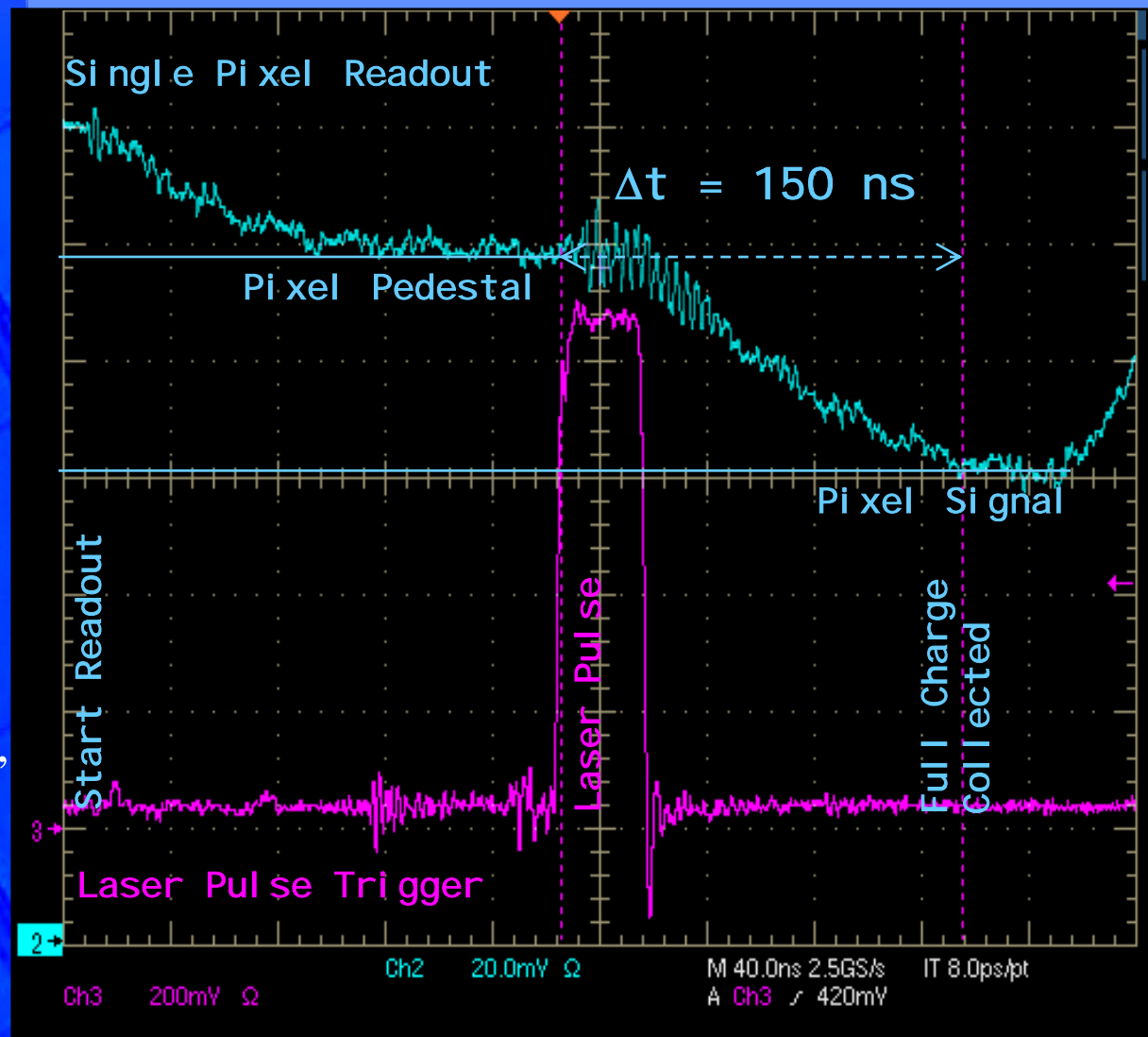First measurement of charge collection time in AMS 0.35-OPTO process;

1 ns 1060 nm Laser pulse collimated on 20x20μm pixel, charge = 1 m.i.p.

Charge collection time
$\Delta t \sim 150$ ns

Single Pixel Readout

$\Delta t = 150$ ns

Pixel Pedestal

Pixel Signal

Start Readout

Laser Pulse

Full Charge Collected

Laser Pulse Trigger

Ch2   20.0mV Ω
Ch3   200mV   Ω
M 40.0ns 2.5GS/s   IT 8.0ps/pt
A Ch3 ∫ 420mV

LDRD-2 Chip

LDRD-2 Chip:

Second generation chip features more complex pixel architecture (20 transistors) with in-pixel CDS, power cycling, different bias options and diode sizes, option of rolling shutter for 50 MHz read out and circuitry for charge injection test.
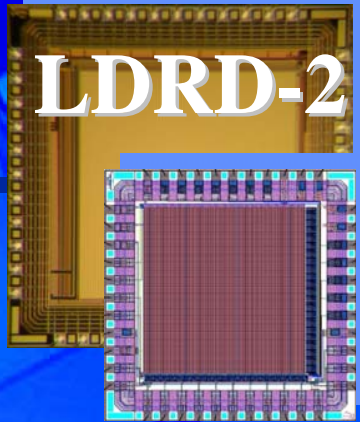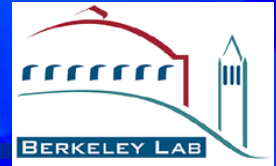
Size: 1.5x1.5 mm^2
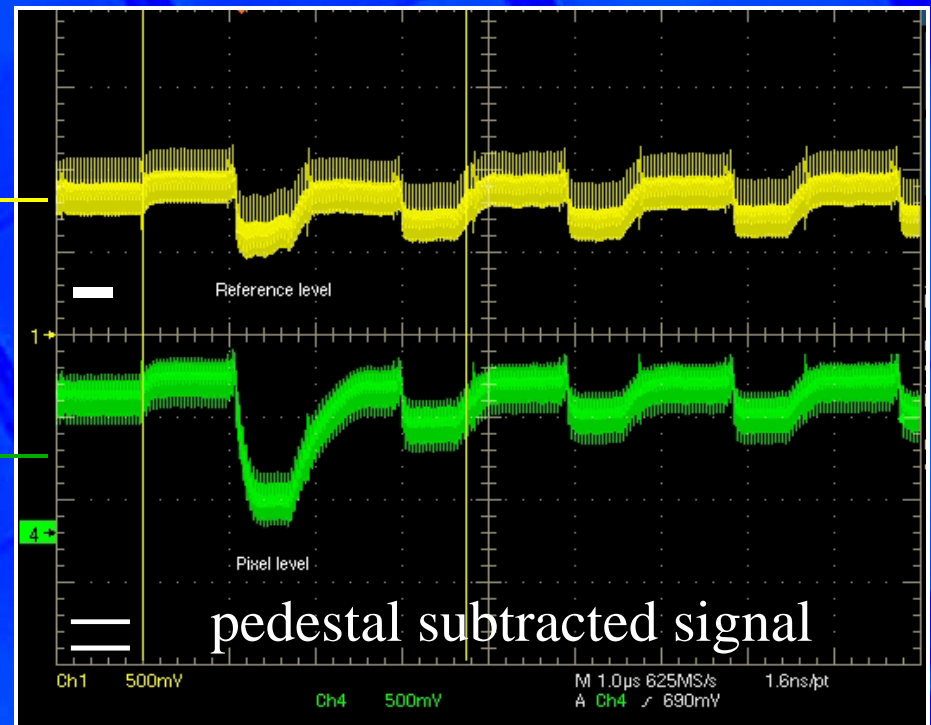6 matrices of 20x20 μm^2 pixels;

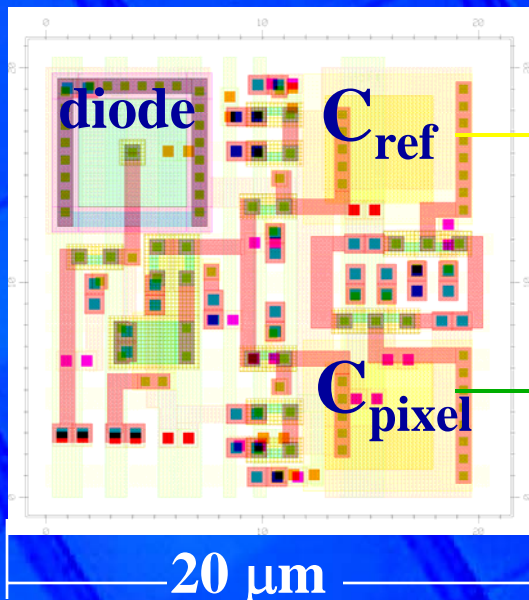AMS 0.35-OPTO process, received October 2006
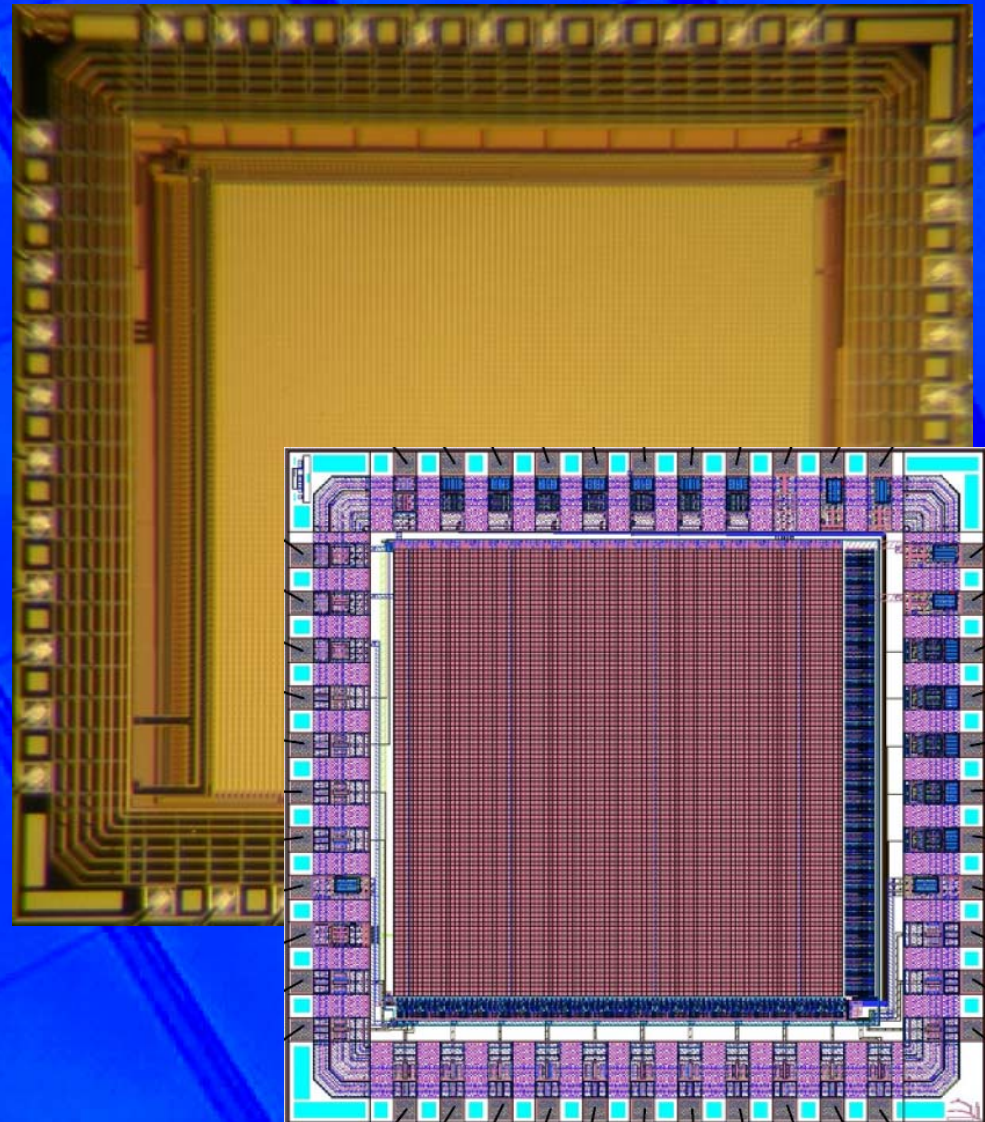
LDRD-2 Chip: In-Pixel CDS

Digitisation at end of pixel column limited in precision by speed and power dissipation: advantageous to subtract pedestal level in-pixel with correlated double sampling.

Stored reference and **pixel level** with pulsed laser light:

diode C_{ref} C_{pixel}

20 μm

Reference level

Pixel level

pedestal subtracted signal

Ch1 500mV   Ch4 500mV   M 1.0μs 625MS/s   1.6ns/pt
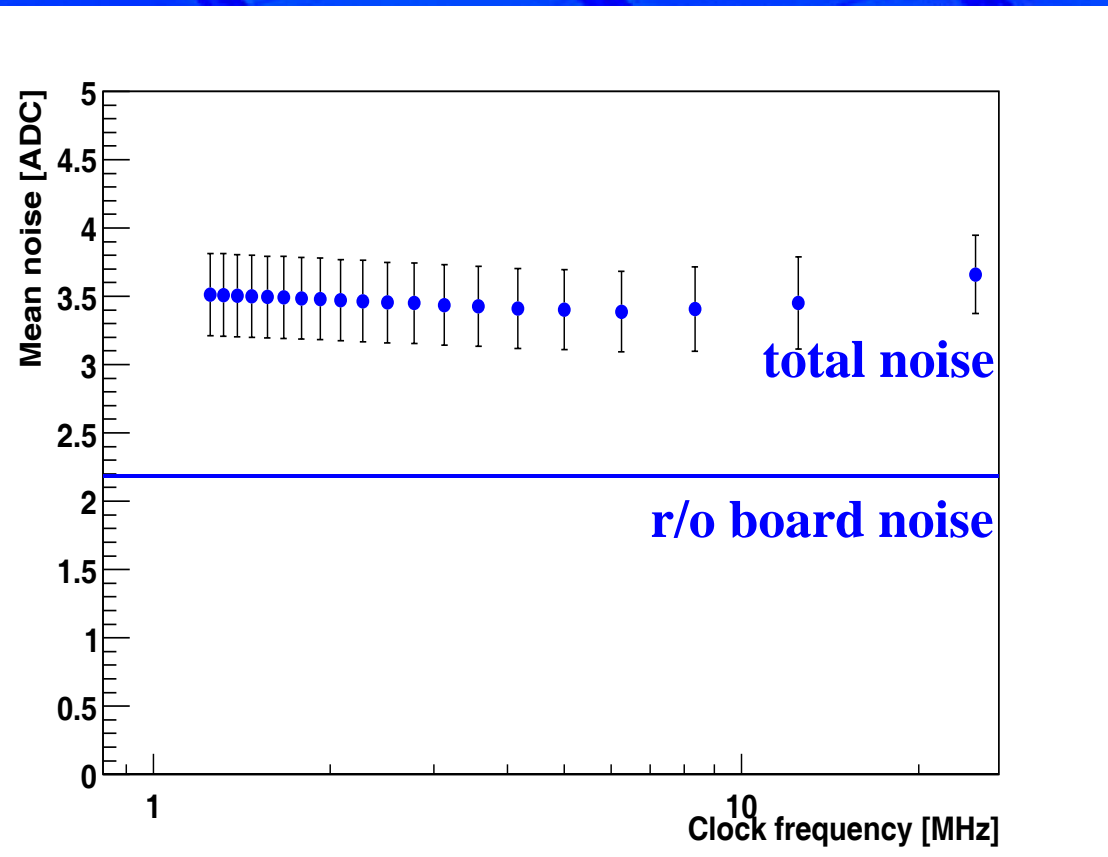   A Ch4 ↗ 690mV
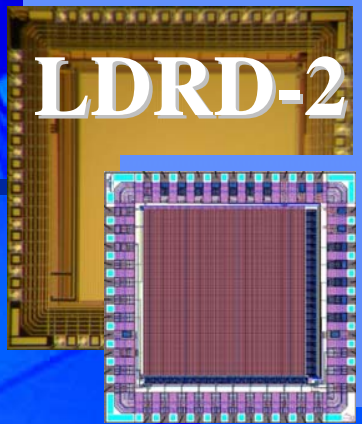
LDRD-2 Chip: r/o Speed
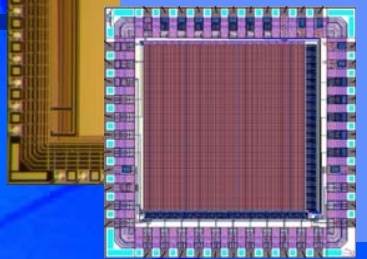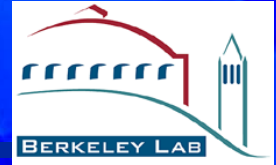
Plan to run LDRD-2 at
15-20 MHz in beam test;

Tested in lab up to 25 MHz
without significant noise
degradation.

Noise vs. T measured down
to 5ºC, shows little variation.
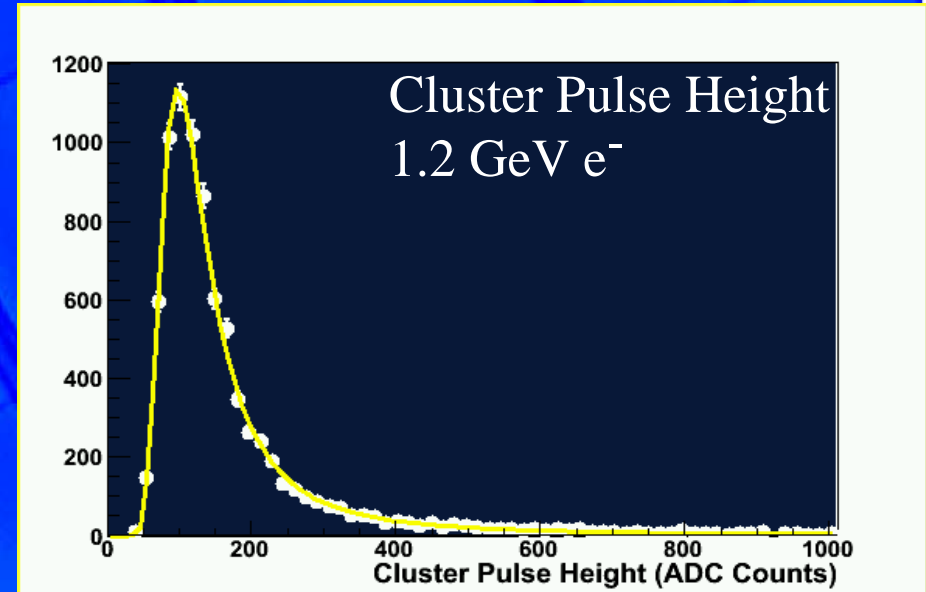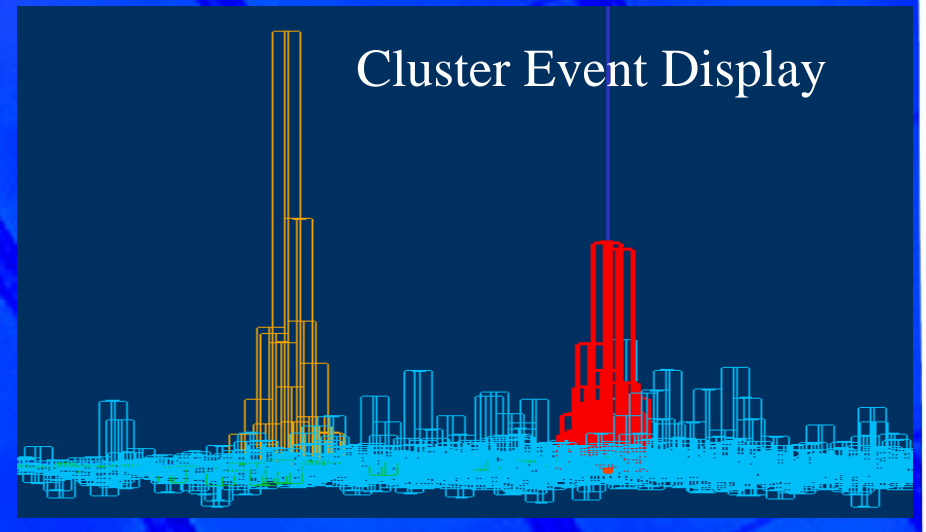
LDRD-2 Chip: ALS Beam Test

First LDRD-2 beam test on ALS BTS 1.2 GeV e⁻ beam;

Operated in rolling-shutter mode, CDS from in-pixel stored ref. charge, 6.25 MHz r/o speed, noise stable up to 25 MHz and limited by r/o board:

Preliminary results @ 27ºC

<Nb. of Pixels in Cluster>	4.9
<S/N>	19.5

Cluster Event Display

Cluster Pulse Height 1.2 GeV e⁻

Multiple Scattering and Sensor Thickness

e⁺e⁻ → HZ→bbμ⁺μ⁻ at 0.5 TeV
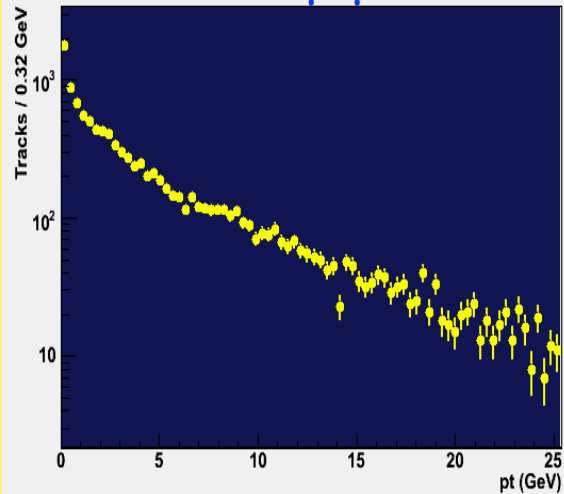
Preserving track extrapolation accuracy to bulk of particles at low momentum requires ultra-thin sensors and ladder structure:

Mokka+Marlin
Simulation of VXD02

$$\sigma = a \oplus \frac{b}{p_t}$$

Sensor Thickness µm	a µm	b µm
25	3.5	8.9
50	**3.7**	**9.6**
125	3.8	11.7
300	4.0	17.5
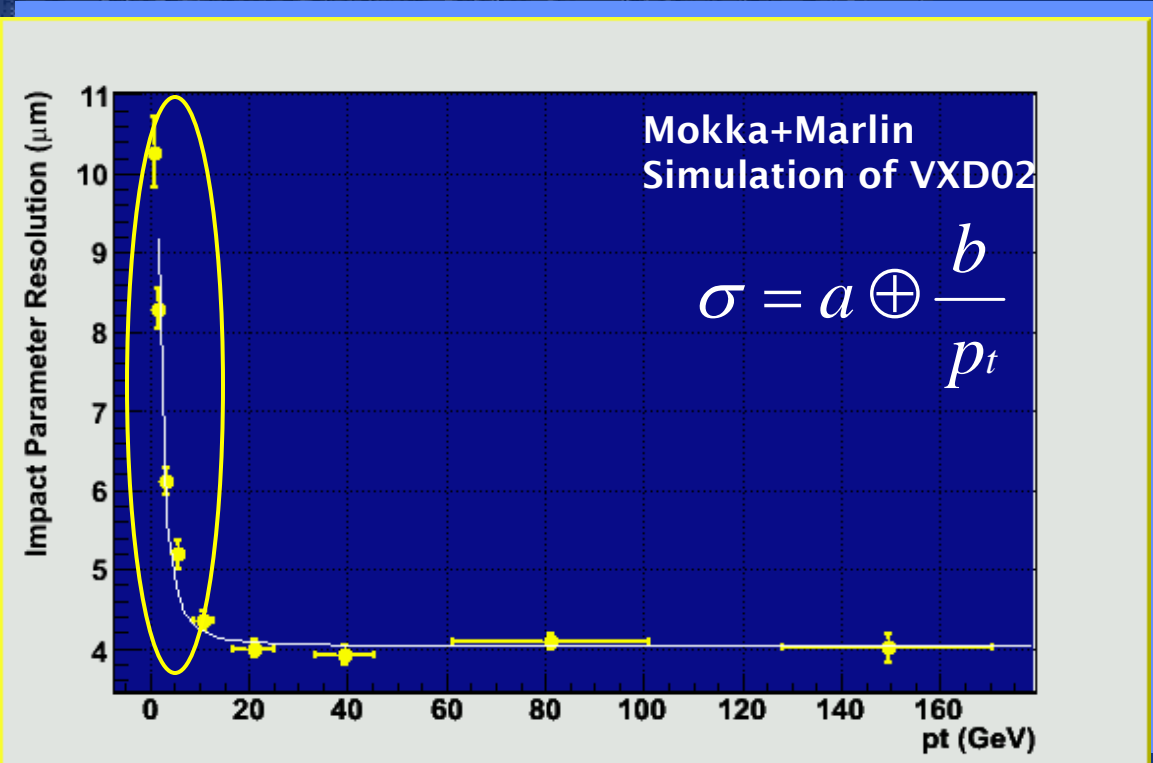
→ need thin monolithic pixel sensor.

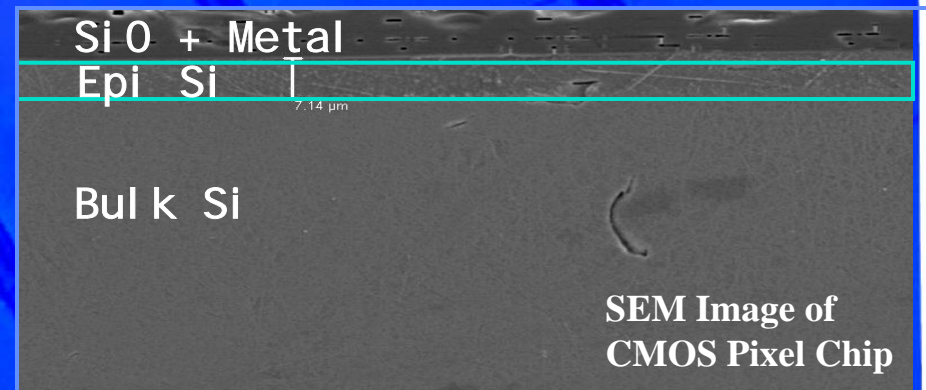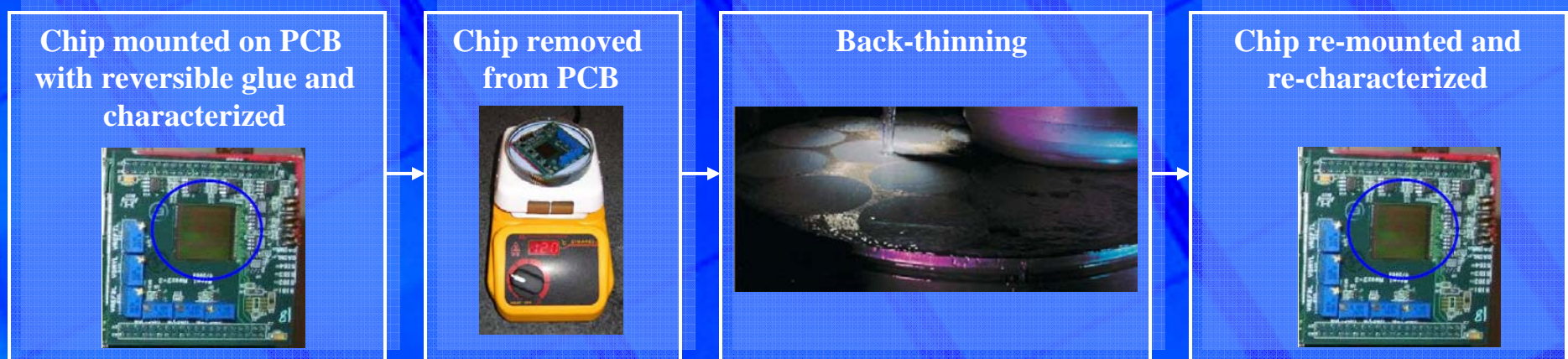# CMOS Sensor Back-thinning

Thin sensitive epi-layer makes CMOS Pixel sensors in principle ideally suited for back-thinning w/o significant degradation of performance expected (especially S/N), but questions arise from earlier results;

Si O + Metal
Epi Si
7.14 μm
Bulk Si

SEM Image of CMOS Pixel Chip

Back-thinning of diced CMOS chips by partner Bay Area company: Aptek.
Aptek uses grinding and proprietary hot wax formula for mounting die on grinding plate:

Backthinning yield ~ 90 %, chip thickness measured at LBNL after processing:
"50 μm" = (50 ± 7) μm , "40 μm" = (41 ± 6) μm; three chips fully characterised:

Chip mounted on PCB with reversible glue and characterized

Chip removed from PCB

Back-thinning

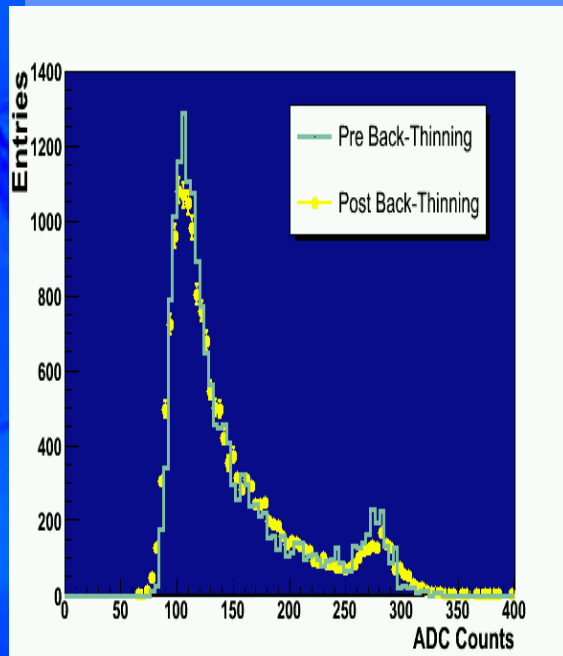**Chip re-mounted and re-characterized**

40 μm Back-thinned Sensor Tests

Study change in charge collection and signal-to-noise before and after back-thinning:
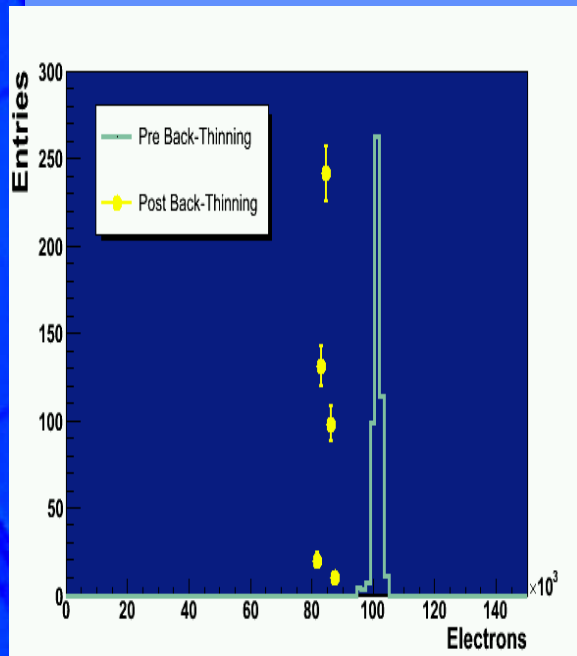Mimosa 5 sensors (IPHC Strasbourg), 1 M pixels 17 μm pitch, 1.8x1.8 cm² surface

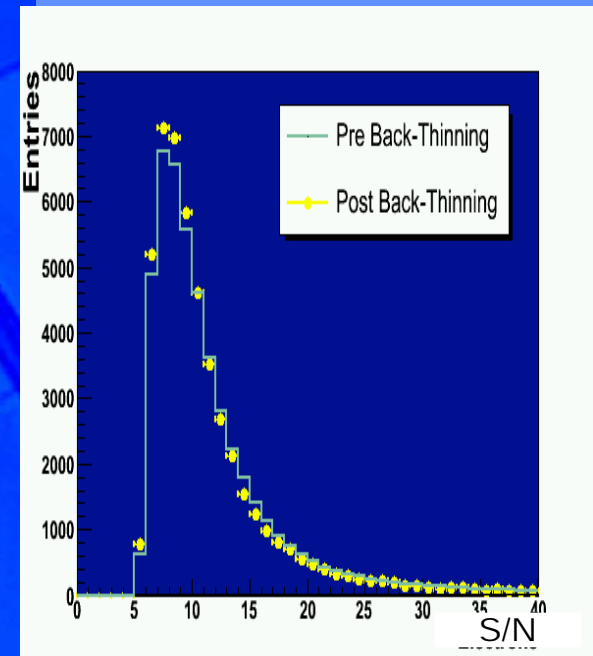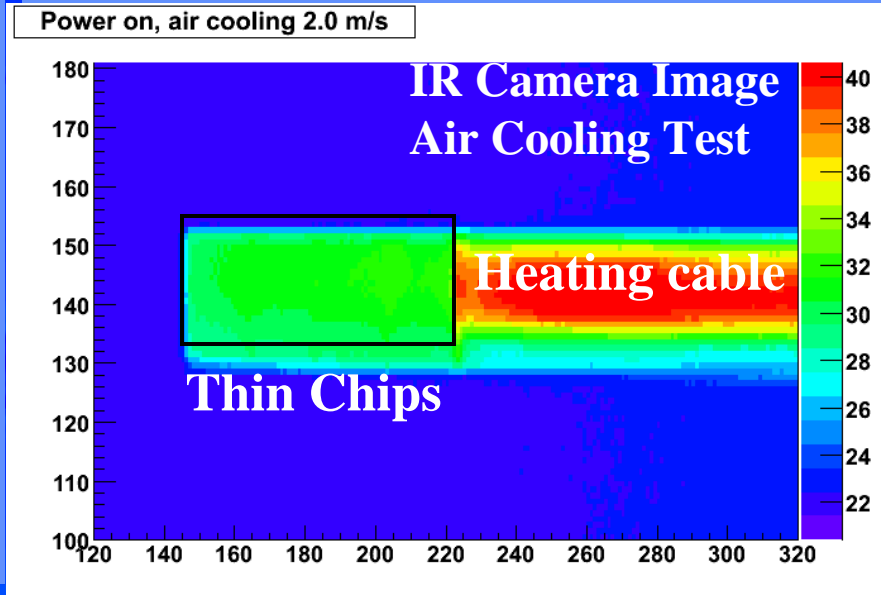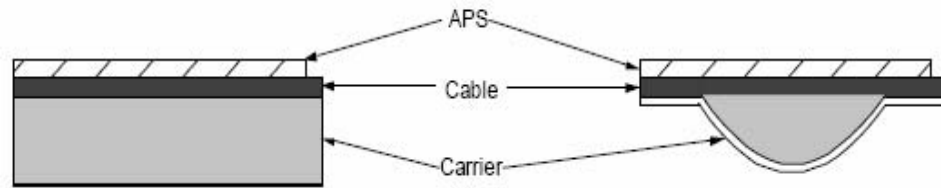| ^{55}Fe	Collimated Laser	1.5 GeV e⁻ beam
Determine chip gain and S/N for 5.9 keV X rays	Compare charge collection in Si at different depths	Determine S/N and cluster size for m.i.p.

Feasibility of Back-thinning CMOS sensors demonstrated

VTX Ladder Design & Testing

LCRD program of engineering design, construction and characterization of full ladder equipped with back-thinned CMOS pixel sensors

• Mechanical and thermal characterization of STAR prototype, study of heat removal using low-speed airflow;

• FEA of prototype structures: (core-cooled Si/CF/RVC sandwich, Si/Al/RVC sandwich, CVD coated CF) in progress using data from surveys of 40 and 50 μm thin chips, first results promising;
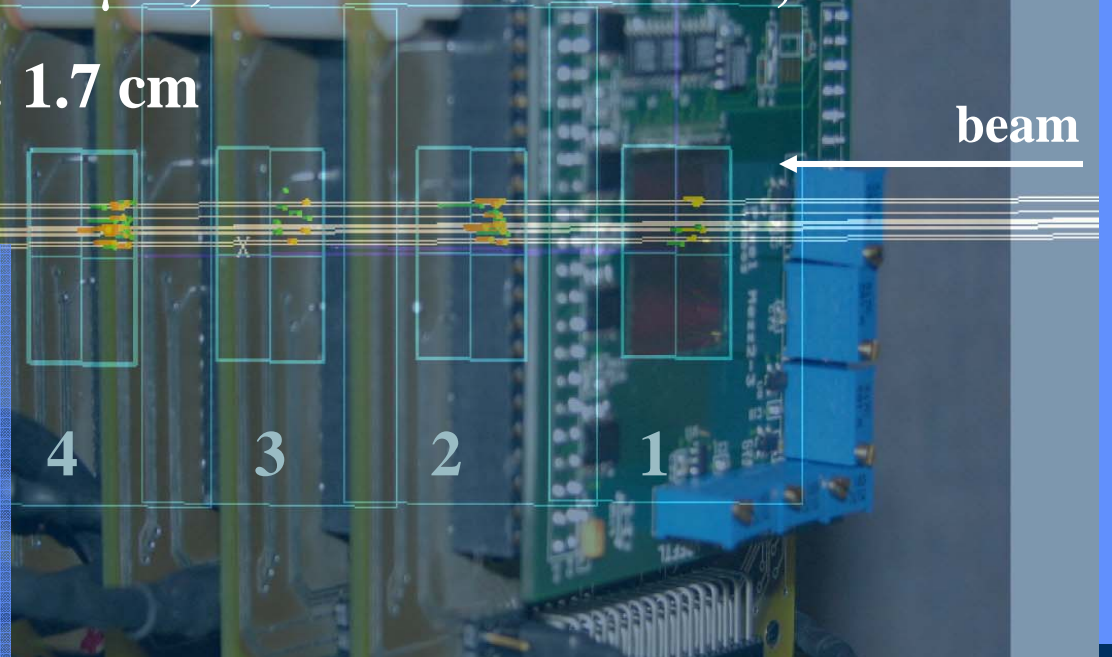

Ladder prototype with 50 μm thin MIMOSA-5 chips

APS
Cable
Carrier

Power on, air cooling 2.0 m/s

IR Camera Image
Air Cooling Test

Heating cable

Thin Chips

The LBNL Thin Pixel Pilot Telescope

Layout: 3 layers of thin Mimosa 5 sensors (17μm pixels) (40μm + 50μm + 50μm) + reference detector;

Sensor spacing: 1.7 cm

beam

- First beam telescope based on thin pixel sensors;
- Prototype for proposed FNAL MBTF telescope;
- System test of multi-M pixel detector in realistic conditions.

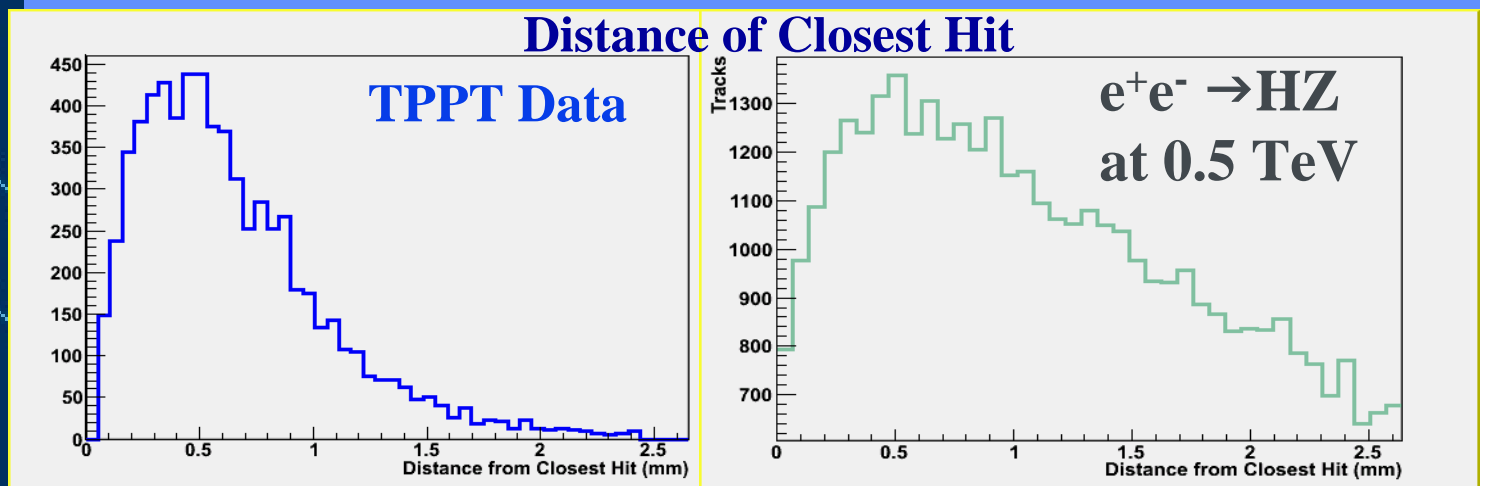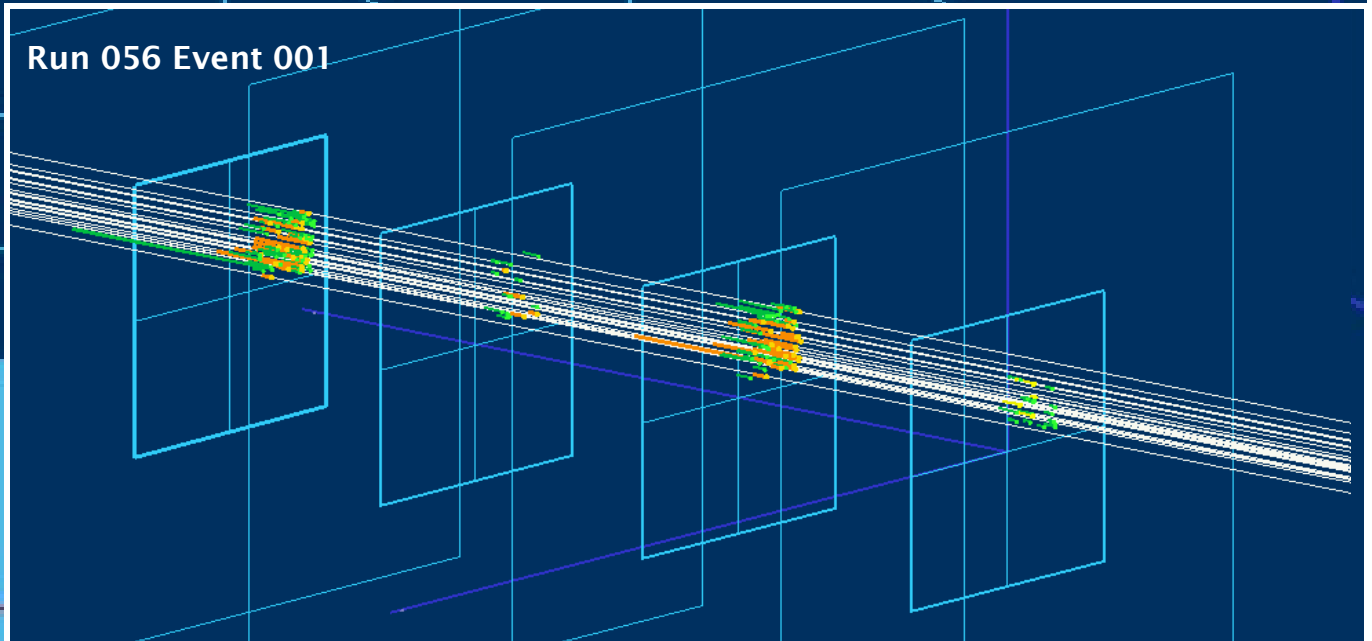**Beam: 1.5 GeV e⁻ from ALS booster at BTS**

Thin Pixel Pilot Telescope

TPPT allows us to perform detailed studies of ILC VTX particle tracking with various, controllable, levels of track density (0.5-5 tracks mm^{-2}) under realistic conditions;

TPPT layout chosen to closely resemble ILC VTX.

Run 056 Event 001

Distance of Closest Hit

TPPT Data

e$^+$e$^-$ →HZ at 0.5 TeV

Thin Pixel Pilot Telescope

Alignment performed using ATLAS optical survey machine and track alignment;

Track Sample	Residual (μm)
2+3 Hits Tracks	9.4
3 Hits Tracks	8.9
High Density	9.5
Low Density	9.2

Extrapolation Resolution on Layer 1: $\sigma = 8.5$ μm agrees with ILC requirements.

$\sigma = 9.4$ μm

TPPT Data

ILC Target Resolution
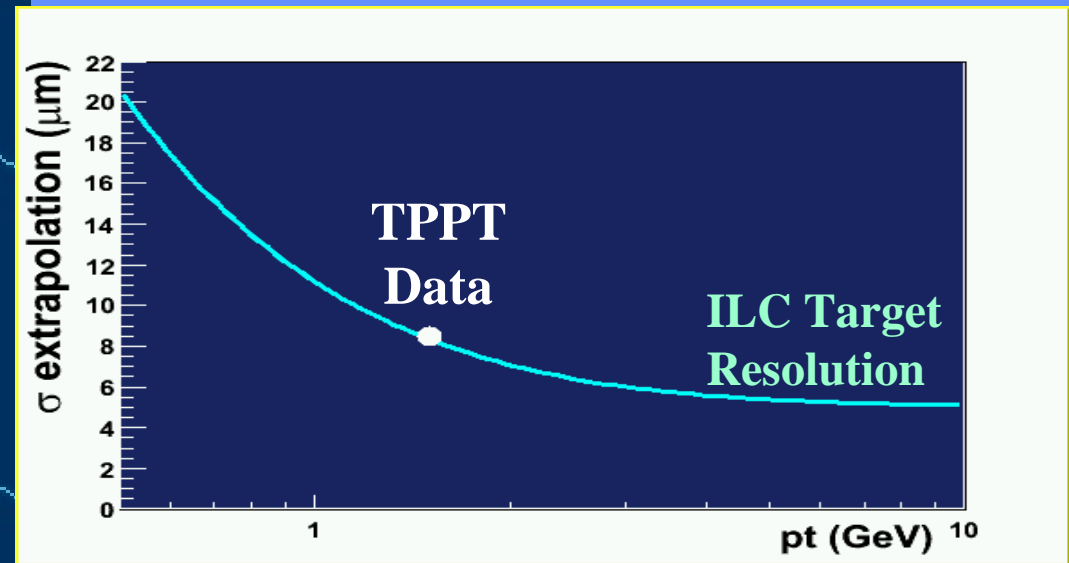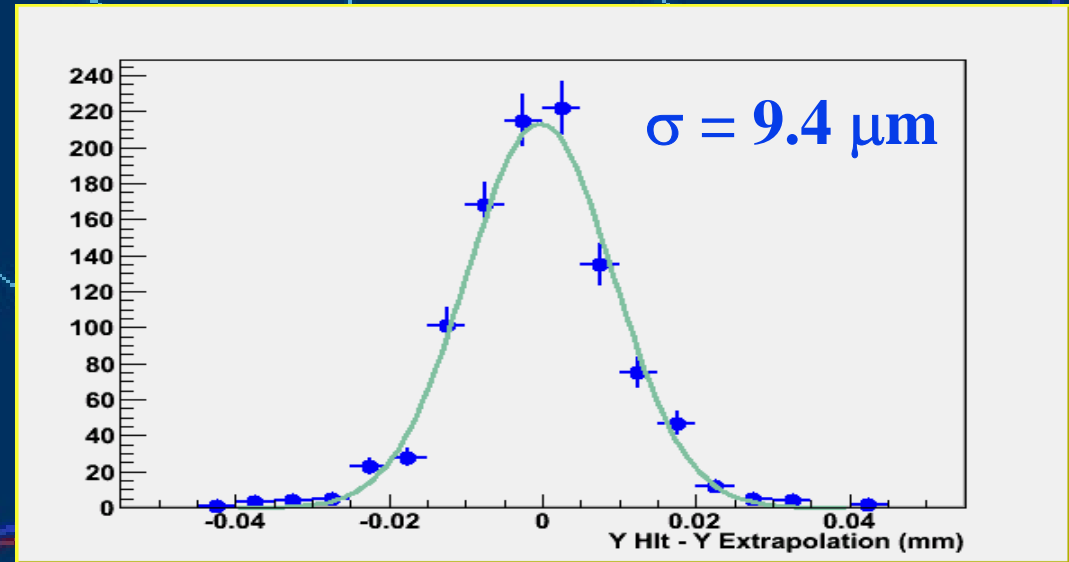
From Sensor Simulation to Physics Analysis

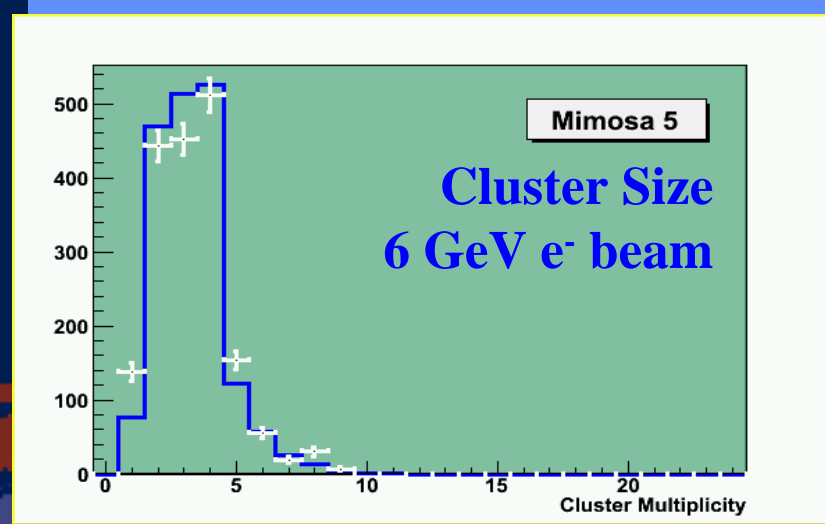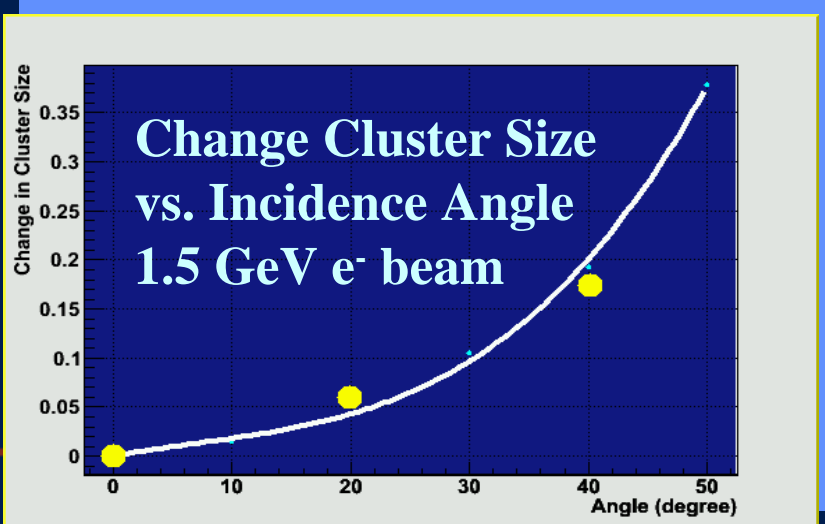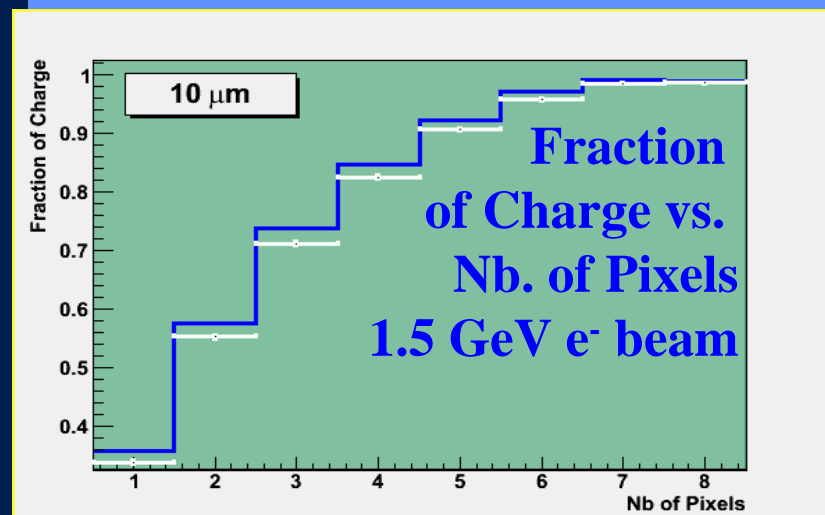Developing full suite of simulation and recontruction from pixel response to analysis of ILC events at highest energy;
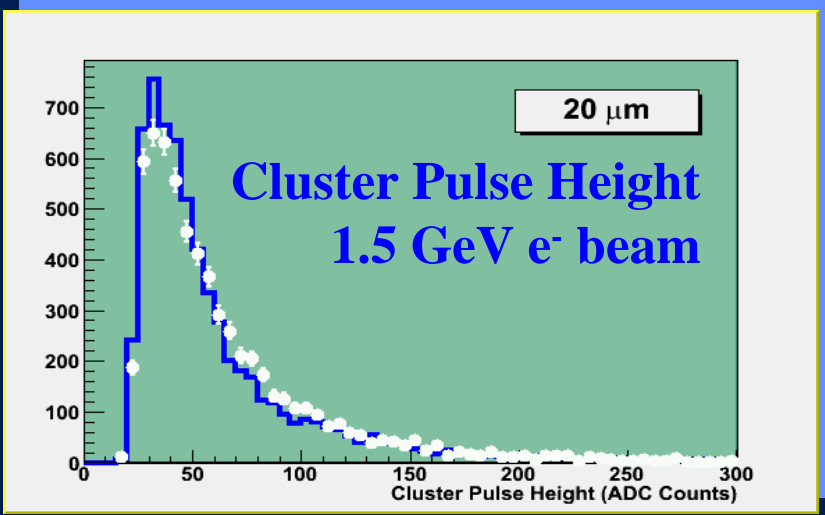
Implemented **sensor simulation** (PixelSim) **&cluster analysis** (PixelAna) in Marlin and interface to LCIO for beam test data (PixelReader)

Marlin Processors to analyze beam test data and validate simulation response, estimate effect of changes in sensors response and detector geometry and obtain realistic digitized simulation of full physics events and overlayed backgrounds;

CDF Vertex Fit and b-tagging ported to Marlin framework, under test;

Jet Flavour Tagging and **Physics Analysis** of Dark Matter-motivated SUSY scenarios with fully simulated and digitized VTX currently in progress: physics benchmarking to provide guidance to sensor R&D.

Simulation Validation

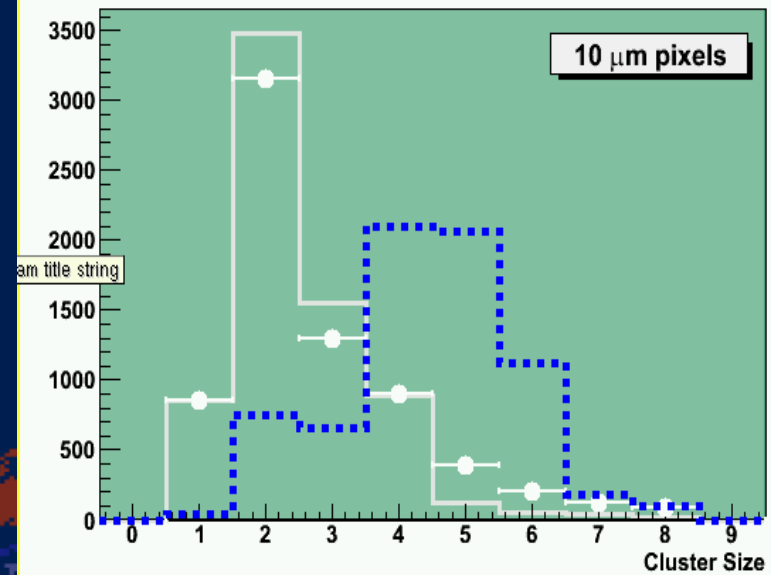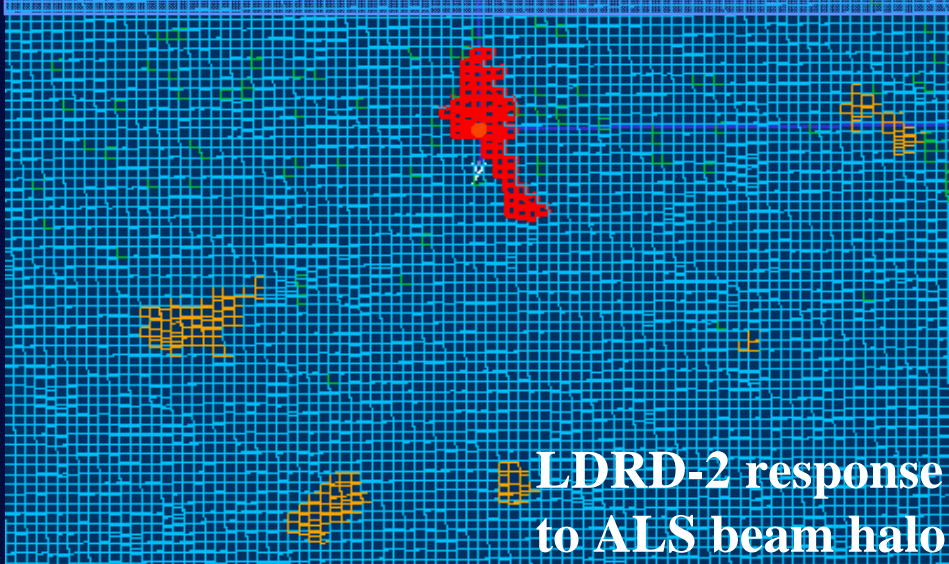# Response to Pair Background

GuineaPig+Mokka Simulation
of 1 BX ILC 0.5 TeV in LDC

Pair e⁻ Hit
Simulated in PixelSim
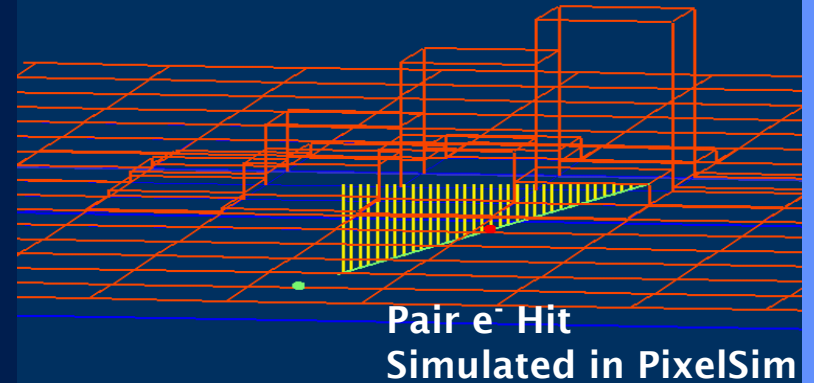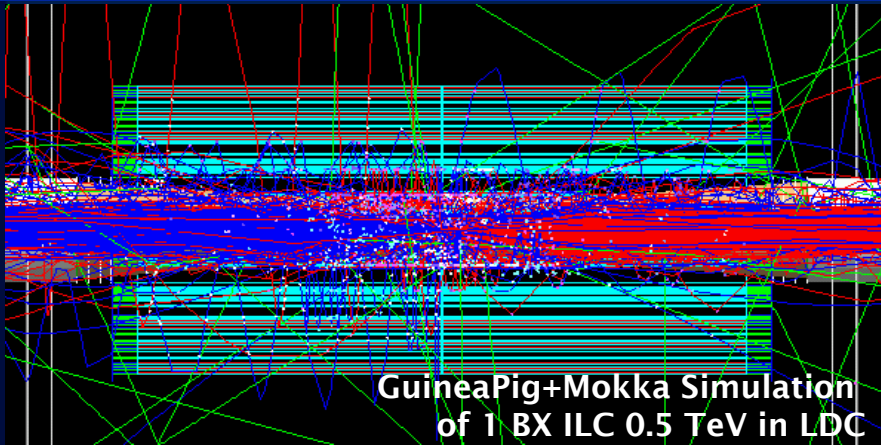
Beam tests using 0.05 - 1.0 GeV e⁻ beams
at LOASI S and ALS to validate simulation.

LDRD-2 response
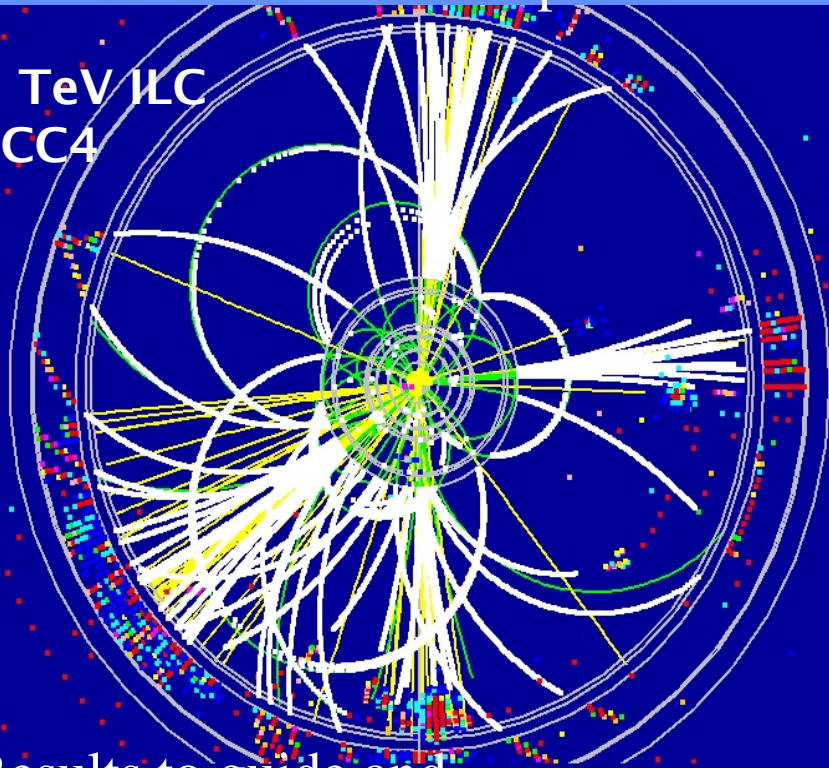to ALS beam halo

10 μm pixels

VTX Physics Studies

Dark Matter-motivated SUSY scenarios important to assess ILC potential
and motivates challenging requirements in terms of detector performance;
Studies on G4 full simulation and reconstruction
for selected benchmark processes:

$$e^+ e^- \rightarrow H^0 A^0 \rightarrow b \bar{b} b \bar{b}$$

**1 TeV ILC
LCC4**

A⁰ Mass Reconstruction

SIMDET Parametric Simulation

G4 + Full MARLIN Reco

Jet Pairs / 1 ab⁻¹

M_{jj} (GeV)

Results to guide and
prioritise sensor R&D, conceptual design and engineered design.
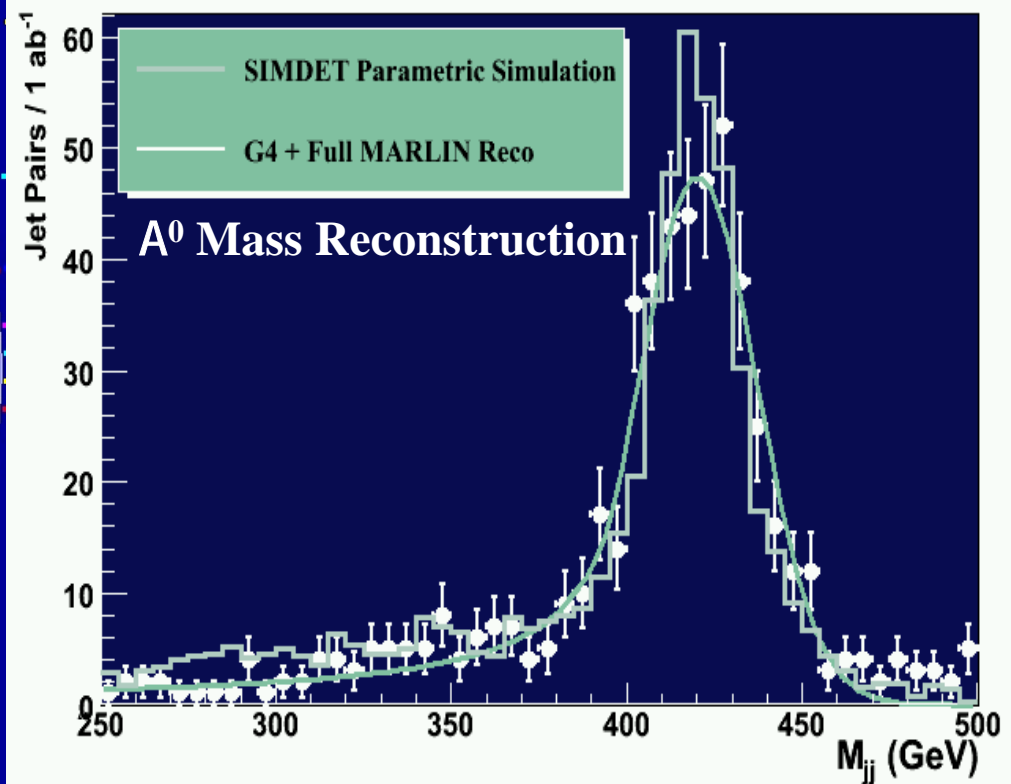
T-966 Beam Test Experiment at Fermilab

Beam Test at FNAL MBTF 120 GeV p beam-line (T-966) (June-July 2007)
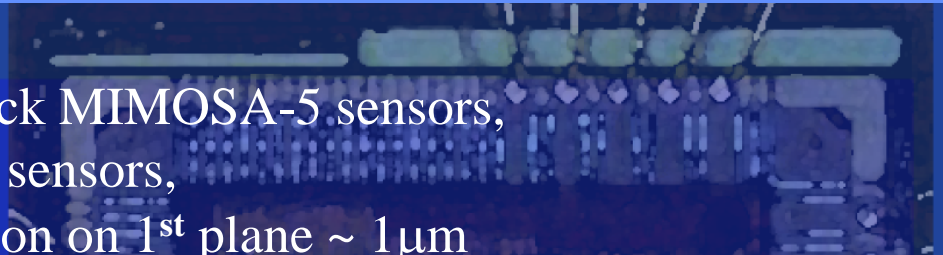(UC Berkeley + LBNL + INFN, Padova + Purdue U. Collaboration)

Plan to deploy two pixel beam telescope:
- TPPT-2 telescope: 4 layers of 50μm thick MIMOSA-5 sensors,
- LDRD telescope: 4 layers of LDRD-2 sensors,

ILC-like geometry, extrapolation resolution on 1st plane ~ 1μm

Study LDRD-1, LDRD-2 and LDRD-SOI sensors:
- single point resolution & sensor efficiency,
- response to inclined tracks,
- tracking capabilities
  in dense environment,
- vertex reconstruction
  accuracy with thin target,

G4 simulation
of 120 GeV p Be
interaction in T-966
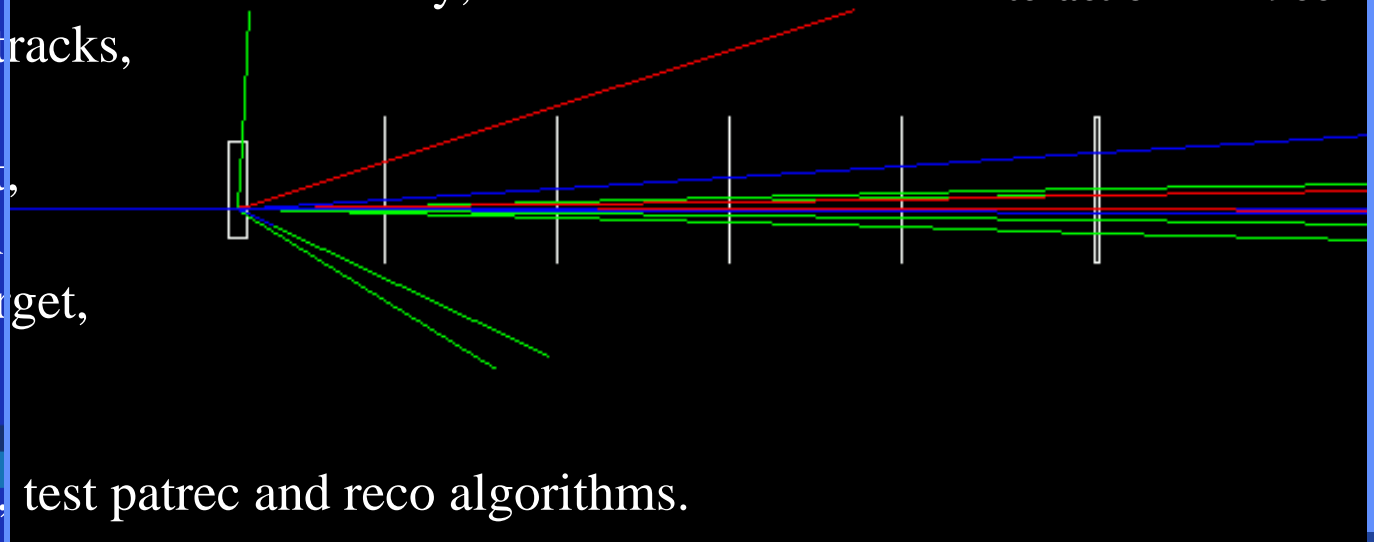
Validate simulation, test patrec and reco algorithms.

Project Outlook

LDRD program to provide basic building blocks for monolithic pixel chip meeting the ILC specifications by end 2007:
(single point resolution, readout speed, power consumption, digitisation)

LCRD project to provide engineered design and prototypes of ladder equipped with back-thinned chips meeting the ILC material budget specs.

T-966 Beam Test first US ILC VTX tracking and vertexing experiment, essential step for detector & system tests, reco sw

Emerging technologies (SOI, triple well CMOS) offer new opportunities to be investigated;

Significant effort to deploy complete suite of simulation, reconstruction and physics tools sharing common lcio interface, validated on beam test data.