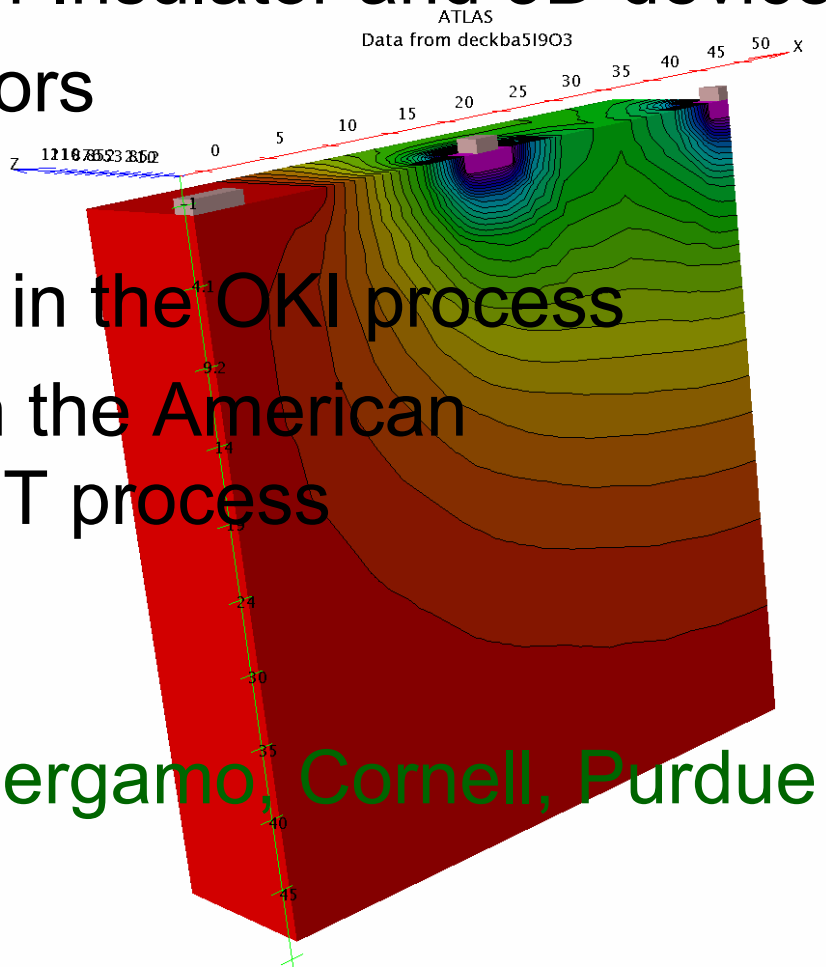
SOI, 3D and Thinned Detectors

Contents:

- Introduction to Silicon-on-Insulator and 3D devices
- Thinned, edgeless sensors
- Laser annealing
- SOI X-ray sensor circuit in the OKI process
- SOI ILC Development in the American Semiconductor FLEXFET process
- 3D Circuit for ILC

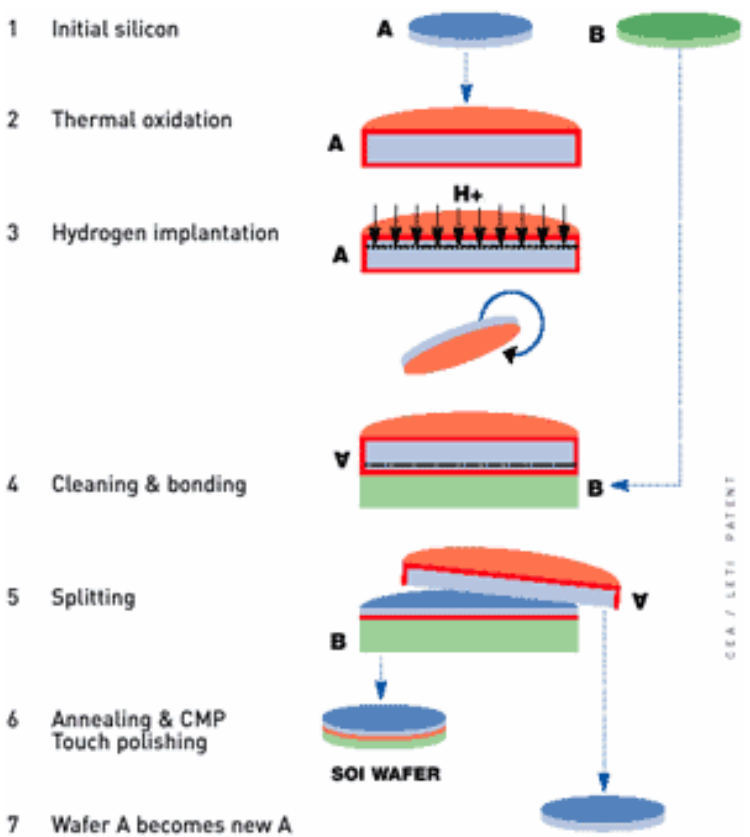


Contributers – Fermilab, Bergamo, Cornell, Purdue

Silicon-on-Insulator

(Soitech illustration)

- SOI is based on a thin active circuit layer on an insulating substrate. Modern technology utilizes ~200 nm of silicon on a “buried” oxide (BOX) which is carried on a “handle” wafer.
- The handle wafer can be high quality, detector grade silicon, which opens the possibility of integration of electronics and fully depleted detectors in a single wafer with very fine pitch and little additional processing.
- Used for high speed, circuits, immune to SEU
- Important for 3D integration

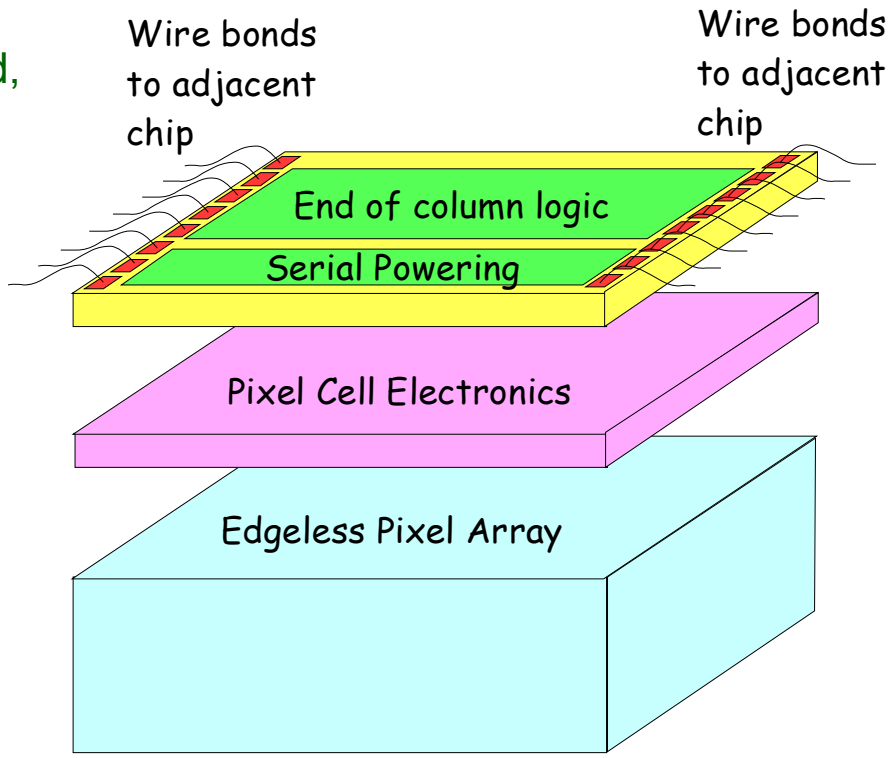


Formation of an SOI wafer

3D Circuits

A 3D chip is comprised of 2 or more layers of semiconductor devices which have been thinned, bonded together, and interconnected to form a "monolithic" circuit. SOI is the favored technology.

- The layers (also called tiers) can be comprised of devices made in different technologies.
- The move to 3D is being driven by industry.
  - Going 3D reduces trace length, Reduces R, L, C
  - Improves speed
  - Reduces interconnect power, crosstalk
  - Reduces chip size
  - Processing for each layer can be optimized
- 3D allows for creative solutions, e.g.
  - Accommodates serial powering
  - Higher functionality/area
  - Thinner assemblies

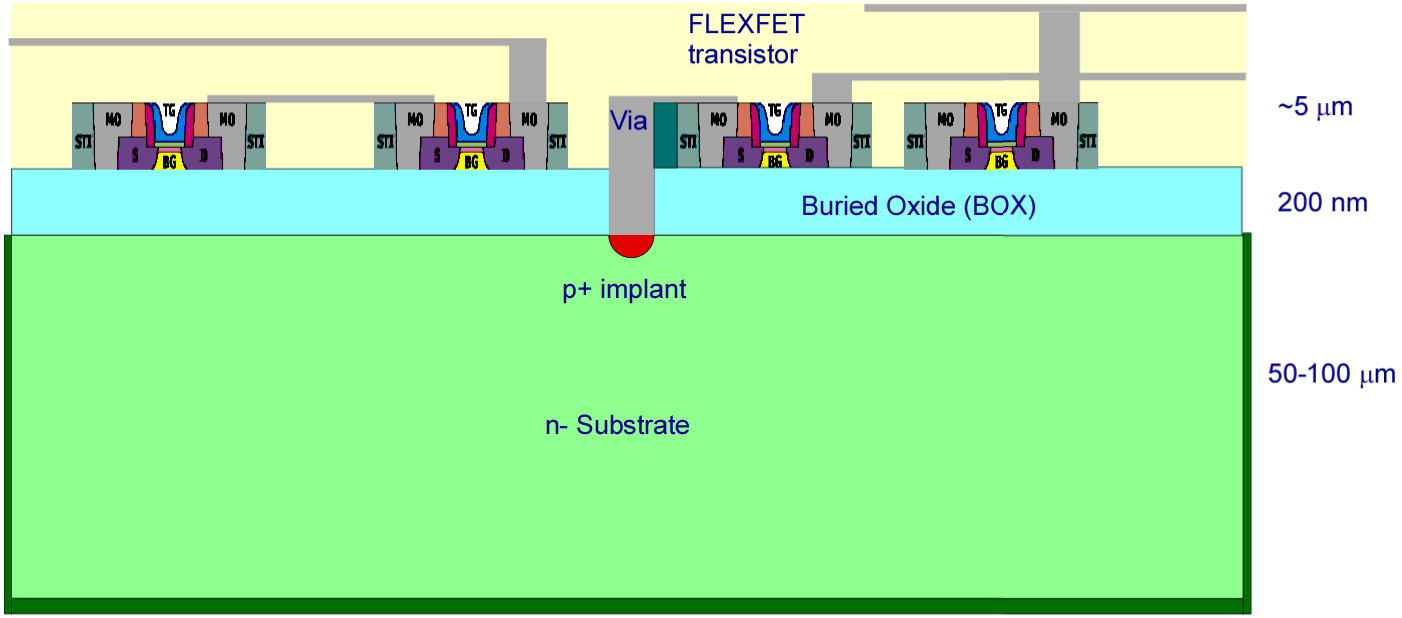


Technology described in R.Yarema talk at CMS/ATLAS sLHC meeting

SOI Concept for HEP

not to scale

Minimal interconnects,
low node capacitance



High resistivity
Silicon wafer,
Thinned to 50-
100 microns

Active edge
processing

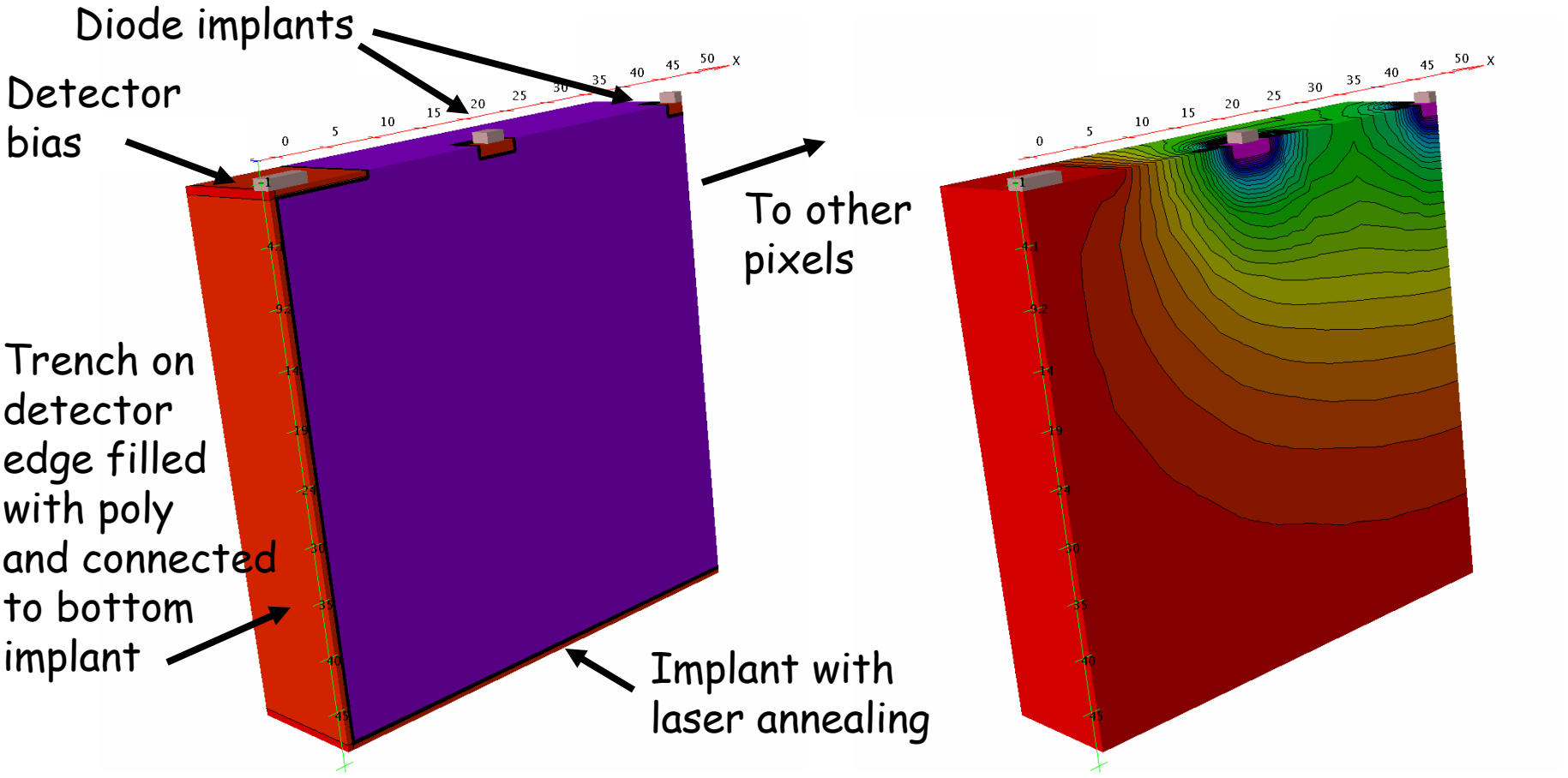
Sensor and circuitry
Can be formed as part
of CMOS processing

Backside implanted after thinning
Before frontside wafer processing
Or laser annealed after processing

Technology "Roadmap"

- Explore commercial processes which include processing of the handle wafer as part of the fabrication process for SOI (OKI, American Semiconductor).
- Understand the available technologies for 3D (MIT-LL, RTI, IZM, Ziptronix…)
- Develop expertise in necessary technologies
  - Wafer thinning
  - Post processing (handing, annealing, dicing…)
  - Pixel physical design (fields, analog/digital coupling …)
- R&D is underway to understand :
  - How to retain good, low leakage current, detector performance through the CMOS topside processing?
  - What is the optimal process for forming the detector diodes?
    - Model charge collection, shielding
  - How does the charge in the BOX due to radiation and potential of the handle wafer affect the operation of the top circuitry?
  - How does topside digital circuitry affect the pixel amplifier?

Edgeless Thinned Detector Concept



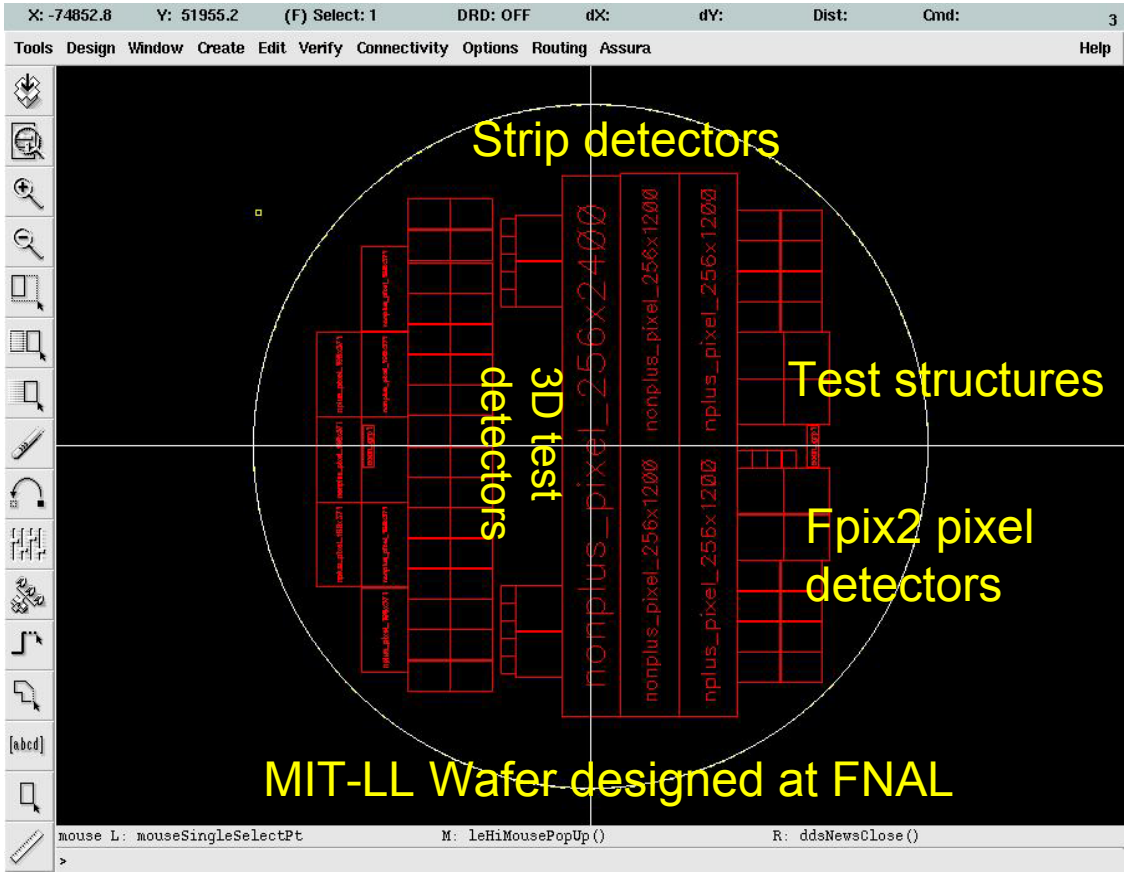
Detector Cross section near one detector edge

Equipotential lines in detector near one detector edge

Thinned Sensor Studies

We are producing a set of thinned, “edgeless” sensors at MIT-LL as a initial test of these concepts

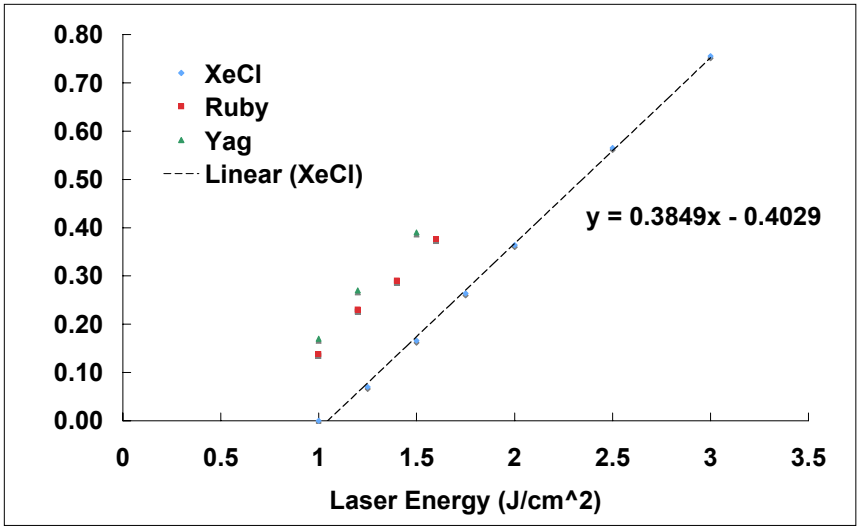
- Producing a set of detectors thinned to 50-100 microns for beam and probe tests.
  - Validate process
- Explore and validate the technologies which provide thinned detectors sensitive to
- the edge
  - Measure the actual dead region in a test beam
- Parts available for prototype vertex structures
- Masks designed at FNAL
  - Test structures
  - Strip detectors (12.5 cm and ~2 cm)
  - FPiX2 pixel detectors
  - Detectors to mate to 3D chip



Laser annealing

Problem: provide backside contact to thinned wafer while keeping topside below ~400 deg C

- Use a raster scanned eximer laser to melt the silicon locally – this activates the implant and repairs the implantation damage by recrystallizing the silicon
- Diffusion time of phosphorus in molten silicon is much less than cooling time therefore we expect ~uniform distribution in melt region

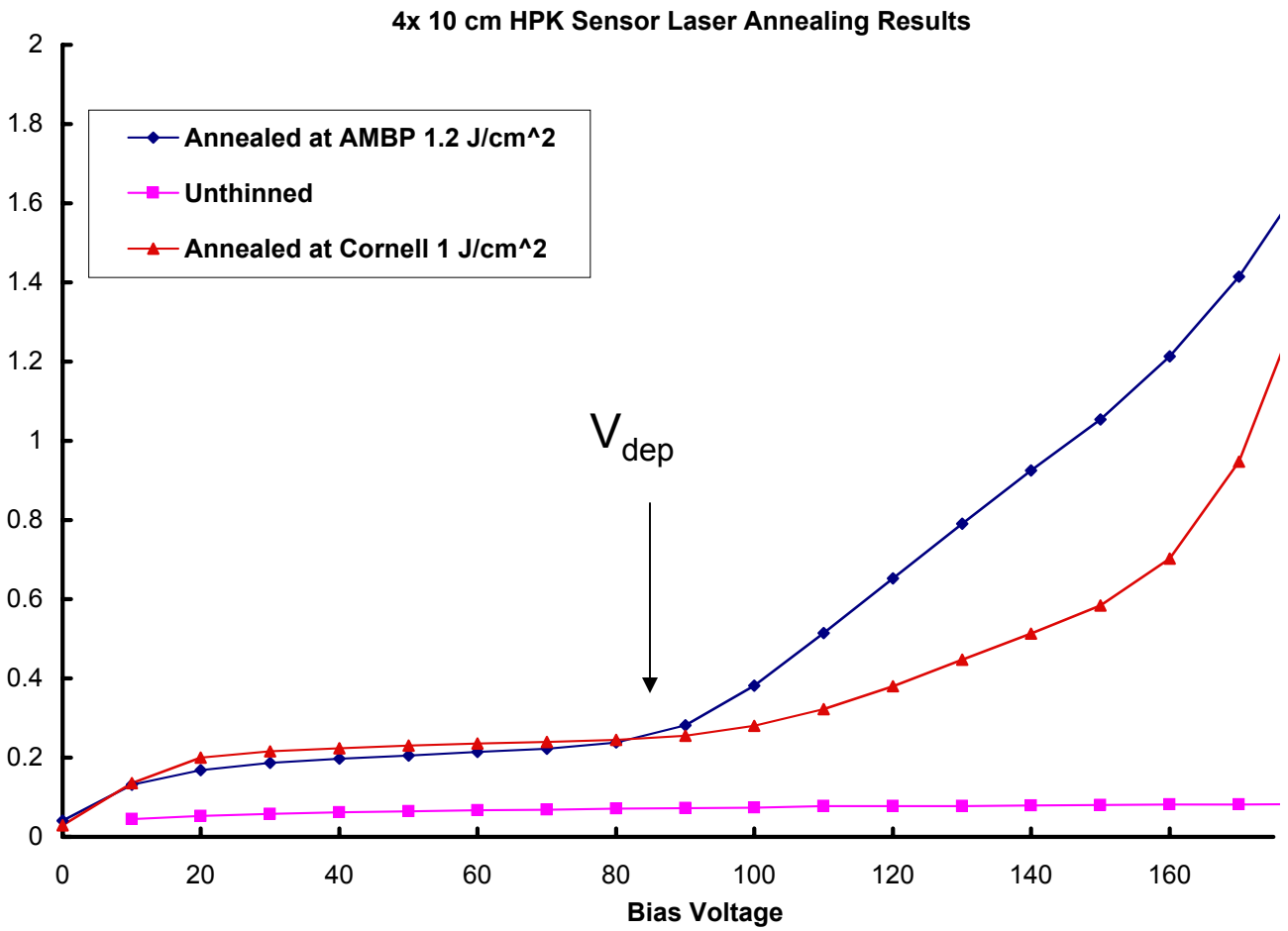


Oak Ridge studies of melt depth vs laser energy

To study and qualify this process we took a sample of Run2b HPK, low leakage 4x10 cm, strip detectors and reprocessed them

- Backgrind by ~50 microns to remove back implant and aluminization, polish
- Re-implant detector using 10 KeV phosphorus at 0.5 and $1.0 \times 10^{15}/cm^2$
- Laser anneal and measure CV and IV characteristics
  - AMBP - 1.2, 1.0, 0.8 J/cm^2, 248 nm laser
  - Cornell - 1.0 J/cm^2

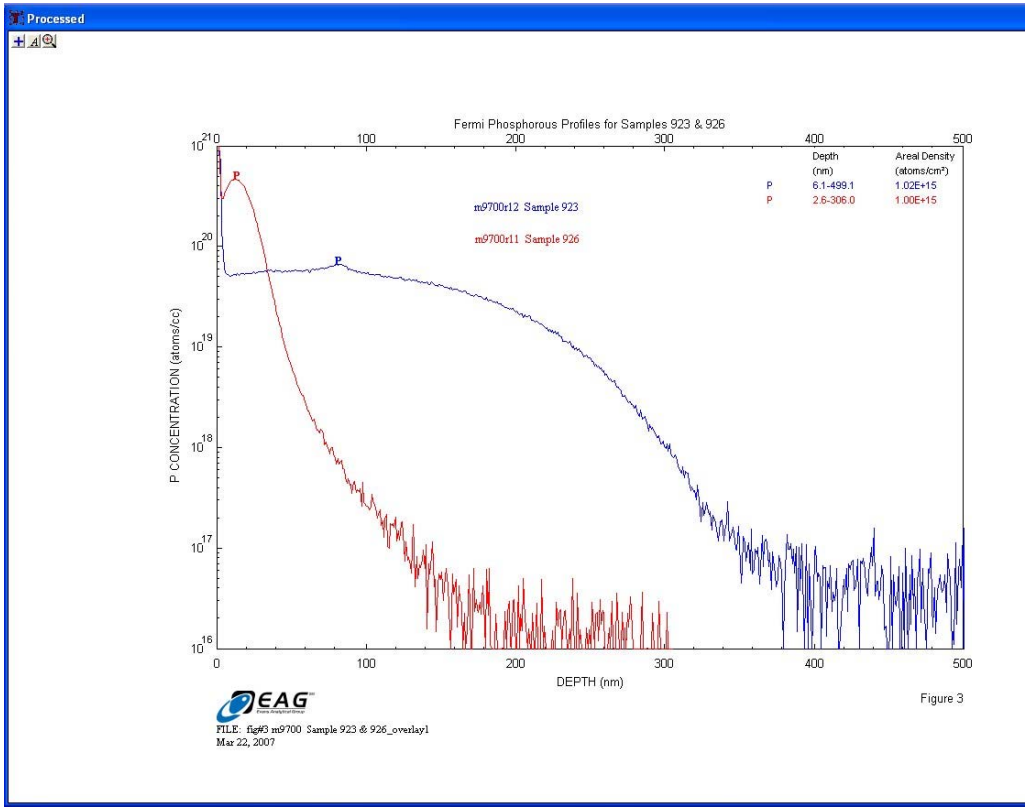
Laser Annealing Results (Cornell)



SIMS Measurements

Secondary Ion Mass Spectroscopy provides implant depth profiles by analysis of ions ejected from the surface upon ion bombardment:

- Two samples, before and after 1.2 J/cm^2 248 nm laser anneal
- Goal was ~>2x10^{19} concentration
- Melt depth ~300 nm



Laser melt depth is close to expectation, phosphorus concentration close to expectation

- We have annealed additional samples with less energy. This should yield better diodes
- Explore leakage current as a function of dose.

Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at two different foundries :OKI in Japan, and American Semiconductor Inc.(ASI)/Cypress in US . The two processes have different characteristics as seen below

Process	**0.15μm Fully-Depleted SOI CMOS process,** **1 Poly, 5 Metal layers (OKI Electric Industry Co. Ltd.).**
SOI wafer	**Wafer Diameter: 150 mmϕ,** **Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick** **Buried Oxide: 200 nm thick** **Handle wafer: Cz、>1k Ω-cm (*No type assignment)*, 650 μm thick (SOITEC)**
Backside	**Thinned to 350 μm, no contact processing, plated with Al (200 nm).**

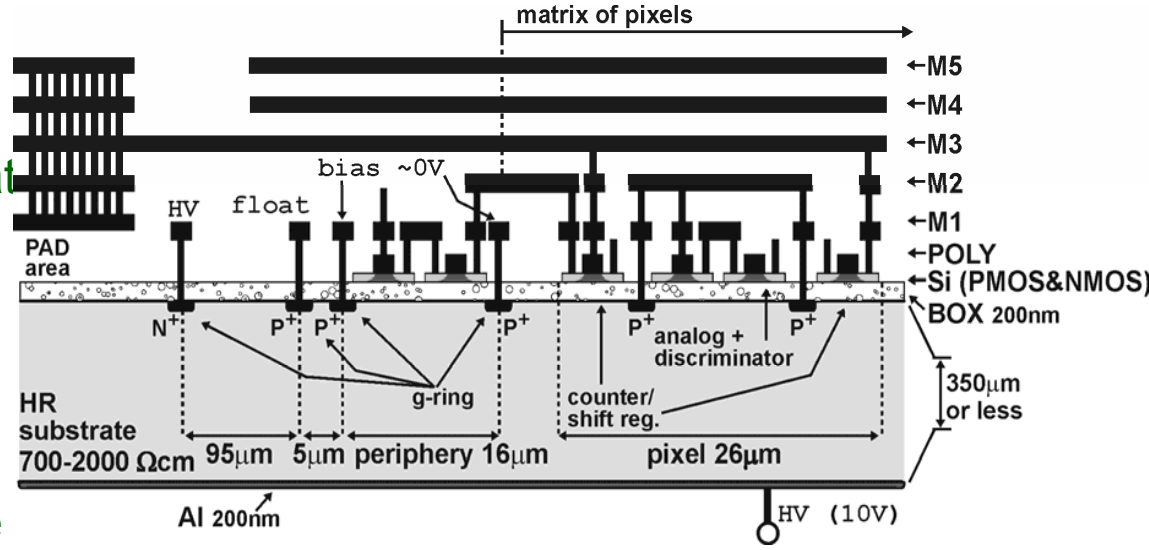
OKI Process

Process	**0.18μm partially-Depleted dual gate SOI CMOS process,** **Dual gate transistor (Flexfet),** **No poly, 5 metal** **(American Semicondutor / Cypress Semiconductor.)**
SOI wafer	**Wafer Diameter: 200 mmϕ,** **Handle wafer: FZ>1k Ω-cm (*n type)***
Backside	**Thinned to 50-100 μm, polished, laser annealed and plated with Al.**

ASI Process

"Mambo"
SOI X-Ray Chip

- Fermilab has submitted a design to a KEK sponsored 0.15 μm SOI multiproject run at OKI which incorporates diode formation by implantation through the BOX. The chip incorporates a 64 x 64 26 micron pitch 12 bit counter array for a high dynamic range x-ray or electron microscope imaging.
- Max 13 μm implant pitch is determined by the "back gate" effect where the topside transistors thresholds are shifted by handle potential
- Should come to FNAL this month.

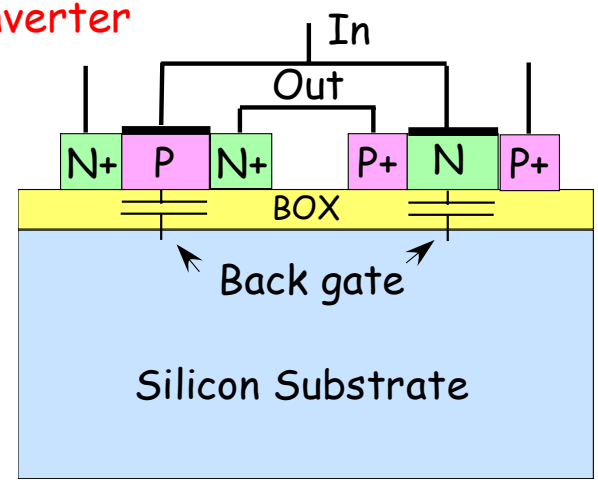


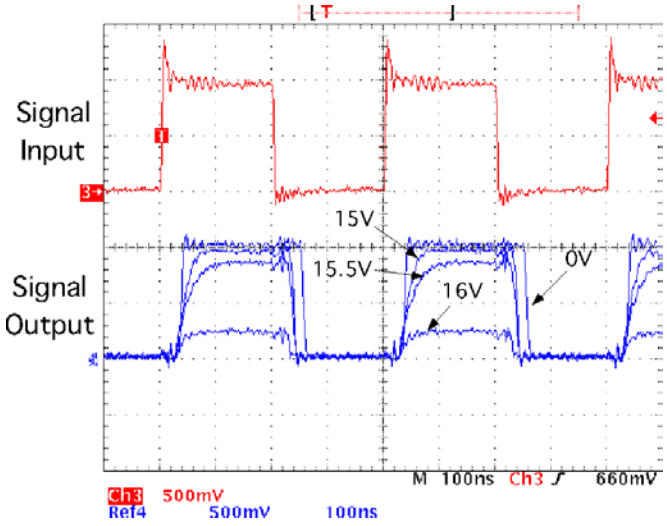
Counting pixel detector plus readout circuit

- Maximum counting rate ~ 1 MHz.
- Reconfigurable counter/shift register
- 12 bit dynamic range
- Limited peripheral circuitry
- Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness

Back gate Effect

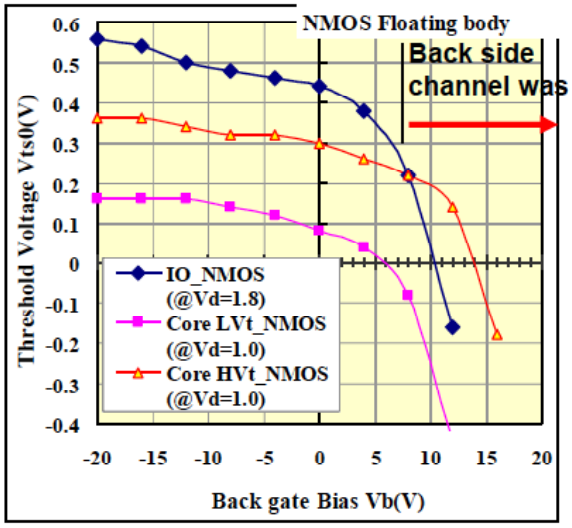
Inverter



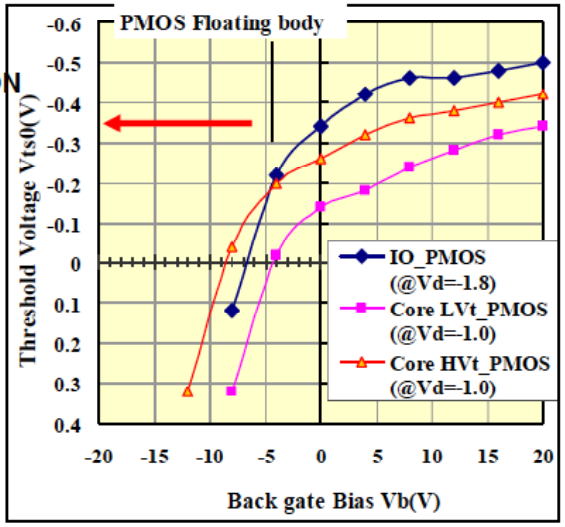


Signal disappears at Vb~16V

NMOS transistor



PMOS transistor



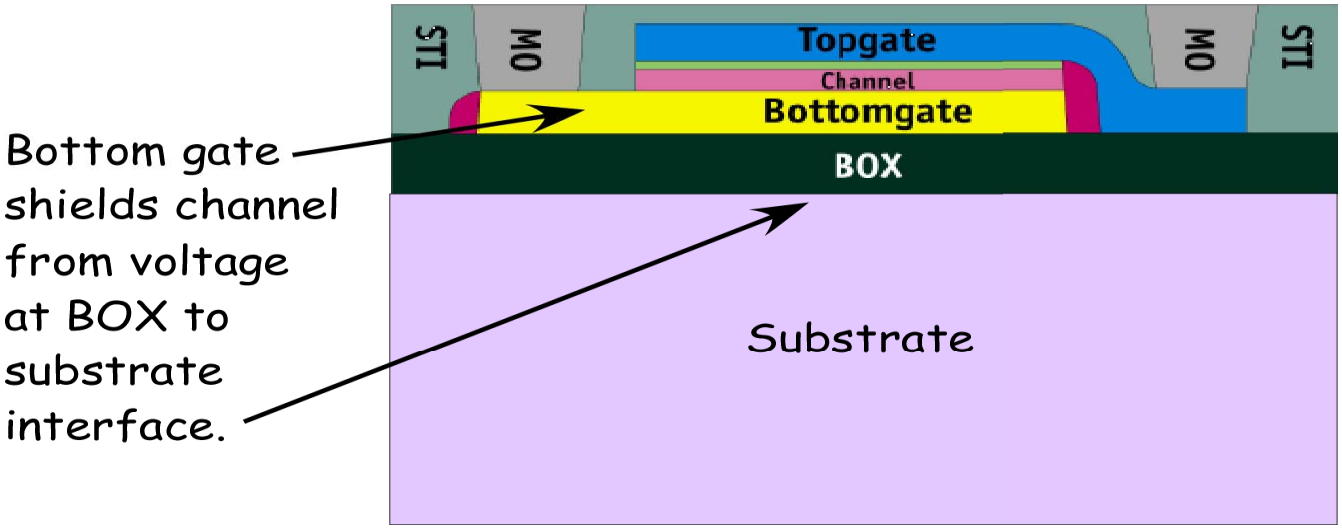
Substrate voltage acts as a back gate bias and changes the transistor threshold - like another gate

- Requires minimum ~15 micron diode spacing to control surface potential

(from Y. Arai (KEK))

American Semiconductor FLEXFET Process

- ASI process based on dual gate transistor called a Flexfet.
- Flexfet has a top and bottom gate.
- Bottom gate shields the transistor channel from charge build up in the BOX caused by radiation.
- Bottom gate also shields the transistor channel from voltage on the substrate and thus *removes the back gate voltage problem*.
- The process can include a “pinning layer” which can be used to shield the analog pixel from digital activity

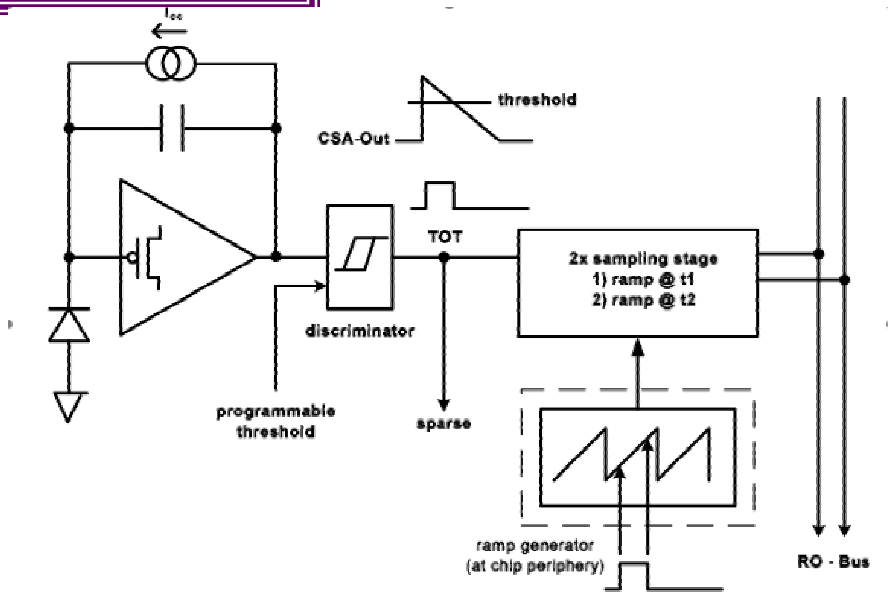


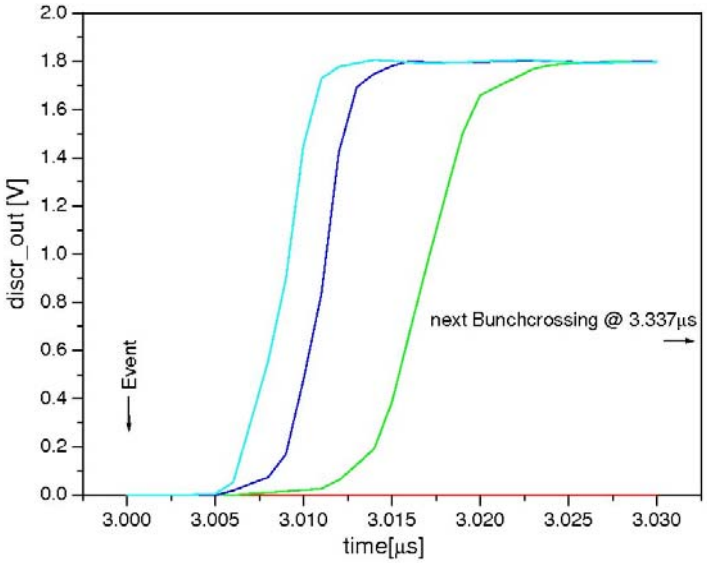
Pixel Design in ASI 0.18μm

As part of a phase I SBIR with ASI FNAL designed a demonstration SOI Pixel cell

- Voltage ramp for time marker
- ~20 micron analog pixel
  - Folded cascode amp
  - Current feedback
  - Discriminator
  - Two time ramp sampling stages
- Sample 1 - crossing time
- Sample 2 - time over threshold for analog pulse height information
- Additional 3-5 bit counter for coarse time stamp
- Provides single bunch resolution

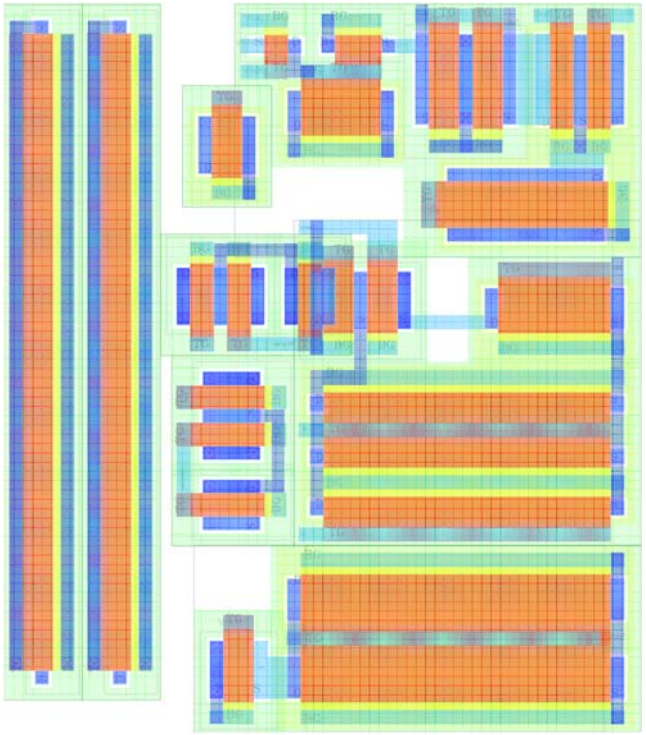
This technique can be tested with the 3D chip

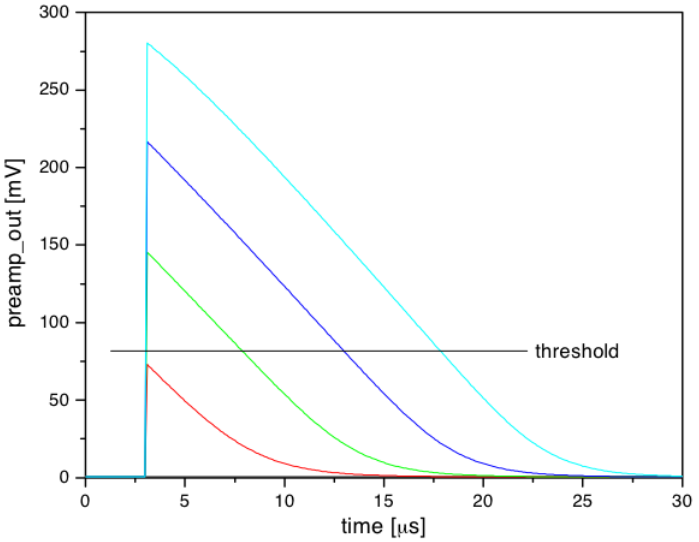


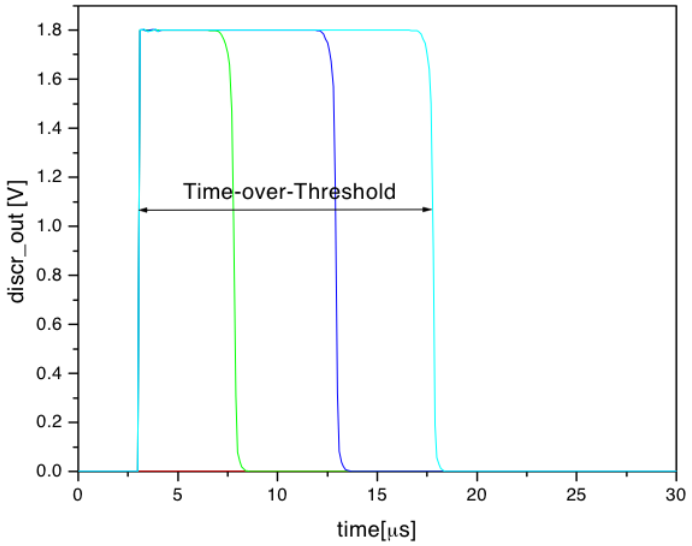


ASI Pixel Simulations

- Analog section layout ~19 x 22 microns
- Simulation of preamp/discriminator system for time over threshold

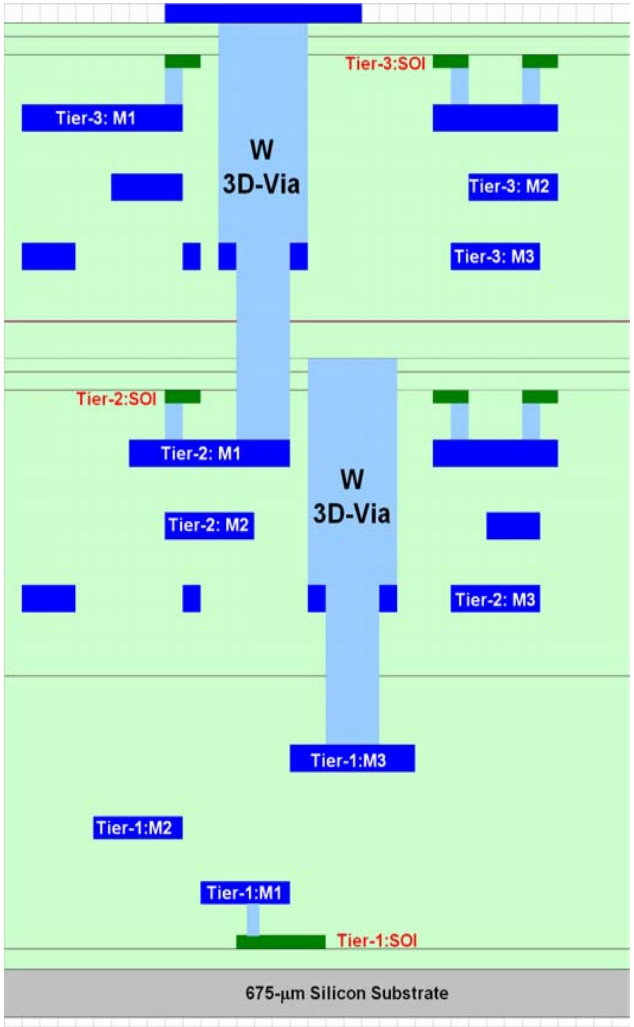






FNAL 3D Chip

- Fermilab has contributed an ILC readout chip design to MIT-LL 0.18 micron three tier SOI 3D multiproject
- ~2.5 mm x 2.5 mm chip, 64x64 20 micron pixels
- Does not include sensor integration
- Design includes amp/disc, time stamp, pixel control, token passing -
  - Store analog and digital time stamps in the hit pixel cell.
  - Store double correlated sample in pixel
- Low node capacitance allows low current front end design
- Due back mid-August



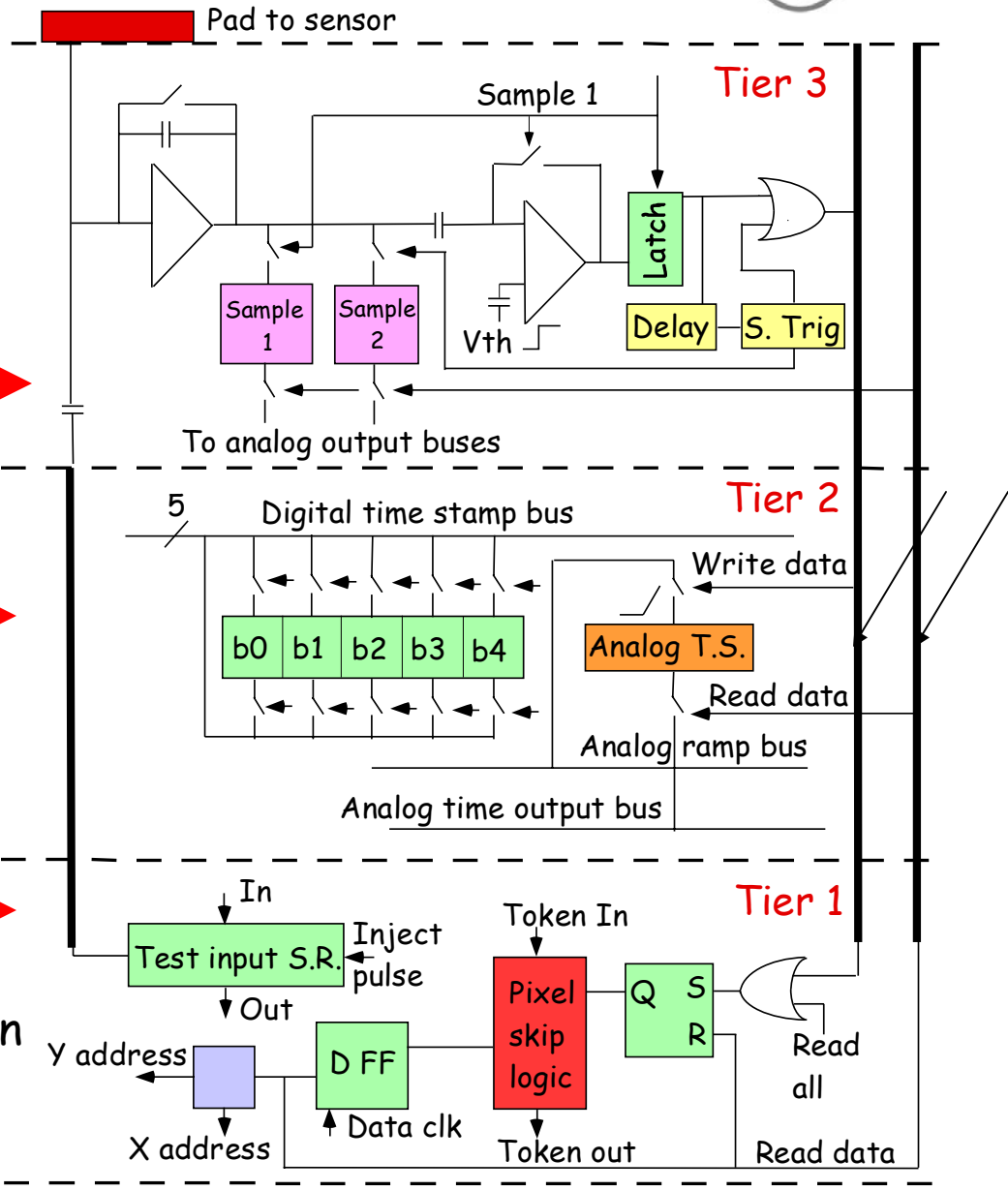
3-Tier Chip

- Correlated double sample
- Noise ~ 35 e-
- Adjustable disc. threshold
- Few hundred nA/pixel
- Most bias currents (times) adjustable.
- Analog and 5 bit digital time stamps – measure analog time resolution
- Sparse readout
- Individual kill/inject
- 3 vias / pixel

Tier 3 analog

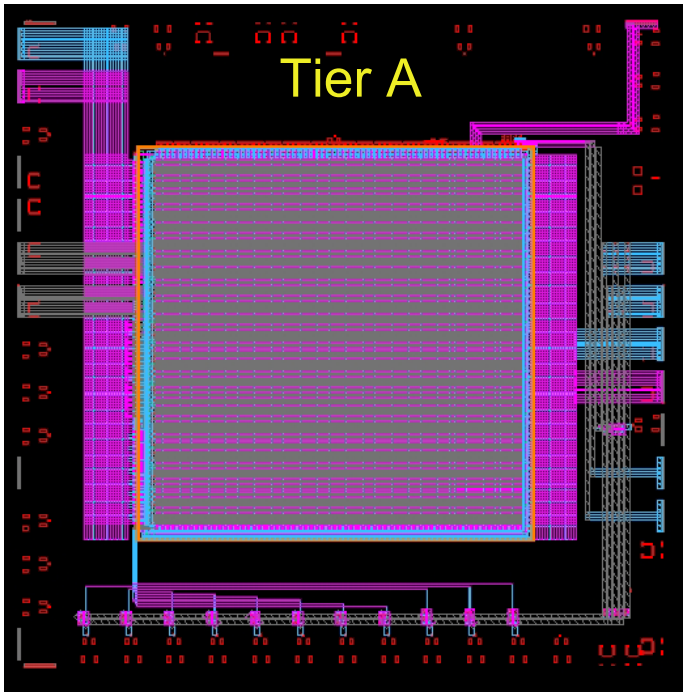
Tier 2 Time Stamp

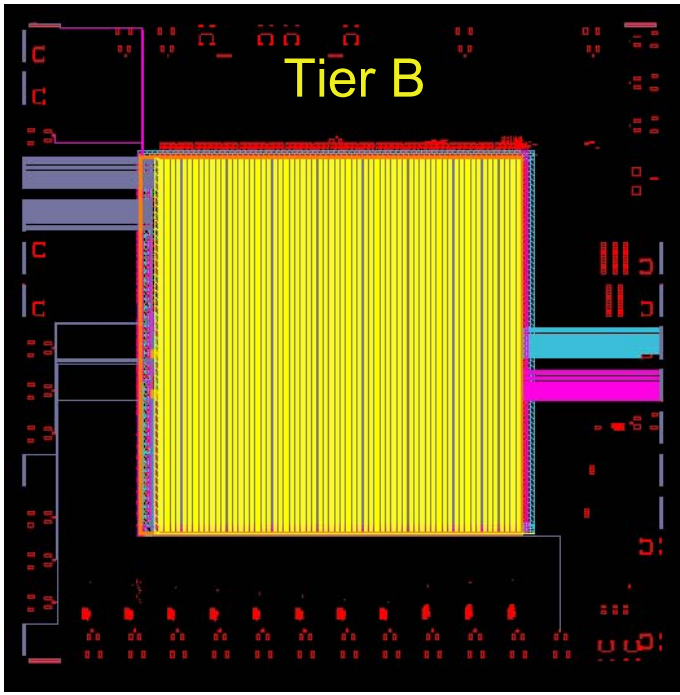
Tier 1 Data sparsification

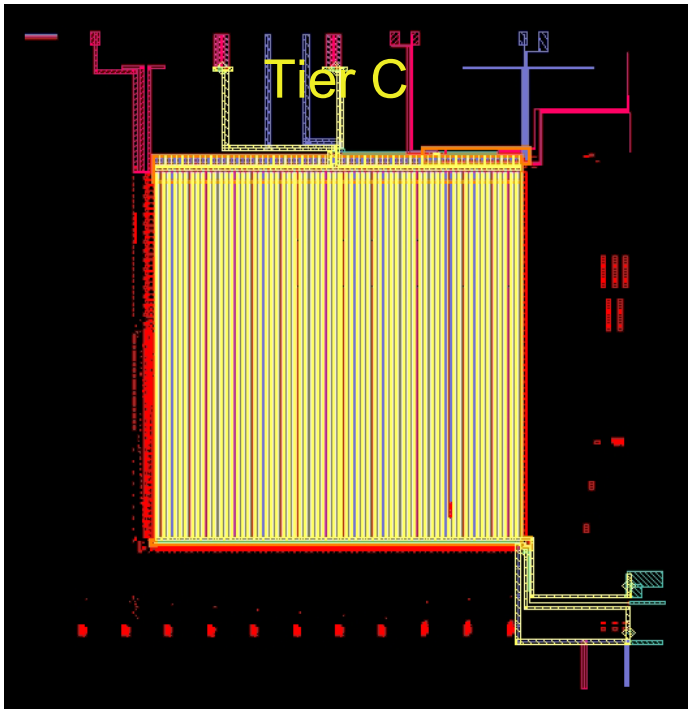


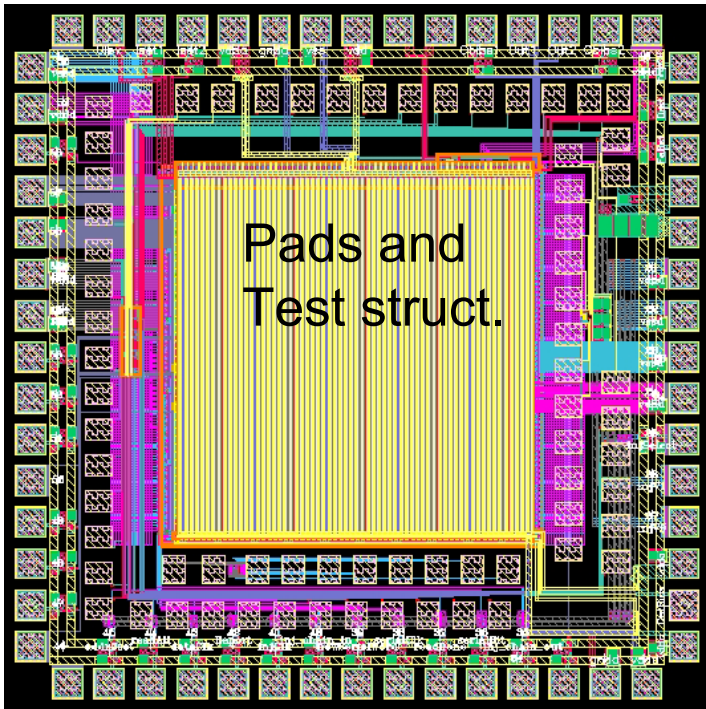
Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff

Completed Design









SOI/3D Advantages

- Advantages of SOI
  - High resistivity substrate available for fully depleted diodes - large signal, controlled charge spreading
  - No limitation on PMOS transistor usage as in CMOS MAPs
    - Full low power CMOS, integration of digital and analog in pixel
    - No parasitic charge collection
  - Sense nodes can have very low capacitance – crucial for low power signal/noise
  - SOI Radiation hard to >1 Mrad, low SEU sensitivity
  - Can be made “edgeless”
  - No bump bonds
  - 100% diode fill factor
- In addition 3D
  - enables mixtures of technologies
  - separate optimization of layers
  - higher density