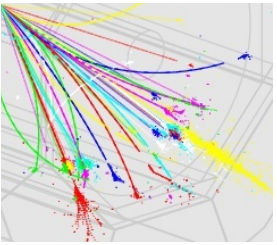

The MAPS ECAL
Status and prospects

Fermilab 10/Apr/2007

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Imperial College London
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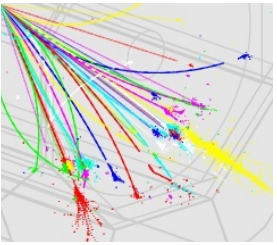
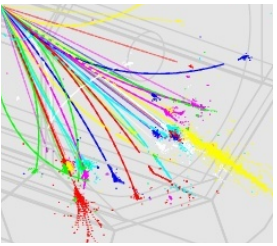
Rutherford Appleton Laboratory



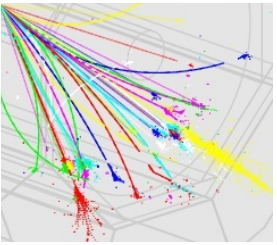
Overview

- Introduction
- Status
  - Sensor Design
  - Sensor Simulation
  - DAQ/Testing
  - Detector Simulations
- Next steps



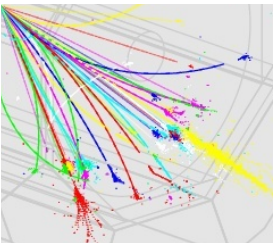
Introduction

- This is done within the context of CALICE
- Not for a particular detector concept
- Development of an alternative readout sensor for a SiW based ECAL
- "Swap-In" Solution leaving mechanical structure untouched
- Using MAPS with high granularity and digital readout
  - Should help Particle Flow Algorithms
  - But it will be a Tera-Pixel Calorimeter...

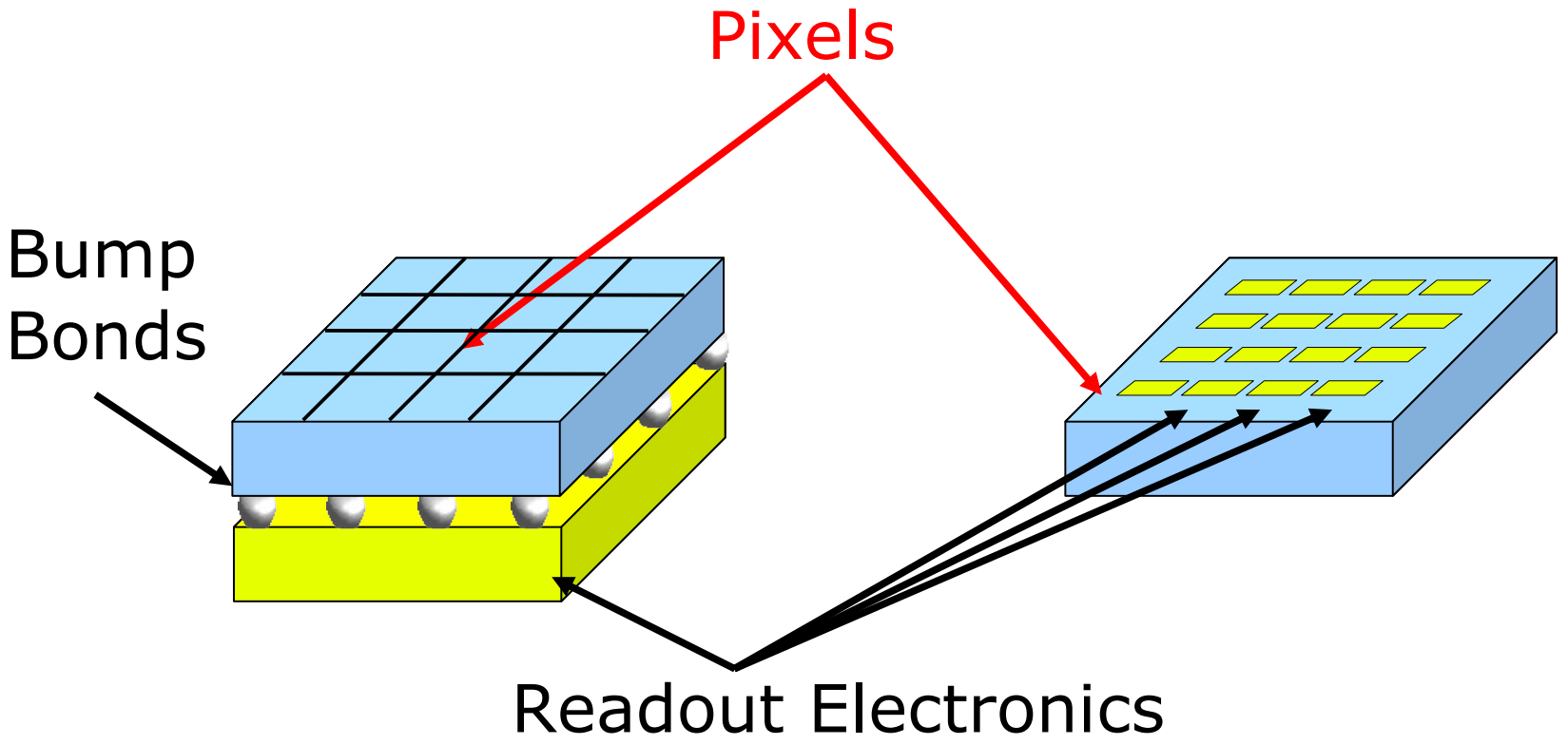


What are MAPS ?

- **M**onolithic **A**ctive **P**ixel **S**ensors
- Integration of Sensor and Readout Electronics
- Manufactured in Standard CMOS process
- Collects charge mainly by diffusion
- Development started in the mid-nineties, now a mature technology

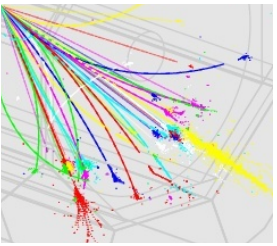


Hybrid Pixels and MAPS

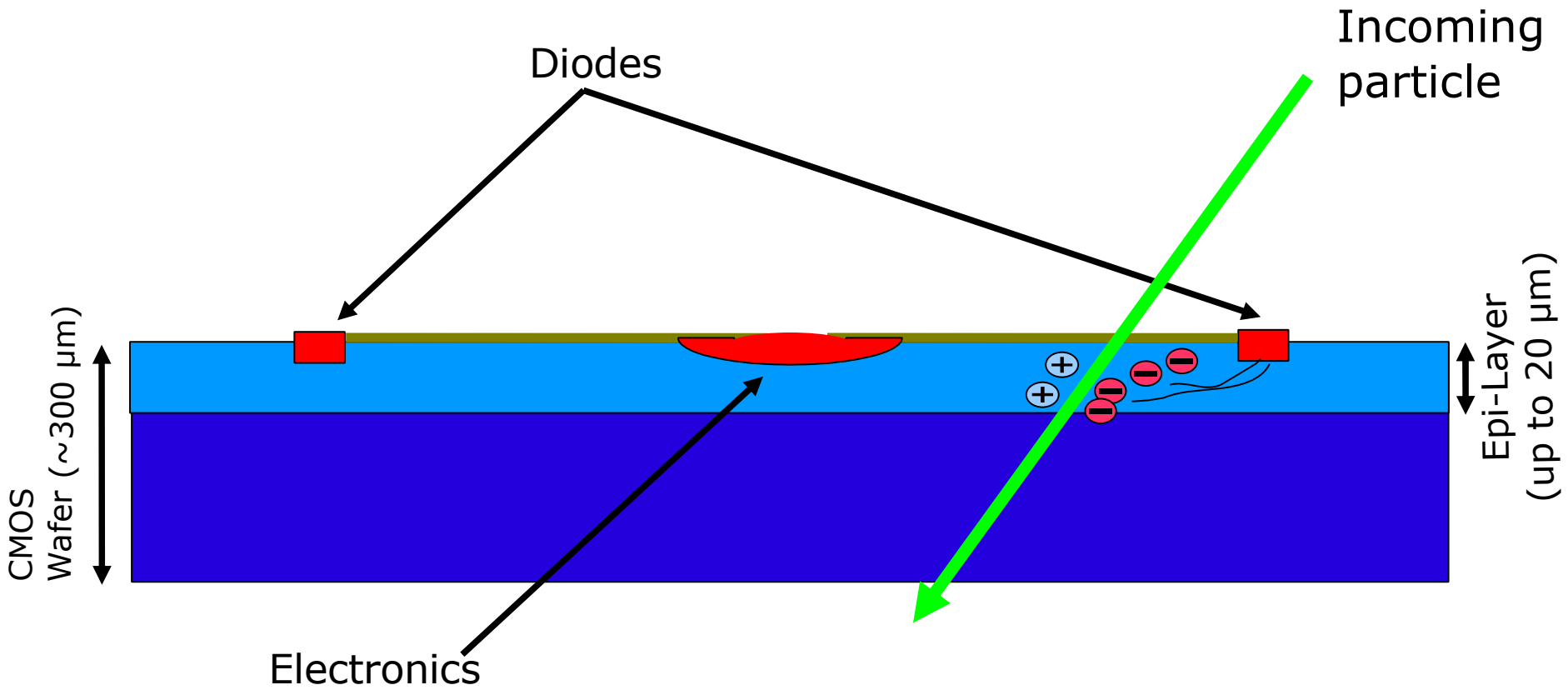


LHC-style Hybrid Pixel sensor

MAPS

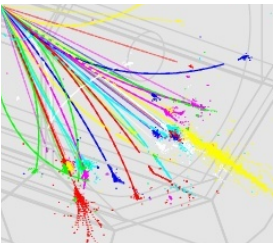


MAPS in Detail



MAPS architecture:

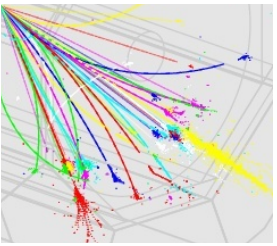
- Sensor and the electronics are integrated in one wafer
- Charge Collection mainly in epi-layer
- Charge collected mostly due to diffusion



The ECAL MAPS

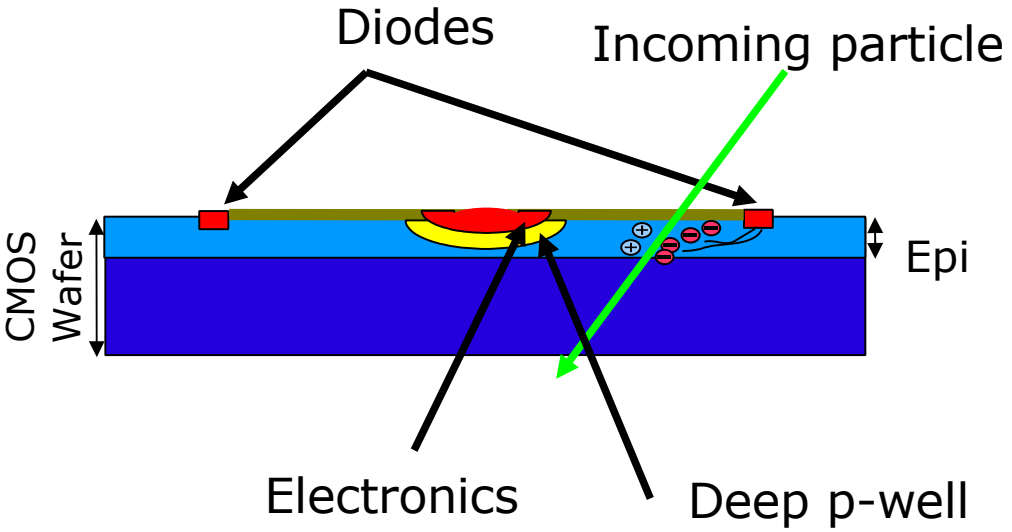
For the MAPS ECAL a specific MAPS was designed:

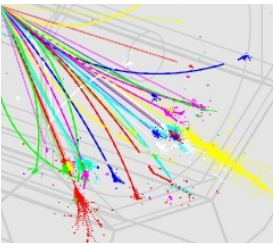
- Pixel Size (50 x 50 µm)
- Binary Readout (1 bit ADC realized as Comparator)
- 4 Diodes for Charge Collection
- Time Stamping with 13 bits (8192 bunches)
- Hit buffering for entire bunch train
- Capability to mask individual pixels
- Threshold adjustment for each pixel



A new process technology

- Simulation showed, that the electronics n-wells absorb a lot of charge (affects the signal)
- We isolated the n-well with a “deep p-well” implant (3 µm thick)
- Standard for deep n-well (“triple well”)
- Novel *INMAPS* process used for the ECAL MAPS



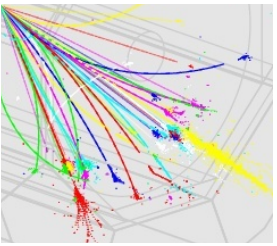


Sensor Electronics

- Two types of pixel readout
- Shaper & Sample

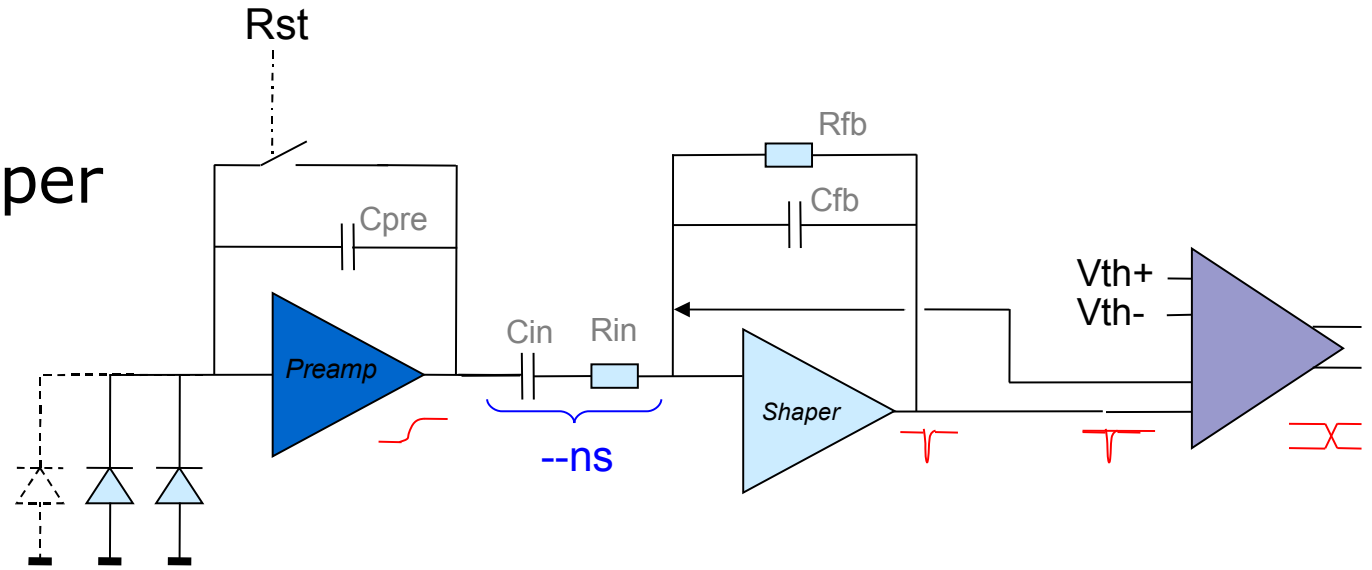
	Pre-Shaper	***Pre-Sampler***
Deadtime	Varies with Signal	Constant
Reset	no reset	Self-resetting
Diode mode	Current	Voltage

- Deadtime (~600 ns/ 450 ns)
- Simulation shows similar noise characteristics
- Both share the Comparator design and everything downstream
- Having two front-end architectures allows us to explore several ideas at once

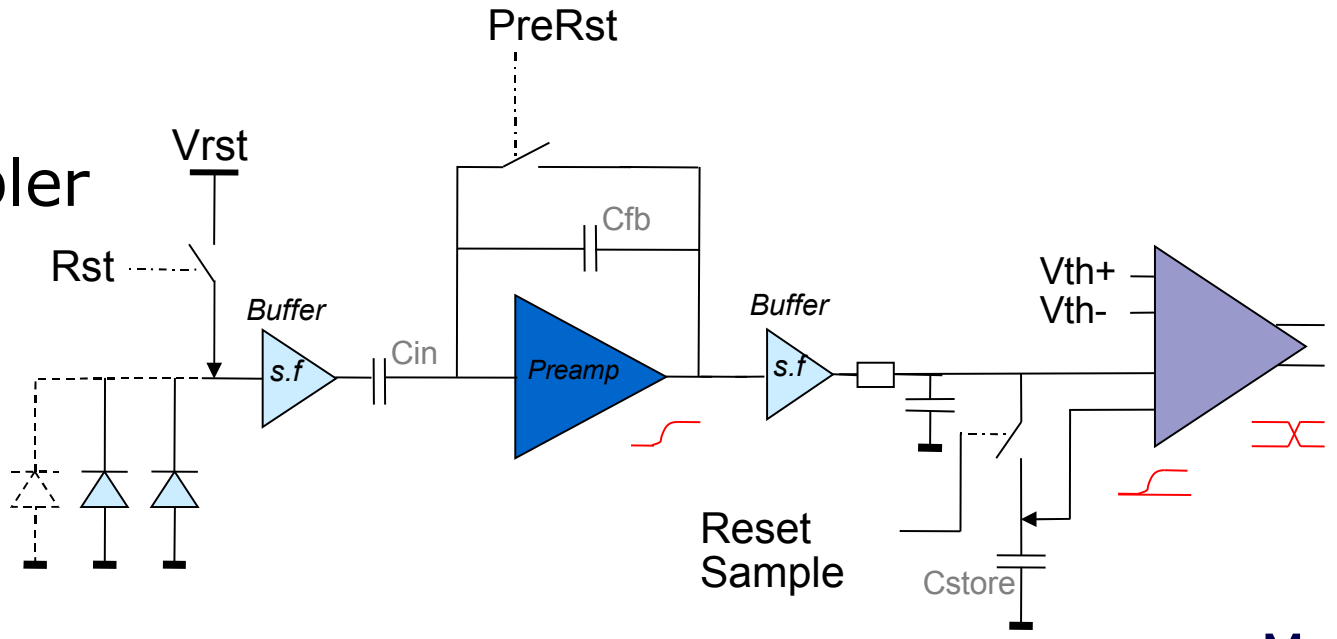


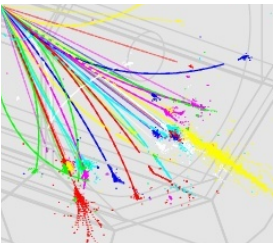
The two pixels

Pre-Shaper



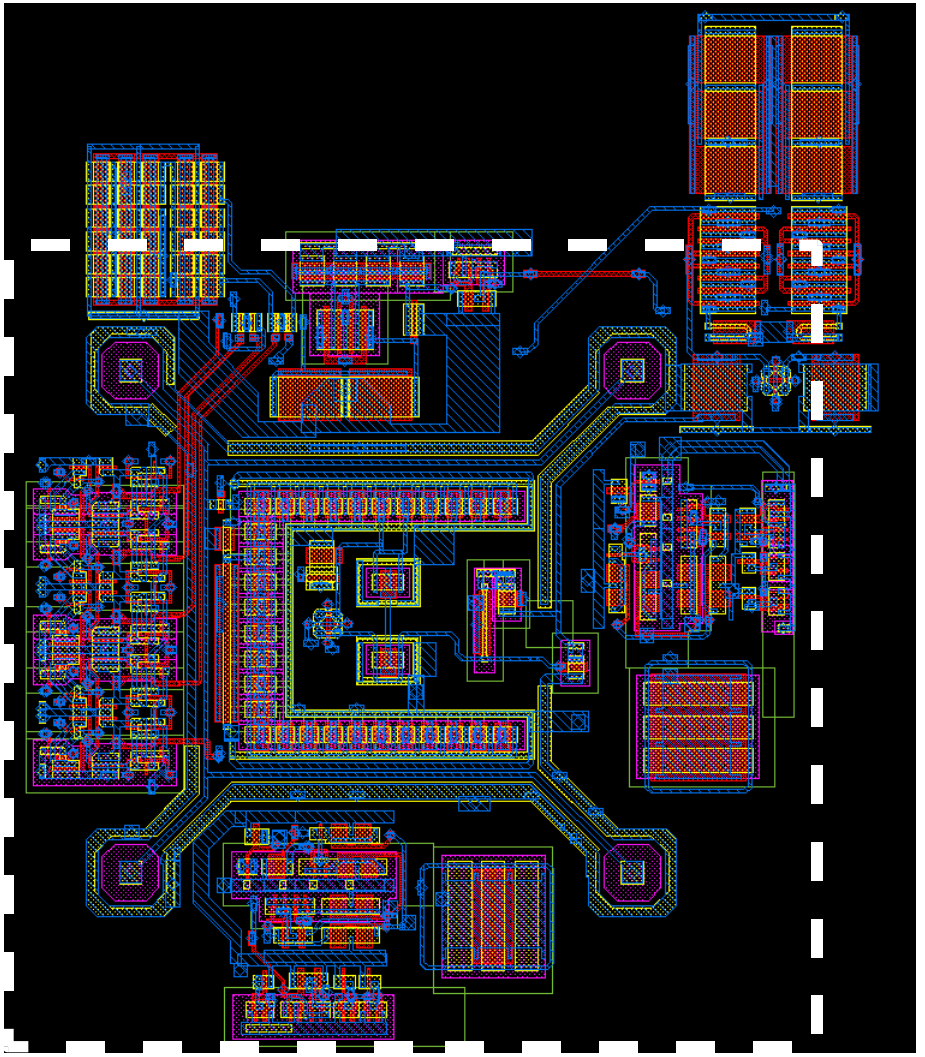
Pre-Sampler

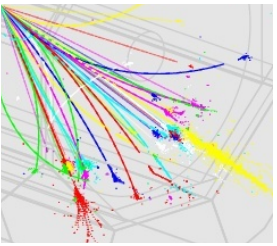




The Pixel

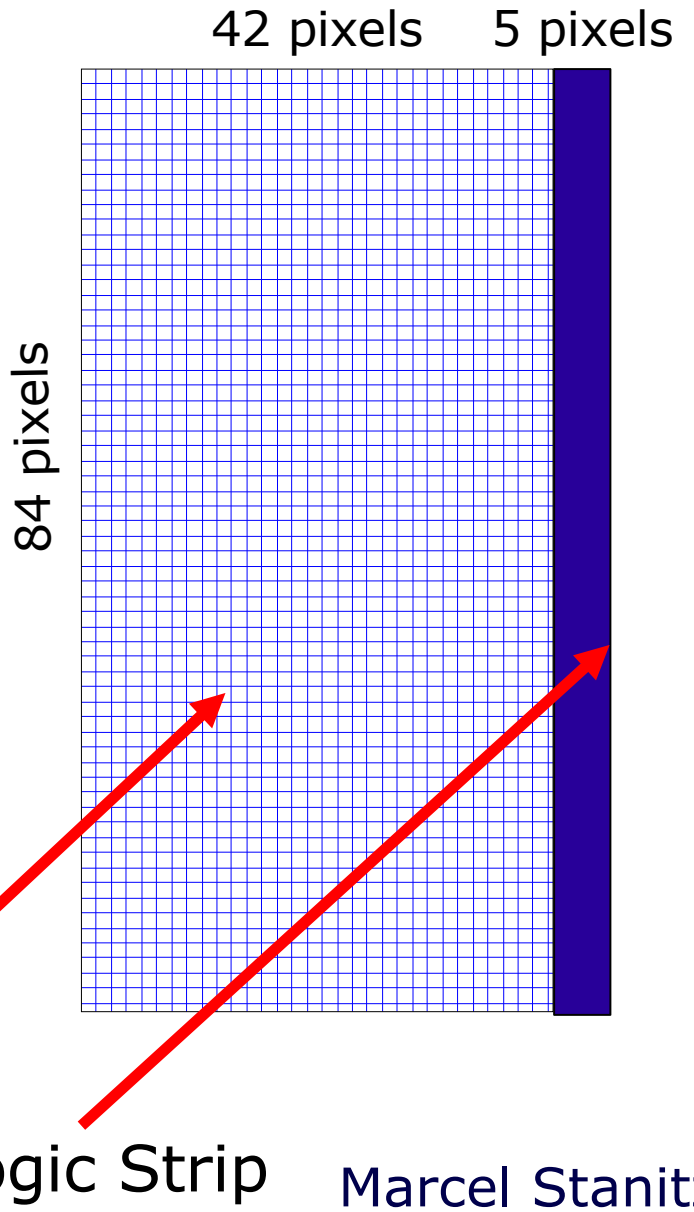
- 50x50 µm size
- 0.18 µm process
- 12 µm Epi-layer (for test run)
- Deep p-wells
- 6 metal layers
- 224 1.8 V transistors
- 1 3.3 V transistor
- 36 capacitors

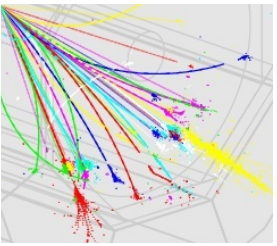




The sensor unit (V1.0)

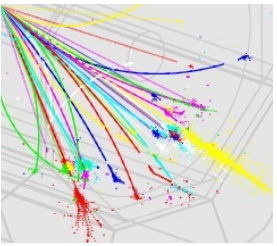
- Consists of 42x84 pixels
- Has a logic strip for
  - 5 pixels wide
  - Hit buffering using SRAM technology, 19 Hits per Row
  - Time stamping (13 bit)
  - Configuration registers
  - the only part with Clock lines
- Logic strip is a “dead area” for particle detection (~ 11 % inefficiency)





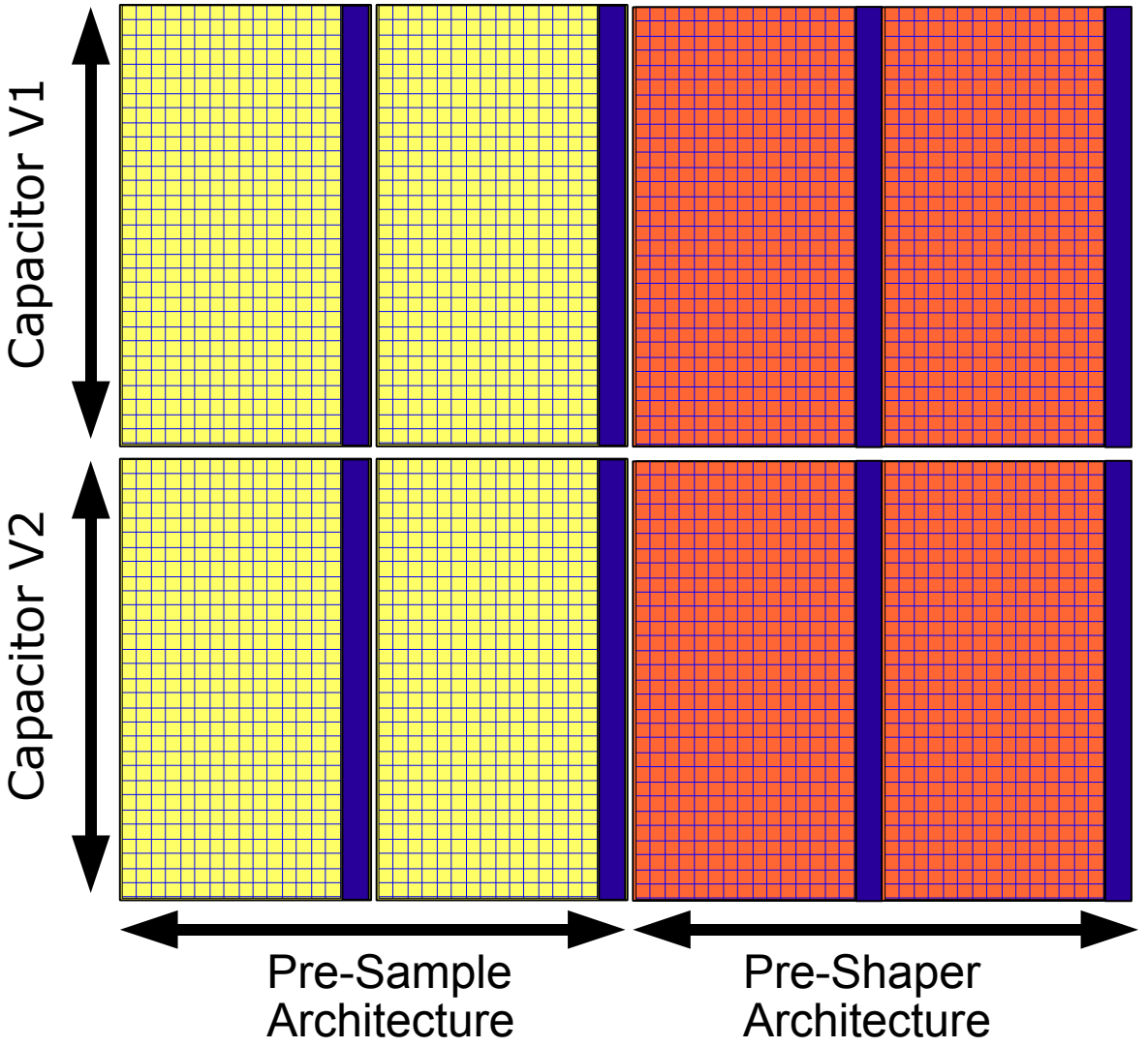
Data format

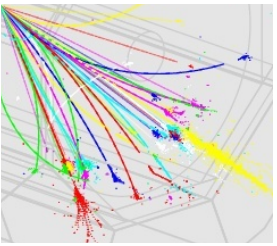
- A row of 42 pixels is split into 7 groups of 6 pixels each (“patterns”)
- The logic writes the following data format for each row
  - Time stamp (13 bits)
  - pattern number (3bits)
  - pattern (6 Bits)
- 1 Hit = 22 Bits
- On top :Row Enconding (9 Bits)
- 1 Hit = 31 Bit altogether



The test sensor (V1.0)

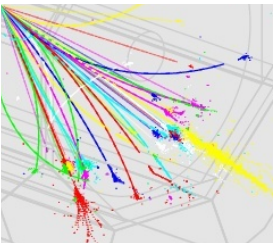
- 8 units (1 x 1 cm)
- A unit is uniform, but units are different
- 2 pixel architectures
- 2 capacitor arrangements
- 6 million transistors in total





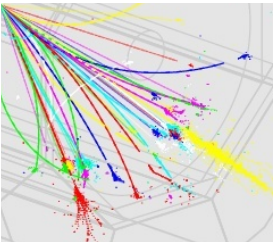
Sensor Simulation

- We are using Centaurus TCAD to simulate the sensor
- Using CADENCE GDS file for pixel description
- Simulate diodes from adjacent pixels for charge sharing effects
- Detailed Pixel performance studies
  - Collection Efficiency
  - Charge Collection Time
  - Signal/Noise

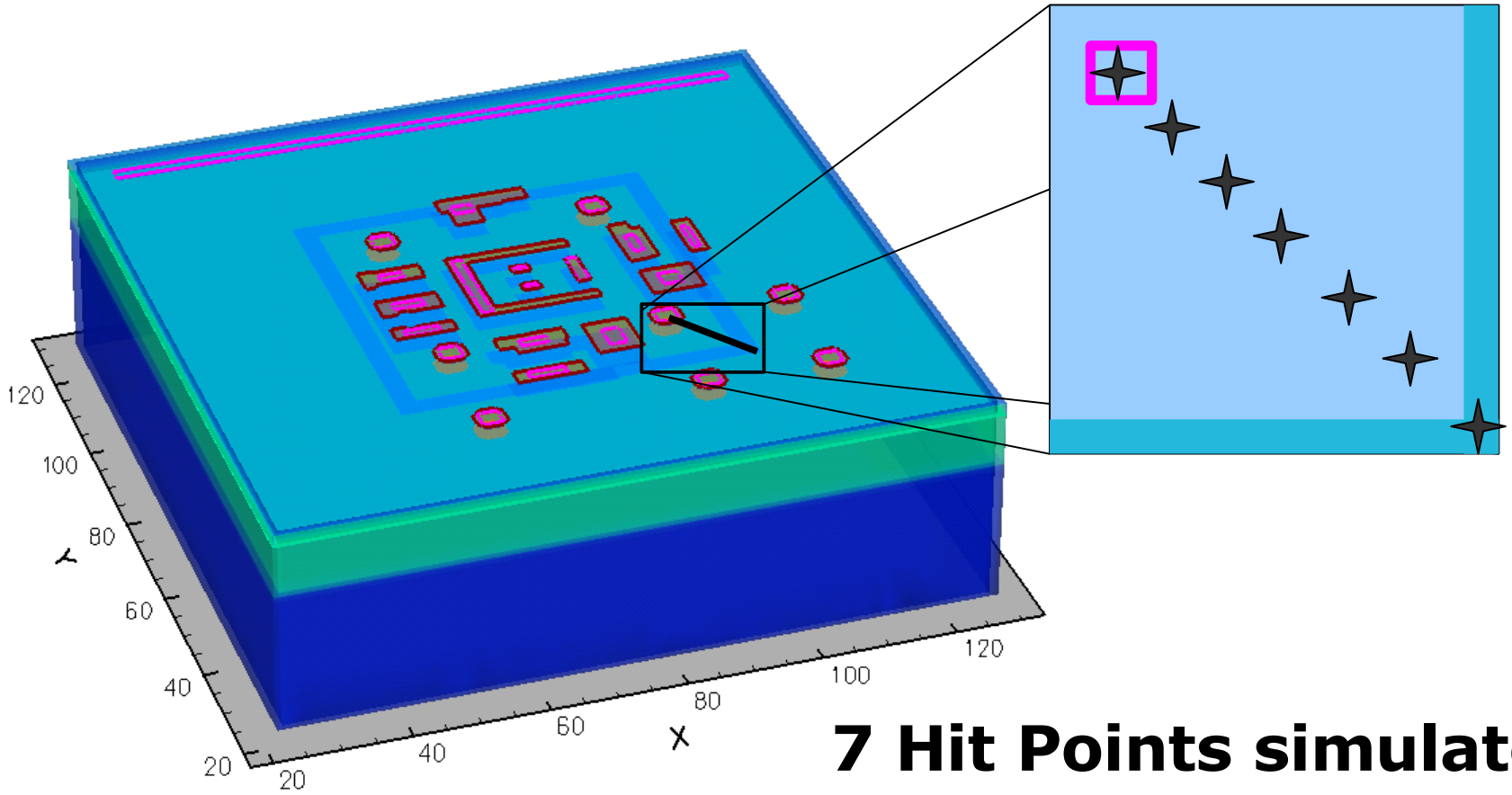


The setup

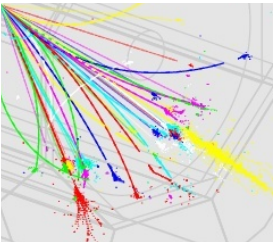
Electronics
Diodes
Adjacent Diodes
Bias:
•n-Well 1.8/1V
•Diodes: 1.5V
Epi-Layer
Substrate (left floating)
120
100
80
60
40
20
Y
X



Simulation Setup

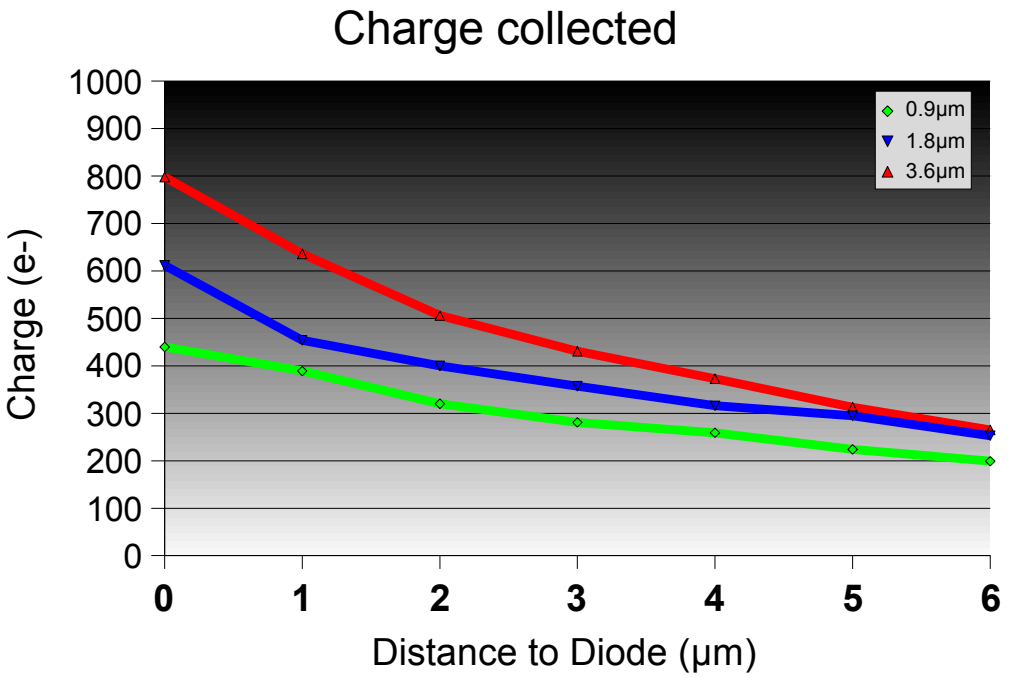


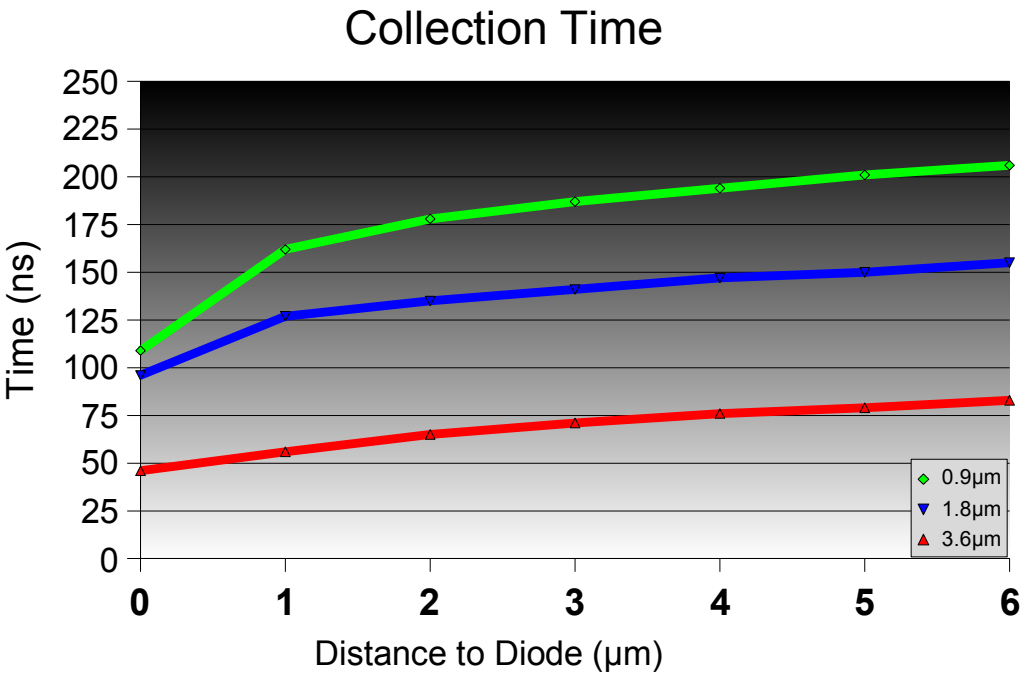
7 Hit Points simulated
1 µm distance



Charge Collection

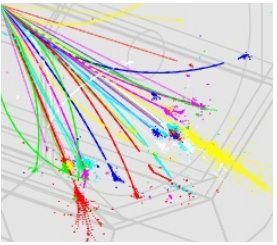
Total charge generated : ~ 1300 electrons



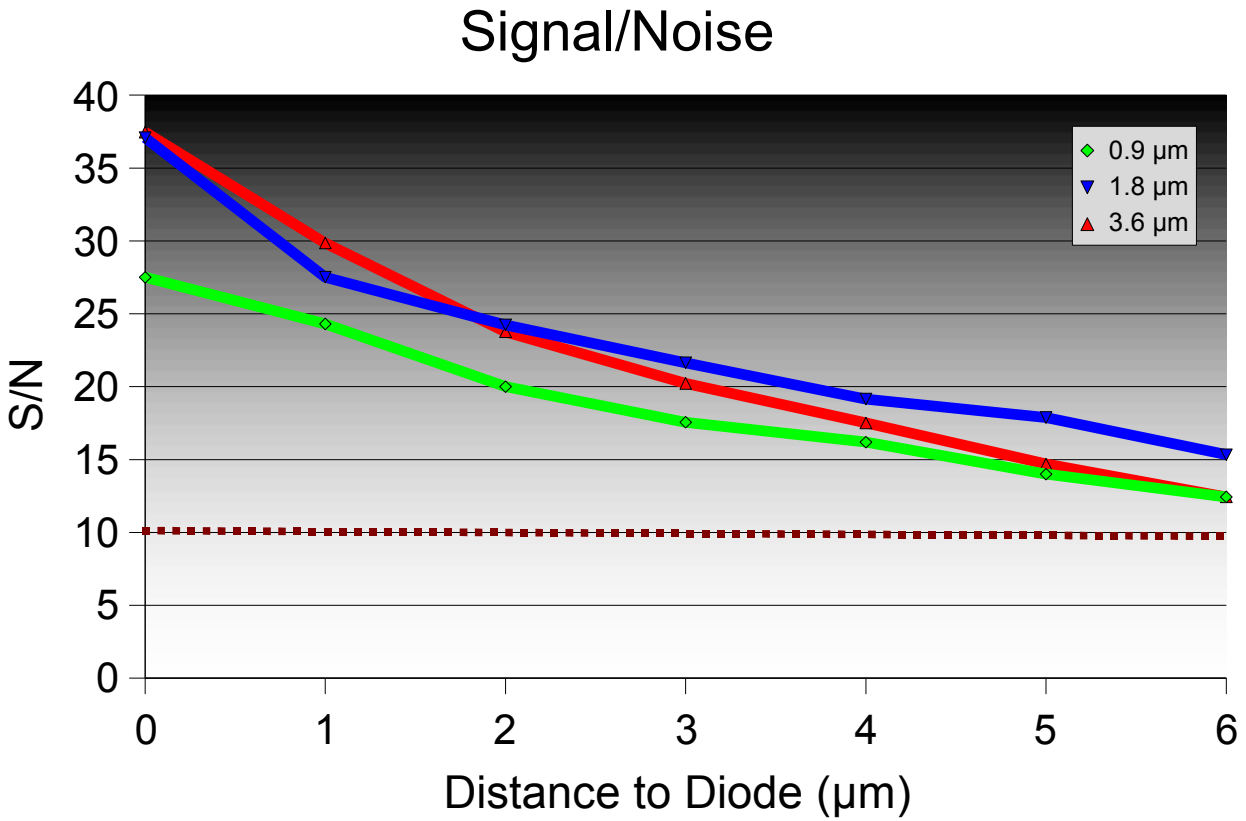


Main parameter to vary is Diode Size

ILC Bunch spacing ~ 300 ns



Signal/Noise

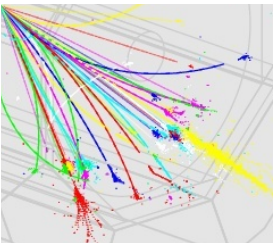


*N.B. S/N 0.9µm N = 16 e^-

*N.B. S/N 1.8µm N = 16.5 e^-

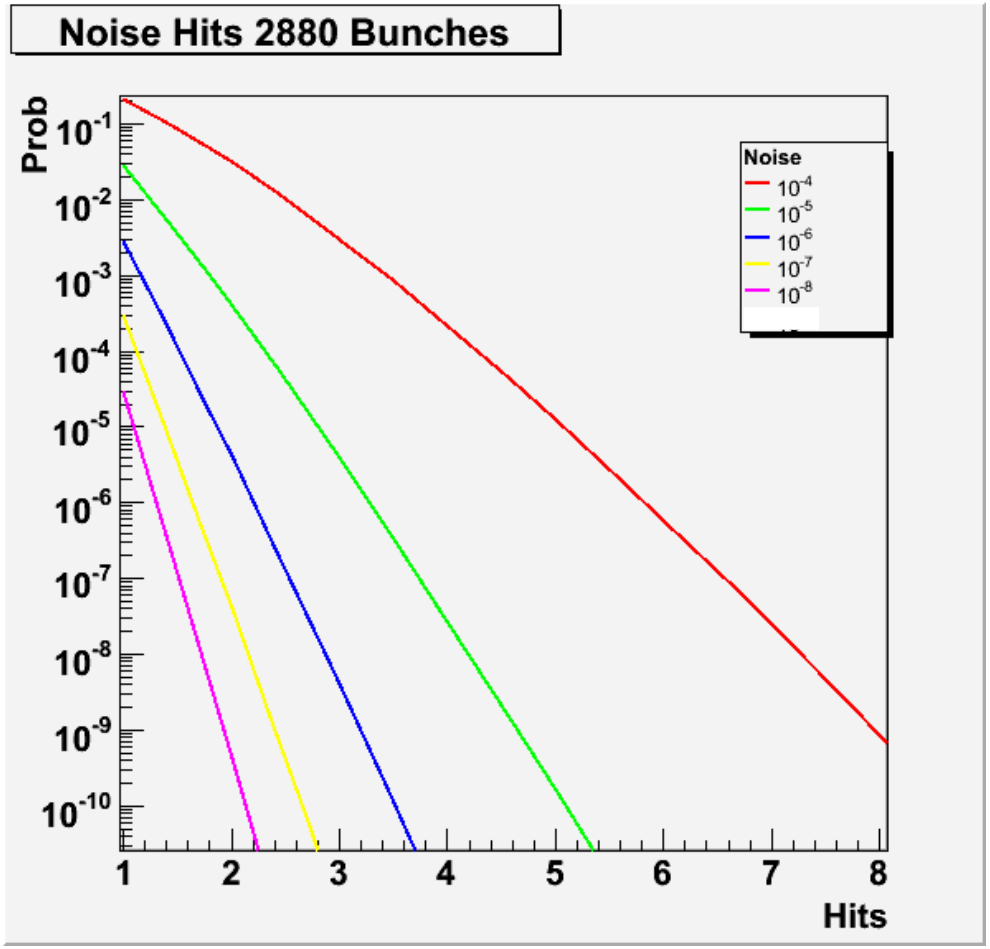
*N.B. S/N 3.6µm N = 21.3 e^-

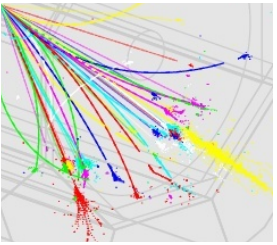
- Signal to Noise > 15 for 1.8 µm Diode Size
- Some uncertainty for the absolute Noise levels, due to simulation imperfections
- Critical Measurement with the real sensor



Noise Occupancy

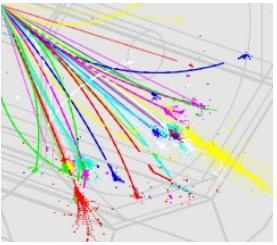
- Noise for 2880 bunches
- With Noise=O(10^{-6})
  - P=0.3 % for 1 hit per pixel
  - P=0.0004 % for 2 hit per pixel
- But O(10^{12}) pixels !
  - ~3 10^{9} single hits
  - ~4 10^{6} double hits
  - ~0 triple hits
- Per Row (42 pixels) 0.15 Hits





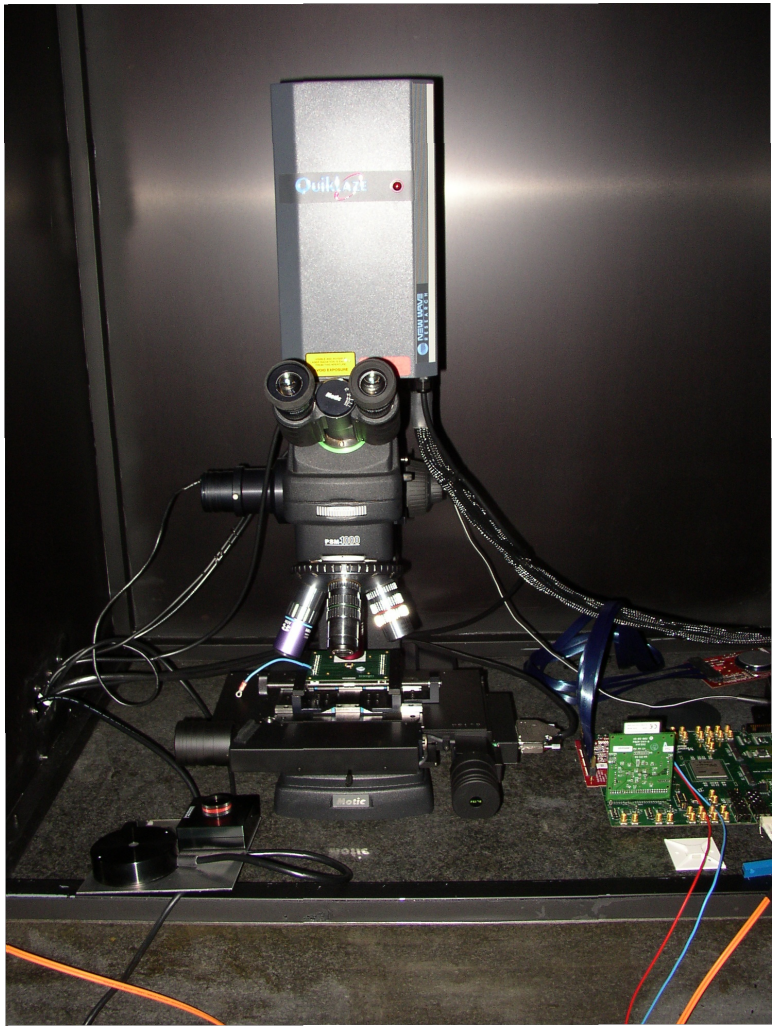
MAPS DAQ & Testing

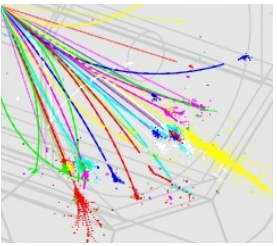
- Development of DAQ board and firmware has started
- Complete test setup foreseen
  - Cosmics
  - Sources
  - Laser
  - Test beam



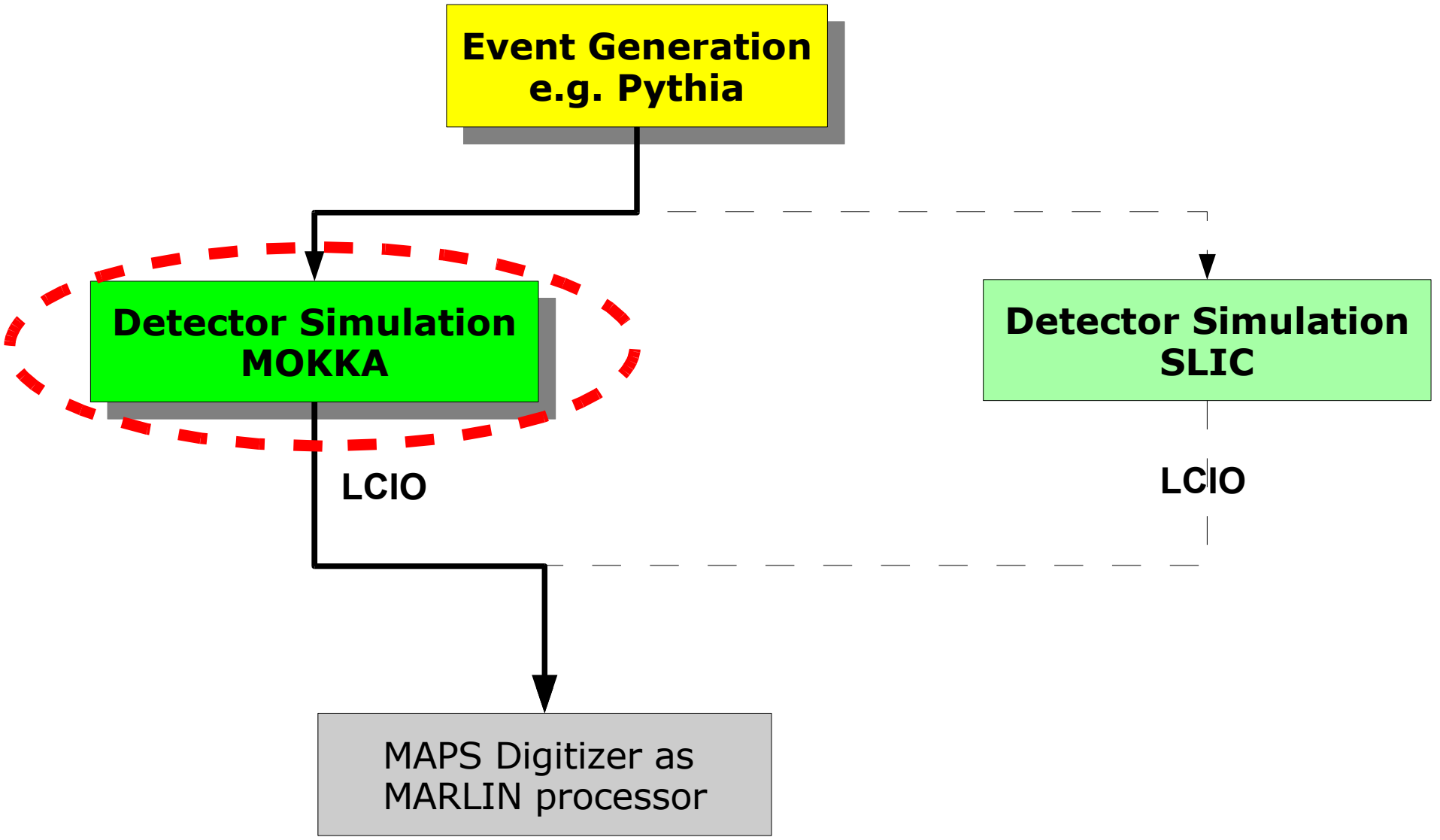
RAL Laser Test setup

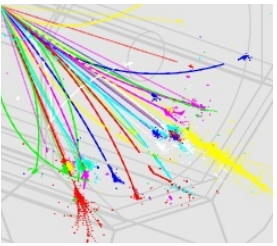
- Powerful Laser setup
- 1064, 532 and 355 nm Wavelength
- Accurate focusing (<2 µm at longest wavelength)
- Pulse Width 4 ns
- 50 Hz Repetition rate
- Fully automatized
- Will be used to test the MAPS





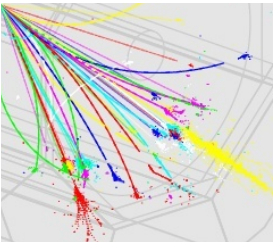
Simulation Chain



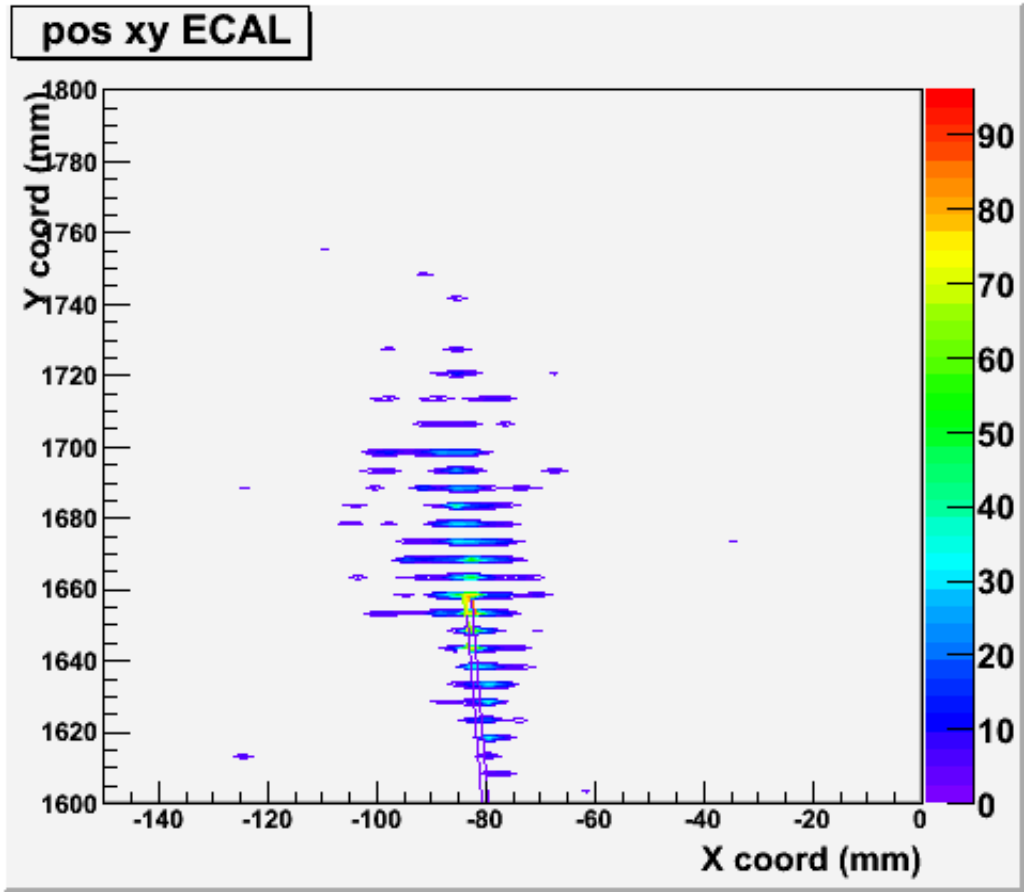


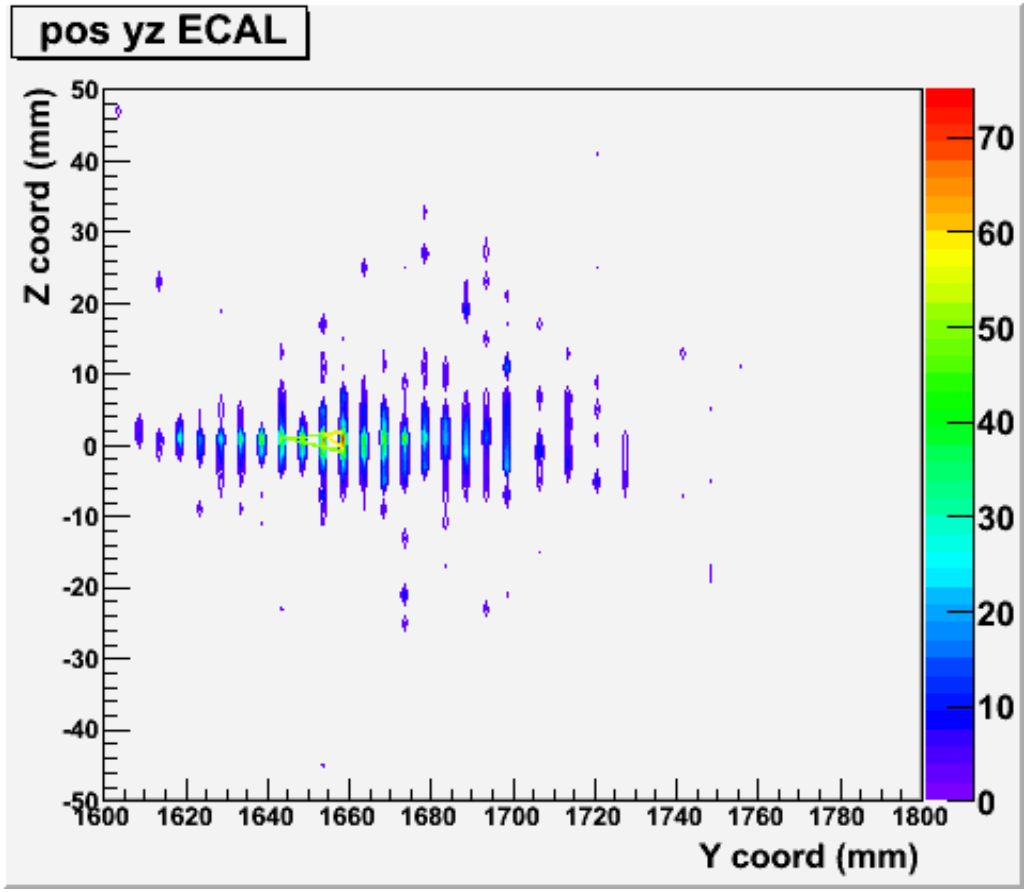
Mokka Detector Simulation

- Implementation of the MAPS into MOKKA
  - Patched MOKKA 6.02
- 50x50 µm pixel size
- 15 µm "Active Area" (Epi-layer)
- Detector Model used LDC01(Sc)
- ECAL with 30 layers
  - 20 layers 2.1 mm Tungsten
  - 10 layers 4.2 mm Tungsten
- Charge diffusion and thresholds are implemented in a separate "Digitization" step

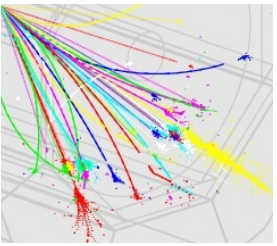


Shower Shapes

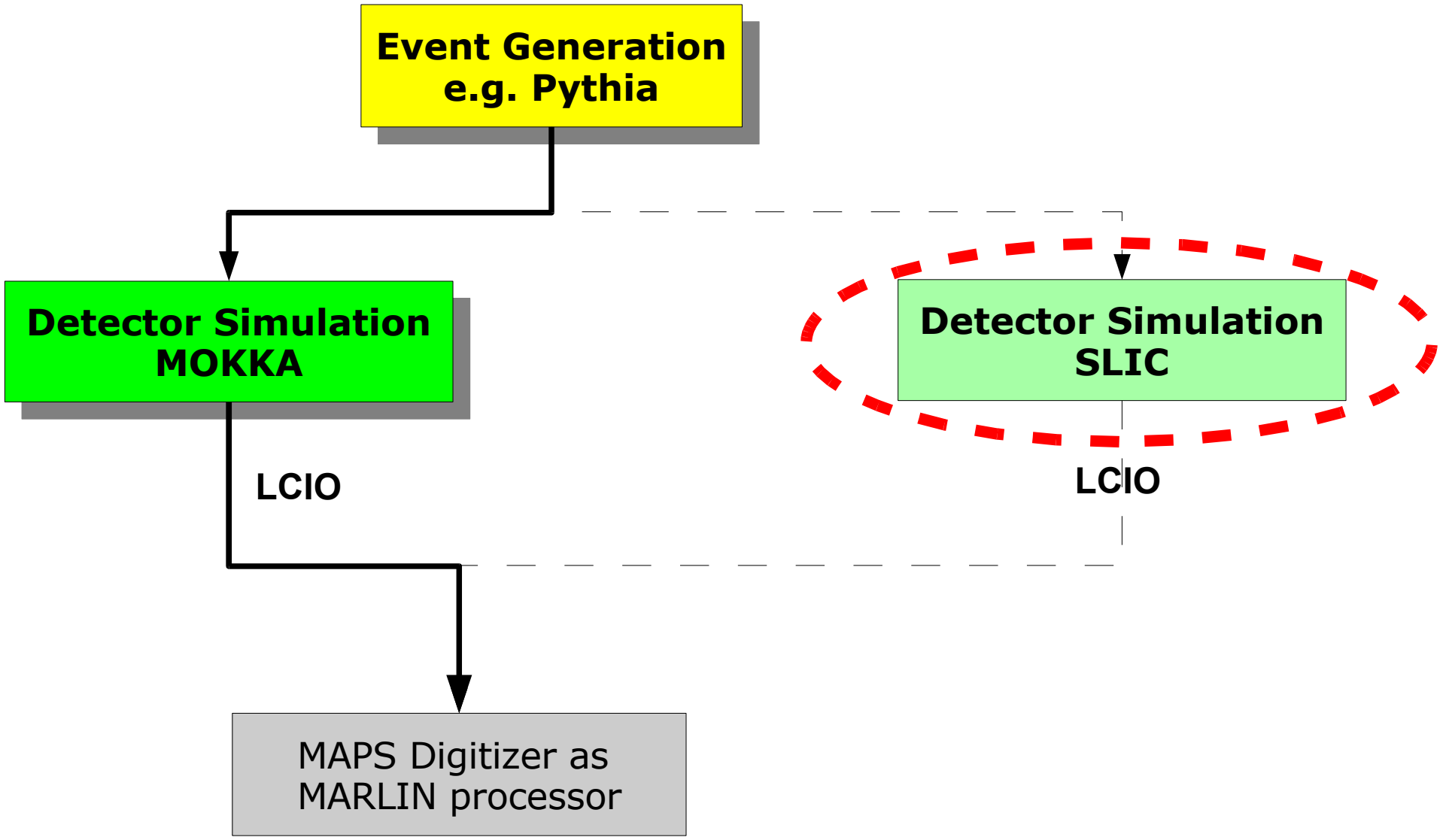


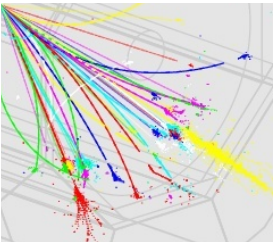


GEANT4 : One 20 GeV Electron shot along y-axis

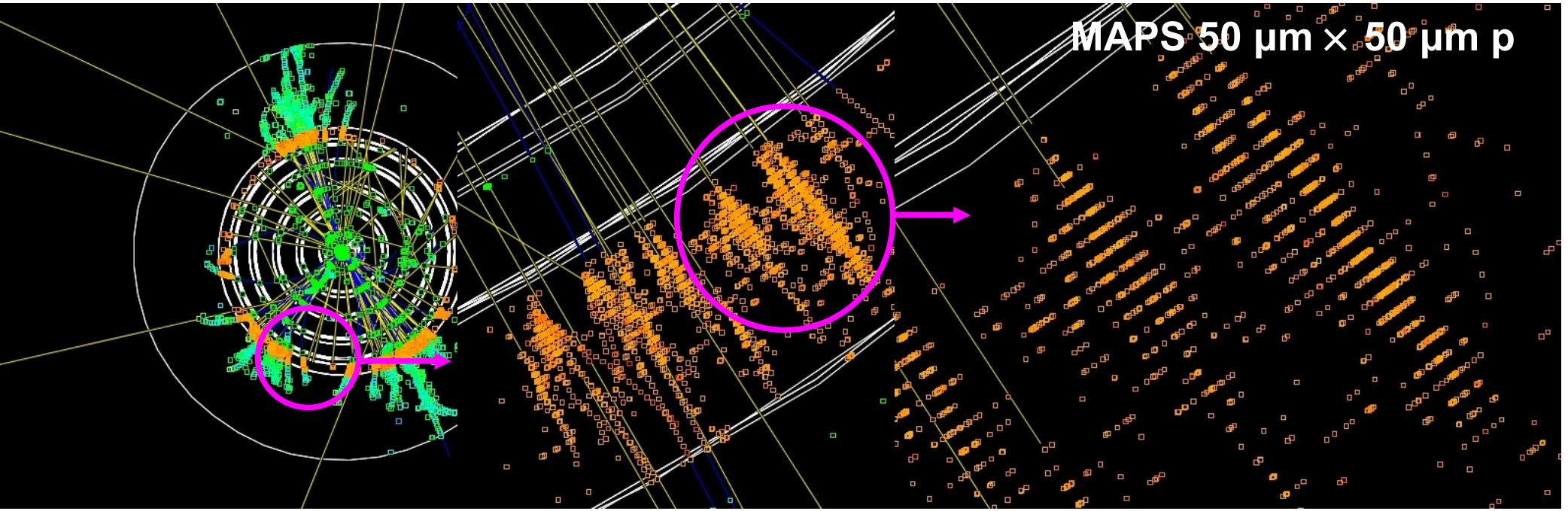


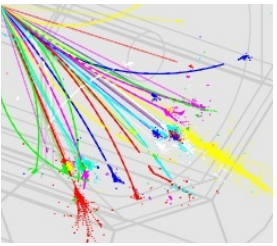
Simulation Chain



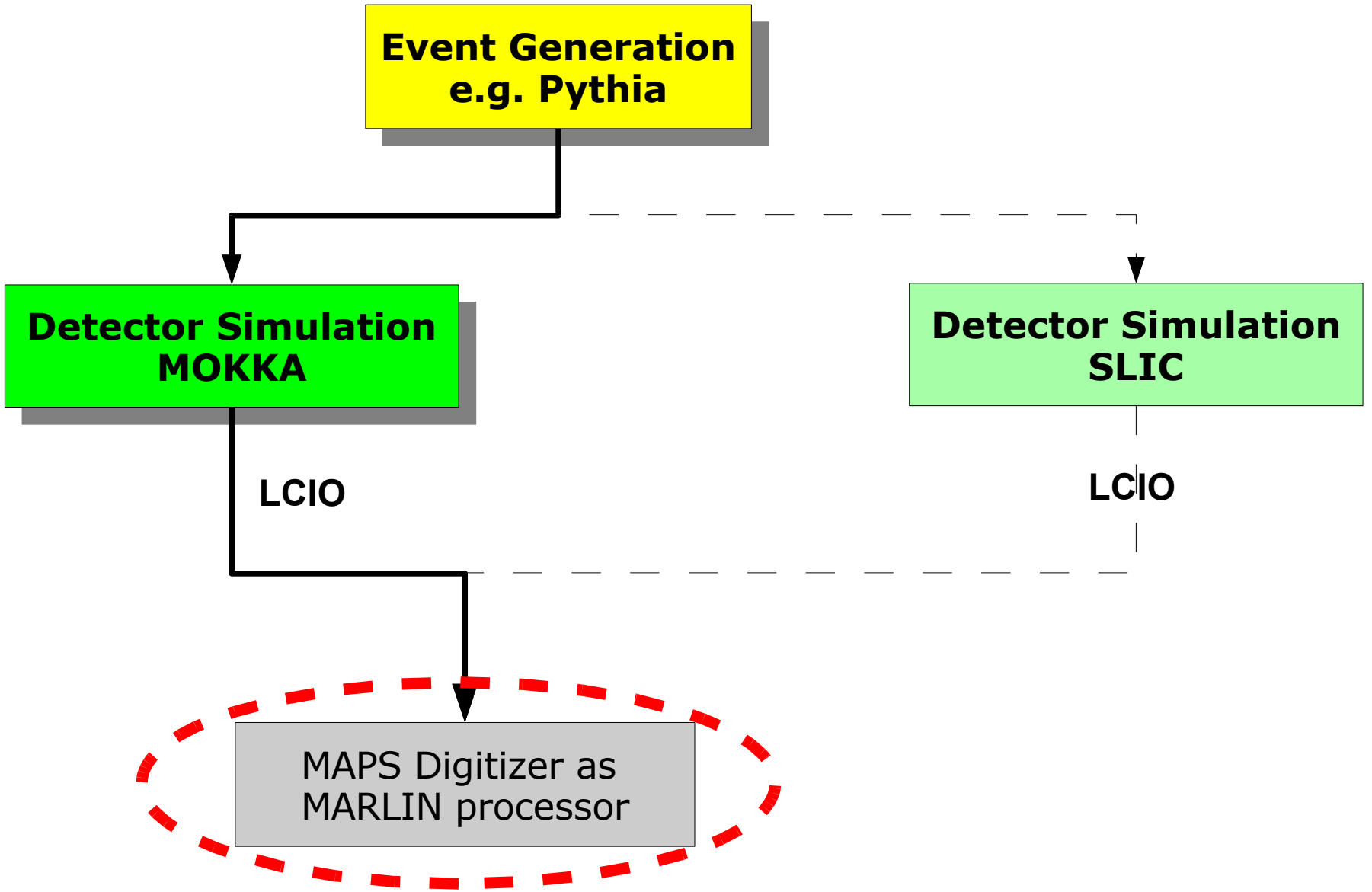


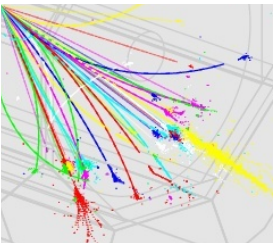
Running with SLIC





Simulation Chain



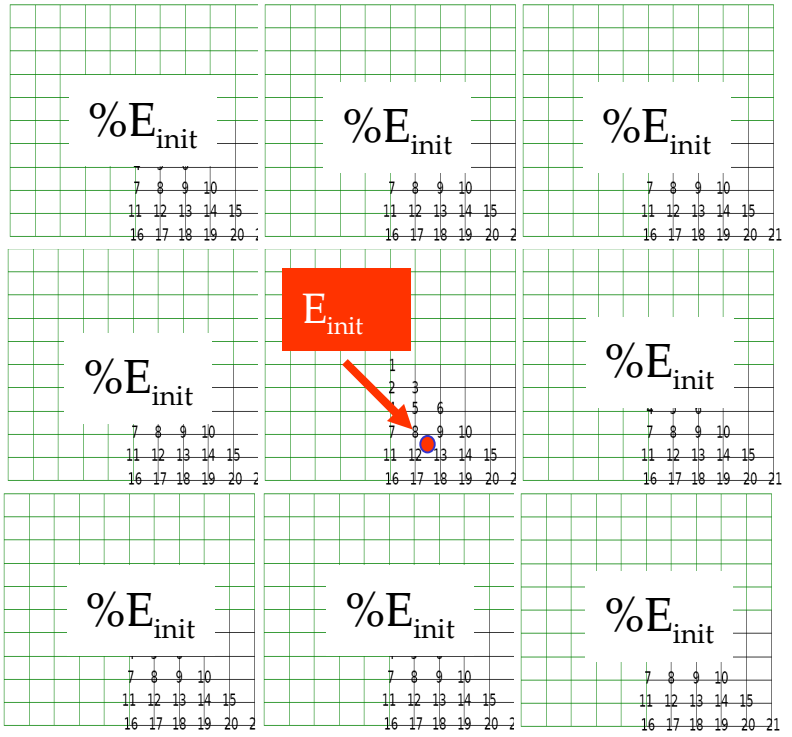


Charge sharing algorithm

Geant4 E_{init} in 5x5 μm² cells

→ Apply charge spread $E_{after\ charge\ spread}$

→ Sum energy in 50x50 μm² cells E_{sum}

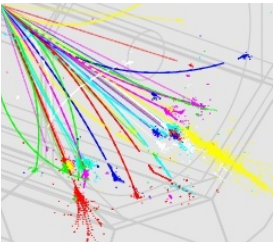


← Add noise to signal hits with σ = 75 eV

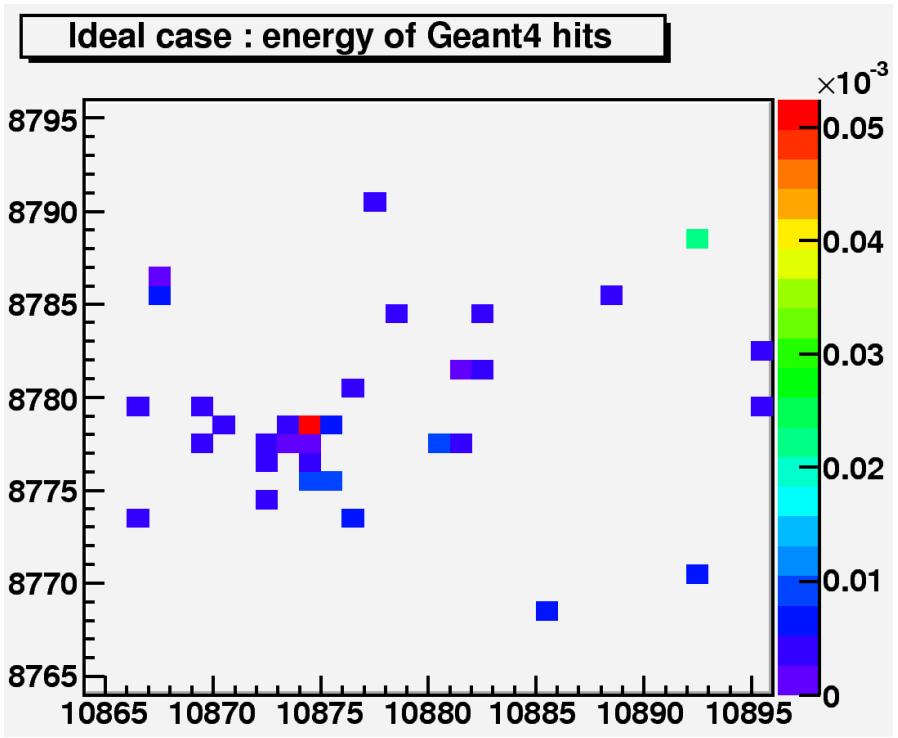
↓ + noise only hits
prob. 10^{-6} ➔ ~ 10^{6} hits in the whole detector
BUT in
a 1.5 x 1.5 cm tower : ~30 hit in 30 layers.

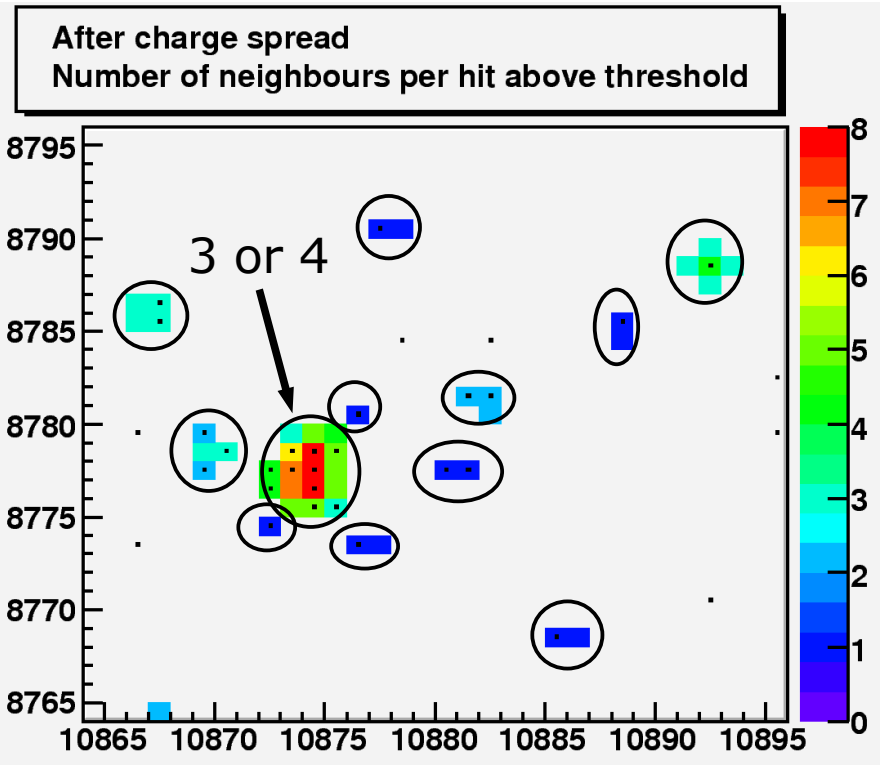
↓ Register the position and the number of hits above threshold

$$\sum E_{neighbours} \sim (50\% - 80\%) \times E_{init}$$



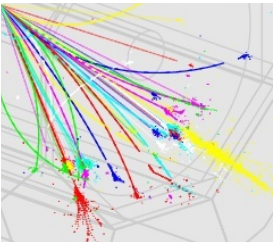
Basic Hit Clustering



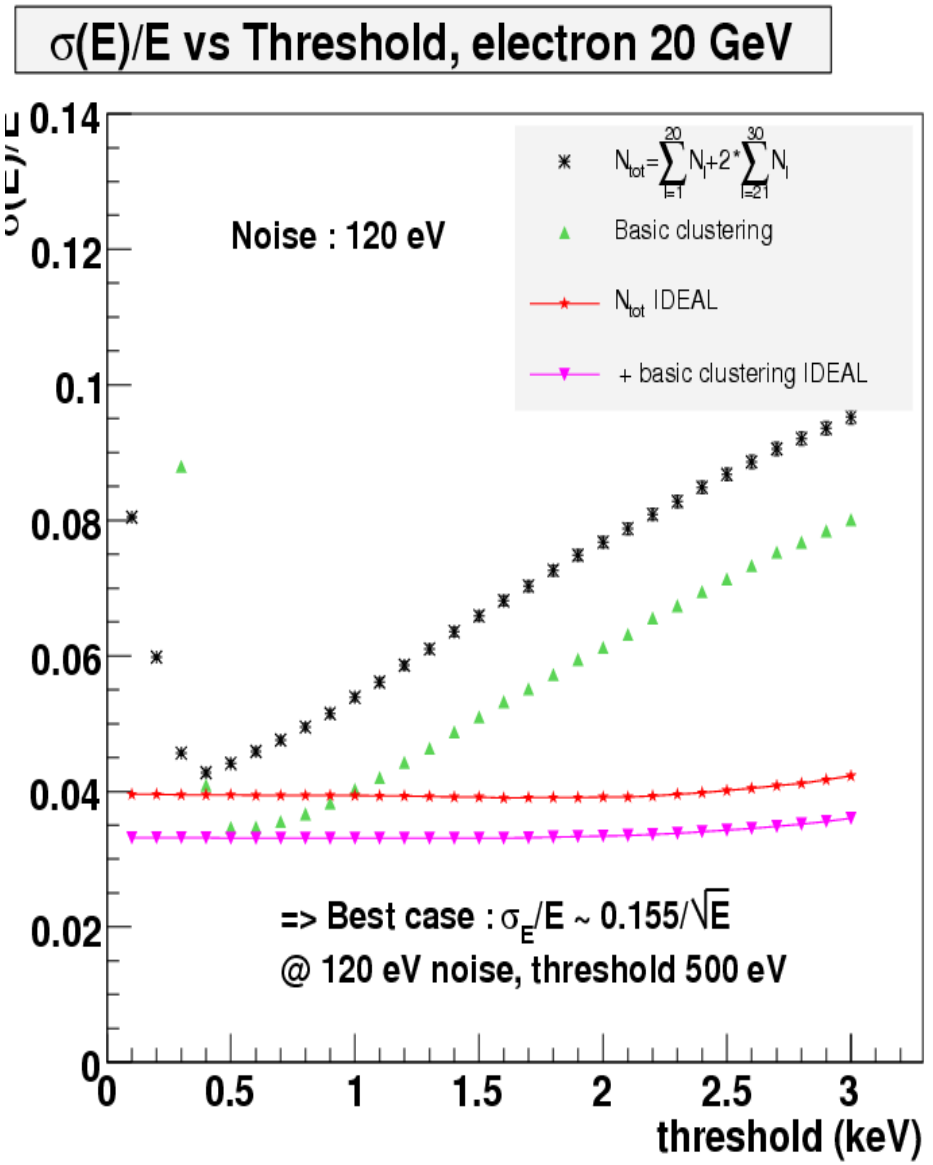


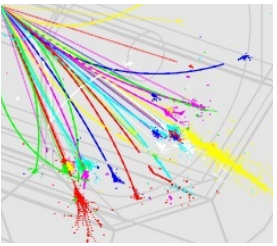
Hit Clustering

- Loop over hits classified by number of neighbors
- Number of neighbors < 8 :
  count only 1 (or 2 for last 10 layers) and discard the neighbors
- 8 neighbors AND one of the neighbor has 8 neighbors :
  count 2 (or 4) and discard the neighbors



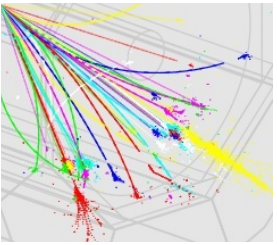
Clustering (II)



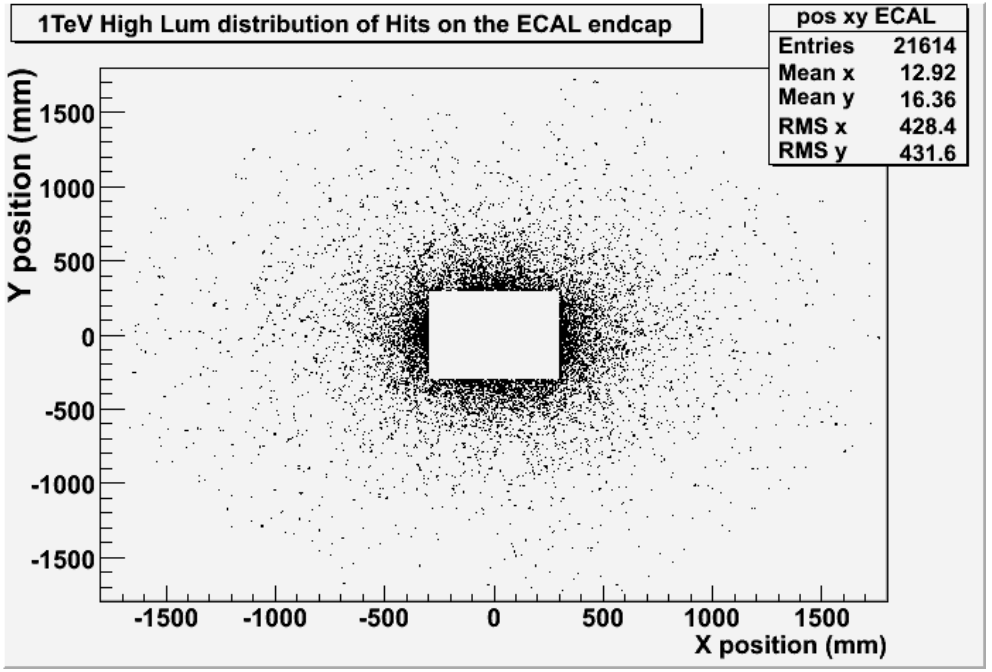


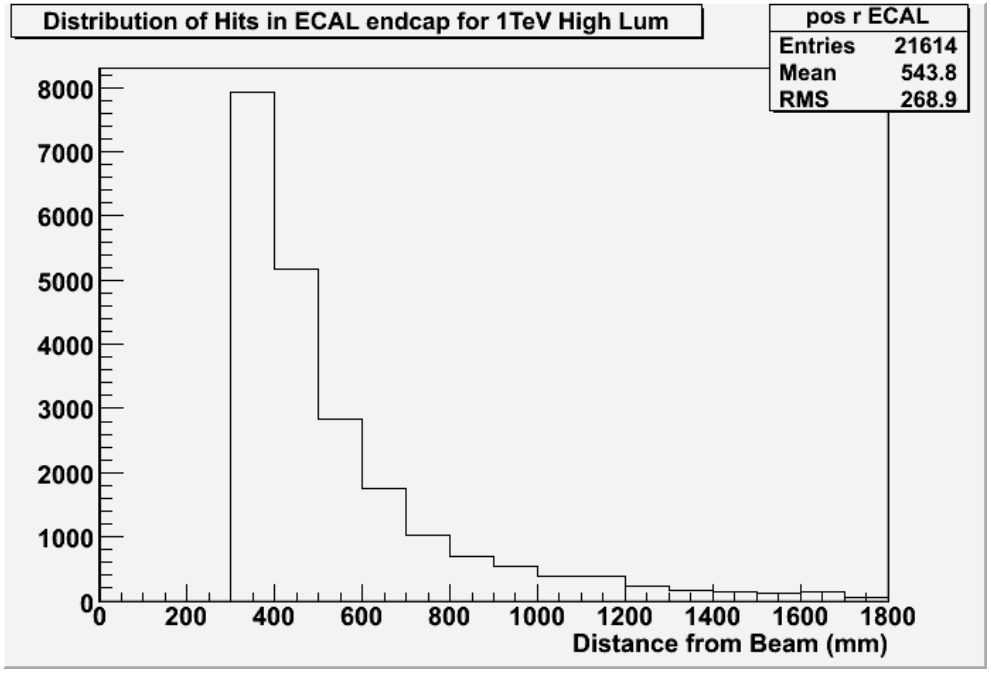
Beam background

- Done using GuineaPIG
- Trying to estimate beam induced background in the ECAL
- Testing two scenarios
  - 500 GeV Baseline
  - 1 TeV High Lum
- 1 TeV High Lum is “worst-case” scenario

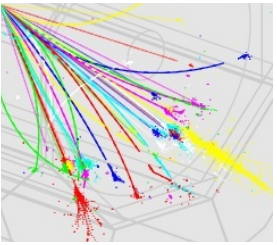


1 TeV High Luminosity



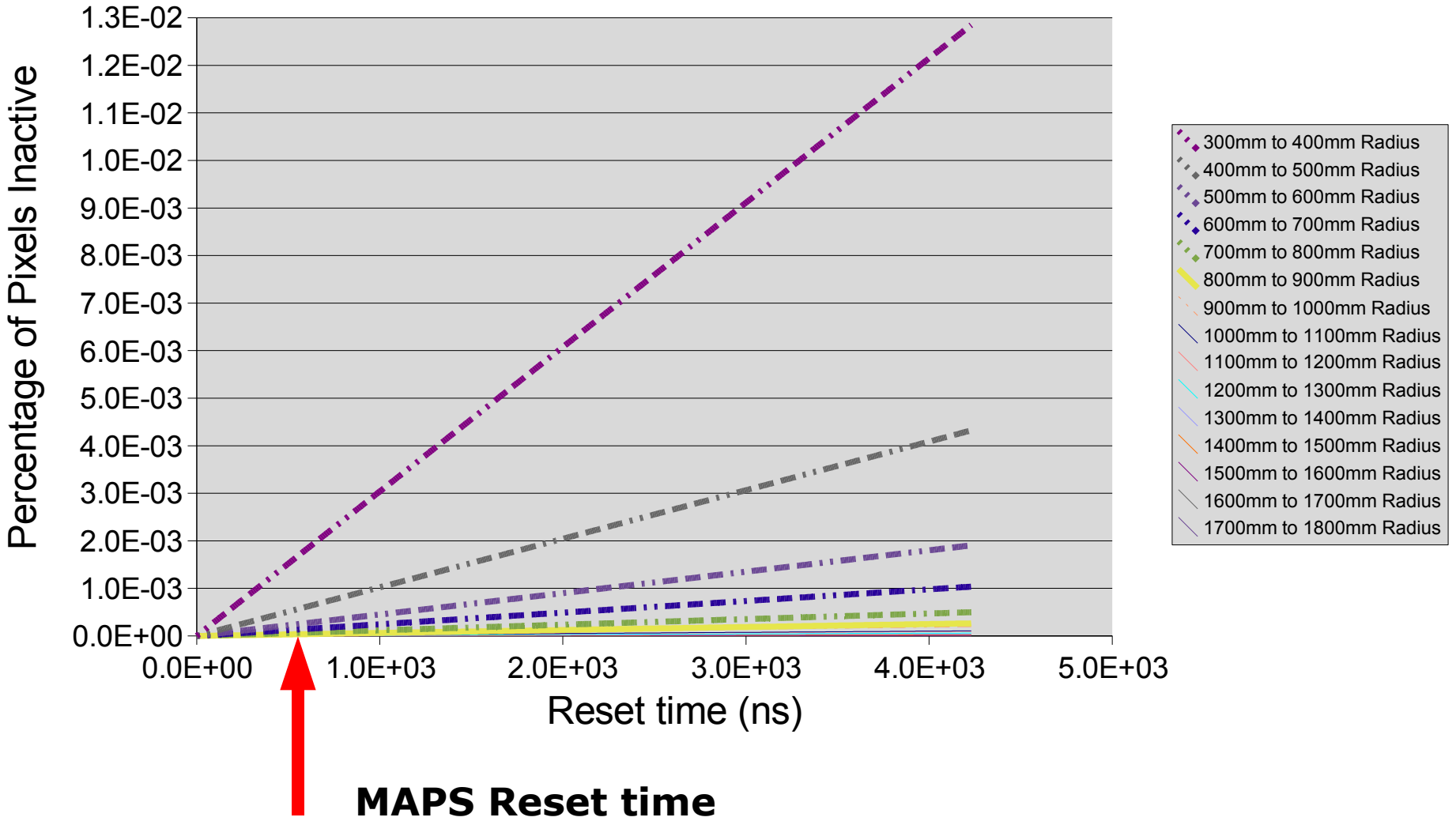


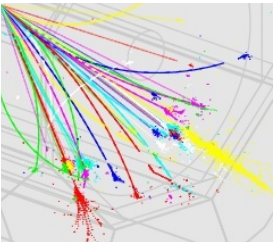
"Ring of Fire" for small ECAL Radii



Beam Background Occupancy

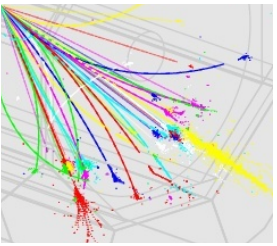
1TeV High Lum Based on 30 layers of 50x50 μm





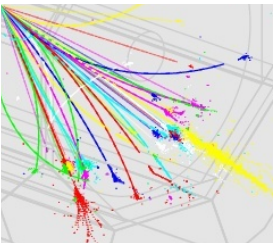
Design Issues

- Pixel parameters
  - Pixel size
  - Number of Diodes / Diode size
- PCB/Readout Chips
- Stave Structure
- Power
- DAQ
- Manufacturing



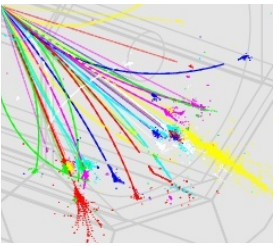
Pixel parameters

- MAPS Pixels improve spatial resolution/granularity by a factor of ~ 1000 compared to analog pad ECAL
- Lower pixel size is set by size of the integrated electronics (lower boundary of 50 µm) and charge diffusion
- Upper bound set by charge collection time/efficiency and multiple hits
- No fixed upper bound, reasonable value is around 100 µm
- Best performance found with 4 diodes is for 1.8 µm diode size

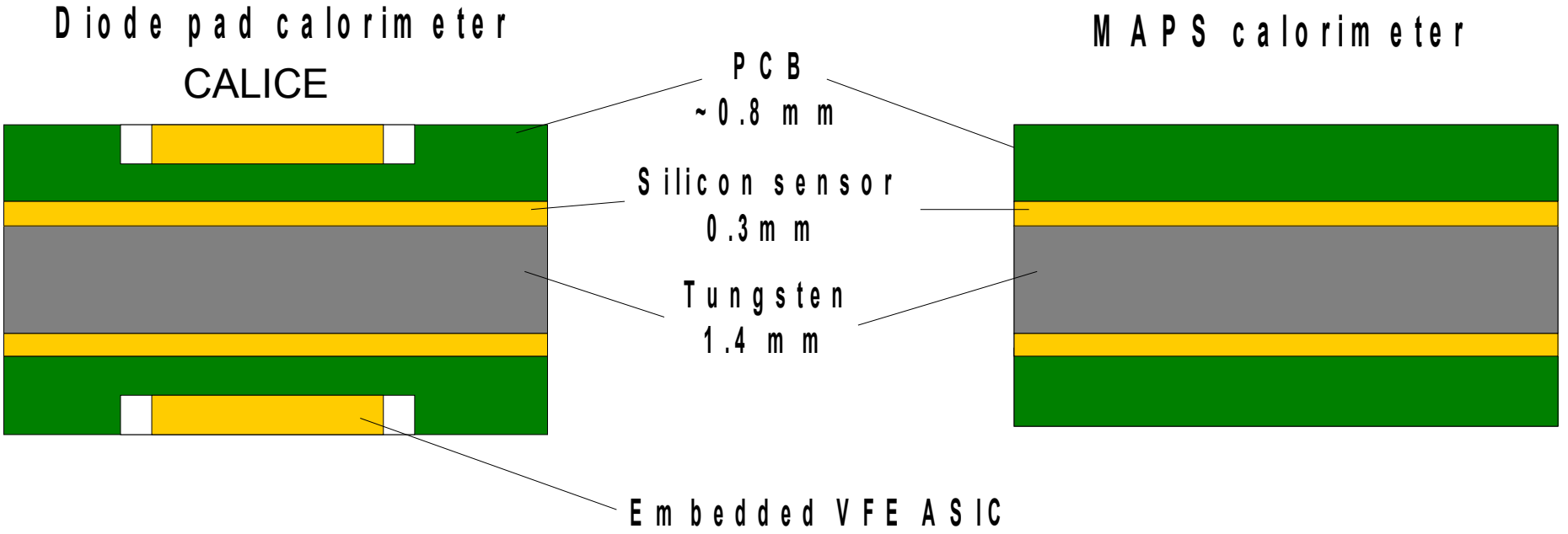


PCB/ Readout Chip

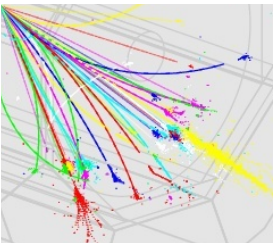
- All the electronics is integrated within the the sensor
- No need for
  - Complicated PCB design
  - Dedicated Readout Chip
- Still needs to provide Power/Clocks/Commands to the MAPS
- Can be done by “Stave Controller” at the end of the Stave



Stave Structure

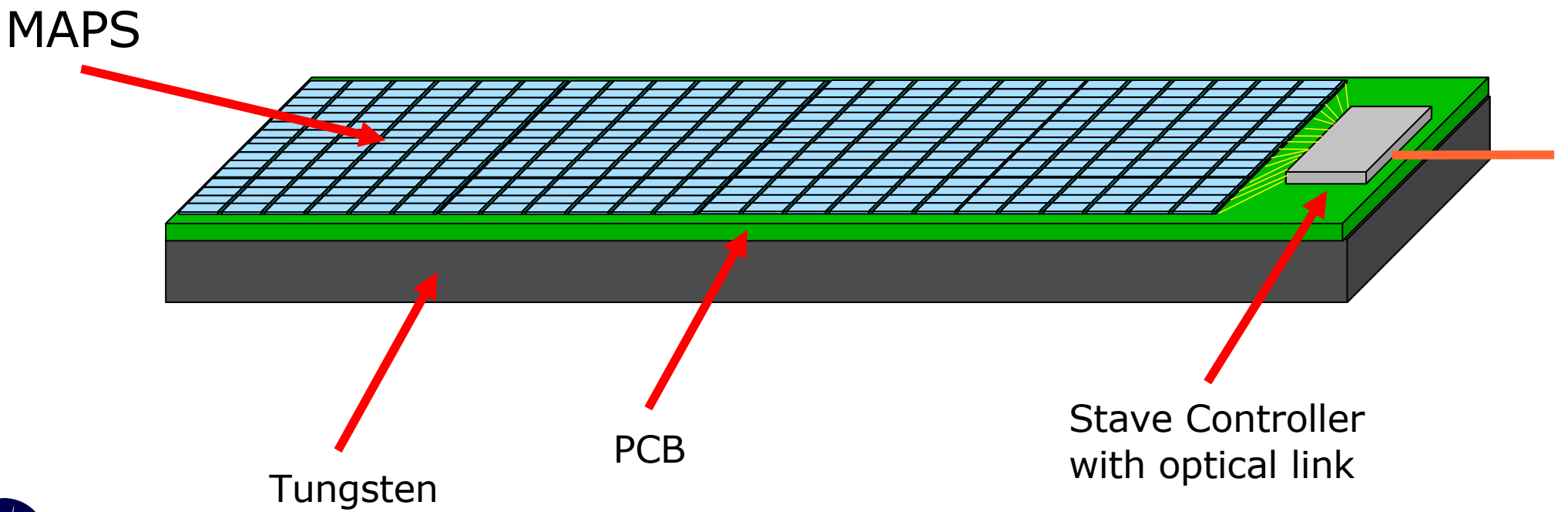


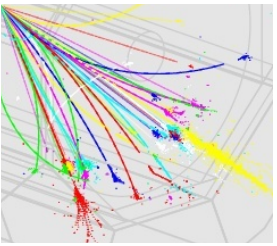
- MAPS can be used as swap-in solution without alterations to the mechanical design (Baseline)
- One can also take further use of MAPS benefits



How it could look like

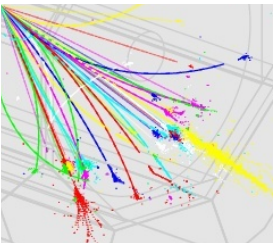
- Take advantage of MAPS benefits
- Lack of hybrids/ASIC allow less complex/thinner PCB
- Thinner sensors (down to 100 µm)
- Bump-bond MAPS





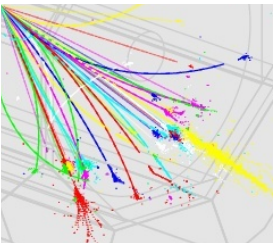
Power

- Cooling for the ECAL is a general issue
- Power Savings due to Duty Cycle (1%)
- Target Value for baseline ECAL 4 $\mu W/mm^2$ (CALICE)
- Current Consumption of MAPS
- ECAL: 40 $\mu W/mm^2$ depending on pixel architecture
- Compared to analog pad ECAL
  - Factor 1000 more Channels
  - Factor 10 more power
- Advantage: Heat load is spread evenly



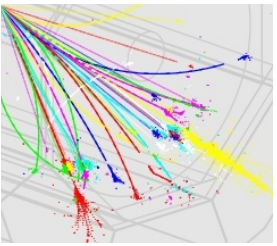
Power prospects

- V1.0 not been optimized for power consumption
  - Proof of Concept and Technology
  - Not the final product
- Options to be explored
  - Larger pixel (50 µm->100 µm) Factor 4 less
  - Longer integrations times if pile-up acceptable, possible factor of 2
  - Smaller feature size (~30-50 %)
  - Lowering Operating Voltages (~10%)
- Sensor V1.0 will allow us to explore some of these



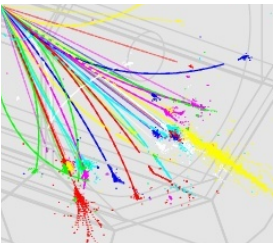
DAQ data volume

- Physics rate is not the limiting factor
- Beam background and Noise will dominate
- Assuming 2880 bunches and 32 bits per Hit
  - 10^6 Noise hits per bunch
  - ~O(1000) Hits from Beam background per bunch (estimated)
- Per bunch train
  - ~88 Gbit / 11 Gigabyte
  - Readout speed required 440 Gbit/s
  - CDF SVX-II can do 144 Gbit/s already



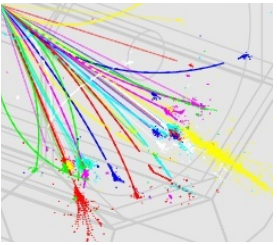
Manufacturing

- Sensor manufacturing
  - Need for large scale process (2000-3000 m^2)
  - Factor 10 of CMS (205 m^2)
  - CMOS is an industry standard process
  - Many foundries can do it
  - CMOS wafers are readily available
  - CMOS is ~2 cheaper than "HEP-style" silicon
- Stave manufacturing
  - Less complex structure due to lack of VFE ASIC
  - No substrate connection to ground required



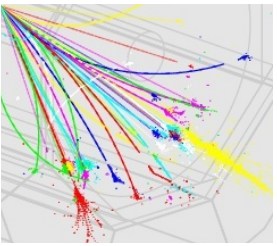
What happens next ?

- Submit Sensor V1.0 April 23rd
- Sensor V1.0 due back Mid July
- Improve/enhance GEANT simulation
- Testing Sensor V1.0
- Do physics studies with a MAPS based ECAL
- Improve sensor simulation with data from V1.0



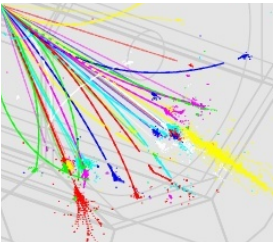
Sensor V2.0

- Will be based on experience made with V1.0
- Larger structures 2x2cm per module
- Only one Pixel readout architecture
- More power optimized
- Submission date Summer 2008

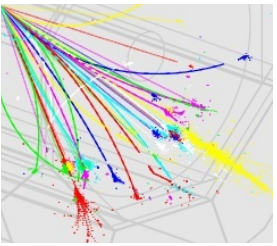


Summary

- MAPS effort is advancing well
- Sensor V1.0 is almost done and be submitted next week
- Will be the proof of concept
- Simulation of a MAPS ECAL is in place
  - Will need tuning with results from sensor V1.0
- Sensor V2.0 will be close to real system
- Will be ready when Detector EDR will be required.

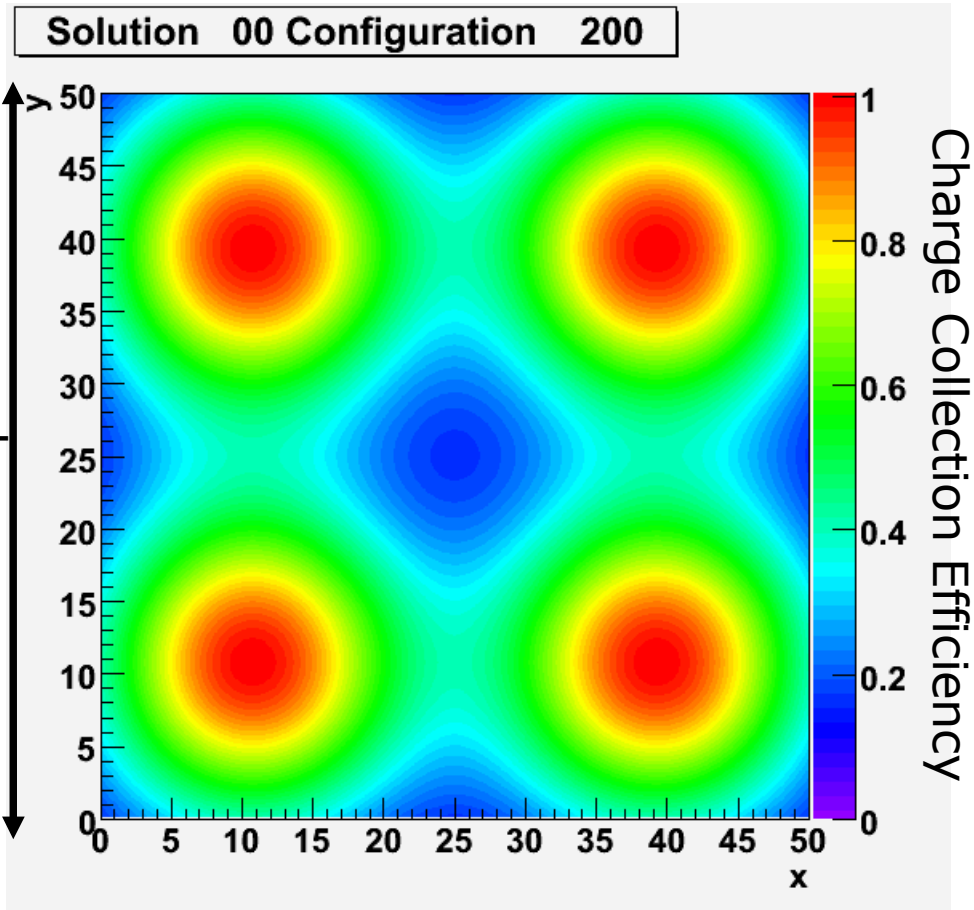


Backup

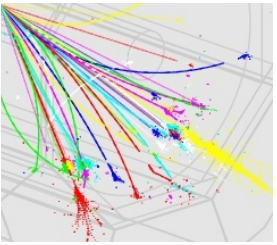


Diode placement

- Classical problem
  - Place n circles in a square
  - No analytical solution
- Only 4 Diodes as a starter
- Mathematics faces reality
  - Constraints due to Design Rules
  - Electronics
  - Space

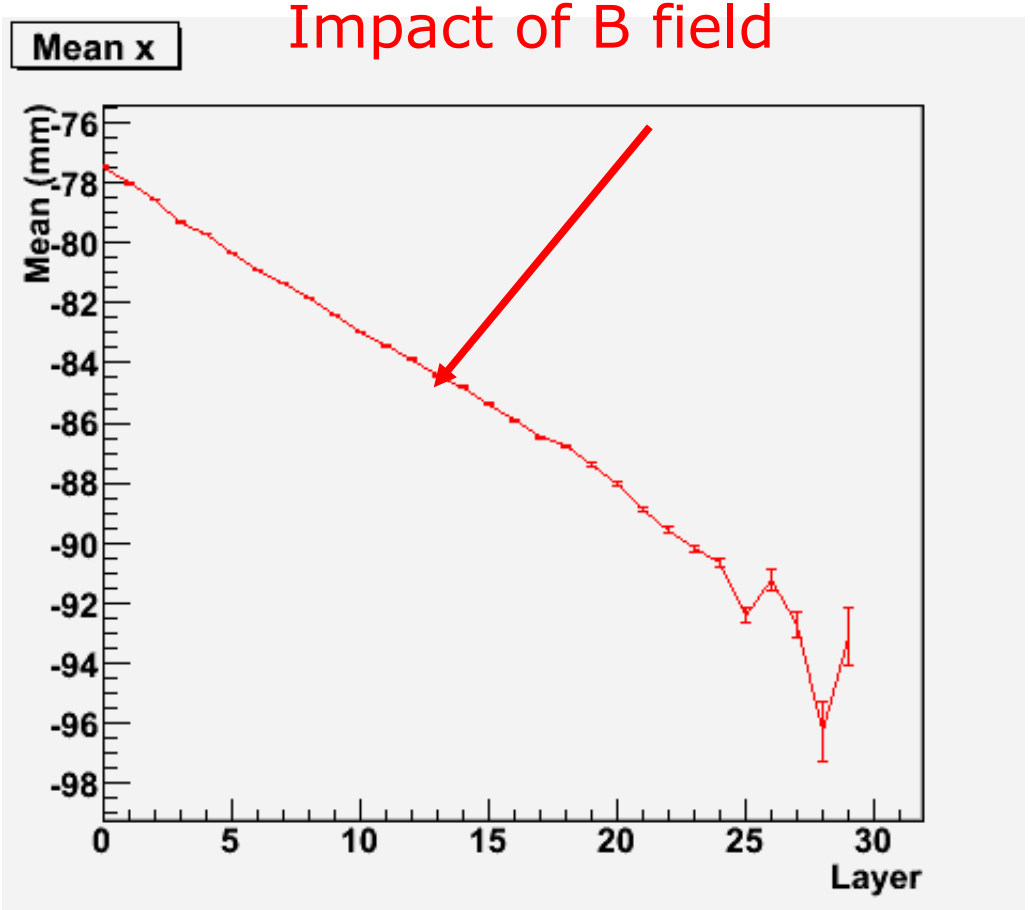


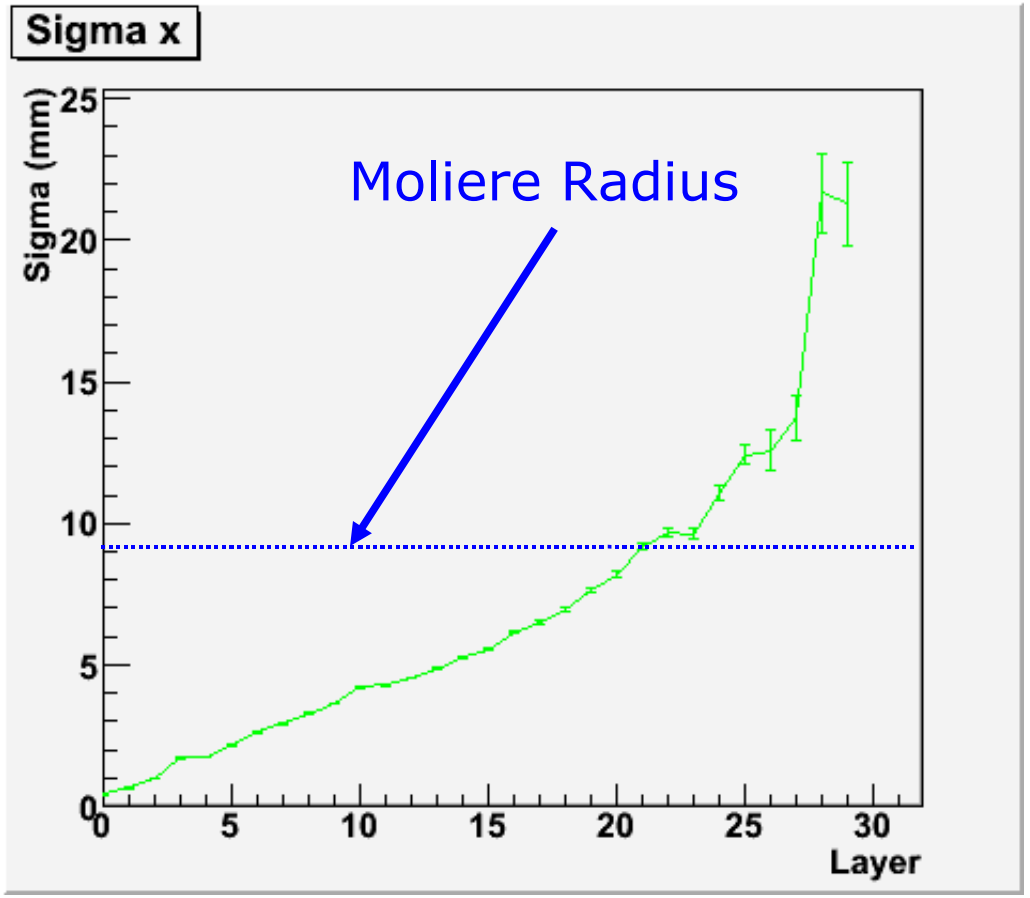
Numerical Solution



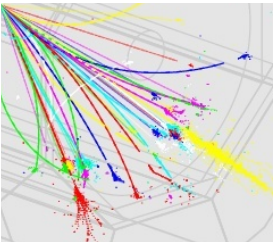
Spatial resolution in x

Impact of B field

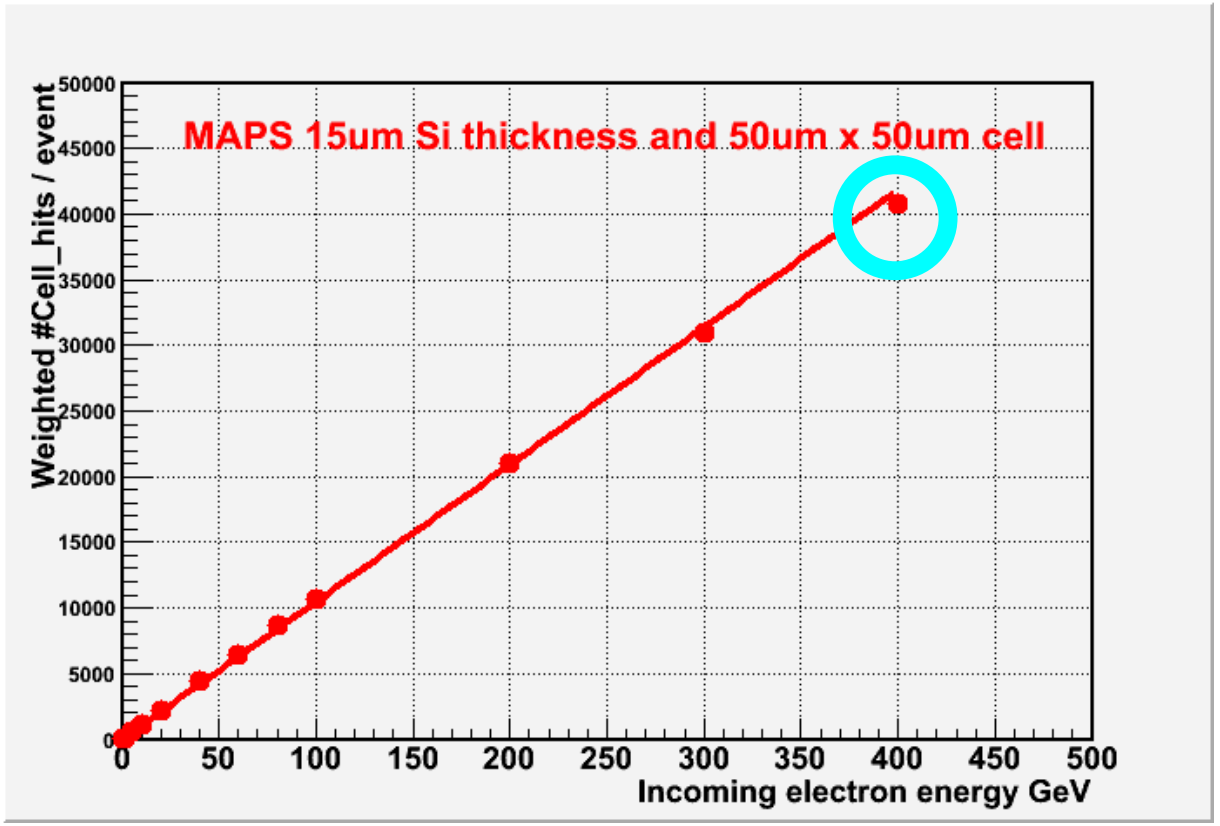




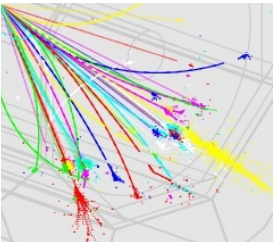
GEANT4 :20 GeV Electrons shot along y-axis



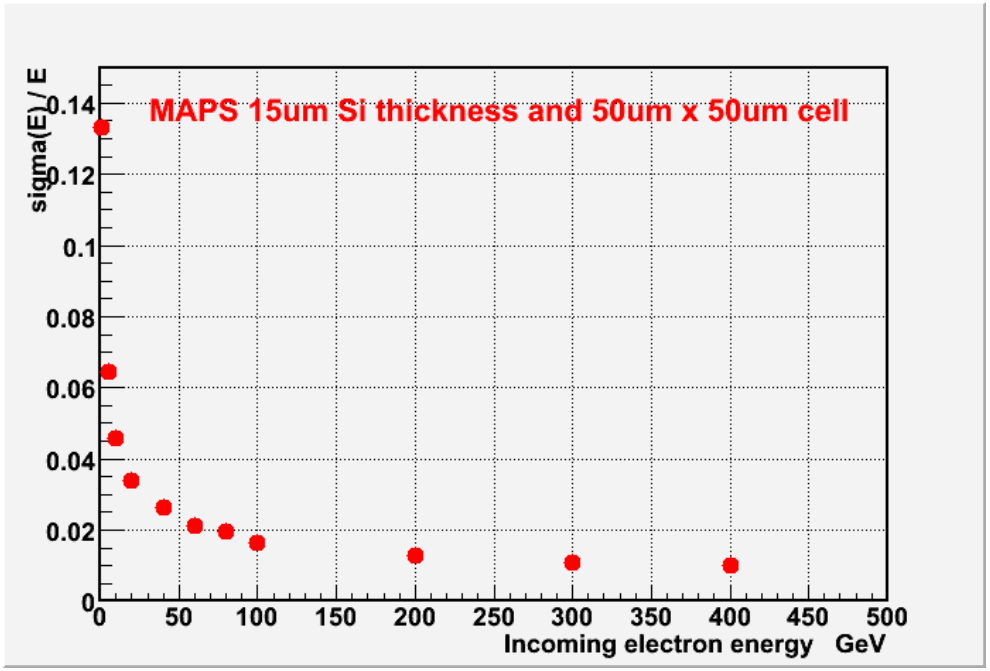
Linear Response

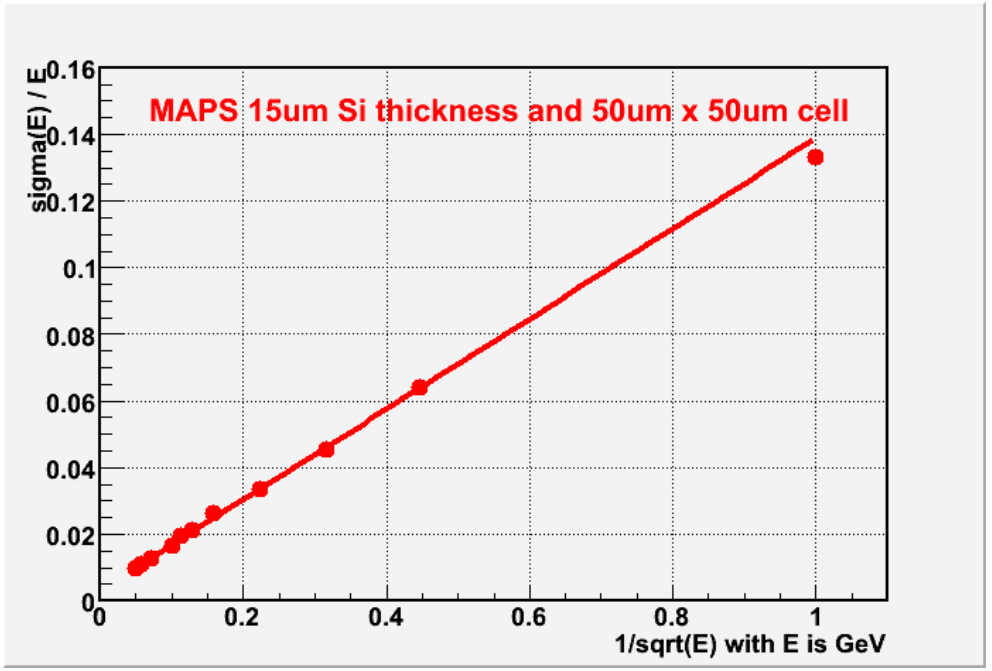


Linear response for electrons up to 400 GeV
GEANT4 level without charge diffusion

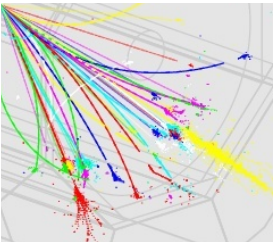


Resolution



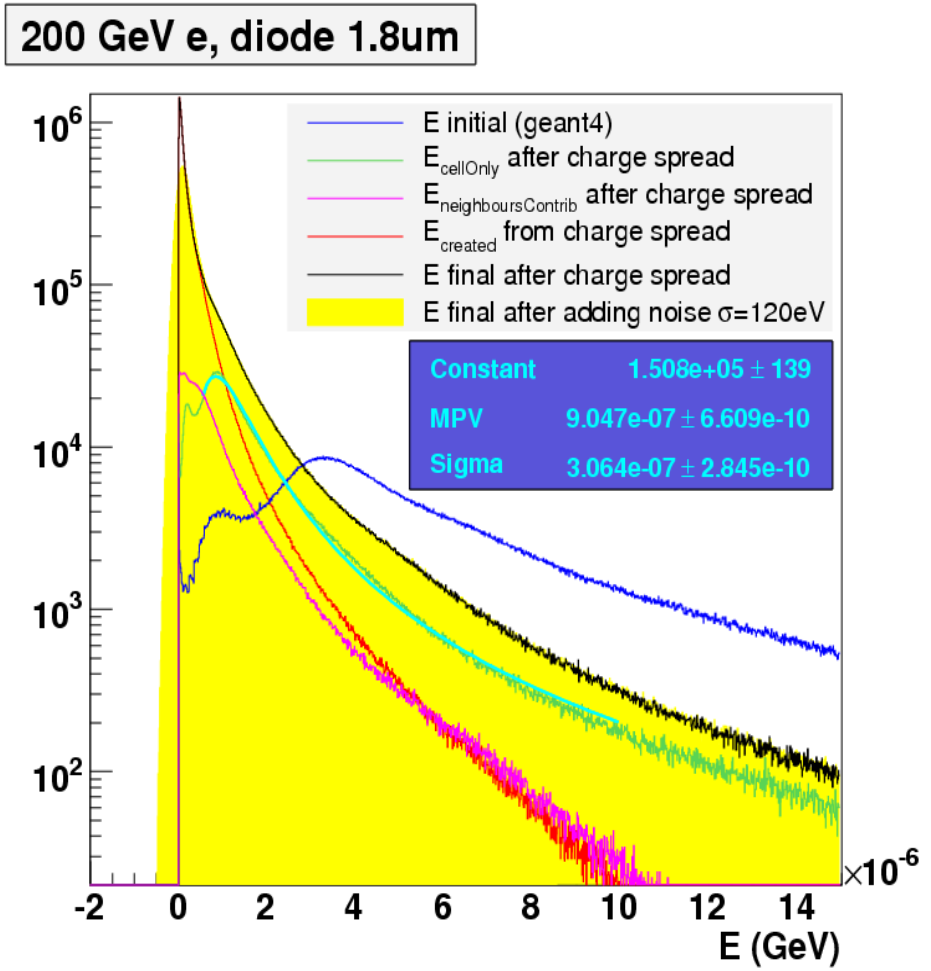


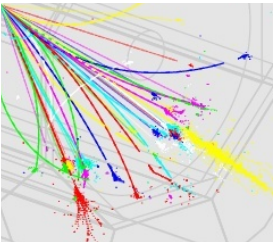
Good resolution over wide energy range
GEANT4 level without charge diffusion



First results

- Algorithm depends on accurate simulation input from Centaurus
- First results shows algorithm work nicely
- Does not take into account deep p-well yet
- Will be updated with the latest pixel simulations and noise estimates

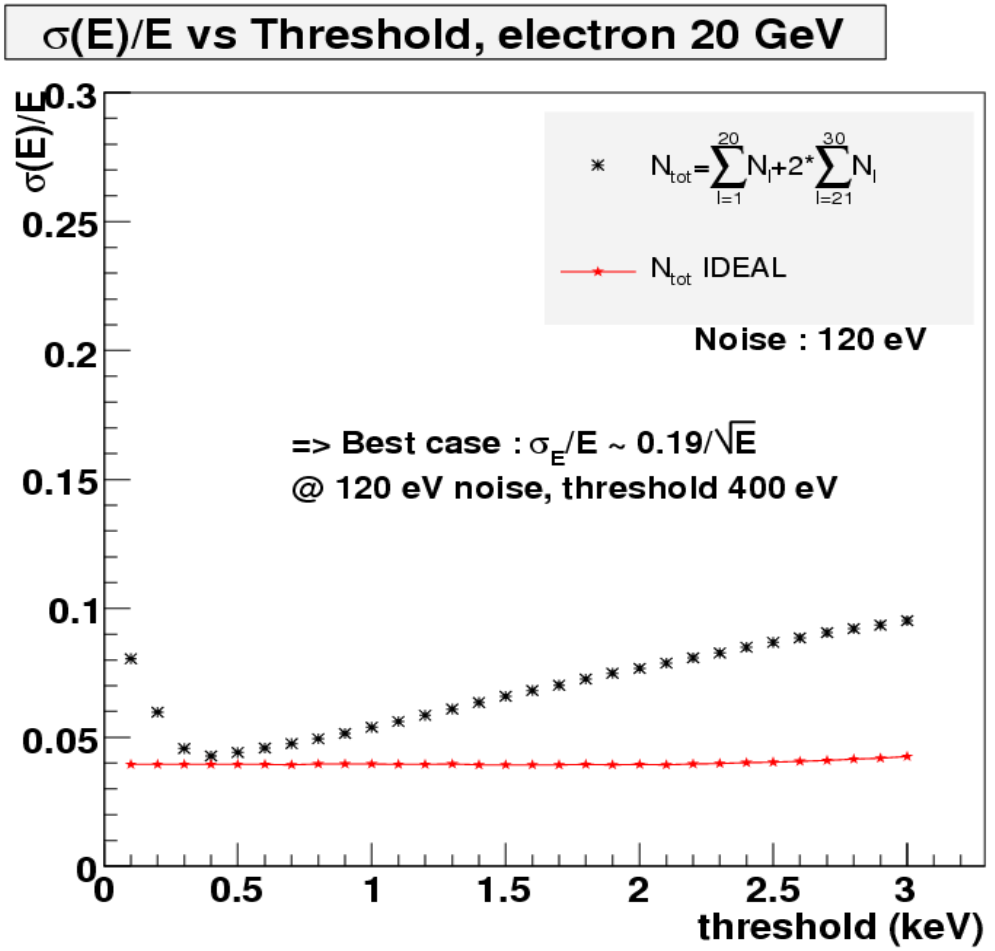


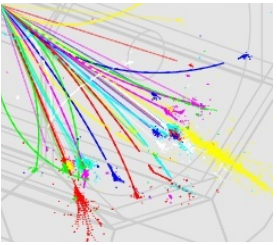


Hit weighting

Hit Counting:
Hit x 2 in the last 10 layers to account for the double tungsten thickness.

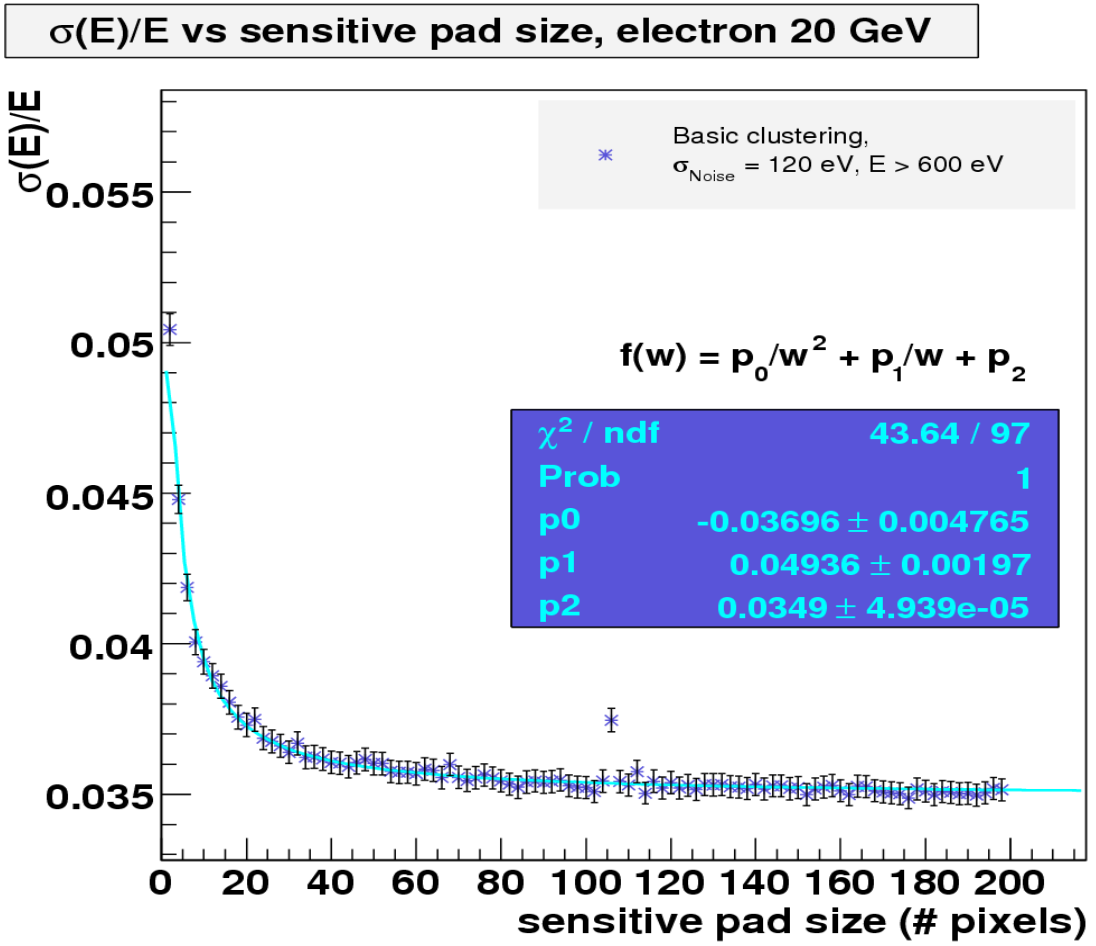
$$N_{tot} = \sum_{l=1}^{20} n_l + 2 \times \sum_{l=21}^{30} n_l$$





Dead area

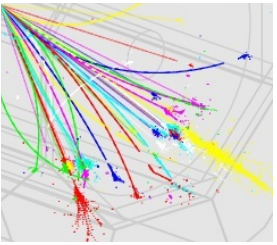
- We have an area of 5 dead pixels every 42 sensitive pixels for the logic strip.



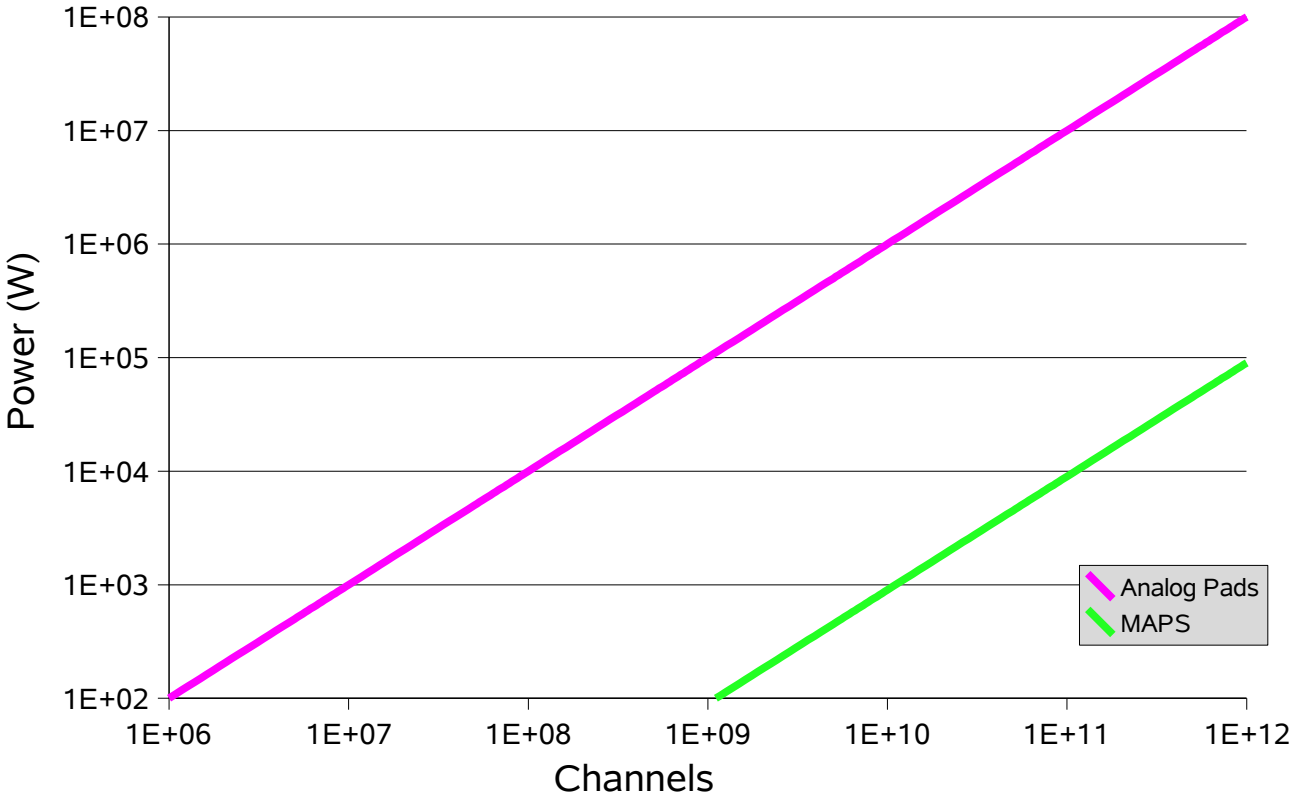
σ(E)/E = a/√E

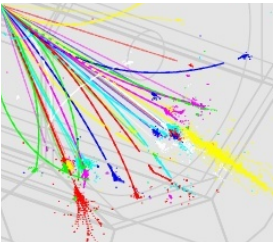
➔a = 0.1561 asymptotical value

➔a = 0.161 @ 42 sensitive pixels



Cooling cont'd





ILC configurations

	Nominal	Low Q	Large Y	Low P	High Lum	Nominal	Low Q	Large Y	Low P	High Lum
Ecms	500	500	500	500	500	1000	1000	1000	1000	1000
gamma	4.89E+05	4.89E+05	4.89E+05	4.89E+05	4.89E+05	9.78E+05	9.78E+05	9.78E+05	9.78E+05	9.78E+05
N	2.05E+10	1.05E+10	2.05E+10	2.05E+10	2.05E+10	2.05E+10	1.05E+10	2.05E+10	2.05E+10	2.05E+10
nb	2625	5120	2625	1320	2625	2625	5120	2625	1640	2625
Tsep [ns]	369.2	189.2	369.2	480.0	369.2	369.2	189.2	369.2	480.0	369.2
Buchets @ 1.3 GHz	480	246	480	624	480	480	246	480	624	480
Iave	0.0089	0.0089	0.0089	0.0068	0.0089	0.0089	0.0089	0.0089	0.0068	0.0089
Gradient	31.50	31.50	31.50	31.50	31.50	31.50	31.50	31.50	31.50	31.50
Cavities / 10 MW klys	26.00	26.00	26.00	26.00	26.00	26.00	26.00	26.00	26.00	26.00
Q0	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10	1.00E+10
Qext	3.60E+06	3.60E+06	3.60E+06	4.68E+06	3.60E+06	3.60E+06	3.60E+06	3.60E+06	4.68E+06	3.60E+06
Tbeam (us)	969.2	968.9	969.2	633.6	969.2	969.2	968.9	969.2	787.2	969.2
Tfill (us)	604.6	605.0	604.6	786.0	604.6	604.6	605.0	604.6	786.0	604.6
Trf (ms)	1.57	1.57	1.57	1.42	1.57	1.57	1.57	1.57	1.57	1.57