RPC-DHCAL Progress Report

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Argonne National Laboratory

SiD Workshop, FNAL, April 9 – 11, 2007

Staged approach

I R&D on RPCs
Concept of electronic readout system

→ **Tests with cosmic rays and in particle beams** — **Done**

II Prototyping of RPCs for prototype section (PS)
Prototyping of all components of electronic readout for PS

→ **Vertical slice test in particle beam** — **Planned for 6/2007**

III Construction of Prototype Section with RPCs

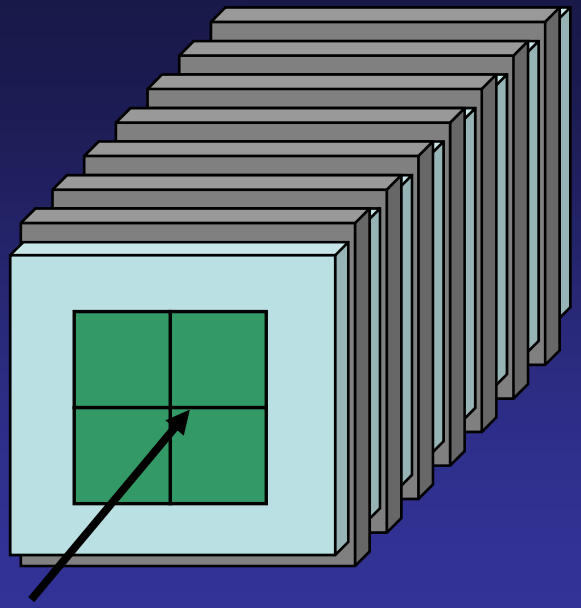
→ **Detailed test program in Fermilab test beam** — **Planned for 2008**

IV Further R&D on RPCs and electronic readout system — **Earliest in 2009**

V Scalable prototype

→ **Detailed test program in test beam** — **Earliest in 2010**

Vertical Slice Test



Uses the 40 DCAL ASICs from the 2nd prototype run

Equip ~10 chambers with 4 DCAL chips each

256 channels/chamber
~2500 channels total

Chambers interleaved with 20 mm copper - steel absorber plates

Electronic readout system (almost) identical to the one of the prototype section

Tests in MTBF beam planned for Spring 2007

→ Measure efficiency, pad multiplicity, rate capability of individual chambers
→ Measure hadronic showers and compare to simulation

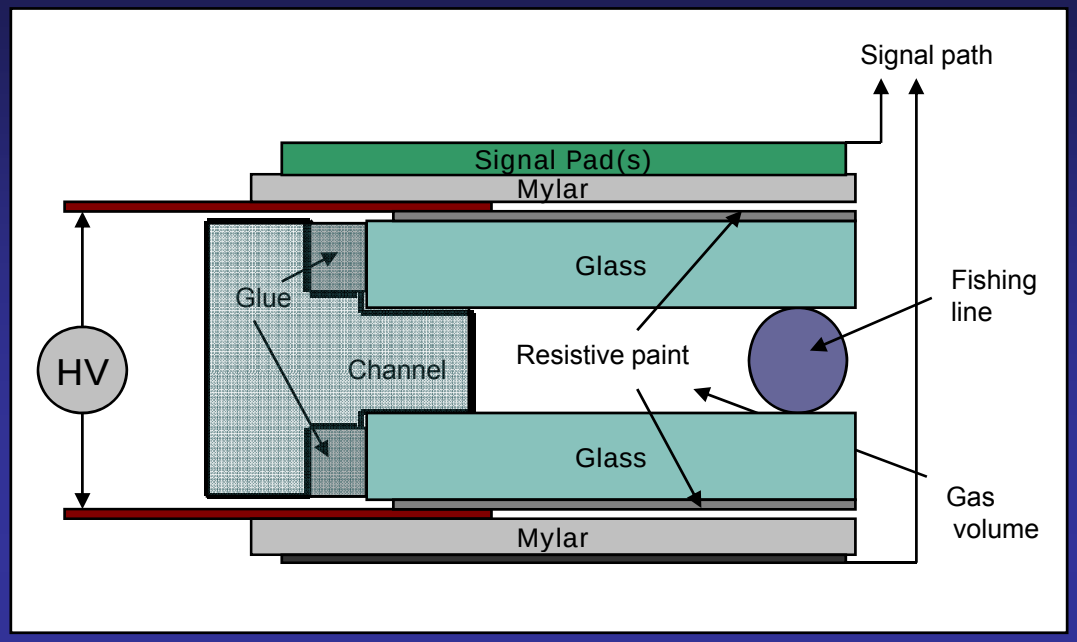
Validate RPC approach to finely segmented calorimetry
Validate concept of electronic readout

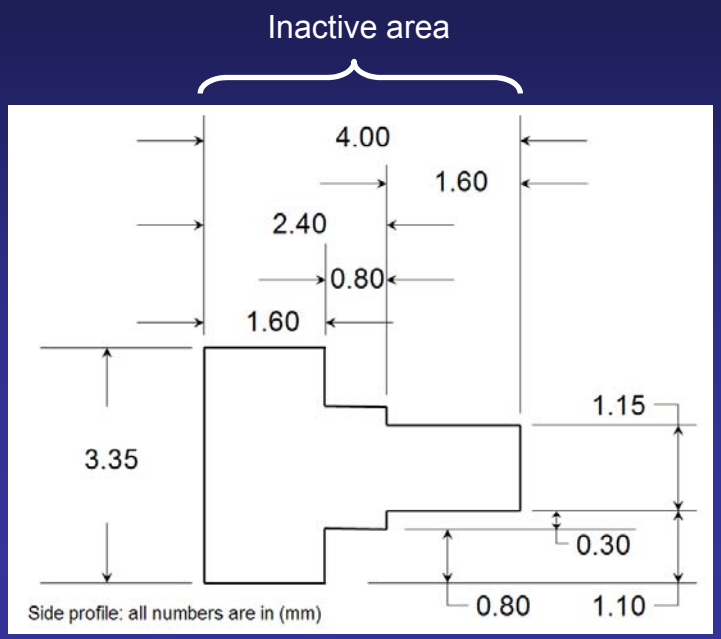
CALICE
Calorimeter for ILC

Responsibilities and collaborators

Task	Responsible institutes
RPC construction	Argonne, (IHEP Protvino)
Mechanical structure (slice test)	Argonne
Mechanical structure (prototype section)	(DESY)
Overall electronic design	Argonne
ASIC design and testing	FNAL, Argonne
Front-end and Pad board design & testing	Argonne
Data concentrator design & testing	Argonne
Data collector design & testing	Boston, Argonne
Timing and trigger module design and testing	FNAL
DAQ Software	Argonne, CALICE
Data analysis software	Argonne, CALICE
HV and gas system	Iowa
Beam telescope	UTA

RPC construction and testing

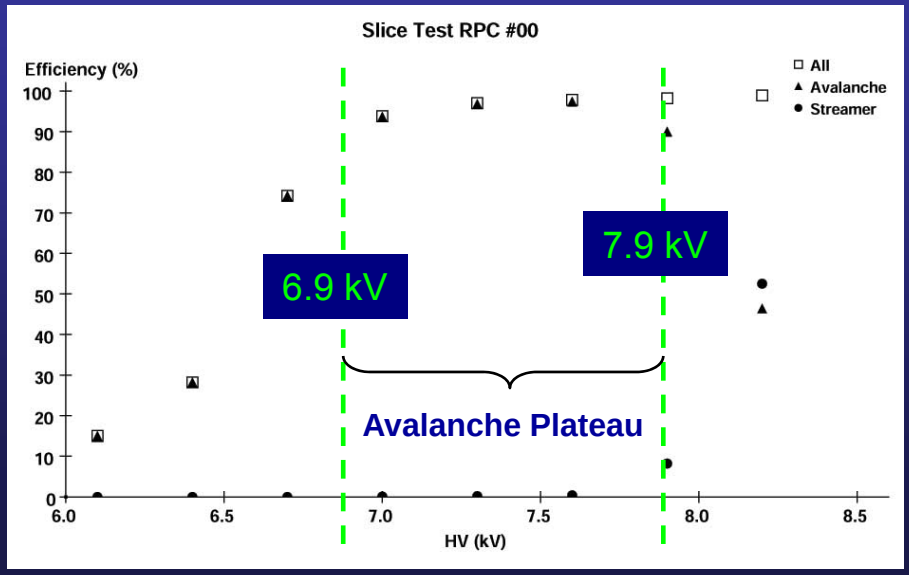




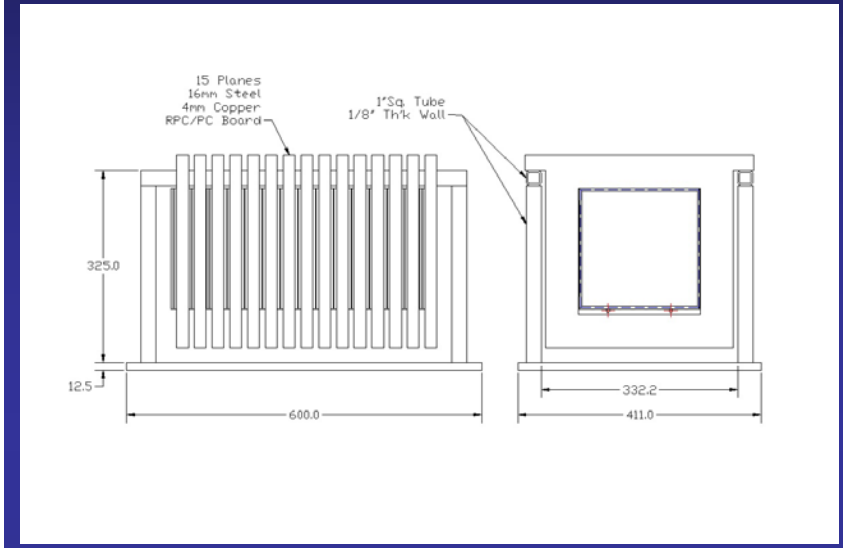
New design with simplified channels

1st chamber assembled and tested
→ Excellent performance
Thickness ~3.5 mm (w/out pads)
2nd chamber assembled and tested
→ Excellent performance
3rd – 6th chamber being assembled

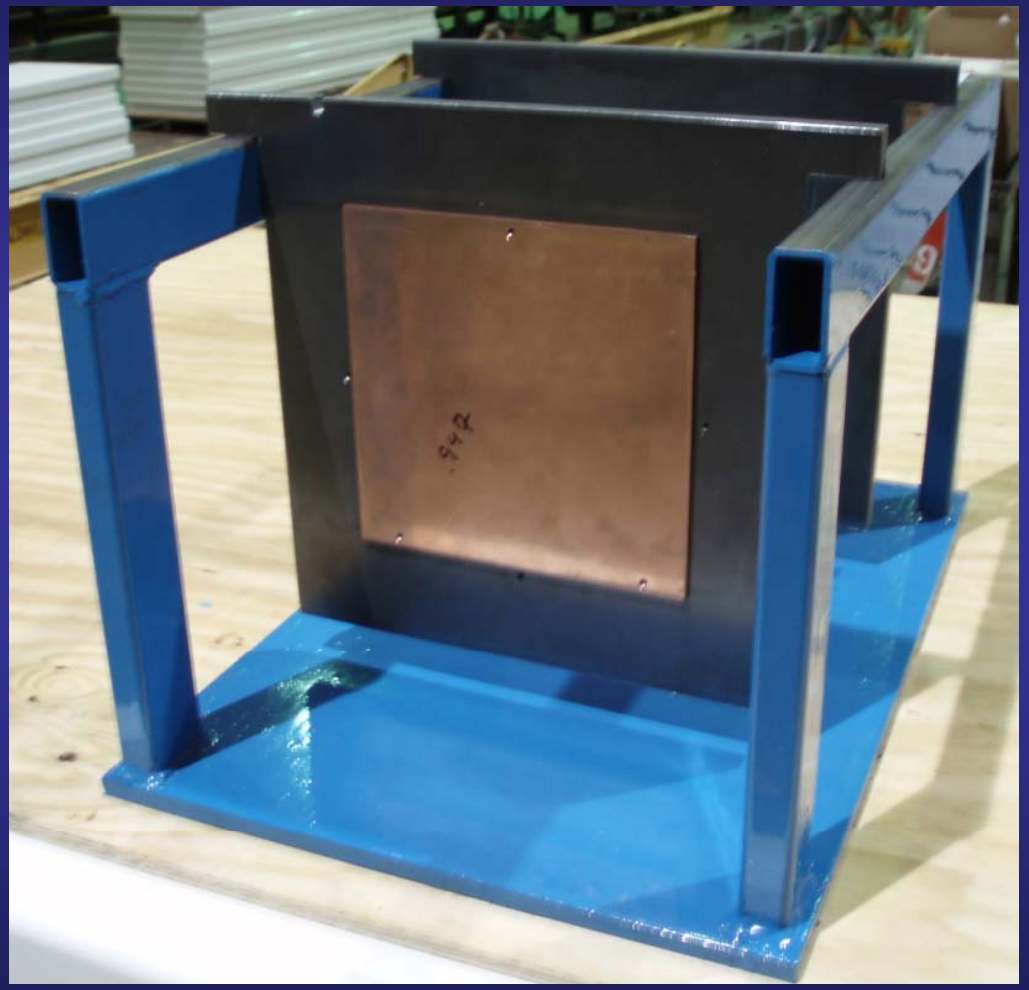
Material in hand for remaining chambers



Mechanical: Stack for Vertical Slice Test



Stack is assembled



Design accommodates 20 x 20 cm^2 RPCs as well as 30 x 30 cm^2 GEMs

Electronic Readout System for Prototype Section

40 layers à 1 m^2 → 400,000 readout channels

More than all of DØ in Run I

I Front-end ASIC

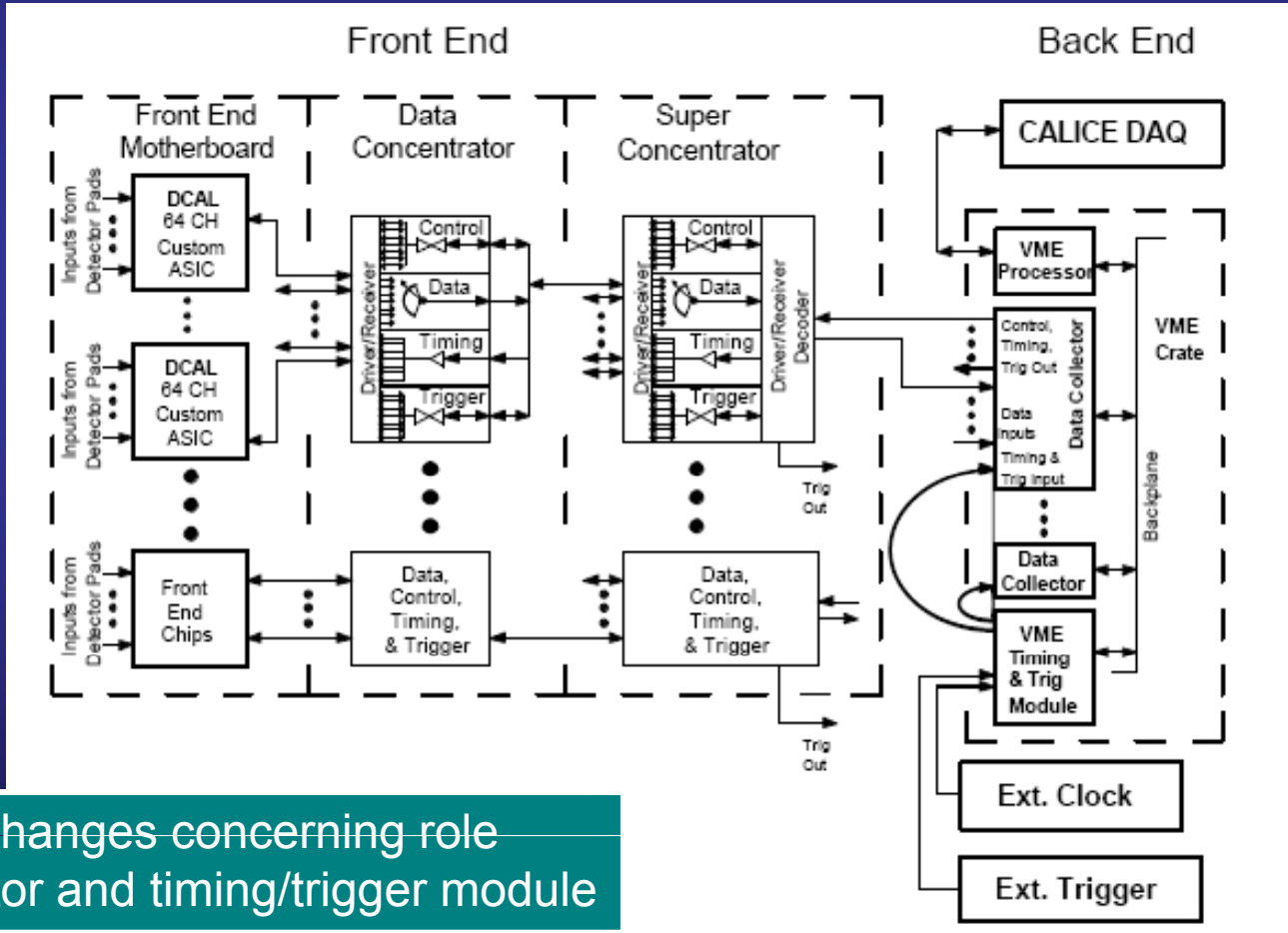
II Pad and FE-board

III Data concentrator

IV Super Concentrator

V VME data collection

VI Trigger and timing system



Some recent changes concerning role of data collector and timing/trigger module

DCAL chip

Design

→ chip specified by Argonne
→ designed by FNAL

1st version

→ extensively tested with computer controlled interface
→ all functions performed as expected

Redesign

→ decrease of gain by factor 20 (GEMs) or 100 (RPCs)
→ decoupling of clocks (readout and front-end)

2nd version

→ submitted on July 22nd
→ 40 chips (packaged) in hand

Test board

→ redesign of test board (changes in pin layout etc.) complete
→ boards fabricated
→ chip mounted on test board

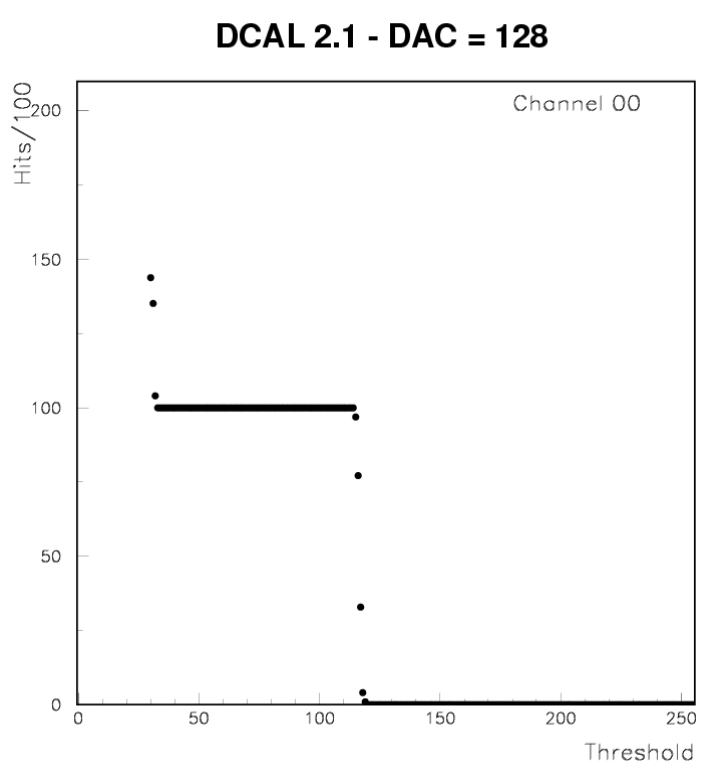
Testing (1/40)

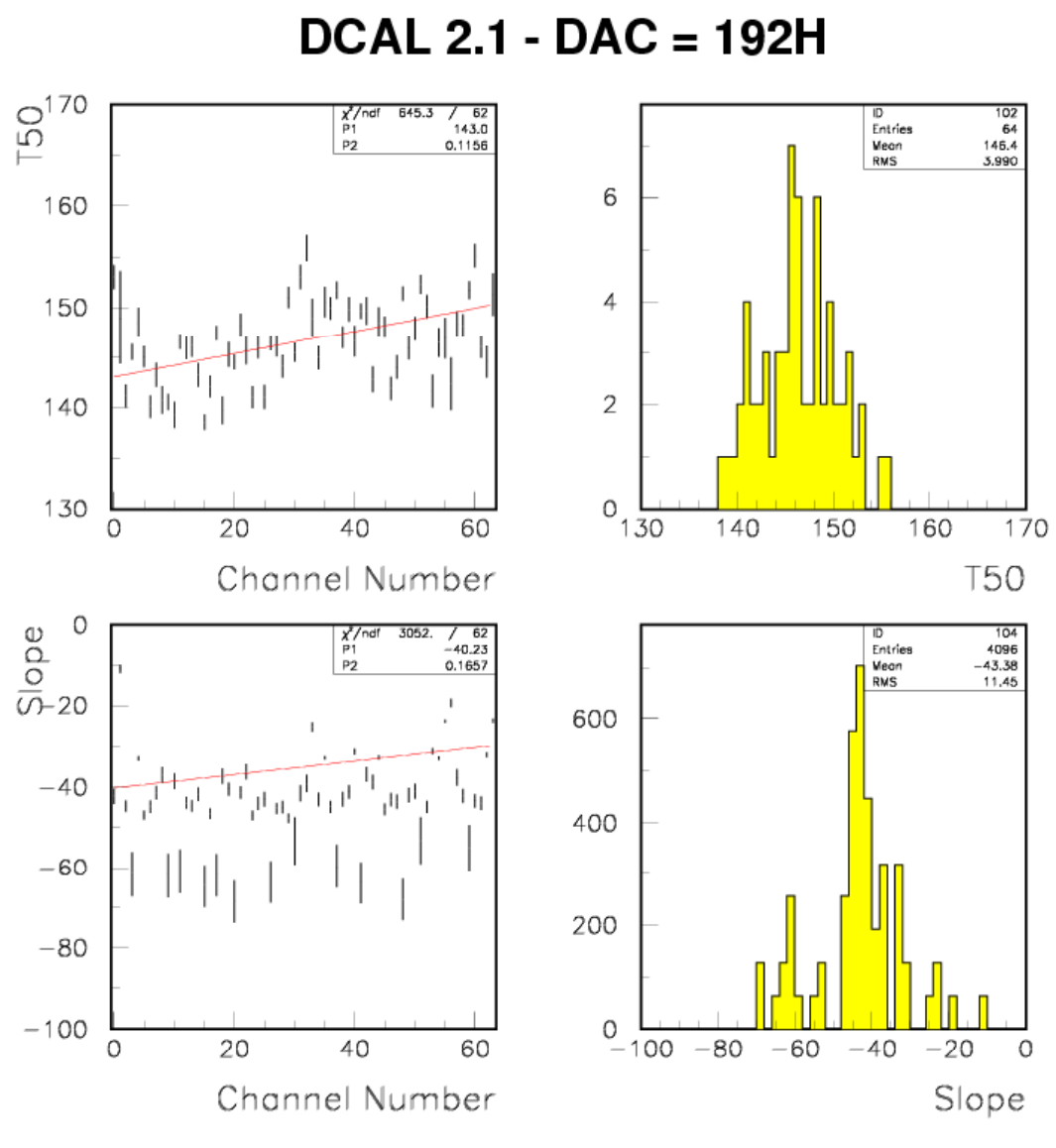
→ tests ~completed

Reads 64 pads
Has 1 adjustable threshold
Provides
- Hit pattern
- Time stamp (100 ns)

Operates in
- External trigger or
- Triggerless mode

DCAL2 Testing I: Internal pulser

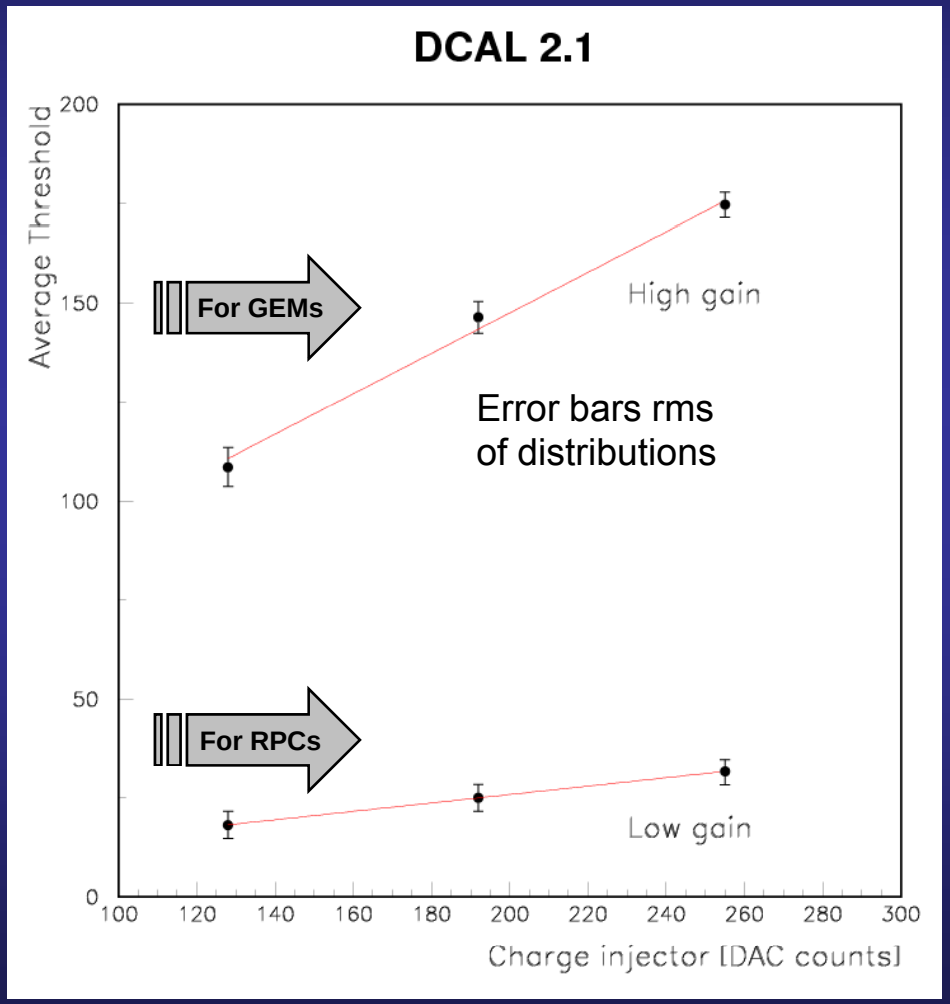




Threshold scans…

All channels OK, except
Channels #31/32 show some anomalies
(understood, no problem)

DCAL2 Testing II: Internal pulser

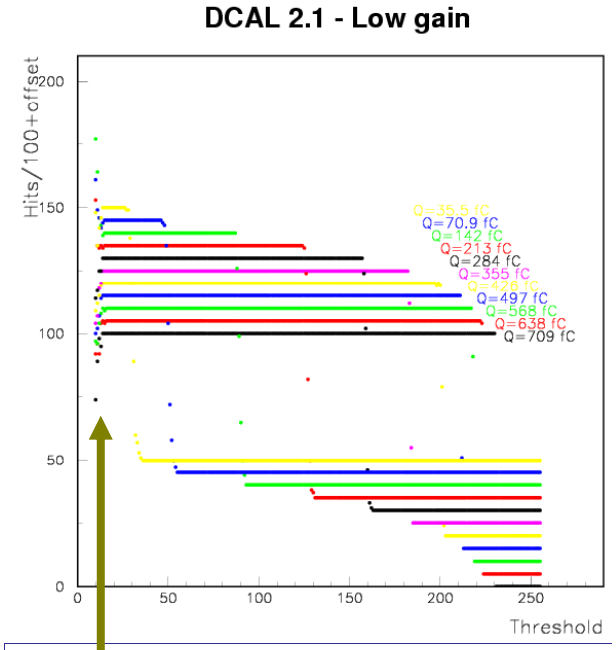


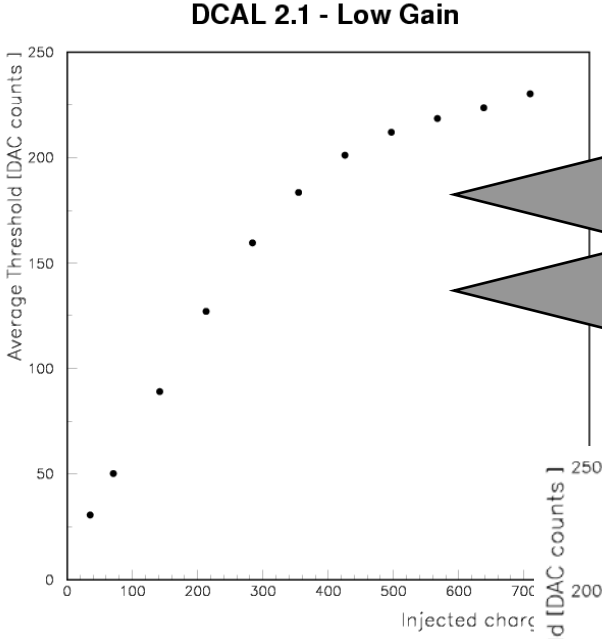
Ratio of high to low gain

R = 4.6 ± 0.2

(roughly as expected)

DCAL2 Testing III: External pulser



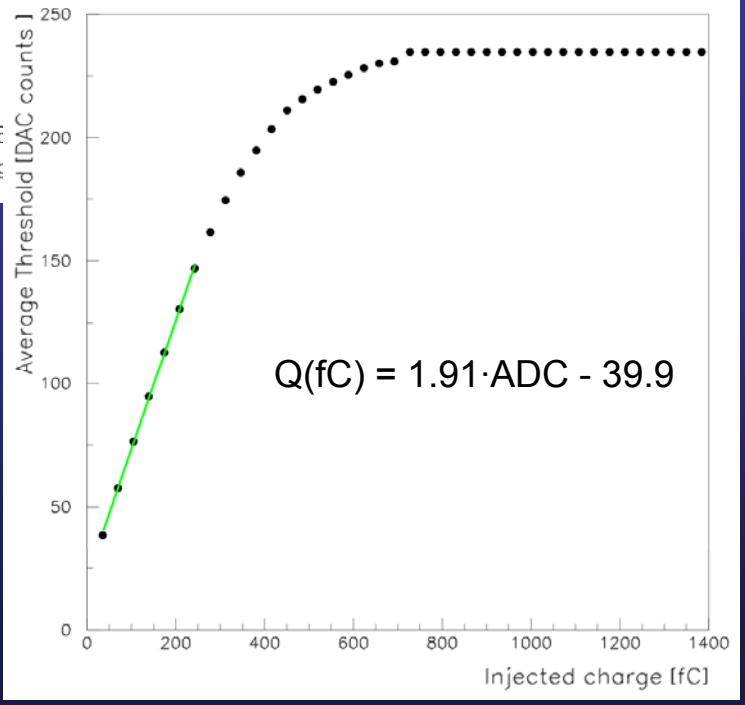


Linear up to ~300 fC

Range up to ~700 fC

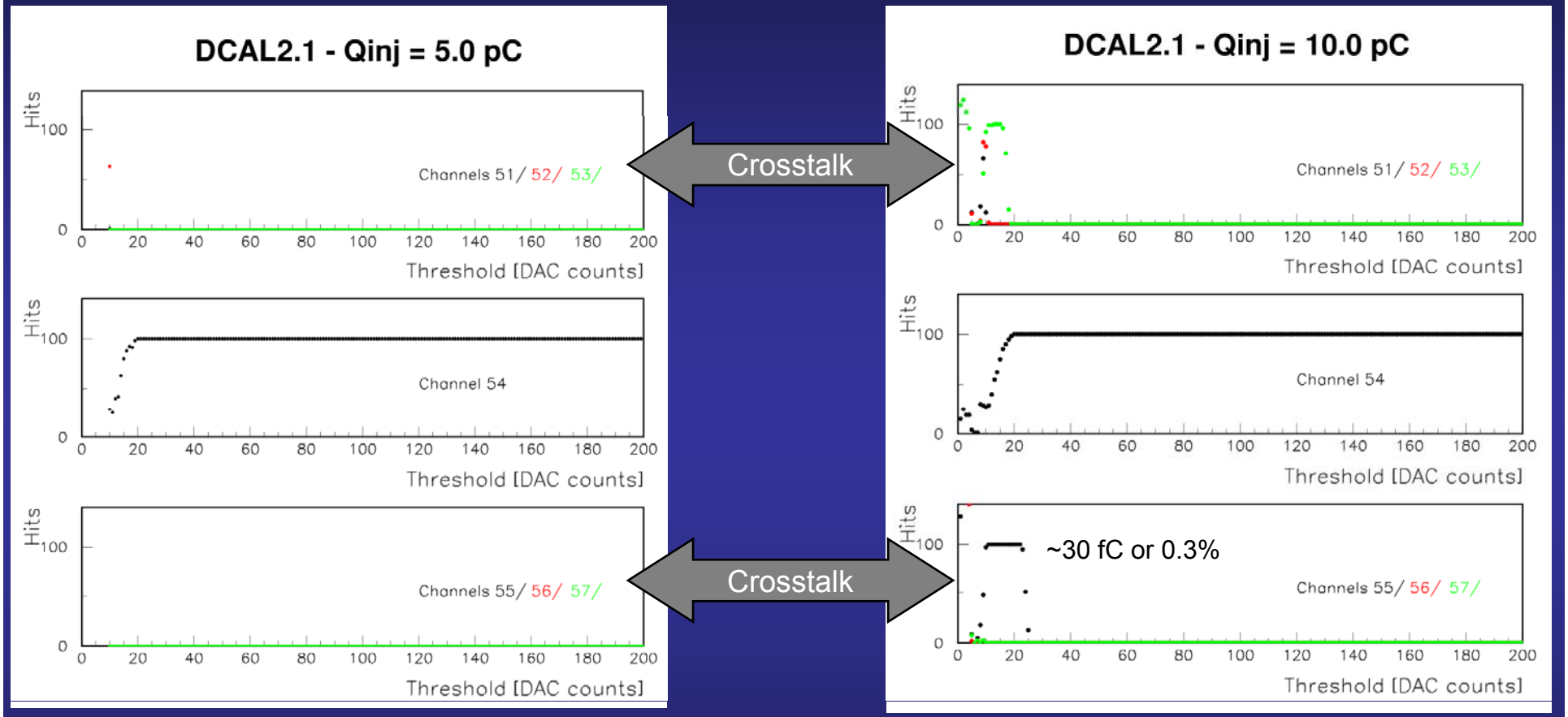
(RPC: Q = 100 fC ÷ 10 pC)

Corresponds to zero charge
(Offset in charge)



100 hits per point
Average threshold defined as ε=50% point

DCAL2 Testing IV: external pulser

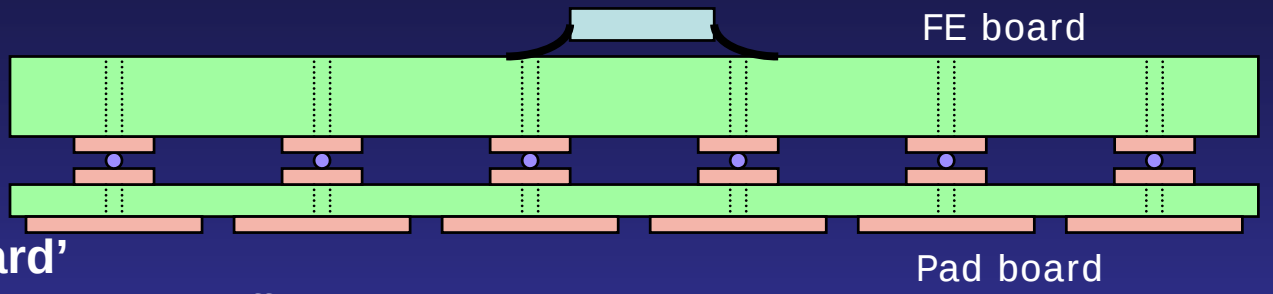


Chips can be used for vertical slice test

Small modifications still necessary for production

Pad- and Front-end Boards I

New Concept

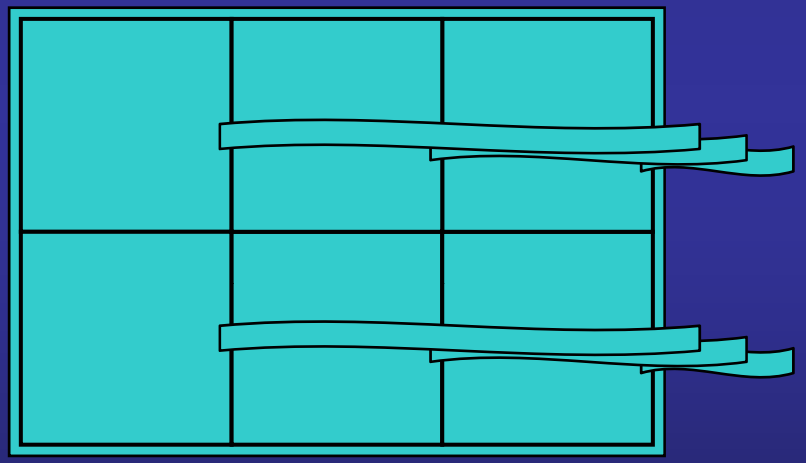


Split old 'Front-end board'

'front-end board' highly complex and difficult
blind and buried vias + large board => (almost) impossible to manufacture
split into two boards to eliminate buried vias

Pad boards

four-layer board containing pads and transfer lines
can be sized as big as necessary
relatively cheap and simple
vias will be filled



Front-end boards

eight-layer board
16 x 16 cm^2
contain transfer lines, houses DCAL chips
expensive and tough to design

Connections

board to board with conductive glue on each pad
cables for connection to data concentrators

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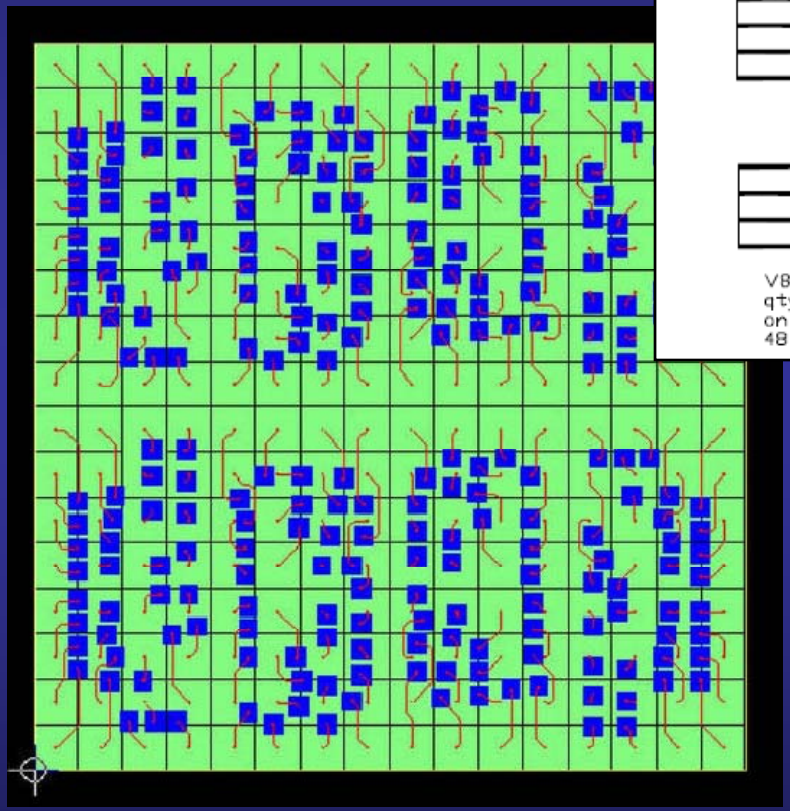
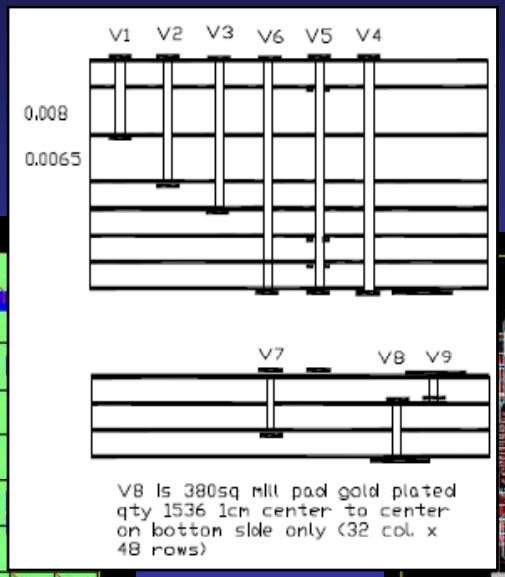
CALICE Calorimeter for ILC

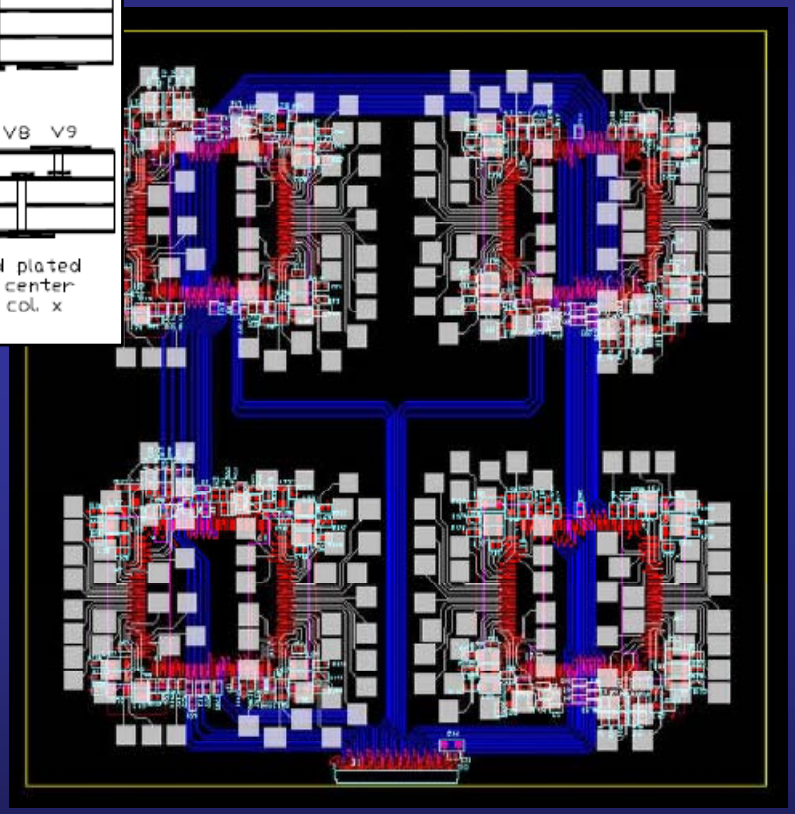
Pad- and Front-end Boards II

4-layer Pad-board





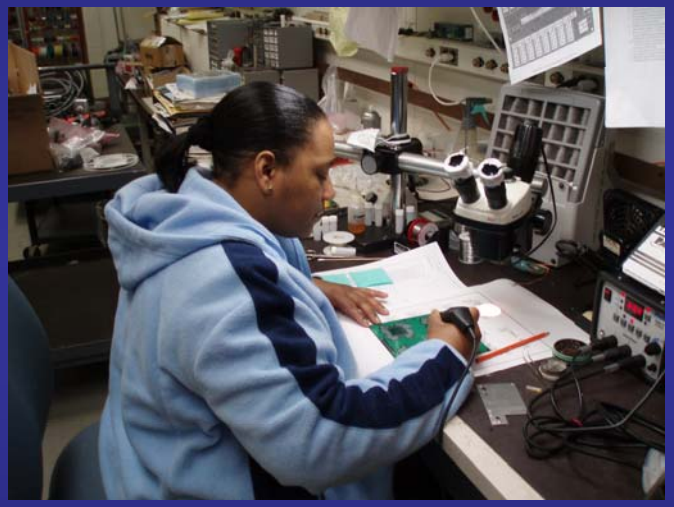
8-layer FE-board
All (almost) layers

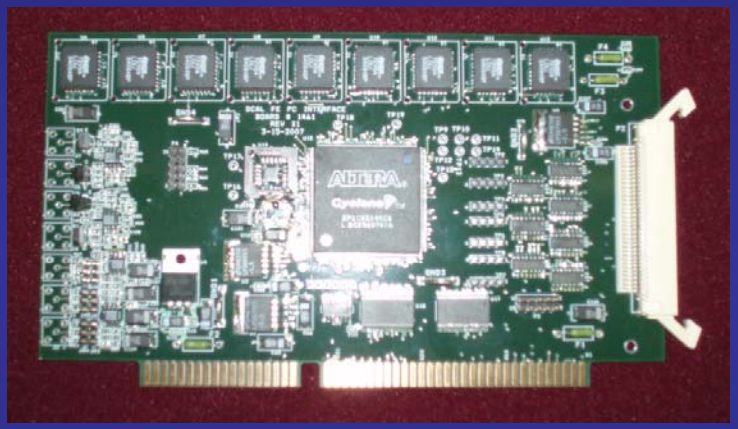


Design completed
→ most intricate so far by Argonne group

Pad- and Front-end Boards III

Front-end board: fabricated and (partly) assembled
Test-board (computer interface): fabricated and assembled
Testing software: to be adapted from previous DCAL2 tests





Tests to start this week

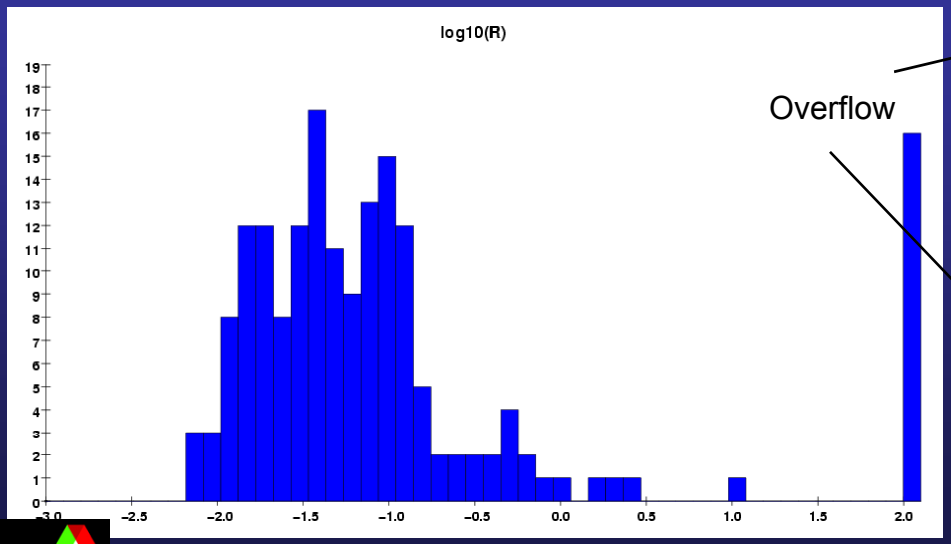
Pad-board: design completed
Fabrication: received *reasonable* quotes

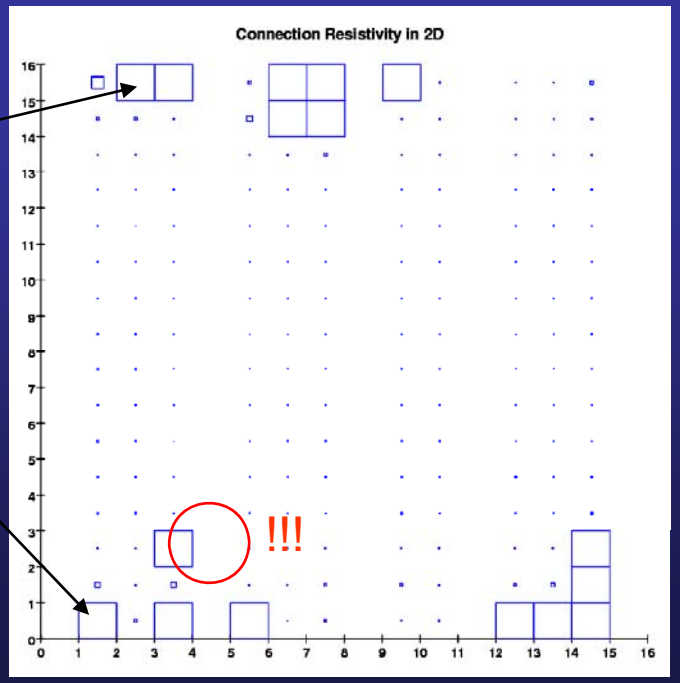
Waiting for OK from Front-end board

Gluing Tests

Performed test with test boards
Glued two boards to each other
→ strips of mylar for constant gap size

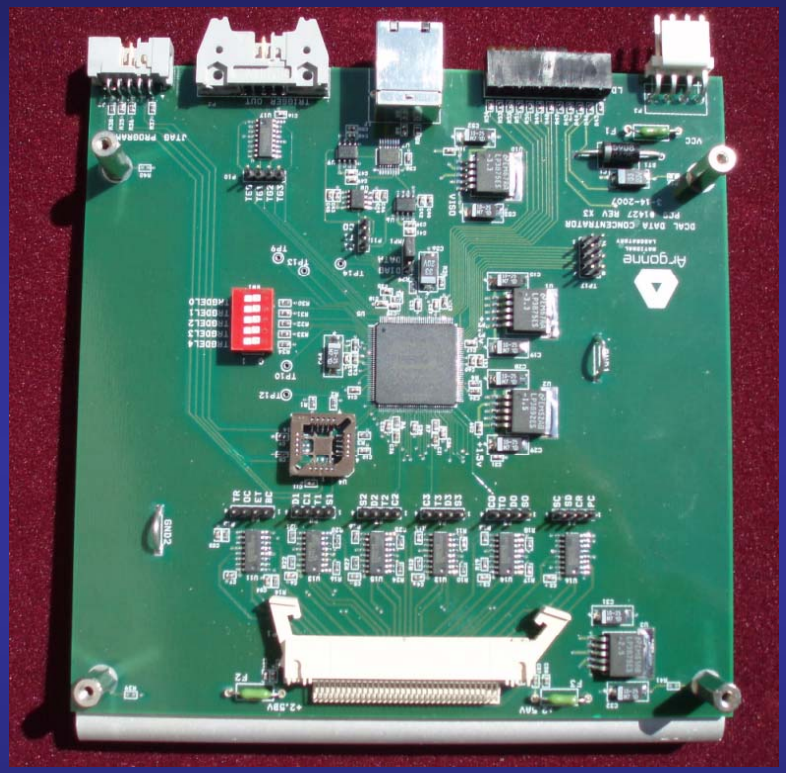
Resistance <~0.1 Ω
Glue dots small (~2 mm) and regular
Edges lifted off → non-conductive epoxy

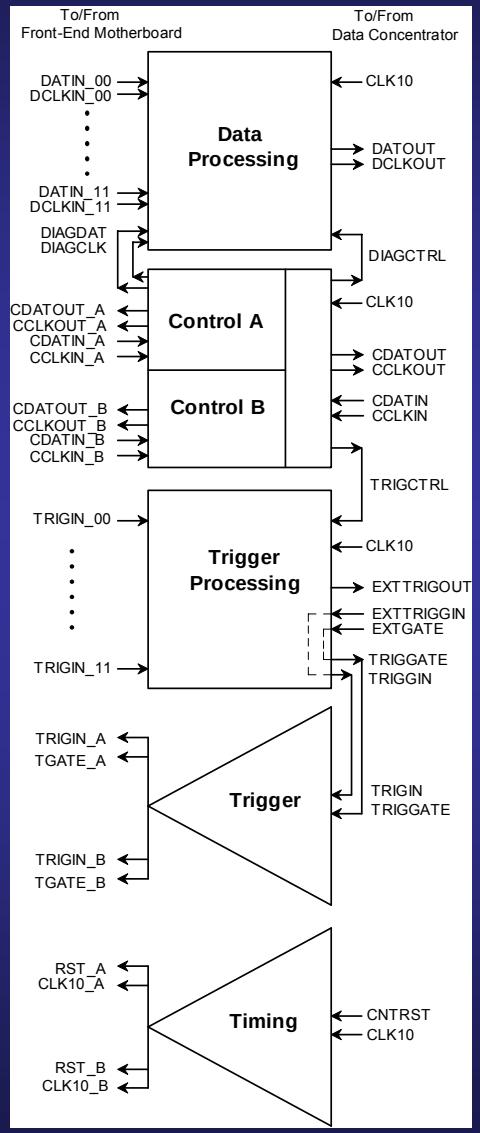




Data concentrator boards

Design completed
Boards fabricated
1/10 board assembled





Test board fabricated
Will be assembled today…

Timing and trigger module

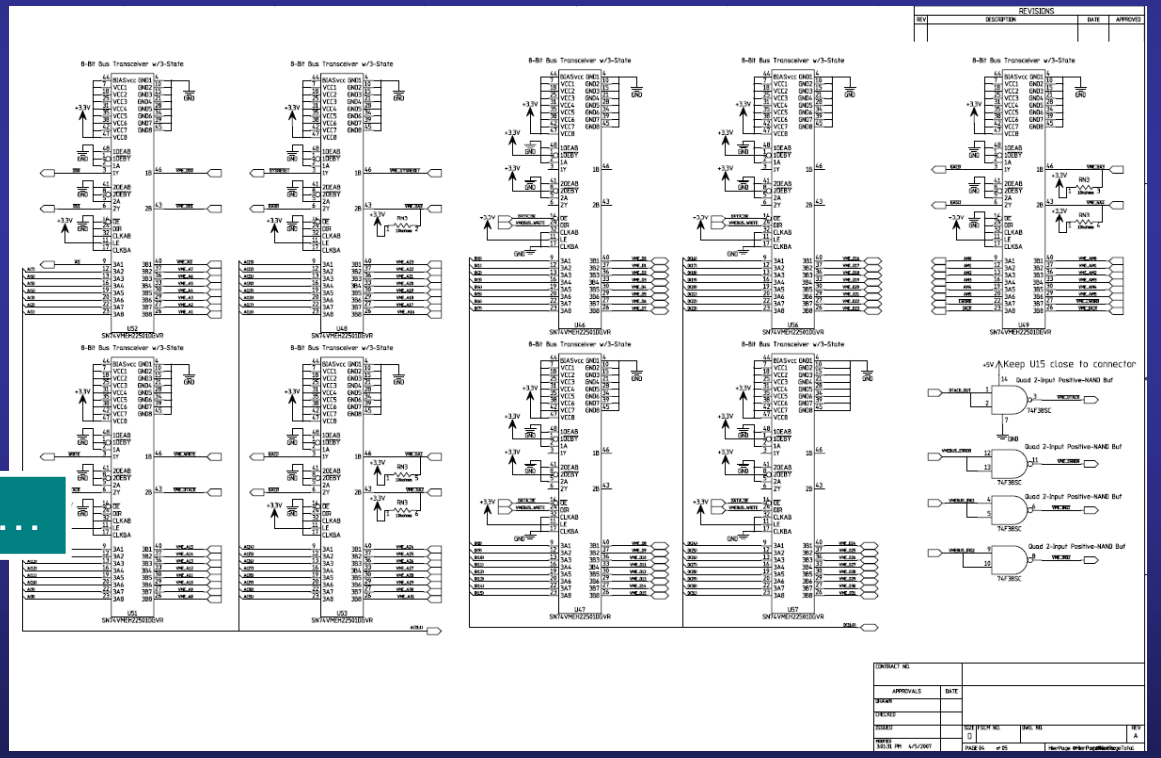
Provides clocks and trigger signals
to individual DCOL boards

Schematic completed

Need 1 module for both the

Vertical Slice Test and the
1 m^3 Prototype Section

Board layout starting today…



Data collector boards

E Haz

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Functionality

Receives data as packets

Timestamp (24 bits) +
Address (16 bits) +
Hit pattern (64 bits)

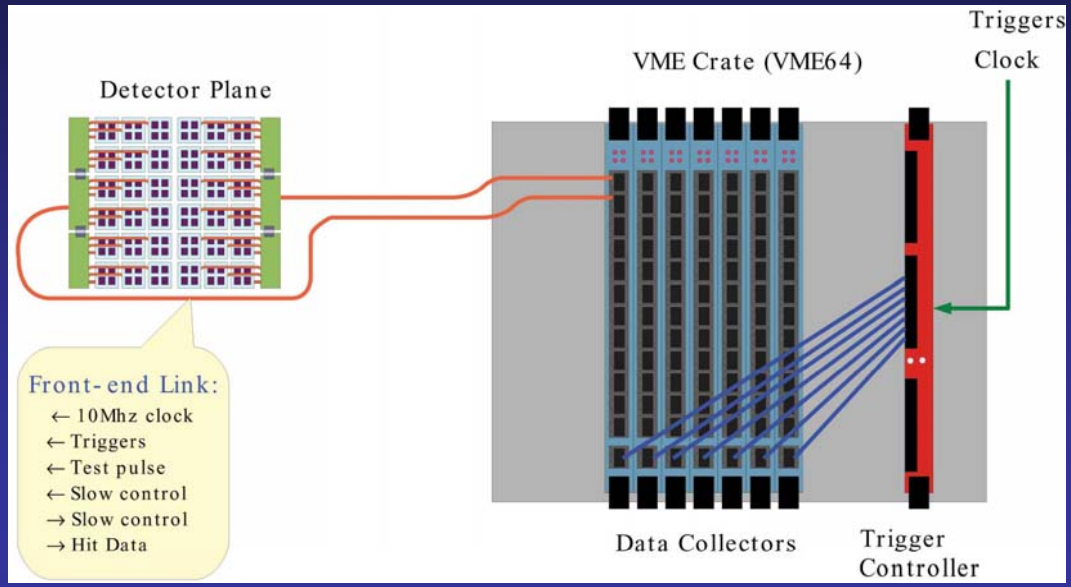
Groups packets in buffers
(by matching timestamps)

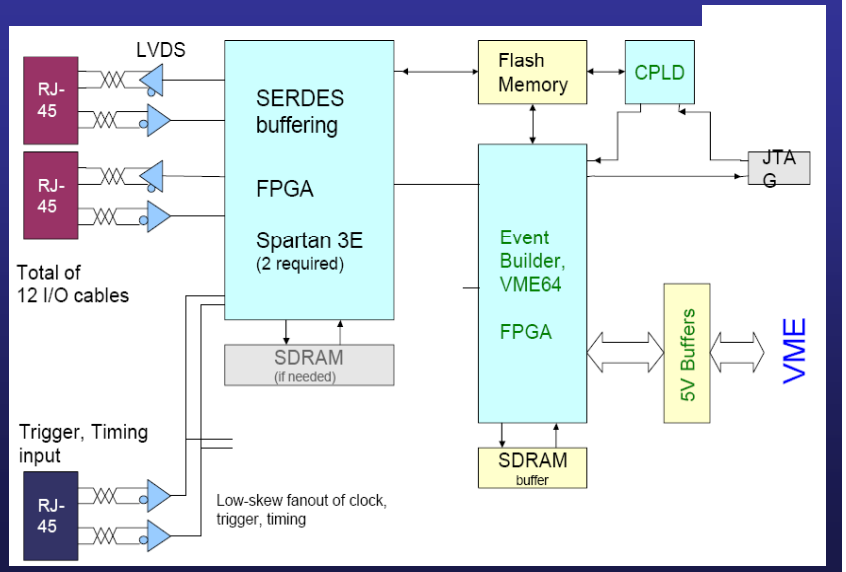
Makes buffers available for VME transfer

Monitors registers (scalars)

Provides slow control of front-end

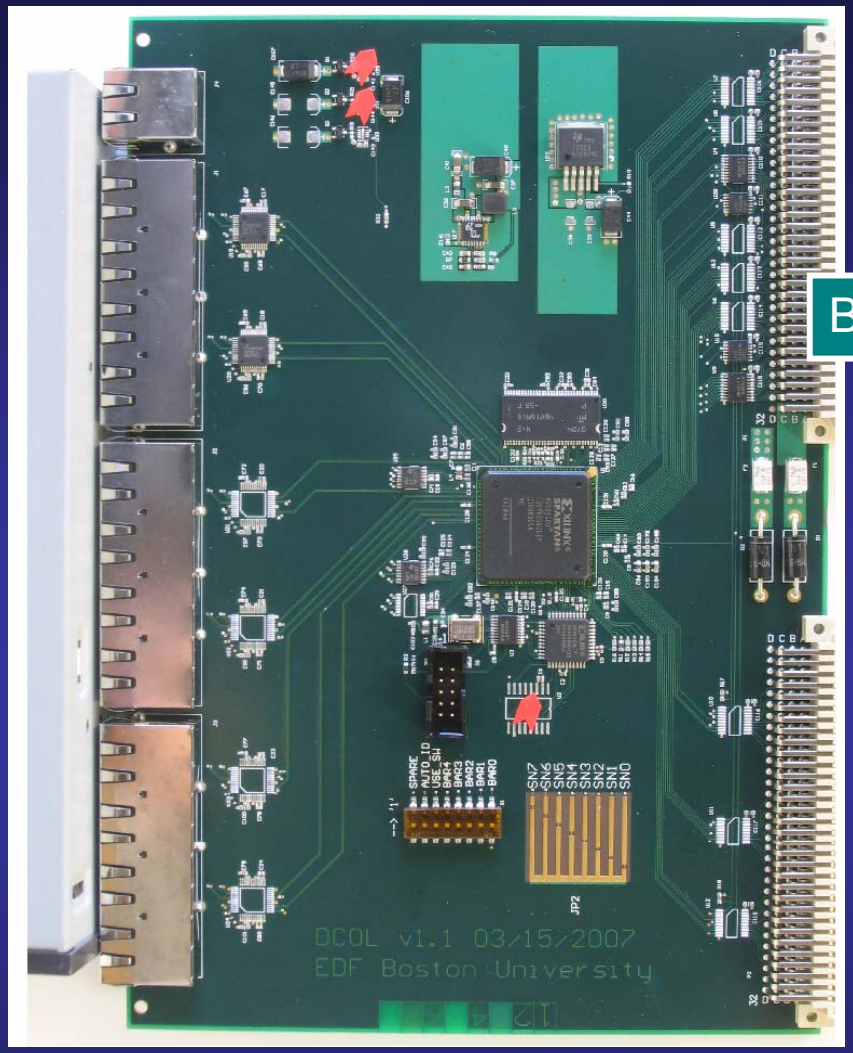
Allows read/write to DCAL chips or
data concentrator boards





Need

1 unit for Vertical Slice Test
7 units for Prototype Section



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CALICE Calorimeter for ILC

Board fabricated and assembled

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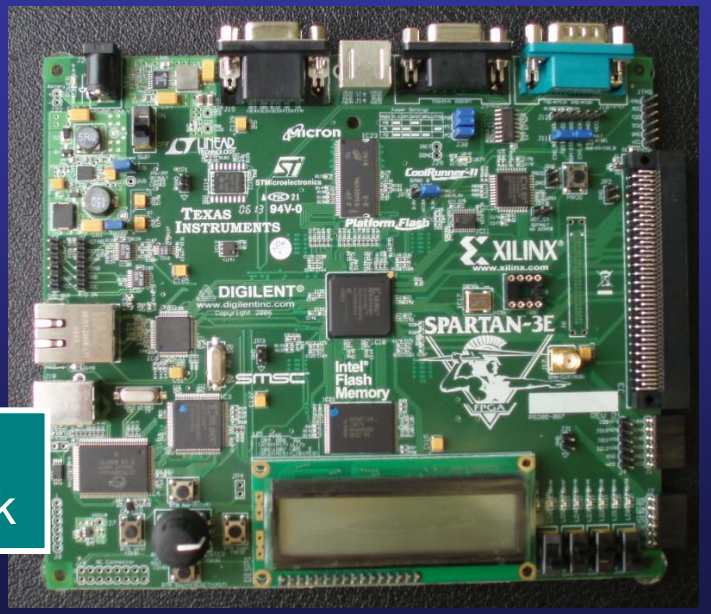
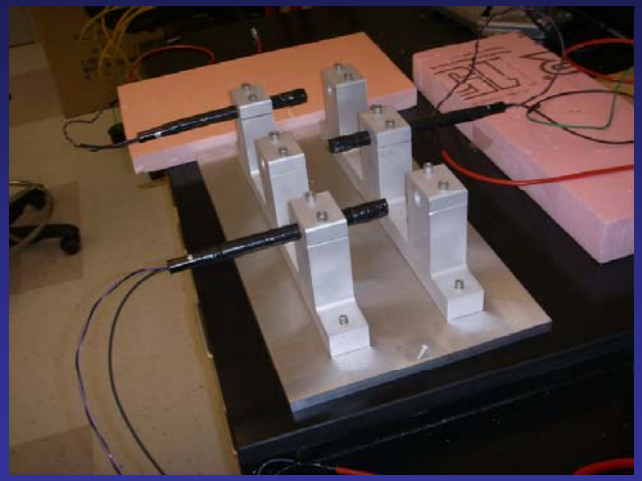


Test board purchased
Testing software ready this week

Beam telescope, HV, and gas



Beam telescope

6 counters (3 x (1 x 1 cm^2) + 1 x (4 x 4 cm^2) + 2 x (19 x 19 cm^2)
Mounted on rigid structure
Counters and trigger logic tested → A.White

HV modules

Need separate supplies for each chamber
Modules (from FNAL pool) being tested

With additional RC-filter perform similarly to our Bertan unit in analog tests (RABBIT system)
Digital tests satisfactory too

Gas system

Need manifold for 10 chambers (in hand!)
Will purchase pre-mixed gas (quote in hand)

DAQ software

Based on

VME hardware interface and PCI-VME interface
CERN HAL library
CALICE DAQ framework (→ combined data taking)
ROOT running on CERN Linux OS

Two configurations

Vertical Slice Test with 10 x 4 ASICs or 2560 channels
Prototype Section with 40 x 144 ASICs or 400k channels

Data archived for offline analysis

Contains: run metadata, hit patterns &
addresses & timestamps
Configuration data stored in SQL database
Data will be converted to LCIO format

DAQ software will be used

For hardware debugging
In cosmic ray and charge injection tests
In FNAL test beam

Status

HAL based testing and debugging system running
Toy version of CALICE DAQ running with *old* VME hardware

Next steps

Define operations for new hardware
Define data structure (binary files)
Define data structure (offline)

Well advanced…

Data Analysis

For Vertical Slice Test only

I Online histograms

Important in debugging phase
Part of CALICE DAQ software
DHCAL specific plots to be added

Σ_{all}hit versus time
Σhit versus chamber
2dhisto of chamber hits (all layers)
2dhisto of chambers hits (per layer)
{Chamber efficiency and pad multiplicity}

II Analysis of binary files

Important in debugging phase
Event display (to be adapted from CALICE-AHCAL)
Track segment finder

III Conversion to LCIO

Standard for LC data bases
Conversion to be done by CALICE expert
(not urgent for VST, but necessary for later tests)

Programming will start soon…

Track Segment Finder

Loops over layers 1 - 8
Loops over hits in layer i
Determines #neighboring hits N_i
Searches for aligned hits in layer i+2,3,4,5
Determines #neighboring hits around aligned hit

N_{i+2}, N_{i+3}, N_{i+4}, N_{i+5}
(N_j = 0 …no aligned hits)

Looks for aligned hits in layer i+1
Determines #neighboring hits N_{i+1}

Efficiency of layer i+1

$$\frac{N_{i+1}>0.\text{and.}N_{i+2}>0(\text{.and.}N_{i+3}>0)}{N_{i+2}>0(\text{.and.}N_{i+3}>0)}$$

Pad multiplicity of layer i+1

N_{i+1}, for N_i=1.and.N_{i+2}=1(.and.N_{i+3}=1)

Component	February	March	April		May		June
ASIC	Complete testing Provide new packing scheme Order 40 additional				Test	Test with cosmic rays	Move to MT6 Test in test beam
Gluing	Test with regular epoxy	Test with conductive epoxy	Develop gluing procedure Test with real boards Glue all boards				
Pad boards	Specify dimensions Complete design		Order for RPCs				
Front-end boards	Complete design Order 15	Fabricate Assemble	Test	Test			
Interface board **(to test FE-boards + ASIC)**	Complete design	Fabricate Assemble					
Data concentrator		Complete design Fabricate Assemble	Test				
Data concentrator test board		Complete design Fabricate Assemble					
Data collector	Complete design Acquire crates	Fabricate Assemble	Test				
Data collector test board		Acquire Write software					
Timing & trigger module	Discuss with FNAL	Design	Fabricate Assemble Test				
Software	Acquire PC	Complete standalone development (with 'old' VME card)	Complete development with DCOL				
RPCs	Complete #1	Test #1 Test #2	Buil#3-6 Test #3-6		Build #7-10 Test		
Offline	Propose concept	Develop plan	Write software				

Comparisons…

Identical

	VST	PS	ILCD
RPCs	20 x 20 cm^2	32 x 96 cm^2	Variable
DCAL chips	64 inputs No power pulsing	64 inputs No power pulsing	> 64 inputs???
Front-end boards	4 ASICs/board No optimization in thickness/cost	4 ASICs/board No optimization in thickness	>4 ASICs/board Token rings?
Pad boards	16 x 16 cm^2	32 x 48 cm^2	Variable
Data concentrator	Input = 4 ASICs	Input = 12 ASICs	?
Super concentrator	Not used	Input = 6 Data concentrator	?
Data collector	12 inputs	12 inputs	?
Timing module	1 unit	1 unit	?
HV	1/chamber	1/3 chambers	?
Gas lines	1/chamber	1/3 chambers?	?

Conservative design

Some optimization

Highly optimized

Conclusions

Going full speed!!!

- Vertical slice test

Concentrated effort with monthly meetings (whole effort)
weekly meetings (ANL group)

All parts coming together (no apparent late comer)

Goal Cosmic ray test sin May 2007
Measurements in test beam in June 2007

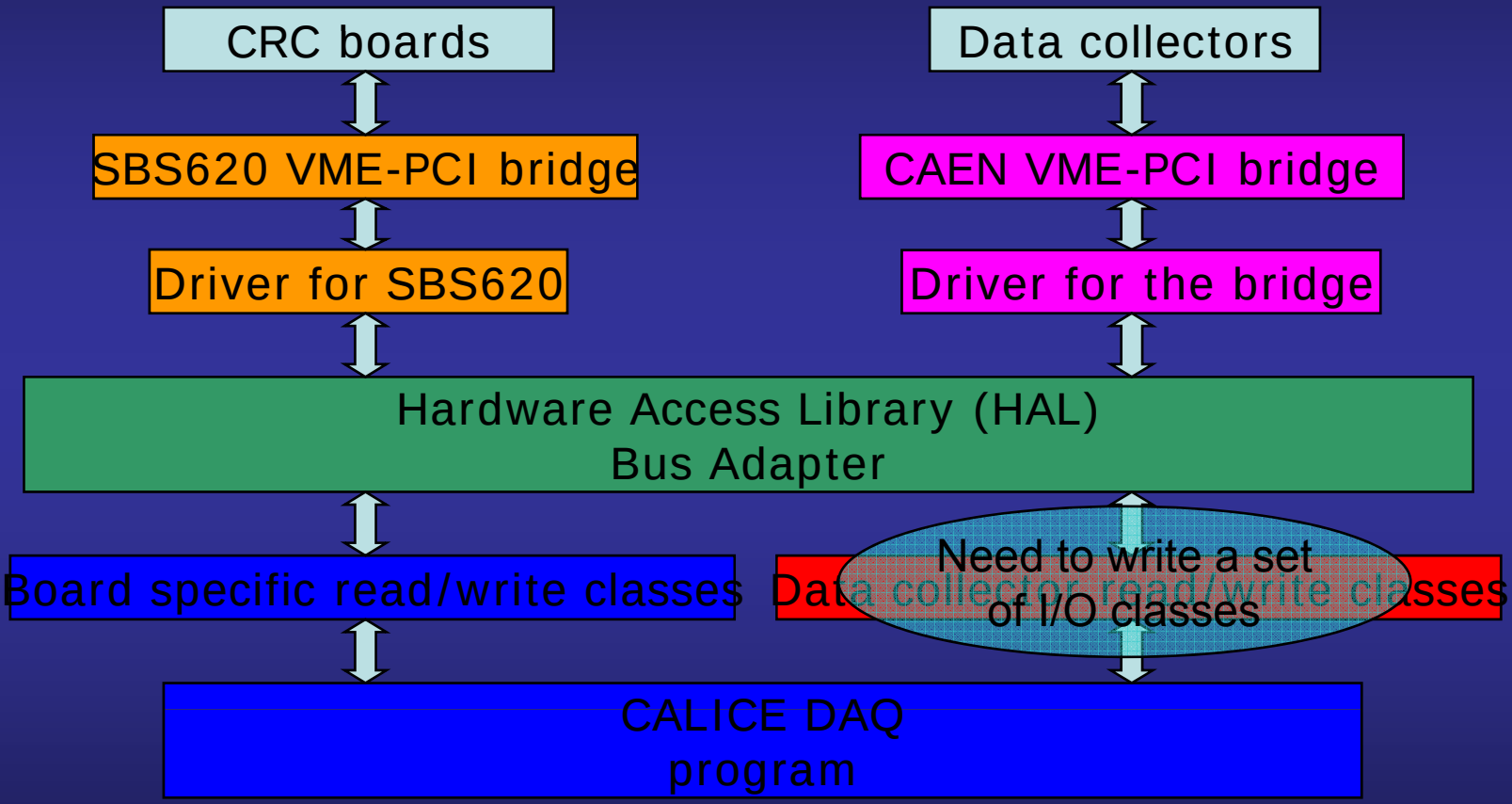
- Prototype section

Expensive! (New revised cost estimate soon)
Funding appears possible
Goal → RPC stack in 2008

Backup Slides

DAQ software

Particular challenge to be compatible with CALICE software



CALICE

Slice test

Programming effort started

Funding

LCRD funds for 2006

RPCs (ANL, Boston, Chicago, Iowa)	$98k
GEMs (UTA, Washington)	$60k

Supplemental LCRD funds for 2006/7

Available funds $1,200k/year?

Submitted pre-proposal for RPC/GEM DHCAL

Requested $1,200k for 2006
~$800k for 2007

2006	build RPC-DHCAL continue R&D on GEMs
2007	test RPC-DHCAL at MTBF build GEM stack
2008	test GEM-stack

DOE asked us to submit proposal for $500k/year (done)

Costs and Funding

A) Slice test is funded by LCDRD06, LDRD06 and ANL-HEP, and Fermilab funds

B) Prototype section not yet funded, but…

Stack	Item	Cost	Contingency	Total
RPC stack	**M&S**	607,200	194,600	801,800
	Labor	243,075	99,625	342,700
	Total	**850,275**	**294,225**	**1,144,500**
GEM stack*	**M&S**	400,000	165,000	565,000
* Reusing most of the RPC electronics	**Labor**	280,460	40,700	321,160
	Total	**680,460**	**205,700**	**886,160**
Both stacks	**M&S**	1007,200	359,600	1366,800
	Labor	523,535	140,325	663,860
	Total	**1,530,735**	**499,925**	**2,030,660**

Proposal for supplemental funds for $500k/year over two years submitted to DOE
Help from ANL (LDRD), ANL-HEP, FNAL expected…