# CCD-based Pixel Detectors by LCFI

Andrei Nomerotski (U.Oxford) on behalf of LCFI collaboration
SiD workshop, Fermilab April 2007

## Outline

- CCD Sensors and Readout
  - Column-Parallel CCDs
  - Storage Pixels : ISIS
- Mechanical Studies

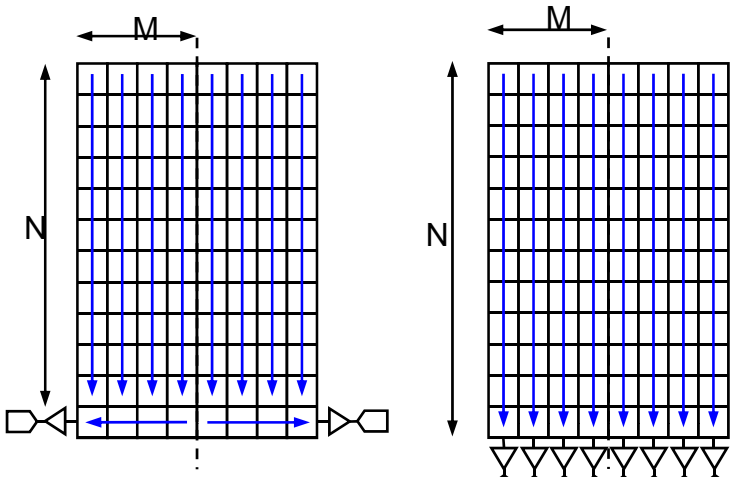
# Column Parallel CCD

- Simple idea : read out a vector instead of a matrix → Readout time shortened by orders of magnitude

BUT

- Every column needs own amplifier and ADC → requires readout chip
- Need to operate at 50 MHz to meet readout rate spec → 20 Amp clock current

Driving of CPCCD is a major challenge




**"Classic CCD"**
Readout time ≈ $N \times M/f_{out}$

**Column Parallel CCD**
Readout time = $N/f_{out}$

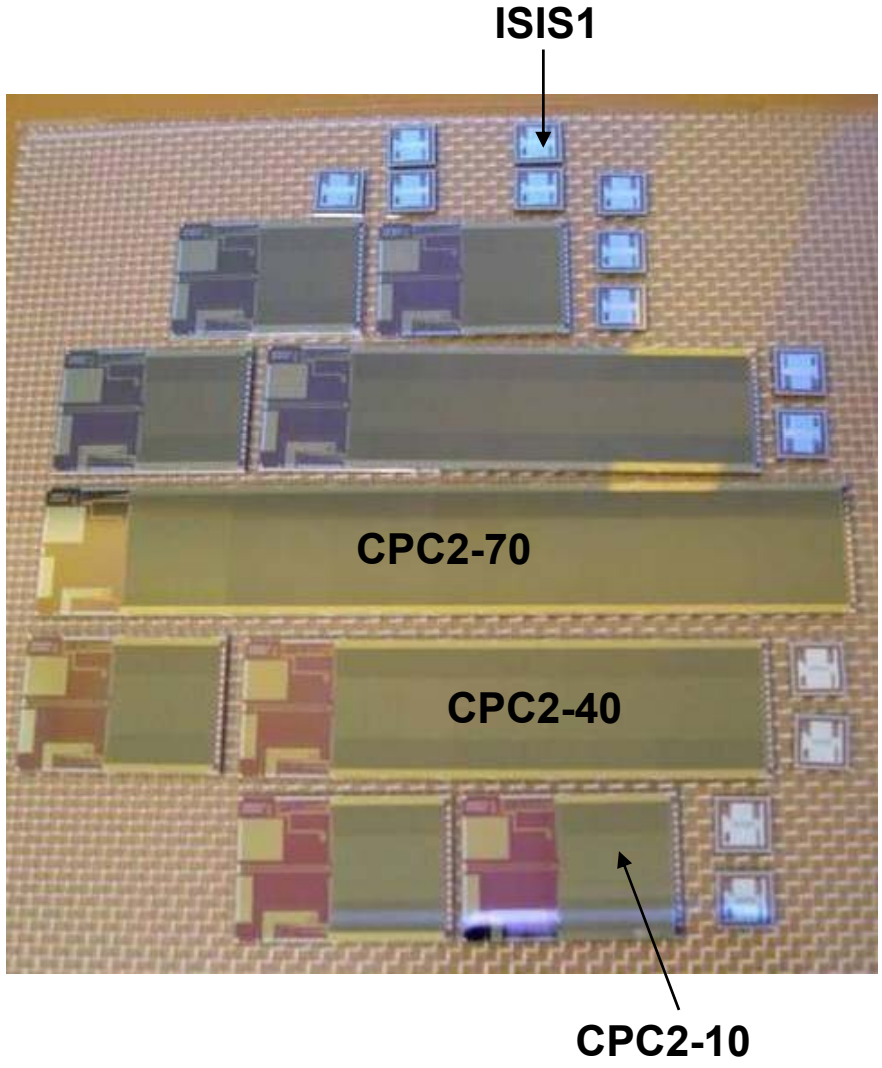
- Voltage drops 20 A x 0.1 Ohm = 2 V
  - Inductance of 1mm long bond wire = 1 nH, corresponds to 0.3 Ohm at 50 MHz

# CPCCD : LCFI R&D Milestones

- Established proof of principle for small area sensors : CPC1
- Established proof of principle for readout chip : CPR1 developed and produced more sophisticated CPR2

- Moved on to large area sensors : CPC2
  - Produced and tested busline free high speed CPC2
  - Testing of CPC2/CPR2 assemblies
  - Need to handle the problem of clock driver
  1. Design dedicated clock driver : CPD1
  2. Find ways to reduce the CCD capacitance
  3. Find ways to reduce the required clock voltage

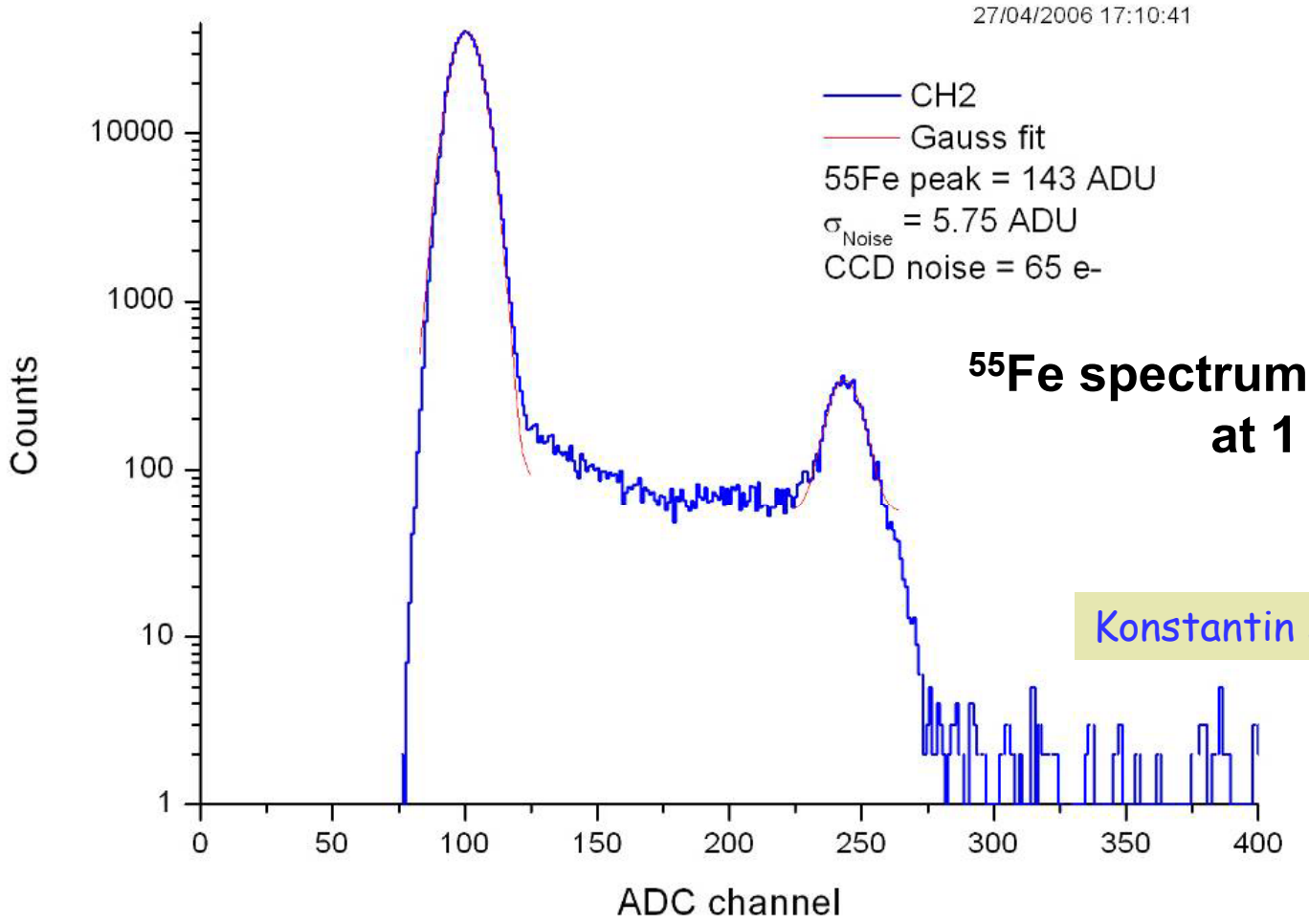
# Second Generation CPCCD : CPC2




- 6 wafers with single level metal:
  - Four CPC2 wafers (3 × 100 Ω.cm/25 µm epi and one 1.5kΩ.cm/50 µm epi)
  - Two 100 Ω.cm wafers bump bonded at VTT to CPR2 readout chip
- 2 CPC2 wafers with 2-level metal (busline-free CCD) delivered in November 2006
  - Designed to reach 50 MHz operation
- Have another 12 wafers to be processed after evaluation of the present variants

Yield from 4 single metal CPC2 wafers: 71% for CPC2-10, 63% for CPC2-40, 25% for CPC2-70

# CPC2 Results at 1 MHz



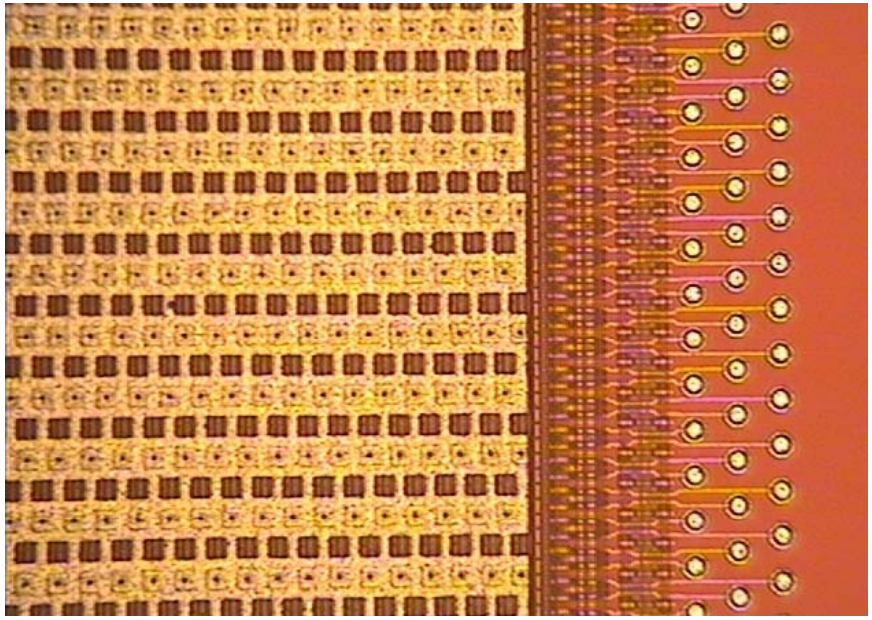

**$^{55}$Fe spectrum from CPC2-10 at 1 MHz**

Konstantin Stefanov (RAL)

- Analogue readout (no RO chip) at -40 °C
- Noise 65 e- ( typical MIP signal 1600 e-)

# CPC2: Double Level Metal

**Busline-free CPC2**

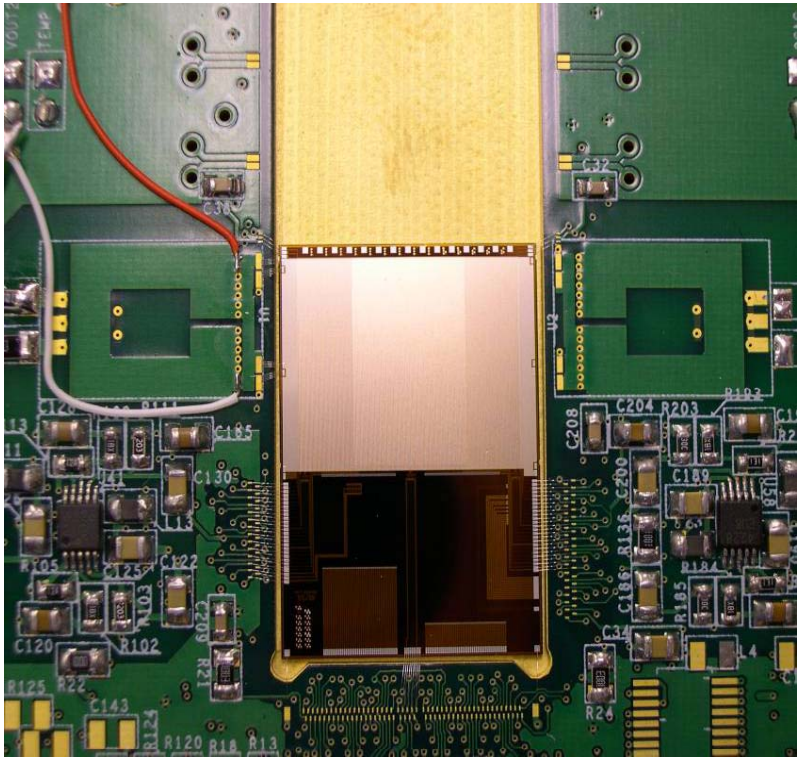


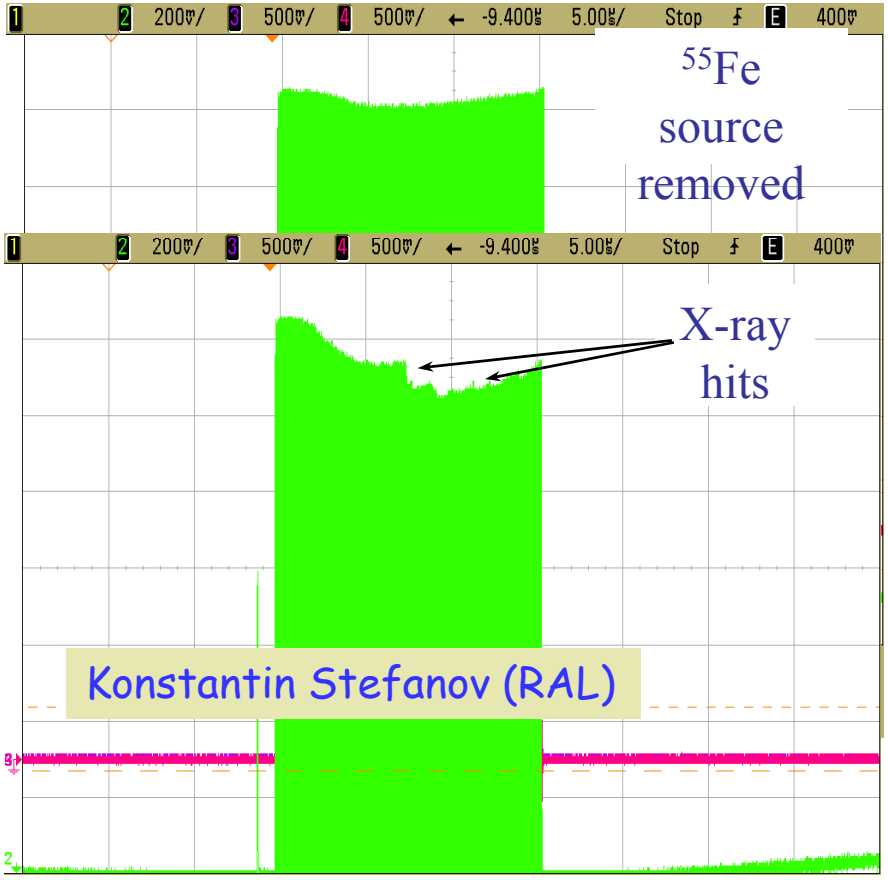
•Devices with 2-level metal clock distribution for high speed (busline-free) have been received

- •The whole image area serves as a distributed busline
- •Parasitic inductance is minimized but capacitance is larger by factor of ~2

# Busline Free CPC2 Testing

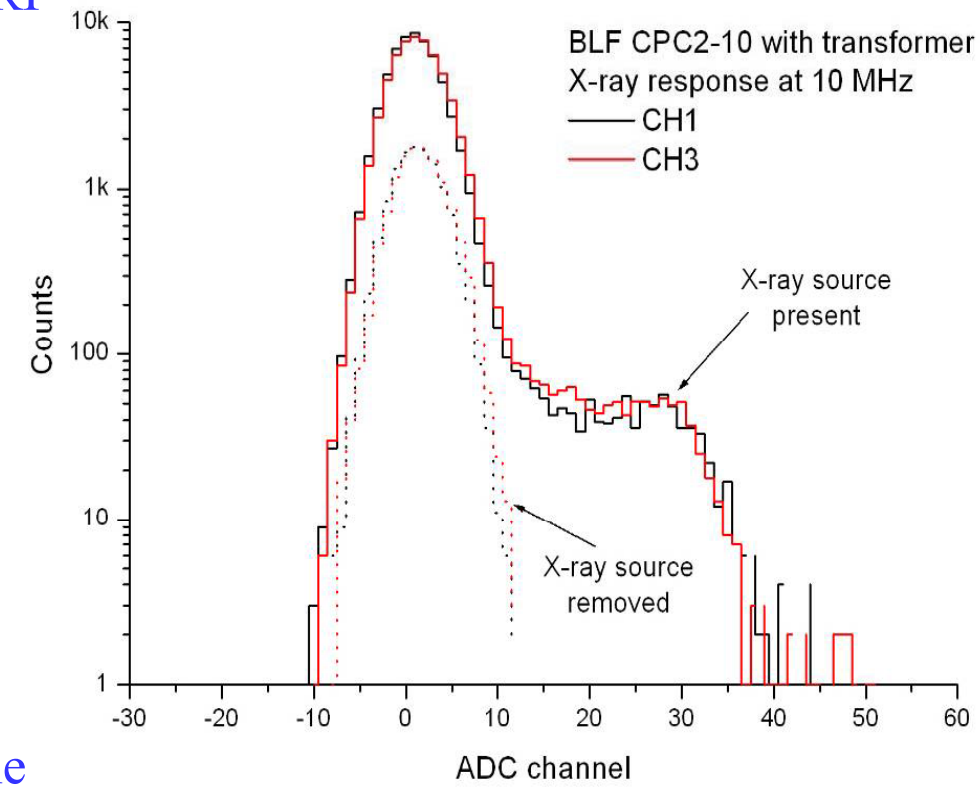
- CPC2-10 wire bonded to mother-board with transformer drive
- $^{55}$Fe X-ray signals observed at up to 45 MHz!





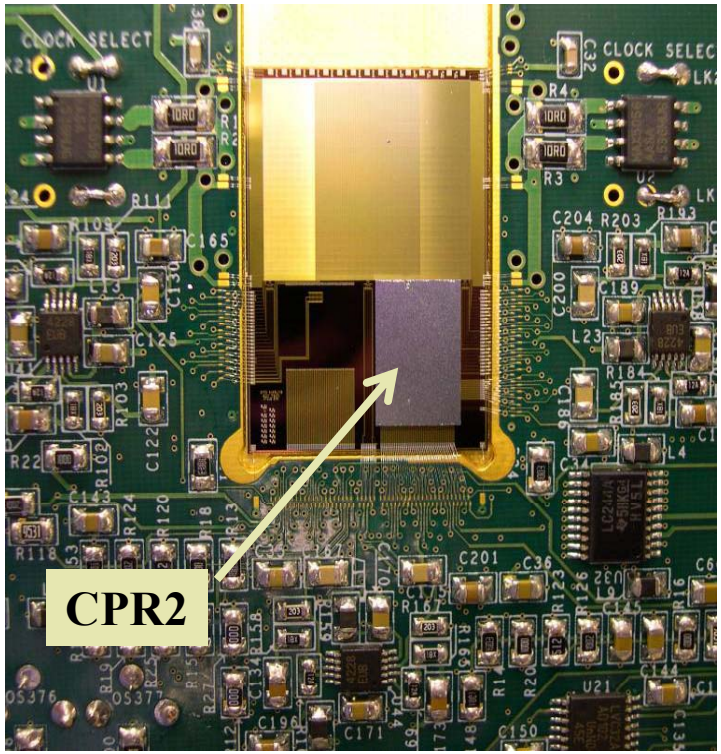
# Busline Free CPC2 Tests

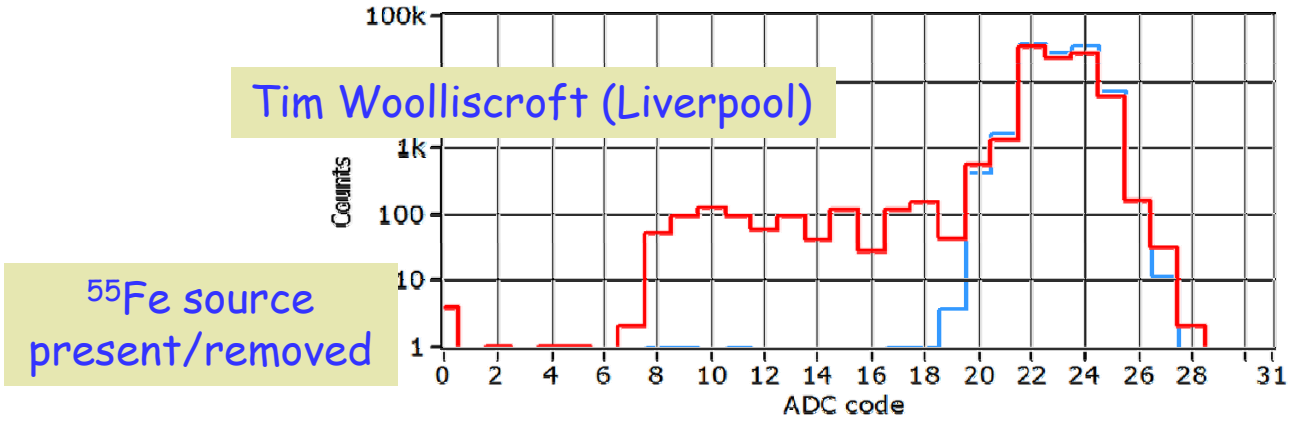
- Established operation at up to 45 MHz
  - Observed higher noise- due to RF amplifier used to provide clock
  - Work is in progress to improve the transformer drive circuit
- Observed efficient charge transfer with 0.4 $V_{PP}$ clock signals
  - Expected 2 $V_{pp}$
  - Not a resonance effect.
  - Studying test structures from the same wafers to understand implant concentrations



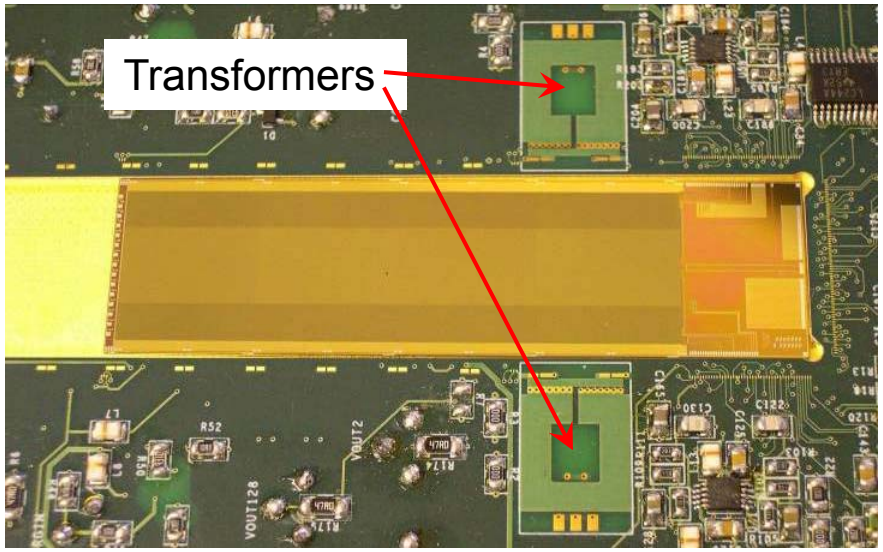
# CPC2 Bump Bonded to CPR2

- CPC2 and CPR2 were successfully bump bonded at VTT
- Tests started – saw first X-ray spectra
- Two assemblies died after a short period
  - Work in progress to understand this and implement more monitoring and safety features



# Clock Drivers for CPC2




*Johan Fopma/Brian Hawes, Oxford U*

Requirements: 2 $V_{pk\text{-}pk}$ at 50 MHz over 40 nF

## Transformer

- Planar air core transformers on 10-layer PC, size 1 $cm^2$
- Parasitic inductance of bond wires is a major effect
- Used to drive high speed busline-free CPC2

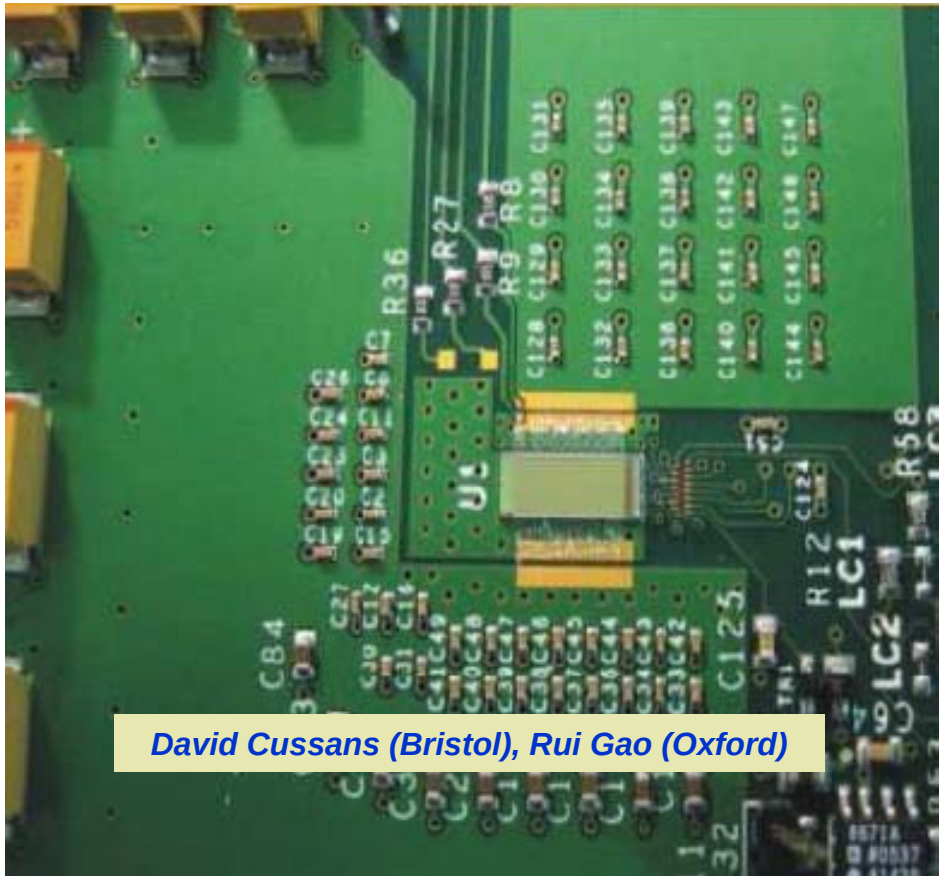
*Steve Thomas/Peter Murray, RAL*

## Custom clock driver: CPD1 chip

- First CPCCD driver chip (CPD1) delivered in October 2006
- Designed to drive the outer layer CCDs (127 nF/phase) at 25 MHz and the L1 CCD (40 nF/phase) at 50 MHz
- One chip drives 2 phases, 3.3 V clock swing
- 0.35 μm process, size ≈ 3 x 8 $mm^2$
- 32 W peak power but 0.5% duty cycle
- Thermal and electromigration issues are under control

# CPD1 Tests

- Standalone tests of CPD1 use a dedicated board
- Test board allows to exercise various modes of operation and provides external capacitive load
- Parasitic inductance is dominated by bond wires
- CPD1 has 8 sections
  - One of the sections is connected to 2nF internal capacitor to test the performance with minimal inductance
  - Outputs have alternating PH1/PH2 pads to minimize inductance

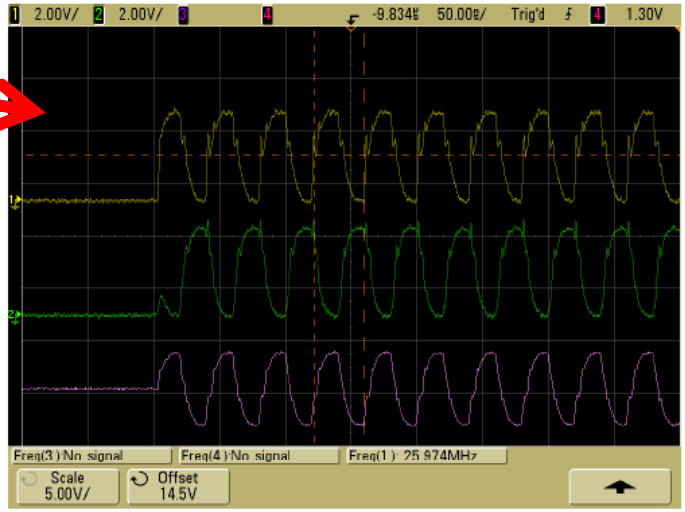


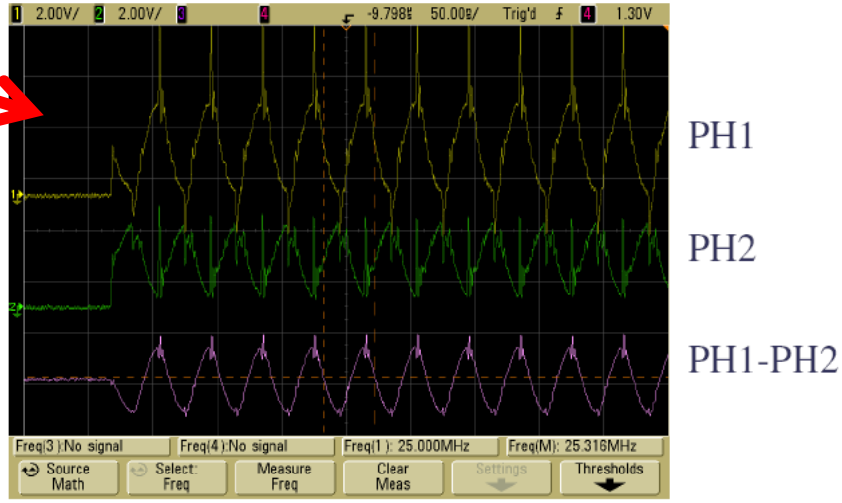

*David Cussans (Bristol), Rui Gao (Oxford)*

# CPD1 Results

- Internal 2 nF capacitor
- External 40 nF capacitor
  - Minimal deterioration of performance
- Initial tests are very promising – CPD1 is able to drive 40 nF load at 25 MHz maintaining proper pulse shape

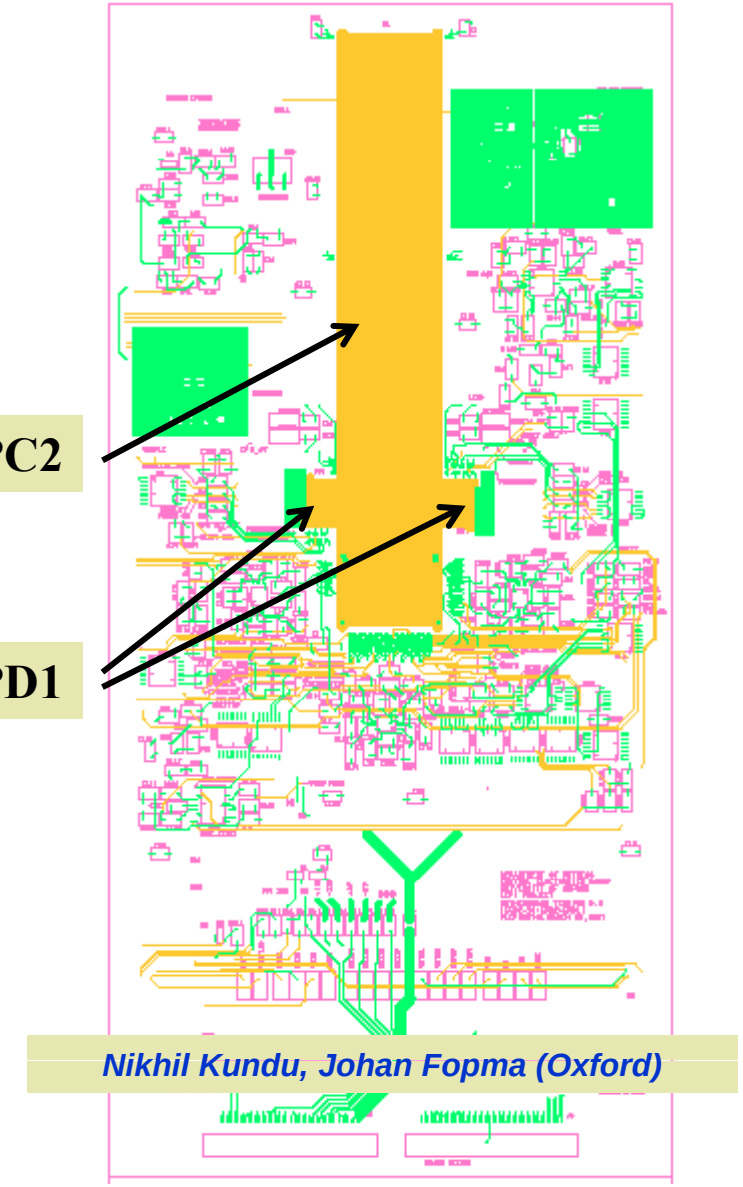
Inverter Mode, 25Mhz



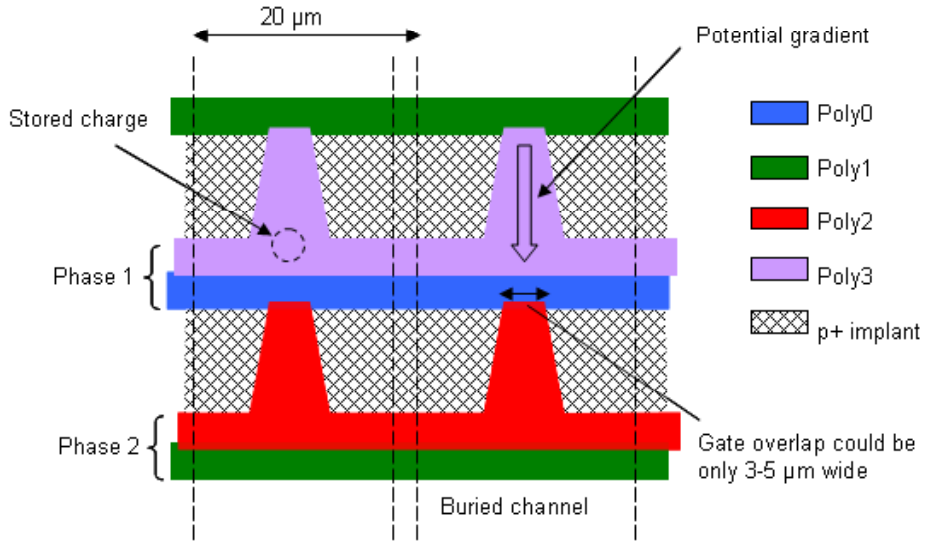



# CPD1 Tests

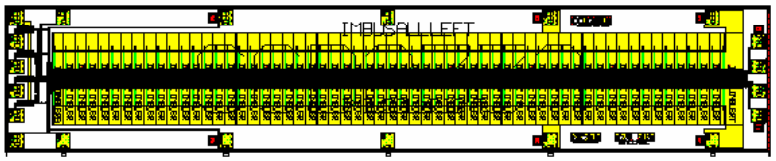
- Next step: operation of CPC2 with CPD1
- New test board in preparation
  - Two CPD1 chips will drive one CPC2
  - Need to interface CPC2 clock bonding pads to CPD1 bonding pads keeping the parasitic inductance low – will have a small adapter board between CPC2 and CPD1
- Should have results by the summer



# New Ideas: CCDs for Capacitance Reduction

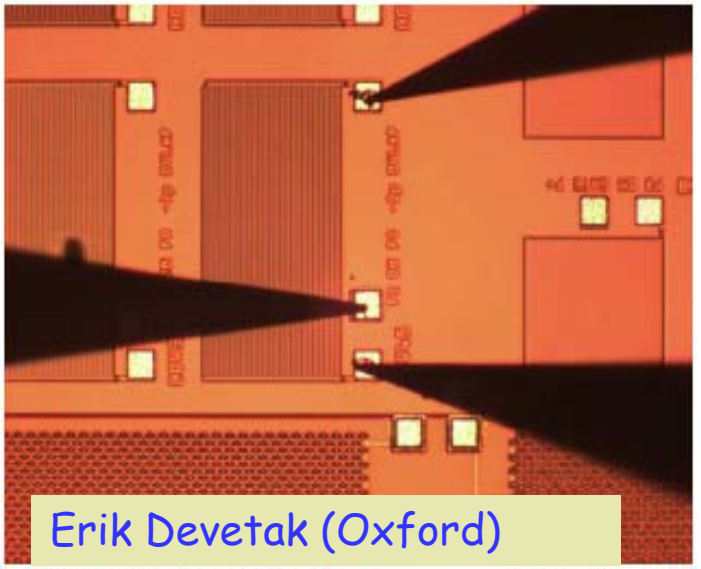


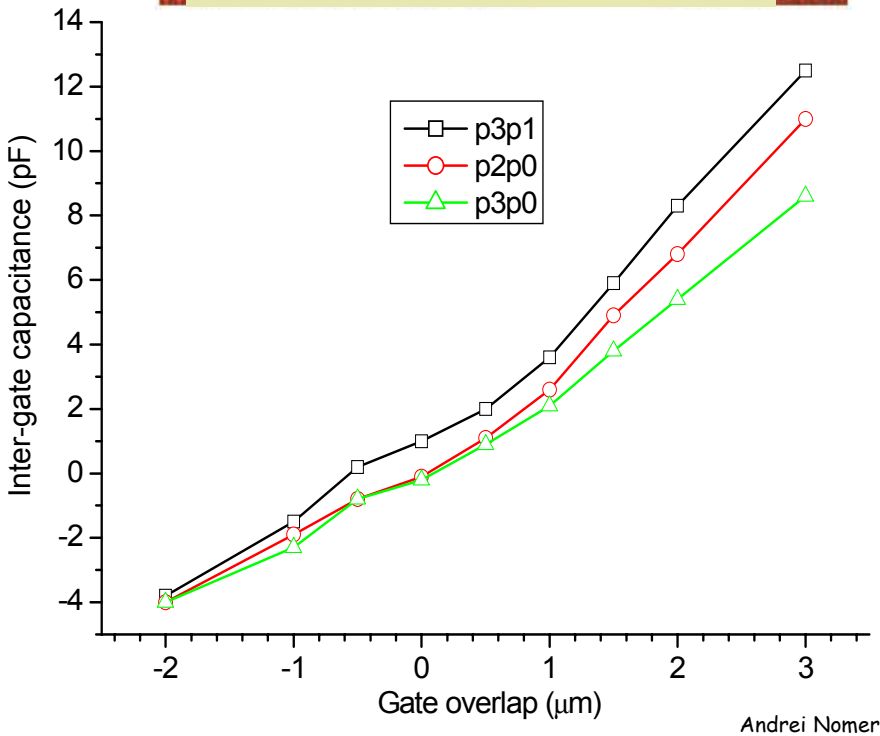

- High CCD capacitance is a challenge to drive because of the currents involved - Can we reduce the capacitance?
- Inter-gate capacitance $C_{ig}$ is dominant, depends mostly on the size of the gaps and the gate area
- Theoretically can achieve factor of 4 reduction in C
- Prepared several designs together with e2V and ordered mini CPCCDs: 10(H)×480(V) pixels



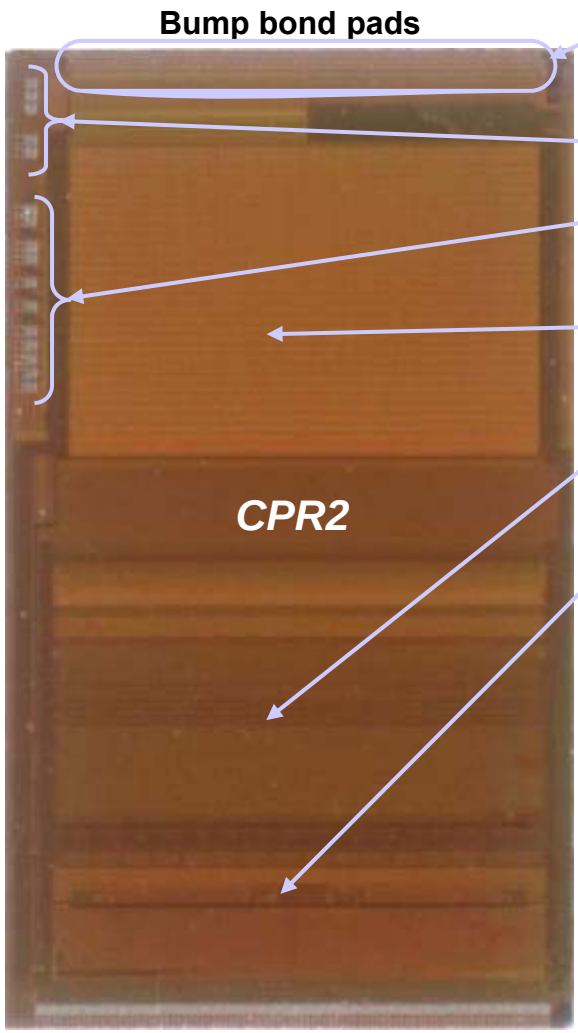
# Capacitance Overlap Measurements

- Have test structures with variable overlap distance between gates
- Will provide data on relationship between design and actual inter-gate overlap
- Useful to verify simulation of intergate capacitance
- First results show evidence of non-linearity around overlap of zero
  - Absolute calibration needs to be improved



# Readout Chips – CPR1 and CPR2




Voltage and charge amplifiers 125 channels each

Analogue test I/O

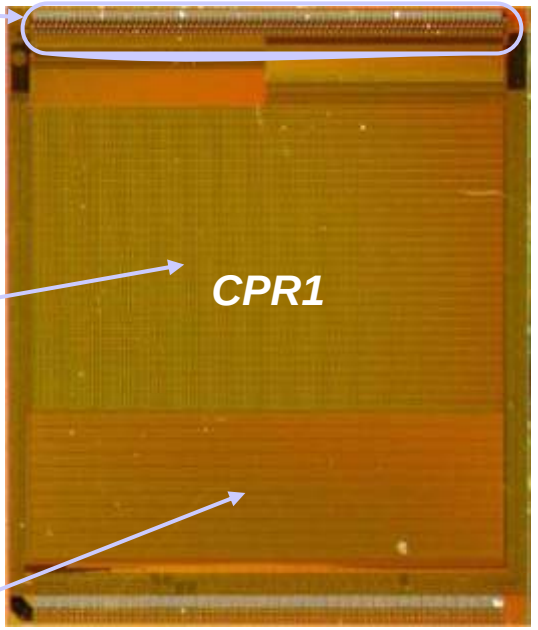
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

Sparse readout circuitry

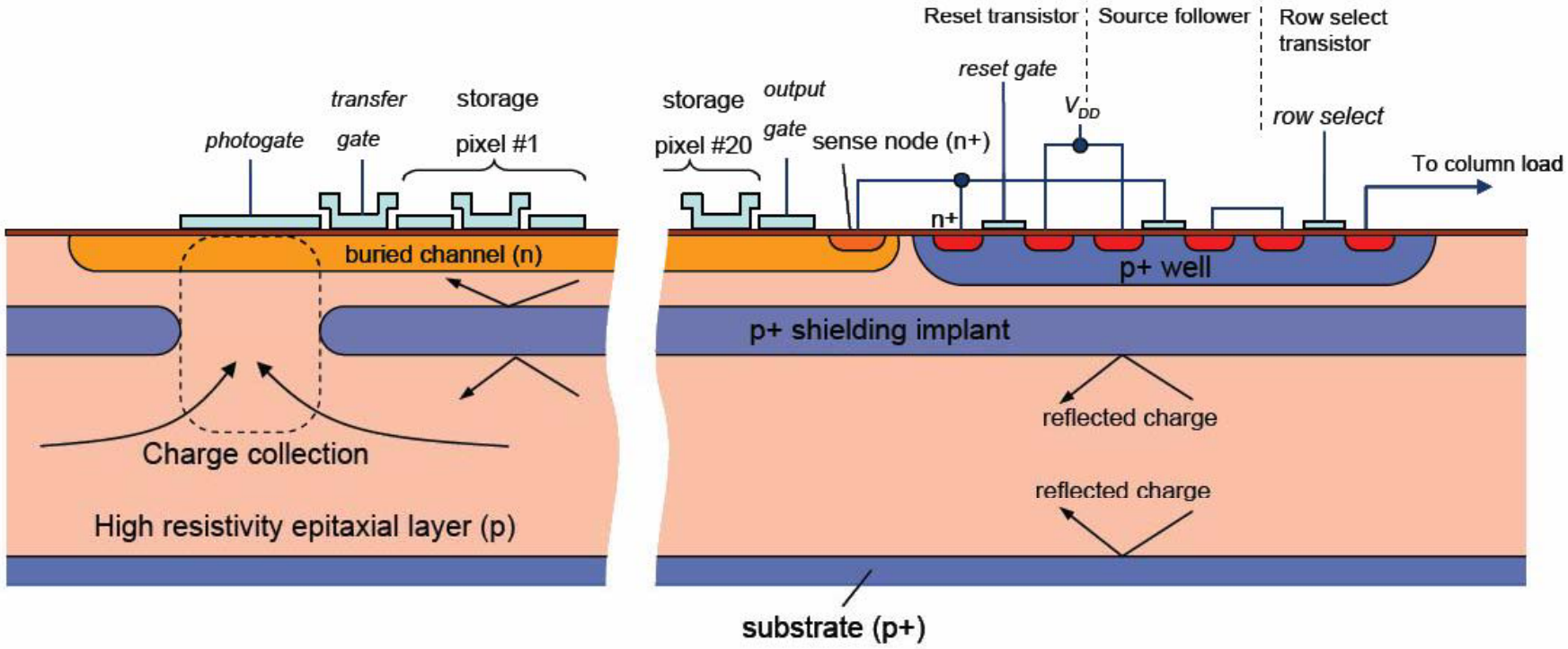
FIFO




- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 μm CMOS process (IBM)
- Work in progress to design CPR2A with improved performance

*Steve Thomas/Peter Murray, RAL*

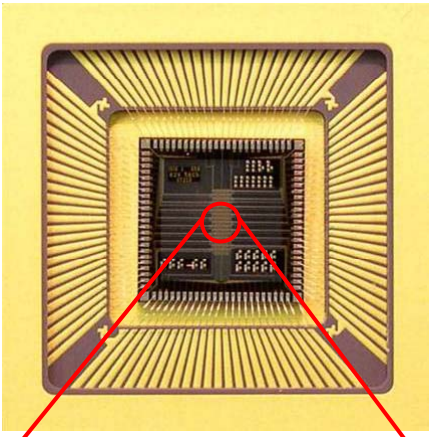
# In-situ Storage Image Sensor : ISIS

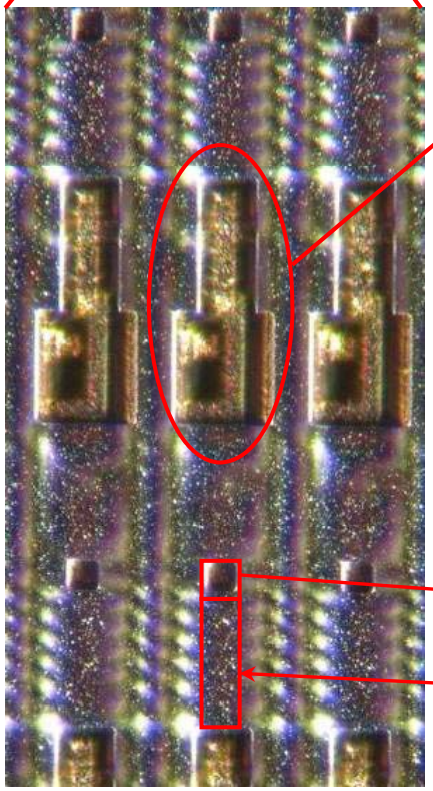


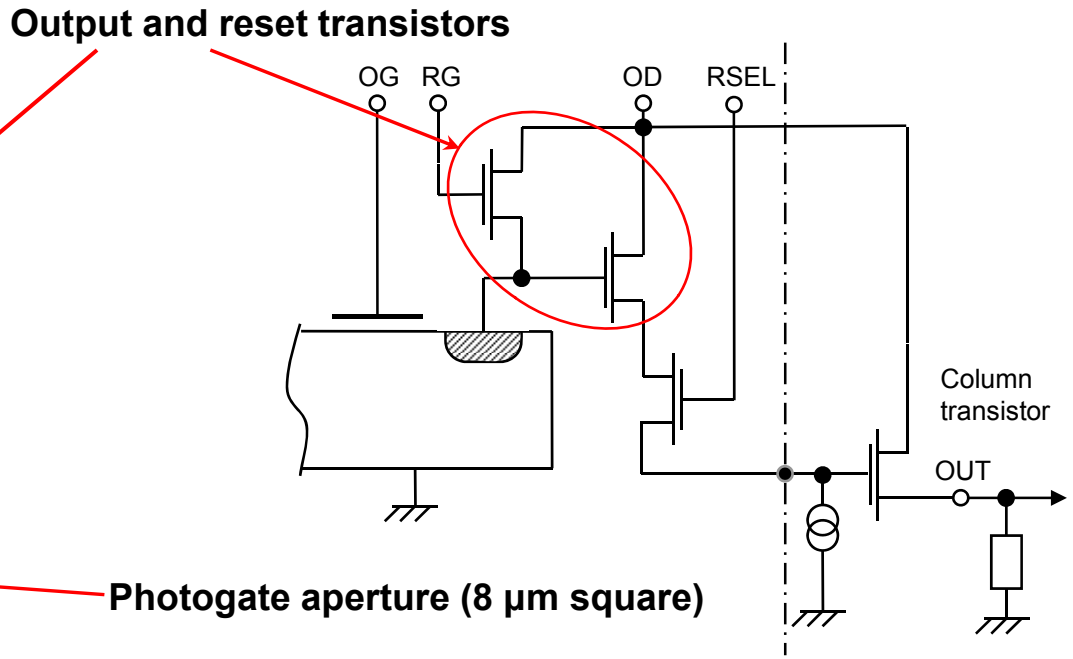

- Charge is collected into a photogate
- Each pixel has its own 20-cell CCD register : store raw charge during collisions
- Increased resistance to EMI
- Column-parallel readout during quiet time at ~1 MHz: much reduced clocking requirements

# The ISIS1 Cell

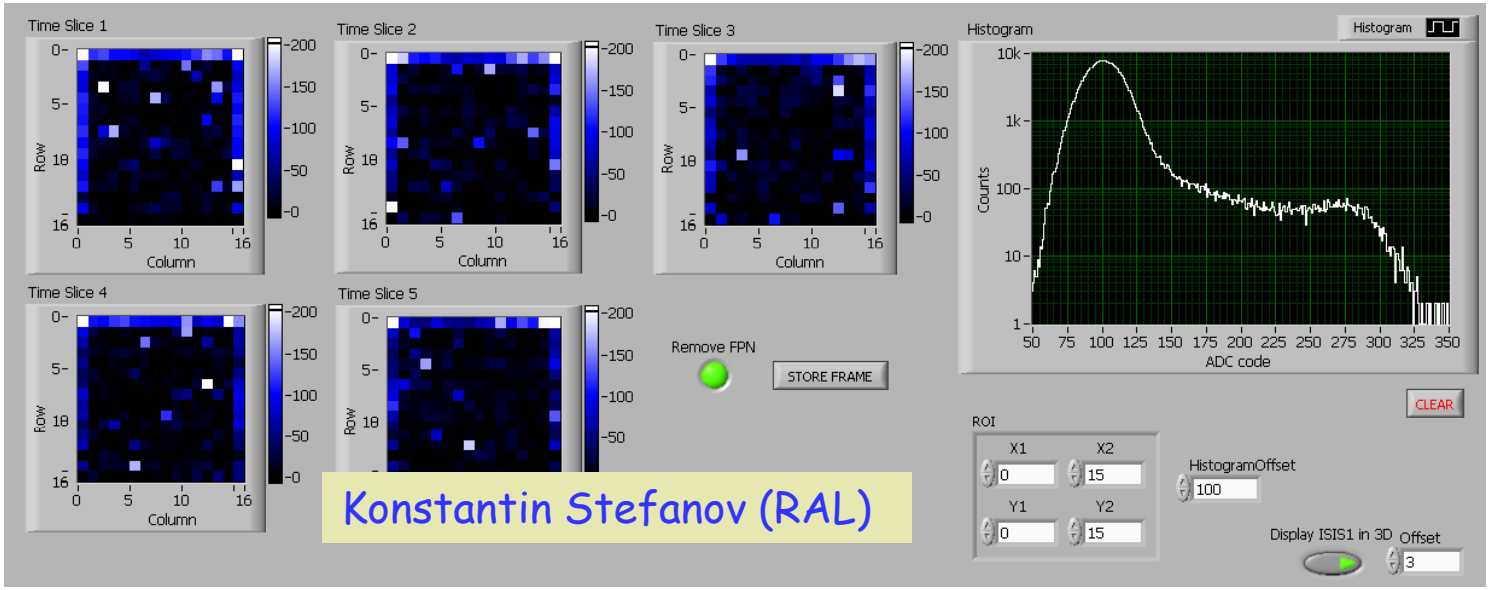
- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm







# Tests of ISIS1




## Tests with $^{55}$Fe source

- ISIS1 without *p*-well tested first and works OK
- ISIS1 with *p*-well has very large transistor thresholds, permanently off – problem understood and e2V is processing a new batch with p-well

Work with 3 other vendors to design ISIS2 with pixel size ~40x50 micron

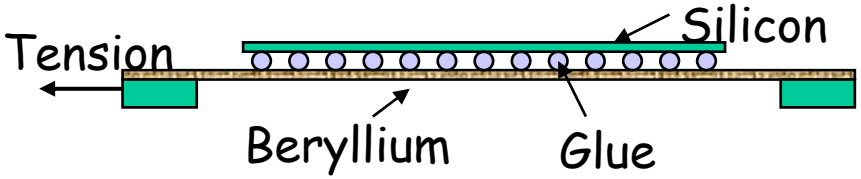
# Mechanical Options

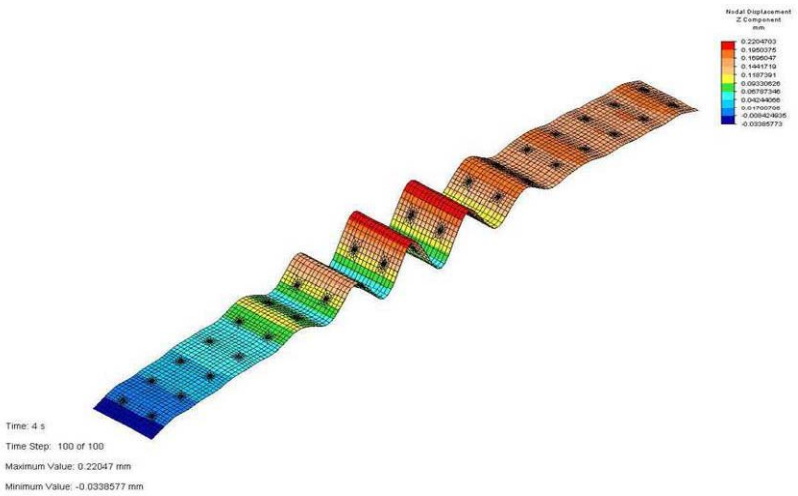
*Target of 0.1% $X_0$ per layer (100μm silicon equivalent)*

- **Unsupported Silicon**
  - Longitudinal tensioning provides stiffness
  - No lateral stability
  - Not believed to be promising
- **Thin Substrates**
  - Detector can be thinned to epitaxial layer (~20 μm)
  - Silicon glued to low mass substrate for lateral stability
  - Longitudinal stiffness still from moderate tension
  - Beryllium has best specific stiffness
- **Rigid Structures**
  - Foams look very promising

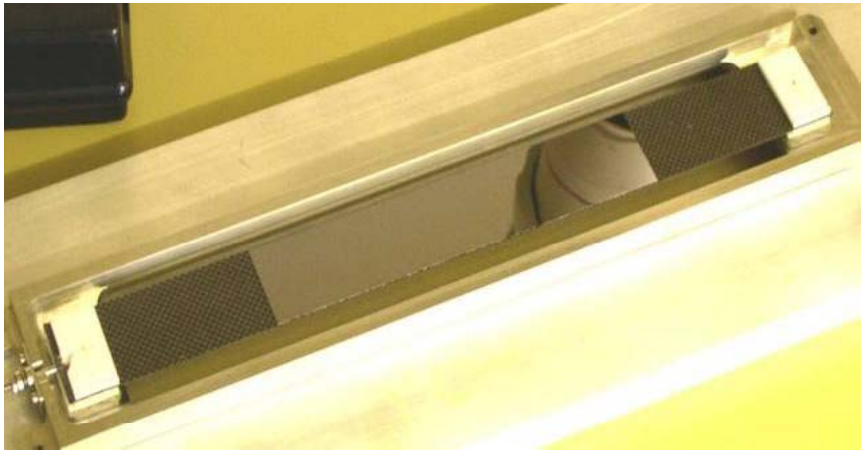
# Be and Carbon Fibre Substrates

- **Beryllium substrate**
  - **Minimum thickness 0.15% $X_0$**
  - **Good qualitative agreement from FEA models and measurement**



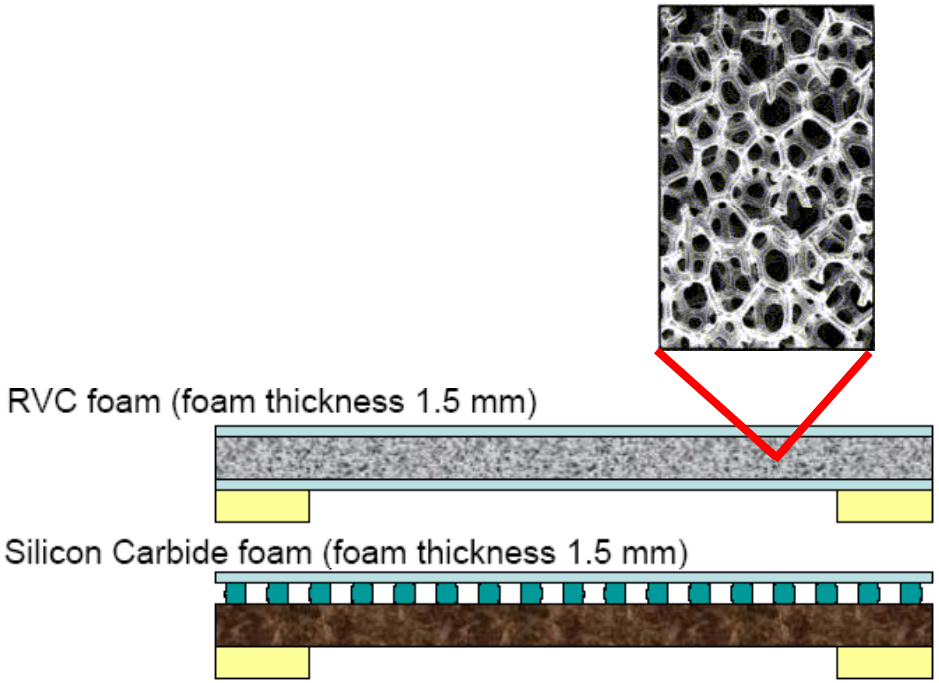



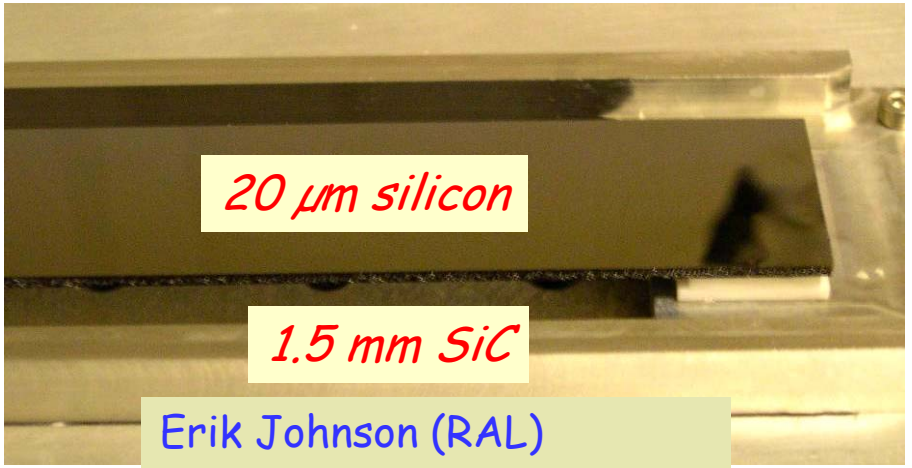

- **Carbon Fibre substrate**
  - **Better CTE match than Be**
  - **~0.09% $X_0$, no rippling to <200K**
    **→ *lateral stability insufficient***



# Rigid Structures: Foams

- RVC (Reticulated Vitreous Carbon) and silicon carbide are excellent thermal match to silicon
- Silicon-RVC foam sandwich (~3% density)
  - Foam (1.5mm thick), sandwiched between two 25 μm silicon pieces – required for rigidity
  - Achieves 0.09% X0
- Silicon on SiC foam (~ 8% density)
  - Silicon (25 μm) on SiC foam (1.5mm);
  - Achieves 0.16% X0
  - 0.09% X0 possible with lower density foams (< 5%)



# LCFI Vertexing and Flavour Tagging Package

- Implementation of ZVTOP algorithm used at SLD
  - ZVKIN part (ghost track) is impelented as well
- Flavour Tagging Package is using Neural Net based on inputs from the Vertexing Package
- Both packages are fully interfaced to MarlinReco reconstruction framework
  - Marlin processes exist for all parts of the two packages
- System tests with SGV (fast MC) and MOKKA (full Geant based MC) both give good results
- Documentation is being finalized
- Pilot testing by users has started
- Plan to officially release in April

# Summary

- Detector-scale CCDs produced and tested
- First successful readout at 45 MHz
- Demonstrated first sparsified readout with CPR2
- Developed and operated 20A clock driver chip CPD1
- Tested first prototypes of storage devices

- Mechanics : rigid foams favoured as sensor support substrates
- Physics studies : Vertexing and flavour tagging package will be released this month