ILC High Availability (HA) Electronics R&D

Prepared for
Institute for High Energy Physics Electronics Department
Beijing, PRC February 2, 2007
by
Ray Larsen
Electronics Division
Stanford Linear Accelerator Center
For the ILC Collaboration

Outline

- I. Why High Availability & Why Now?
- II. Controls & Instrumentation Standards
- III. Power Systems Architectures
- IV. Summary of R&D Programs
- V. Conclusions

I. Why HA and Why Now?

- Overarching Goal of HA Design:

  "*Design and build systems that do not interrupt machine operation when components fail.*"

- Computer Modeling[1] demonstrates that ILC will only run ~20% of the time unless all systems designed for High Availability.
- ILC has adopted HA design principles to evaluate all systems, subsystems & components.
- Strong investment needed in hardware and software R&D over next several years to design, implement effective HA at modest incremental cost.

[1] *AvailSim*, Ref. T. Himel, SLAC. See US Linear Collider Technology Options Study, USLC Steering Group, March 4, 2004,. Chapter 4: Availability Design.

I. Availability Defined

- *Availability:* Fraction of time machine/system is in "full production mode," i.e. *delivering design luminosity to user[1].*

$$A = MTBF/(MTBF+MTTR) \leq 1$$

  - MTBF = Mean Time Before Failure (Reliability)
  - MTTR = Mean Time To Repair
  - Note: If MTTR→0, A →1 regardless of *Reliability*

[1] Most Machine Availability statistics do not account for times of degraded luminosity or time lost in getting from zero to full luminosity, which are significant.

I. High Availability Design

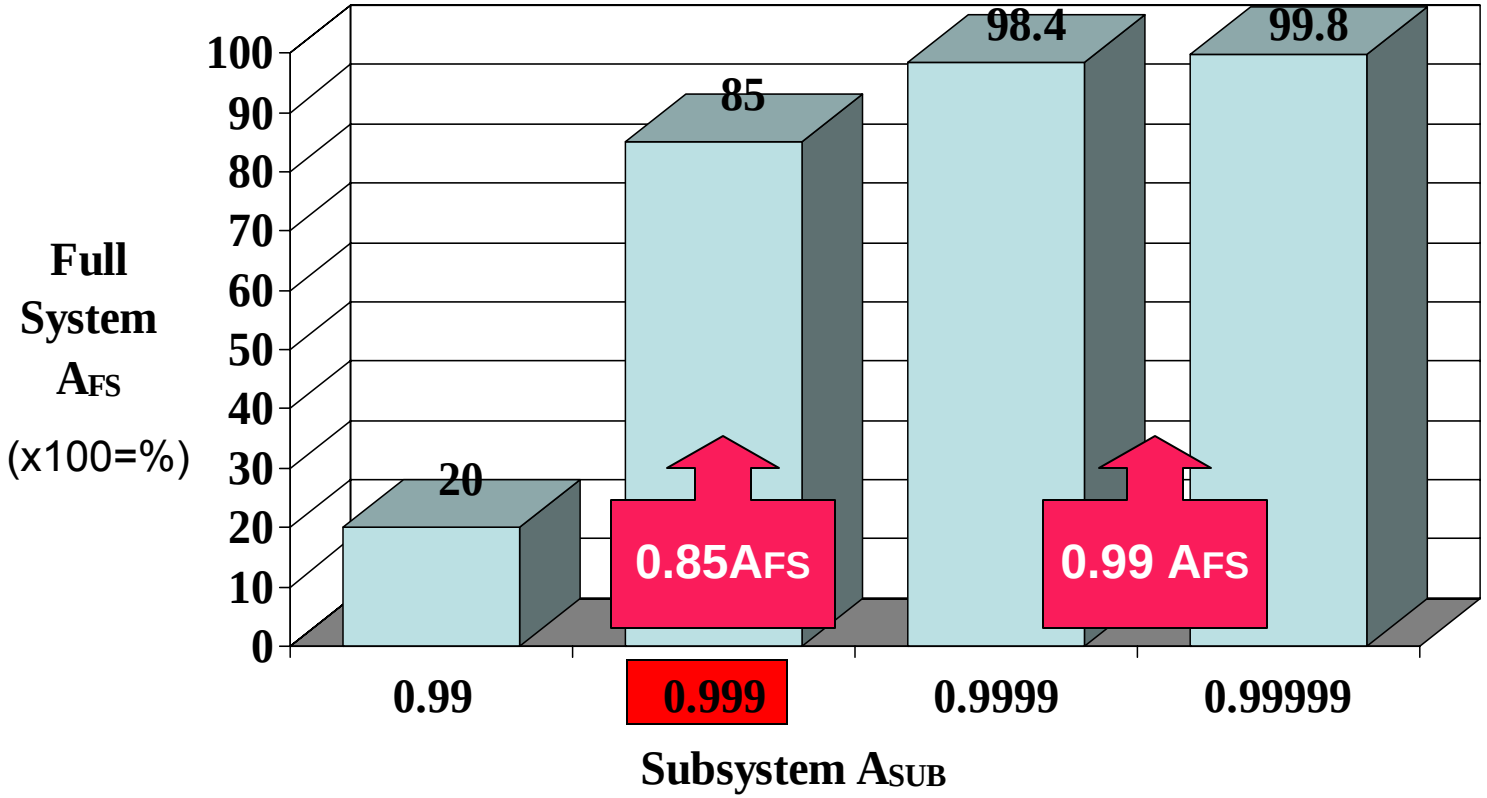
- A → 1 Achieved by 3 simple means:
  - *1. Modular Design at sub-unit level*
  - *2. Redundancy at unit level (typically N+1)*
  - *3. Hot swappable design if loss of sub-unit or unit brings down machine, or*
  - *Extra redundancy at system level where failed unit critical and can automatically switch in spare, e.g., RF station.*

I. Setting the ILC Availability Goal

- Assume 16 Systems each w/10 Subsystems
  - *1. Beamlines*
  - *2. Modulators*
  - *3. Klystrons*
  - *4. LLRF*
  - *5. Instrumentation*
  - *6. Control System*
  - *7. Vacuum*
  - *8. Cryogenics*
  - *9. AC Power*
  - *10. Water and A/C*

I. Required Subsystem Availability A_{SUB} for Full System A_{FS} >0.85 = 0.999 Avg

Comprising 16 Systems, 10 Subsystems each System



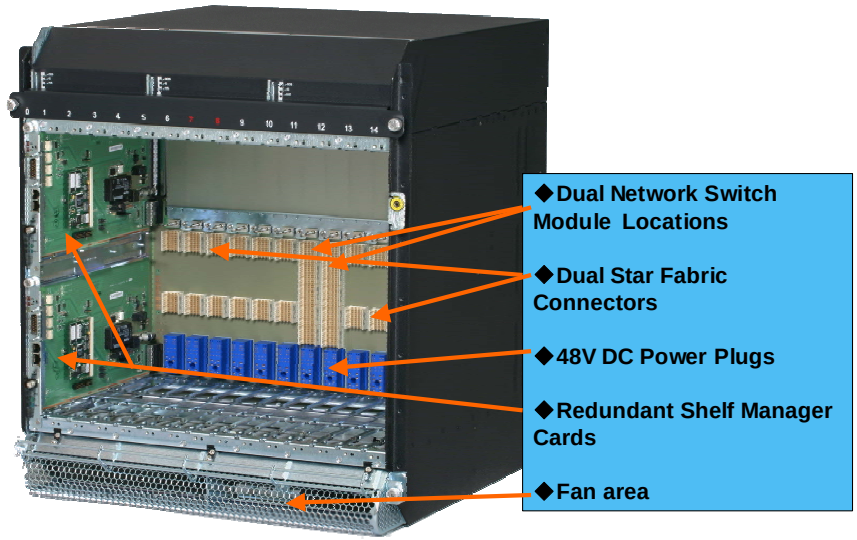
Ref: Larsen & Downing, 2004 IEEE NSS, Rome

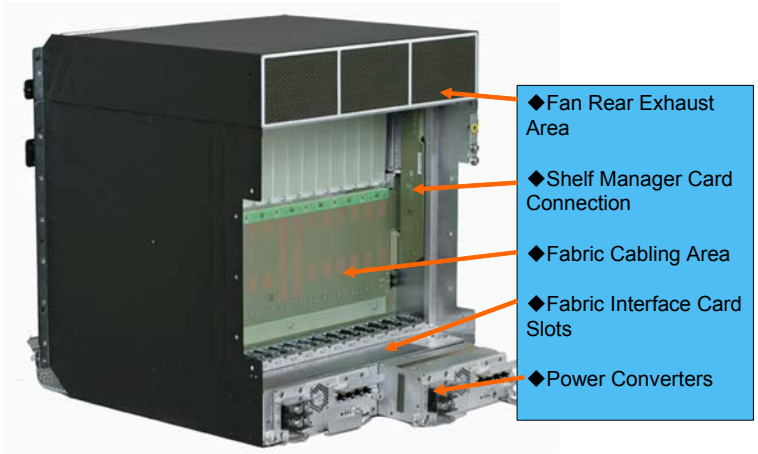
II. Controls & Instrumentation

- Baseline Controls & Instrumentation Platform
  - *Advanced Telecom Computing Architecture (ATCA)*
  - *2004 Telecom Industry Open Standard*
  - *Designed for "five nine's" 0.99999 Availability*
- Topics
  - *ATCA "5-nines" Shelf (Crate) Platform*
  - *Boards and Mezzanine Boards*
  - *Power & Fabric Connectors*
  - *Controls & Instrument Architecture*
  - *Board Level Power Systems*

II. 2004: Introduction of ATCA*

- Telecom Industry Open Standard
- Driven by $10B/year server and switching market
- A=0.99999 = Downtime of 5 minutes/year
- All Gigabit serial Dual Star or Mesh backplane
- Dual controllers, 48V PS, hot swappable,
- 200W/module air cooled, 3+1 Fans hot swappable
- Shelf Manager controls failover, power metering, hot swap

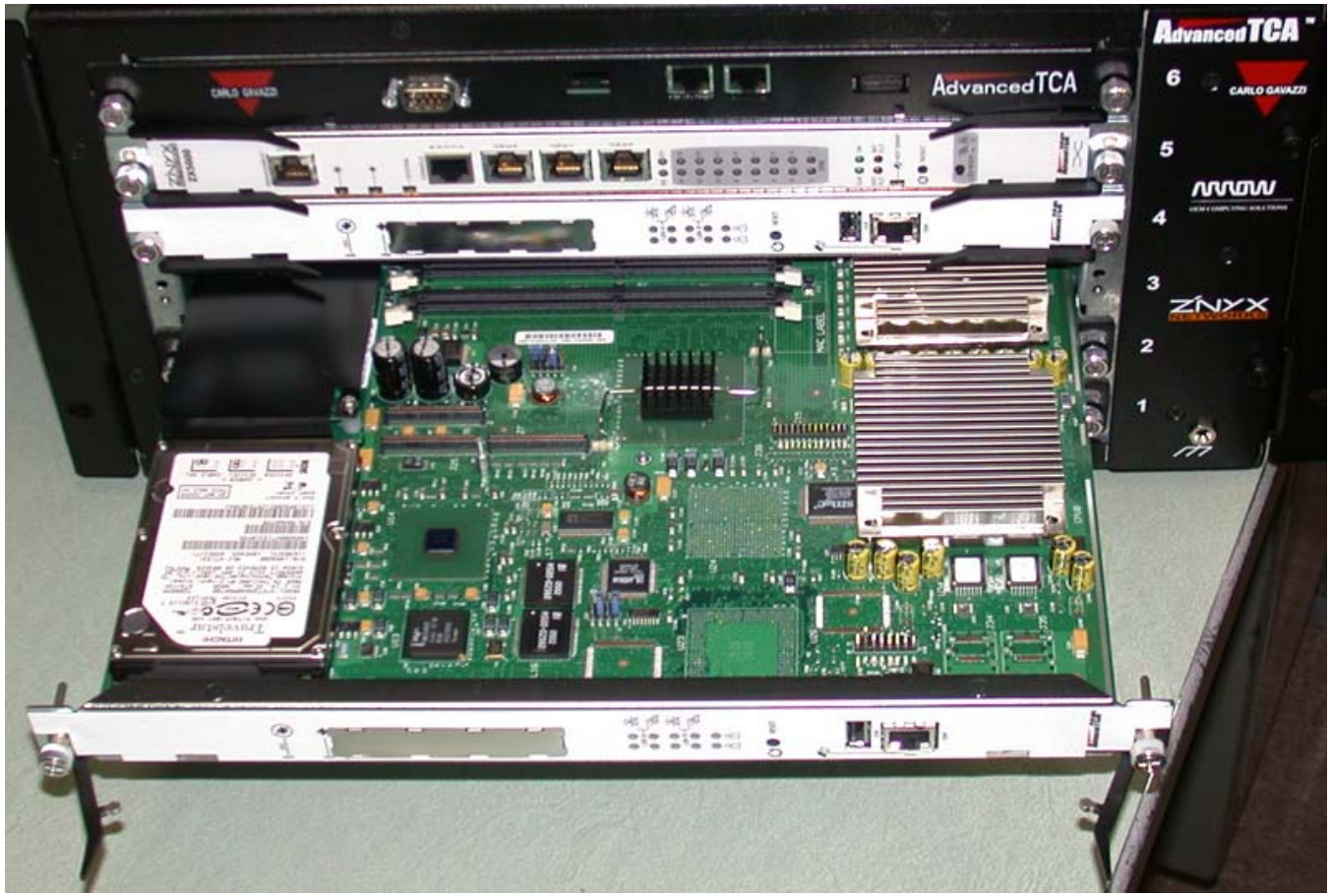




**Advanced Telecom Computing Architecture*

Courtesy PICMG-ATCA

II.5-Slot Crate (Shelf) Starter Kit



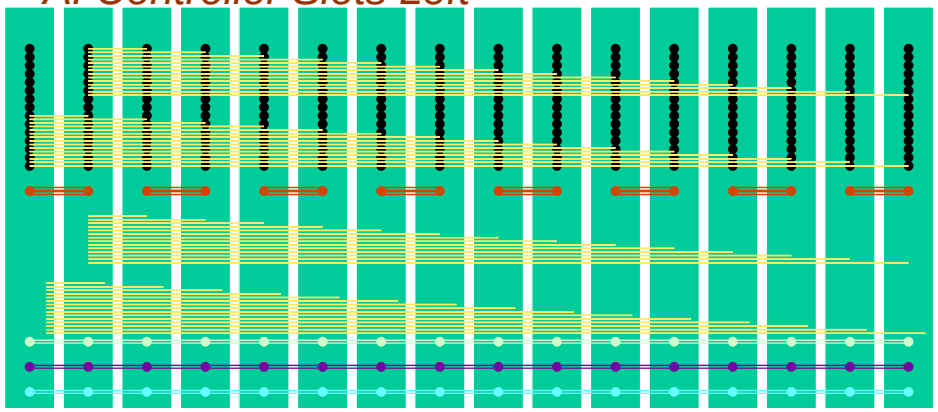
2 Processor Blades, 1 Fabric Switch 3.125 Gb/s, Shelf Manager (Inside box, not shown)

-Arrow Electronics

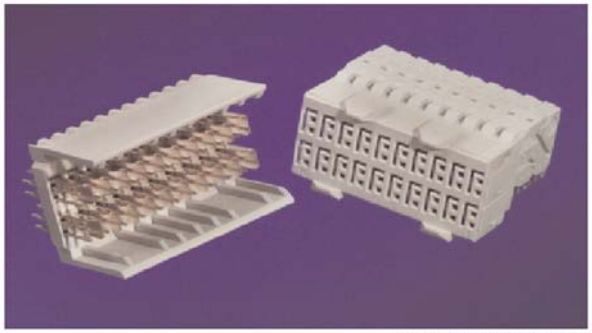
II. Dual Star Backplane & Fabric Connector

AdvancedTCA Backplane Routing Dual/Dual Star

A. Controller Slots Left



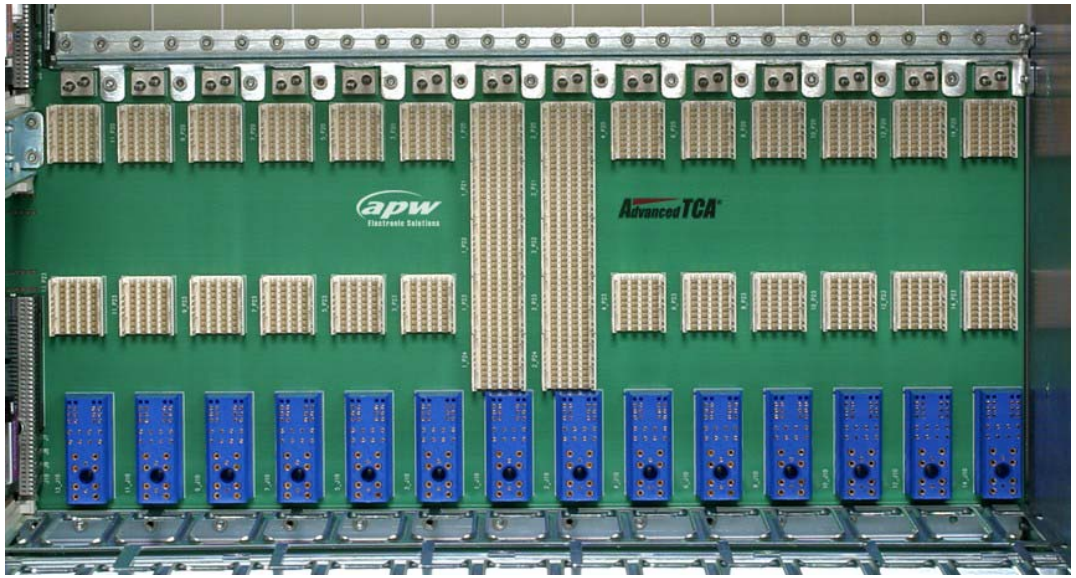
Full Mesh Fabric
Update Channel
Base Interface
Analog & Test Bus
System Management Bus
Power



20 Pair Header and Receptacle

- Data Fabric, Update Channel, and Timing Clocks
- Up to 3.125Ghz clock rates
- Pins protected by ground shield from bending
- Up to 5 connectors can be used on a backplane per slot

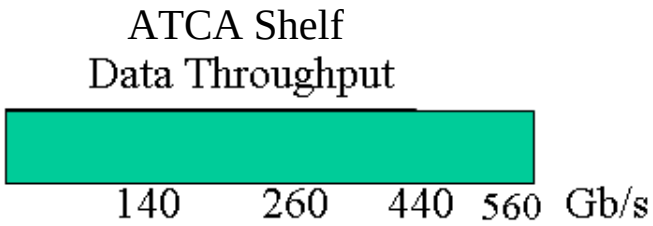
B. Controller Slots Center

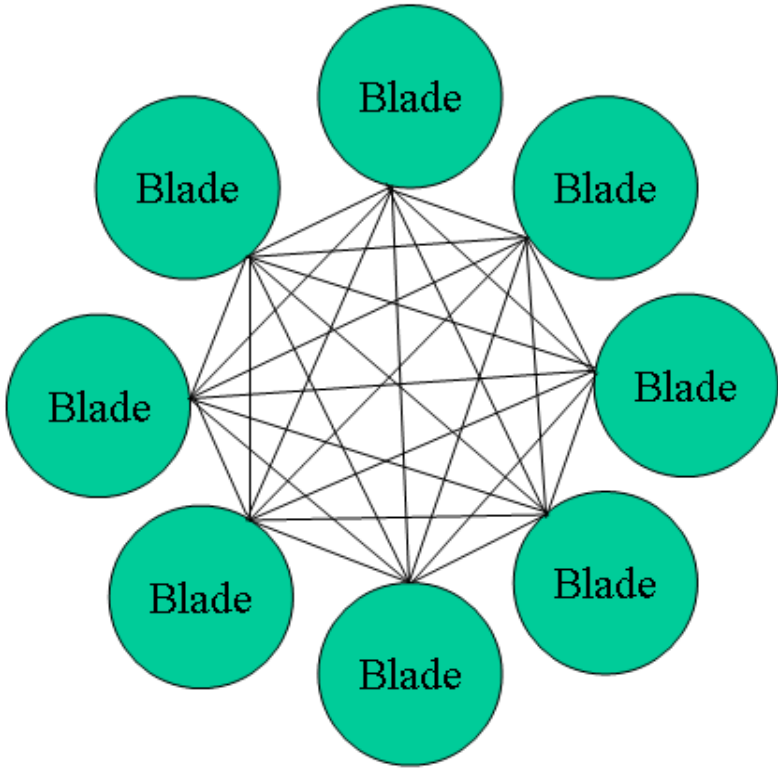


Courtesy PICMG-ATCA Consortium

II. ATCA Topology Options

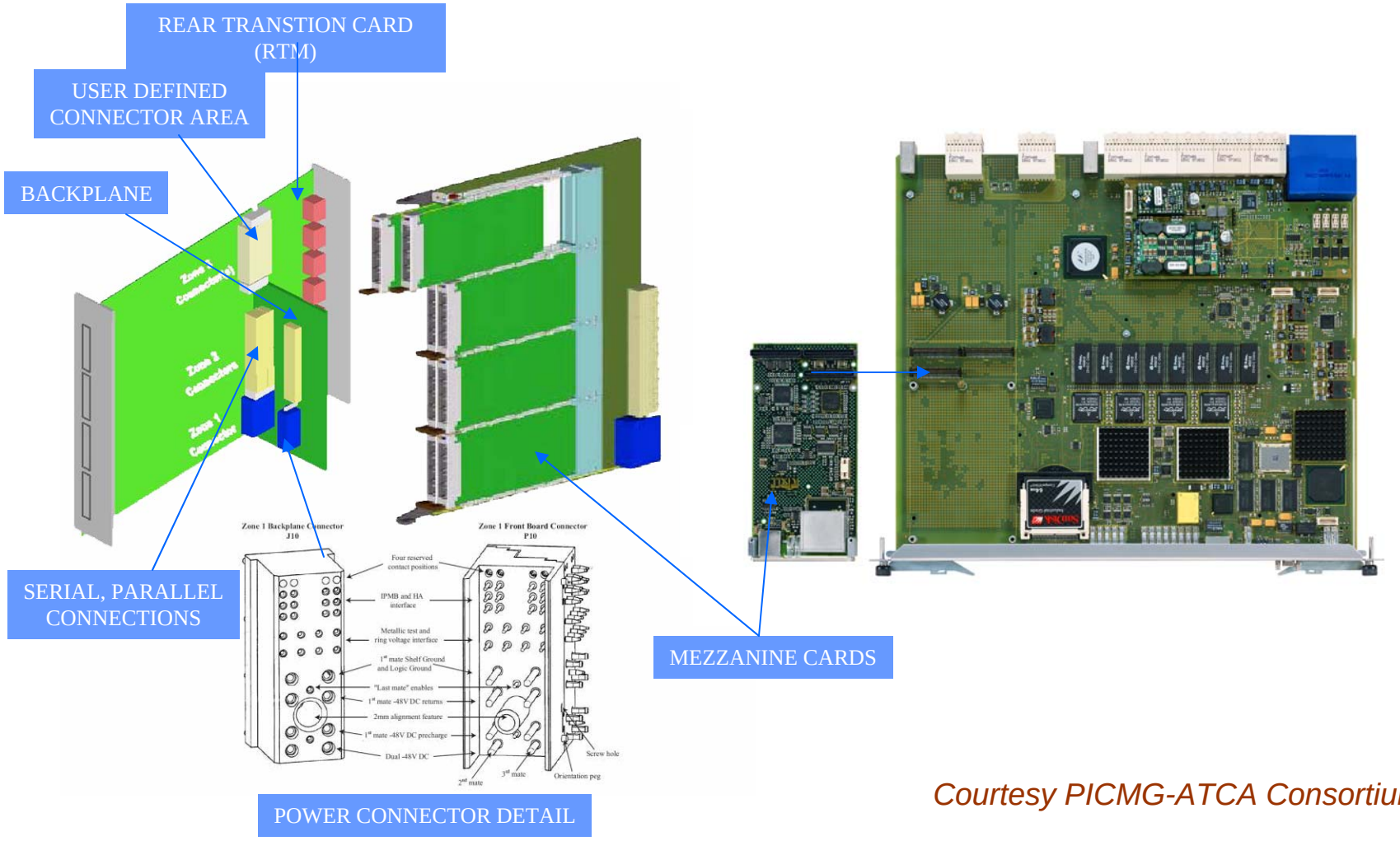
- PICMG 3.0 supports multiple topologies
  - Star (140 Gb/sec in 8 slots)
  - Dual Star (280 Gb/sec)
  - Full Mesh (560 Gb/sec in 8 slots)
- A 14 slot ATCA shelf could support data rates to 2.1Tb/s





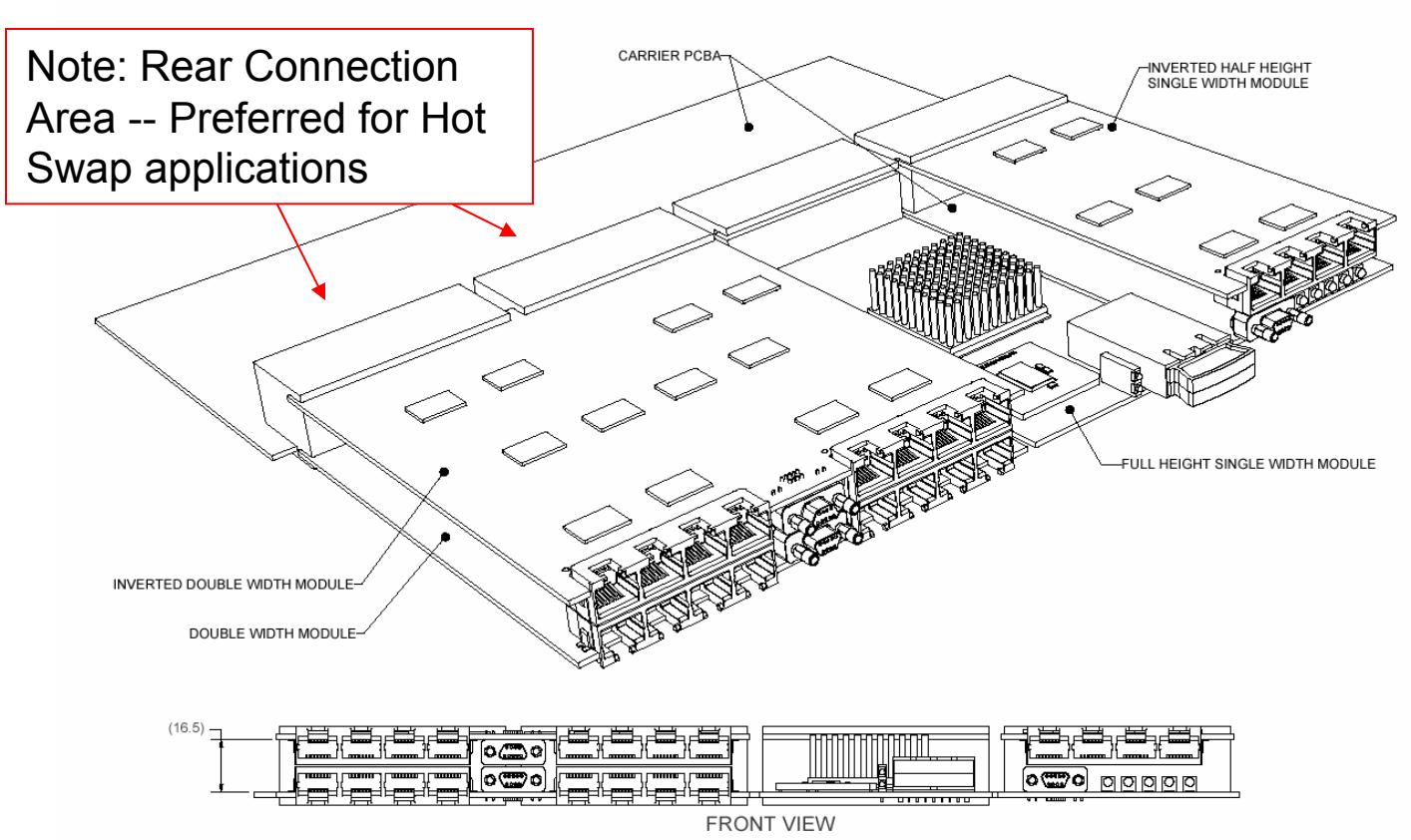
Courtesy PICMG-ATCA Consortium

II. ATCA Card Options



Courtesy PICMG-ATCA Consortium

II. ATCA Carrier & Mezzanine Cards

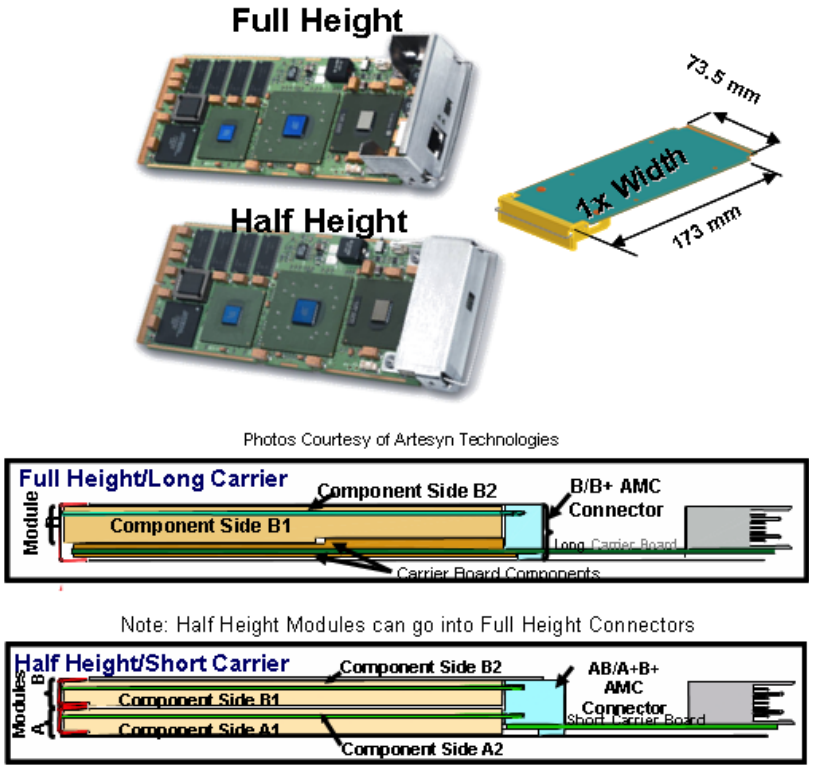


Courtesy PICMG-ATCA Consortium

II. Advanced Mezzanine Card

Full Height & Half Height

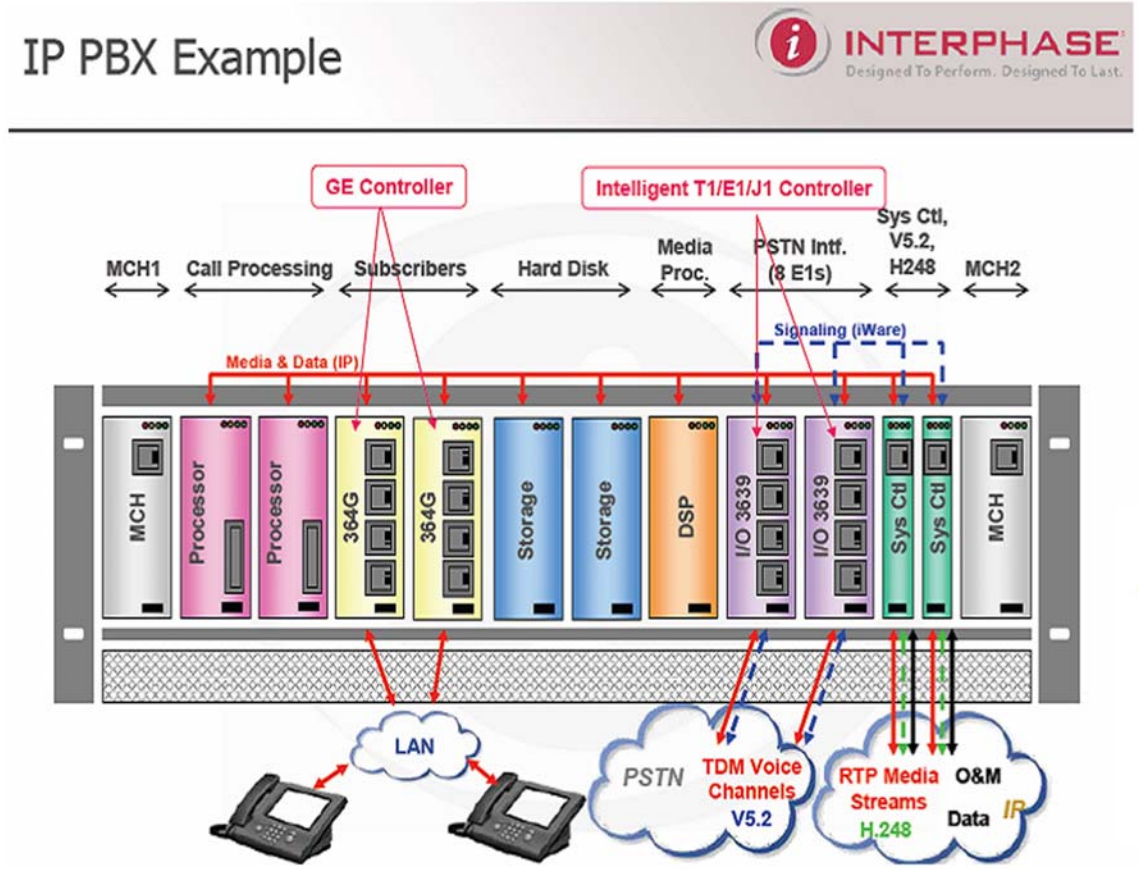
- What's an AMC?
  - A next generation mezzanine standard optimized for ATCA and high-speed interconnects such as PCI Express and Advanced Switching
- What's it good for?
  - Design simplification
  - Reduced board complexity
  - Increased throughput
    - 21 duplex ports @ up to 12.5 Gbits/s each
    - Designed to also enable SPI-4.2
  - Increases high availability with IPMB and Hot Swap
  - Modularity increases system density and improves TTM
    (due to less baseboard redesign)



IPBM=Intelligent Platform Management Board
TTM = Time To Market

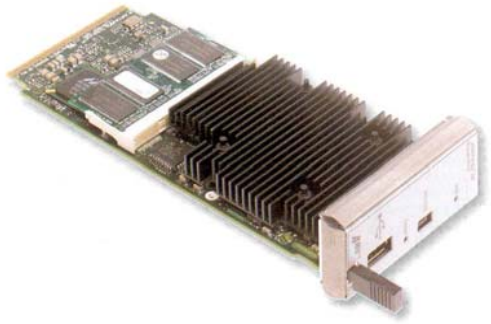
Courtesy PICMG-ATCA Consortium

II. MicroTCA Chassis



MicroTCA

Platform designed for standard Mezzanine cards in separate low profile package. Current design is NOT rear-only connection.



Courtesy Interphase Corp.

II. Commercial DAQ Instruments Example

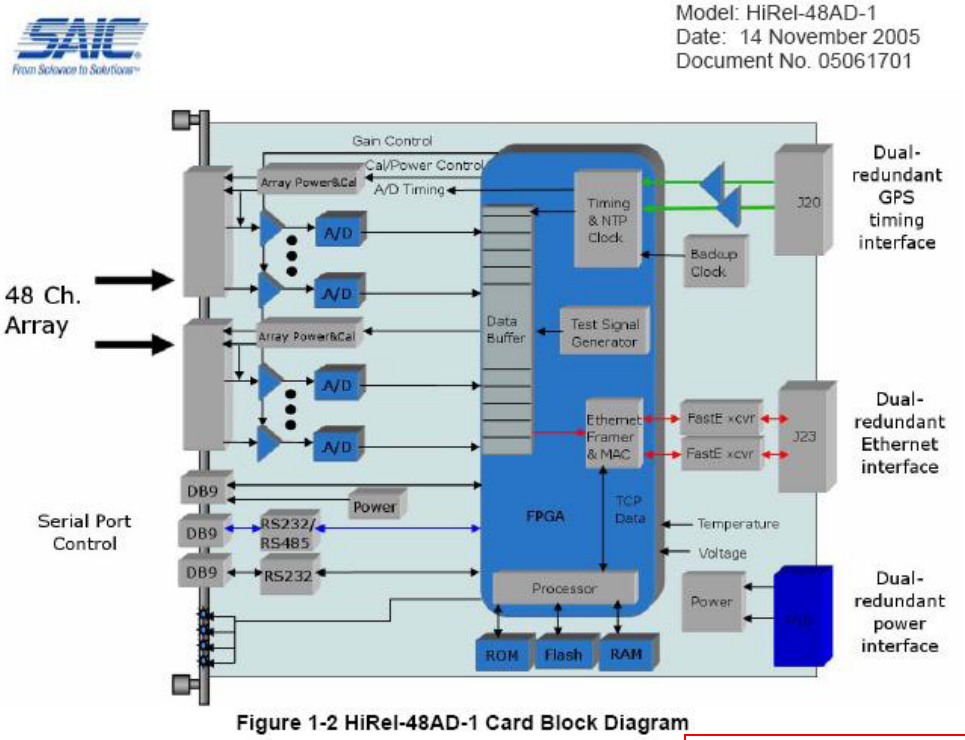
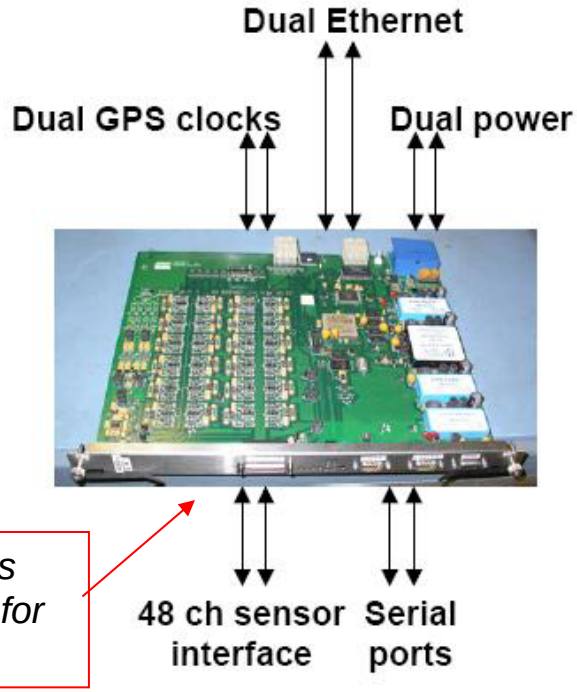


Figure 1-2 HiRel-48AD-1 Card Block Diagram

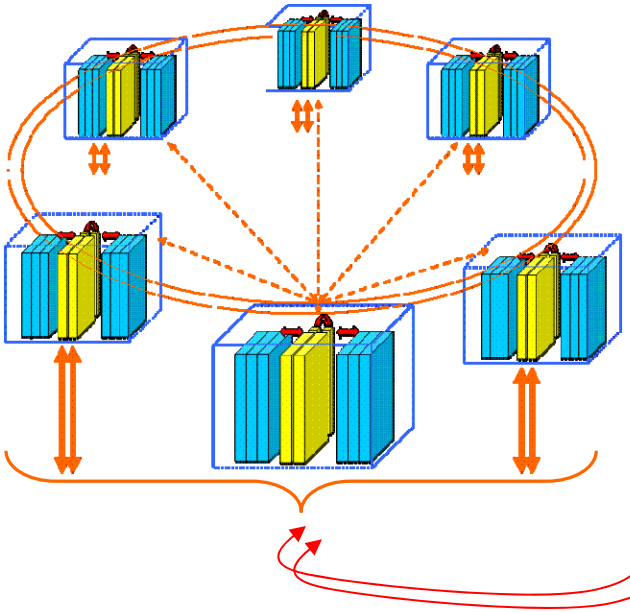
Designed for large array underwater sonar experiment, early ATCA, redundant for high reliability, 10W total board power, GPS timing.

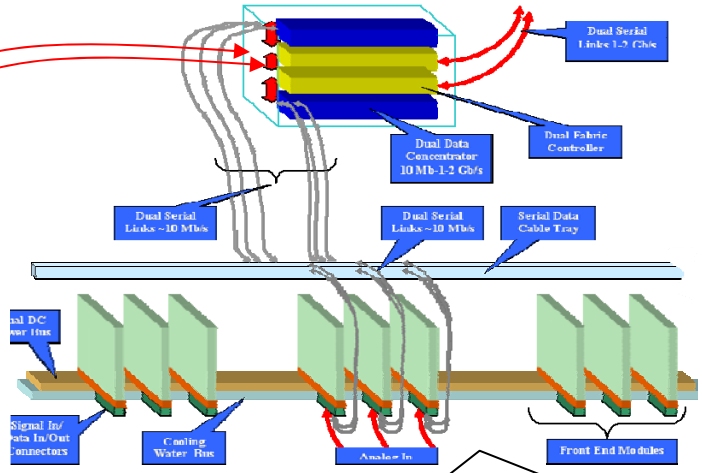


Note – FP connections can be moved to rear for hot-swap.

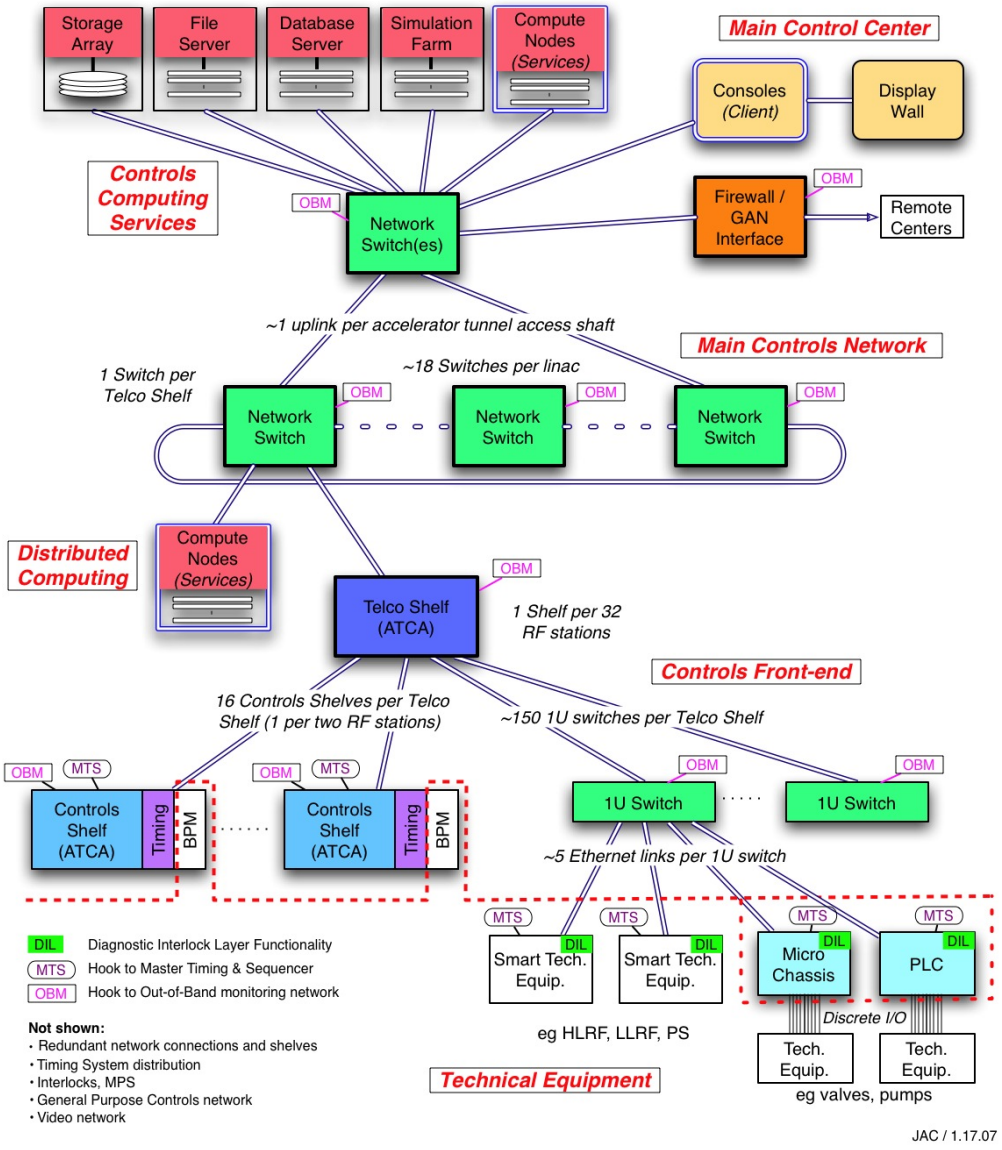
II. Proposed ILC Applications

- Controls Backbone
- Main Control
- Remote Sector Nodes
- Front End Instruments





Front End Instruments in standard crates & racks or special structures, e.g. Detectors



II. ILC Controls Architecture Details

Courtesy J. Carwardine Argonne National Lab

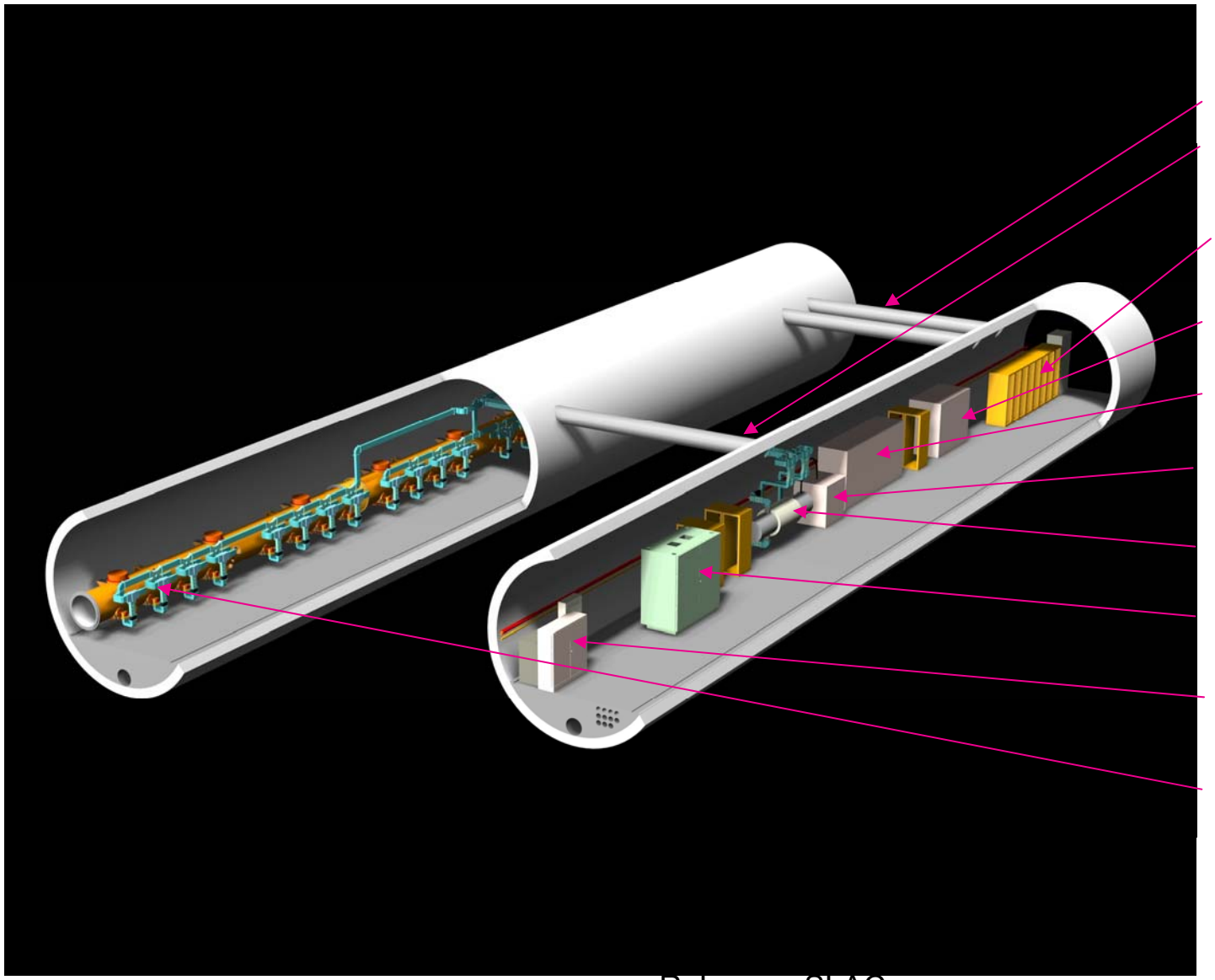
III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

III. Main Linac RF Power

- Dominate electronic systems costs:
  - *~650 10 MW 1.3 GHz RF Stations (modulators, klystrons, waveguide distribution)*
  - *~5000 equipment racks for LLRF, BPM, magnet supplies, vacuum, tuners etc*
  - *~1,500 ATCA crates.*
- Main limitation to availability:
  - *RF power, DC power systems*

ILC Baseline: 38m 10 MW Linac RF Station



Penetrations:
Cable & Plumbing
Waveguide

LLRF, Controls,
Protection Racks

Charger

Main Modulator

HV Pulse Transformer

Horizontal Klystron

LCW Chiller for Racks

HV Supply Switchgear

Waveguide
Distribution
System

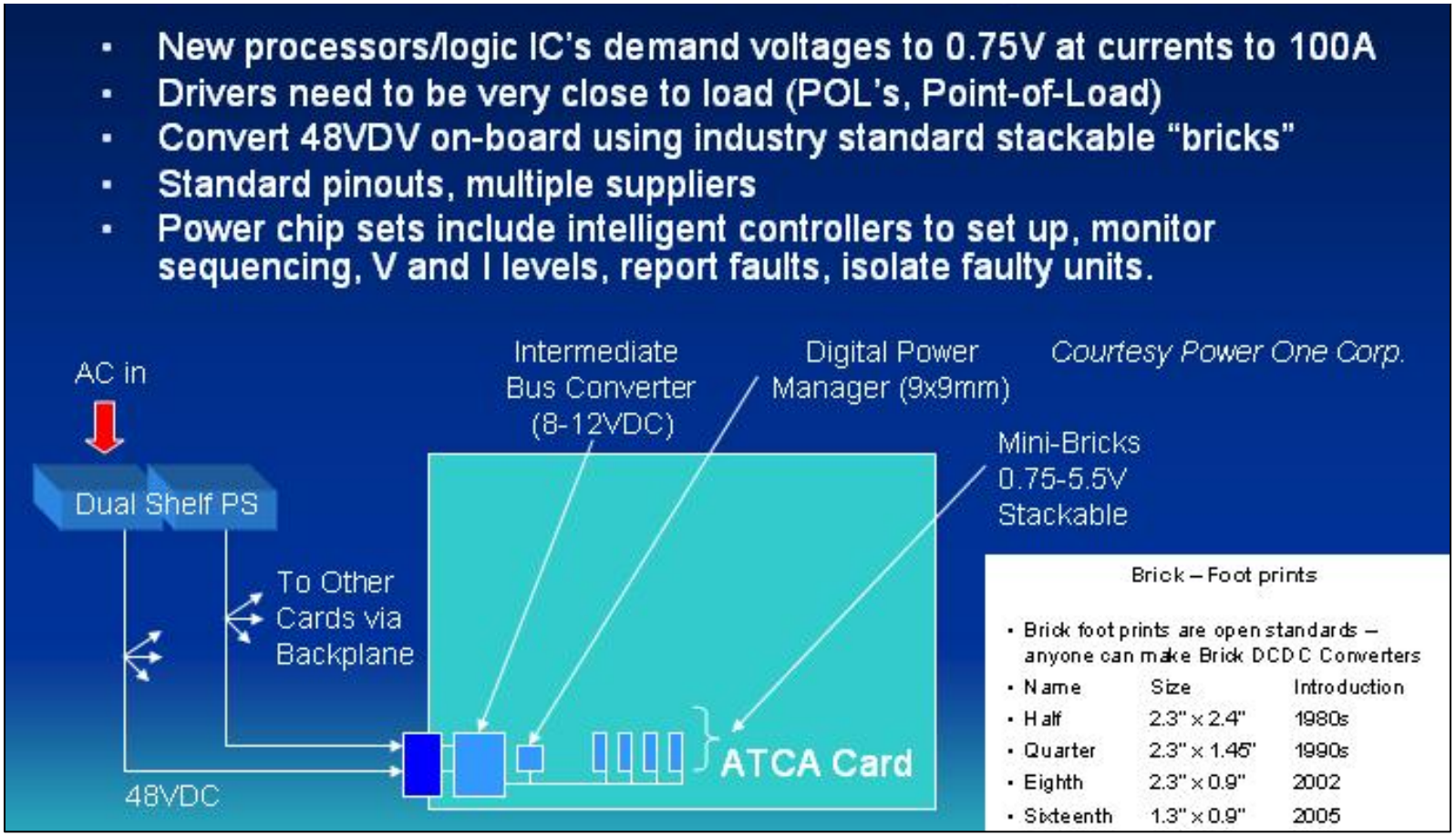
Courtesy: J. Liebfritz, FNAL

III. Power Systems Architectures

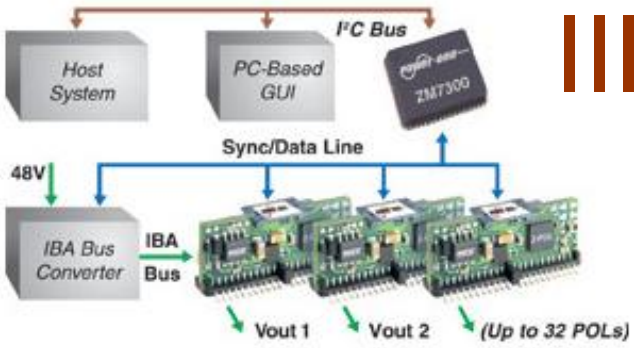
- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

III-1. Card Level Power Systems

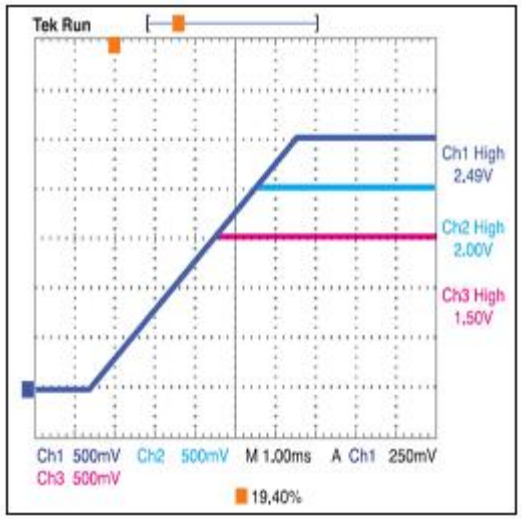
Commercial Solutions from Telecom Industry



III-1. Power Converters*



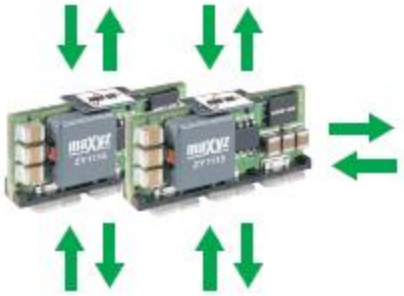
Z-One® Digital Power is a multi-source open-architecture power solution that optionally utilizes an industry-standard I²C interface.



No-Bus™ Z-1000 POLs feature guaranteed tracking between multiple outputs

Output Voltages and Currents

- Output voltages (0.5 to 5.5V) and turn-on delays are configured with an external resistor and a capacitor, respectively.
- Up to ten Z-1000 POLs can current share using a single control trace.
- Z-1000 POLs can start up with pre-biased outputs.
- Sink and source current capabilities for active bus termination.



Signals and Protections

- Reporting of output current and temperature via signal pins.
- Thresholds for overvoltage, undervoltage, and Power Good track the output voltage settings.

Coordination and Optimization via Simple Pin Strapping

- Frequency synchronization and phase interleaving reduce EMI.
- Comprehensive sequencing and cascading management.
- Feedback loop compensation and enable logic.
- Frequency synchronization, fault propagation, and current sharing are implemented, without external components, by interconnecting the respective pins on the Z-POLs being coordinated.

**Courtesy Power-One Corp.*

III-1. Intelligent Power Application - Beijing*

Xinwei Configures Z-One® Digital Power for "Big Smart" Wireless in Under 10 Minutes

DC-DC Converters Quick Links

The Z-One® POLs pictured below provide point-of-load power for Beijing Xinwei Telecom's "Big Smart" SCDMA wireless service. SCDMA incorporates advanced technologies, such as smart antenna, software radio, and synchronous wireless access protocol, to target a Chinese market projected to grow from 3 million users in 2005 to over 20 million by 2007. This extremely complex application requires six different voltages, from 1.3 to 3.3VDC, with peak currents approaching 60 amps.

Xinwei's Chief scientist, Dr. Guanghan Xu commented, "Using the Z-Series graphical user interface, we were able to configure a power system in less than ten minutes.

This is extremely impressive considering that the diverse range of functionalities we implemented included paralleling, turn-on cascading, and fault management. Z-One Digital Power saved weeks of design time compared to analog power management. The complex power requirements of our base station control board, combined with our need for on-the-fly reconfiguration, would have been extremely difficult to support without Power-One's revolutionary Z-One Digital Power."

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

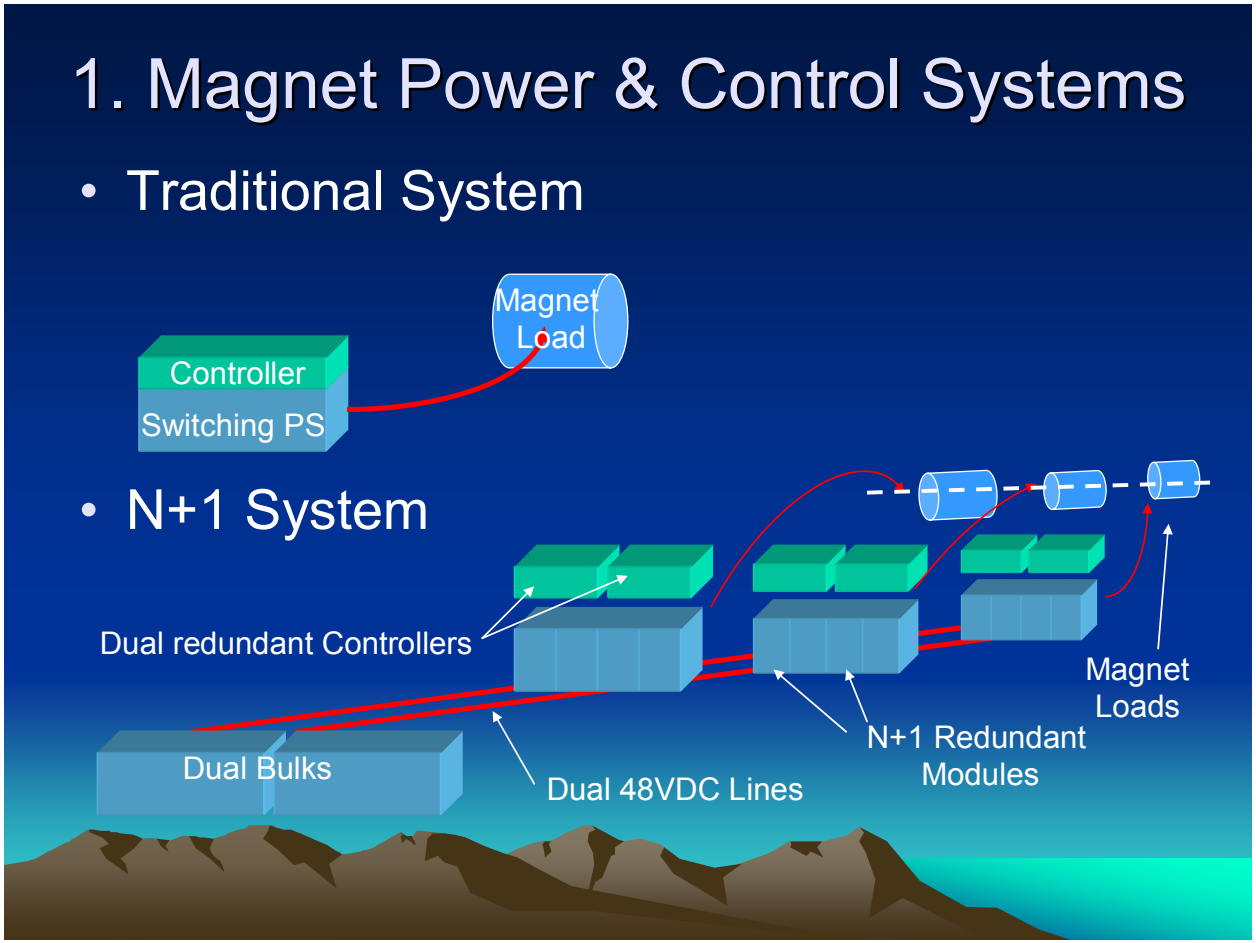
III-2. HA High Power Systems R&D

- *Pulsed & DC Power Systems are major limitations to achieving High Availability in current machines.*
  - *HA principles being applied to all ILC power systems.*
  - *Goal is >0.99 for RF Power System, DC Magnet Power System*
- 1/n Redundancy at 3 levels in Magnet PS, Modulators & Kickers:
  - *High current/power switches*
  - *Modular construction*
  - *System level or Unit level hot spares or hot-swap*
- Intelligent Diagnostics Layer
  - *Minimize Mean Time to Repair, monitor health at card level.*

- *Goal: Keep operating with 1-2 failed cells; change failed cells while machine keeps running if possible.*

III-2. DC Magnet Power & Control Systems

- *For A=0.99, need redundant Bulk, Modules & Controllers*



**Modular Supplies <1 to 60 kW*
**Current stability to .01% typical.*
**Strings & Single magnet applications*

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

III. Marx Modulator

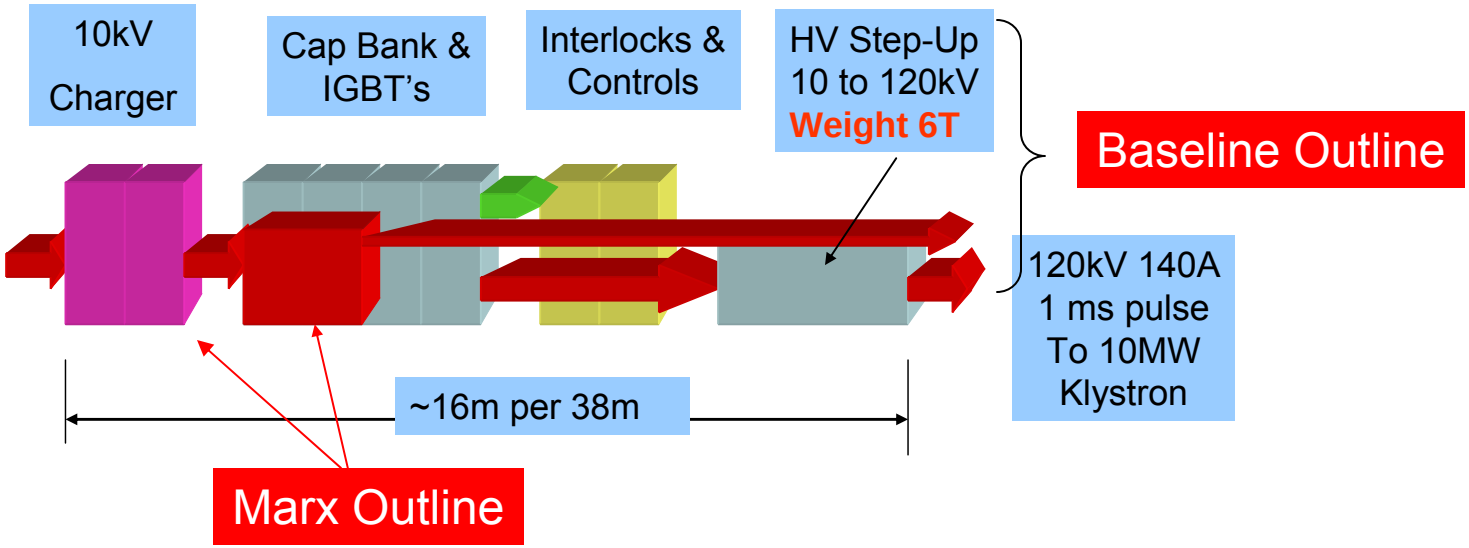
- Being investigated as alternate design to present switched cap "Bouncer" design

Goals:

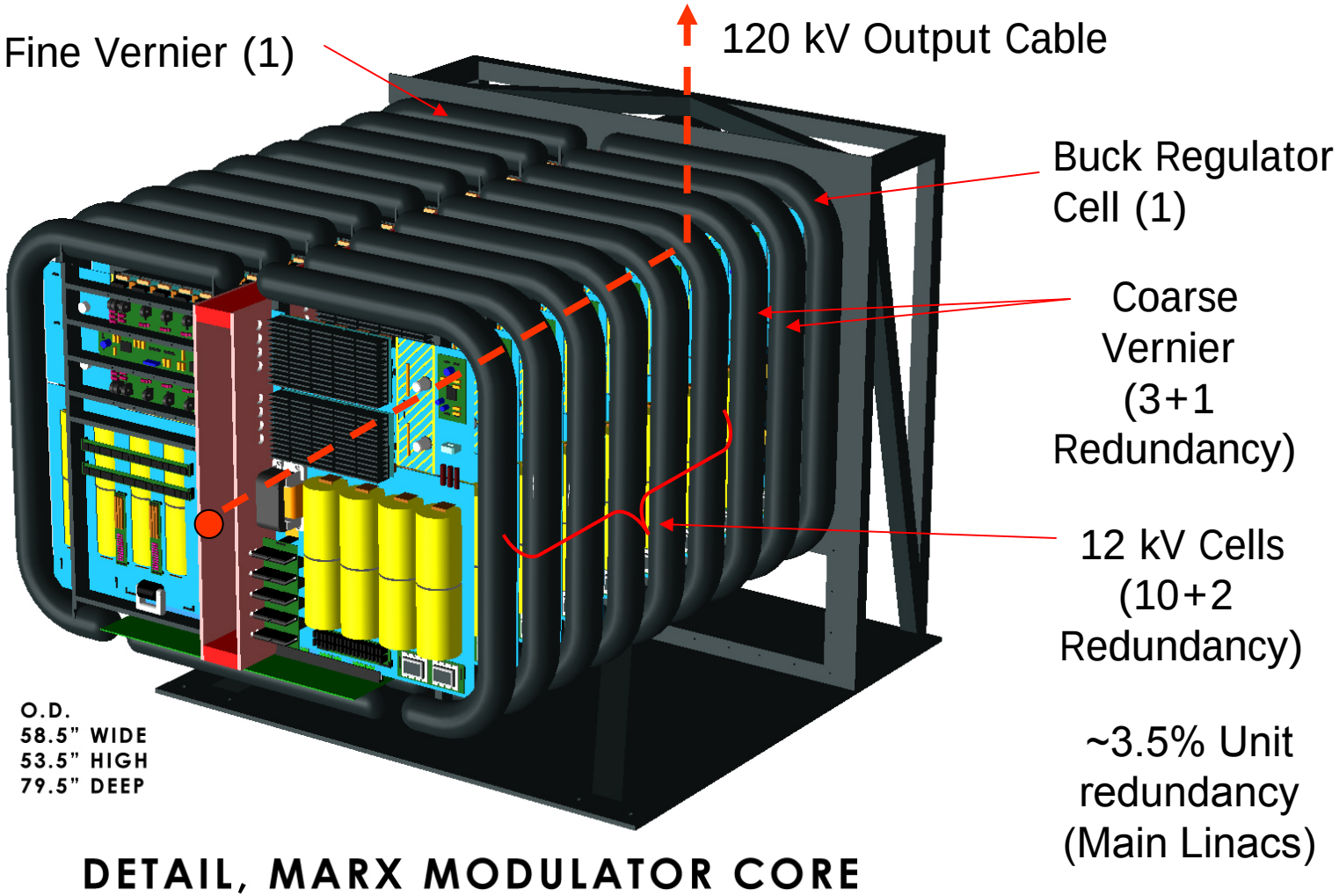
Reduce size, weight, space by 3-4X
Reduce cost by >2X
Increase efficiency
Demonstrate operation in 2007.

Specifications:

120 kV, 140 A, 1.63 ms, 5 Hz
125 kW output power to klystron
Efficiency from wall-plug ~90%

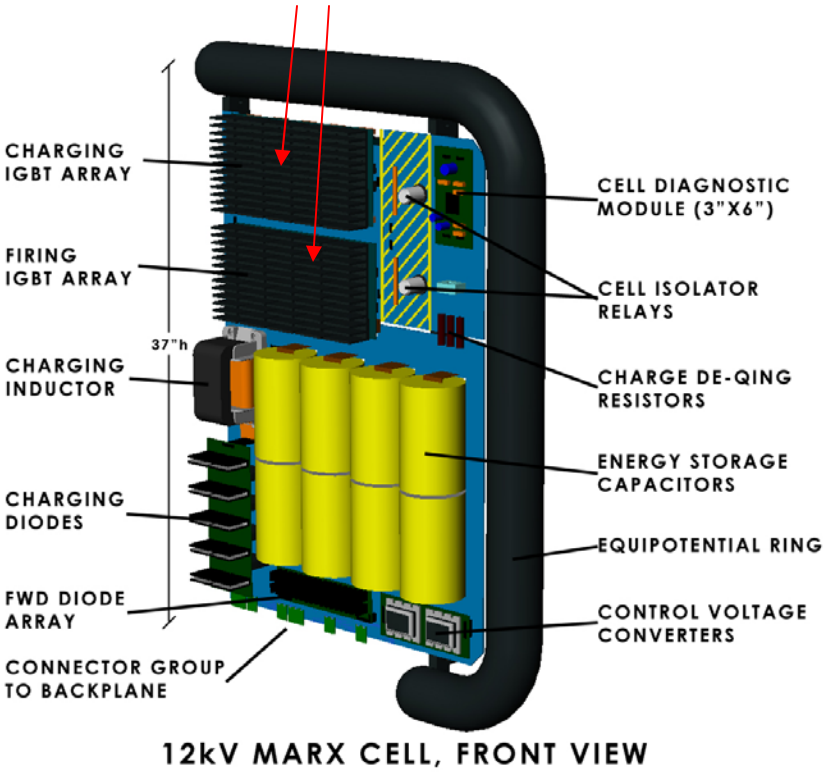


III. Marx Assembly Overview*



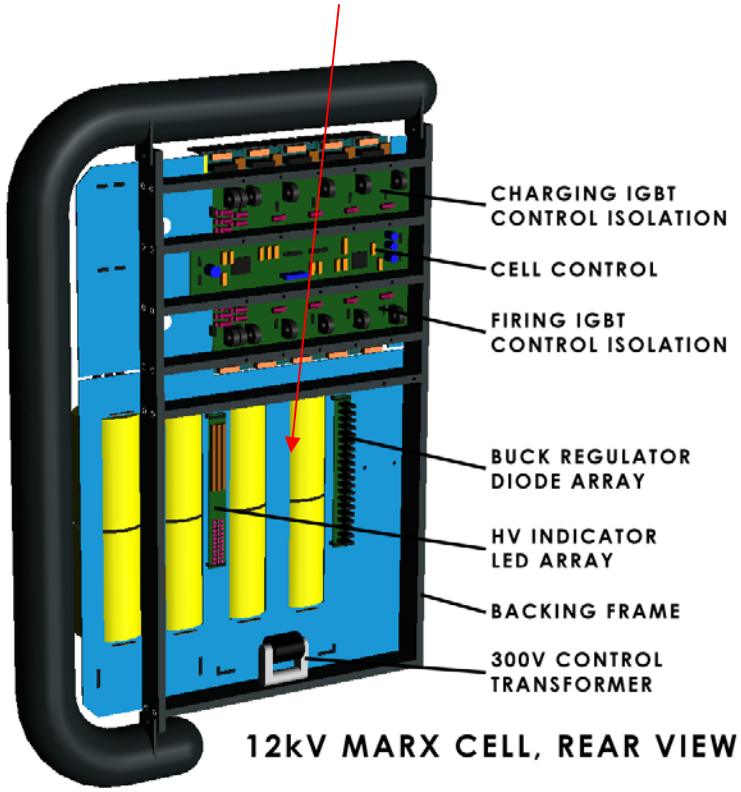
III. 12 kV Cell Detail*

4+1 Redundant Switch Arrays for charge, discharge



12kV MARX CELL, FRONT VIEW

6+2 Redundant Capacitors



12kV MARX CELL, REAR VIEW

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

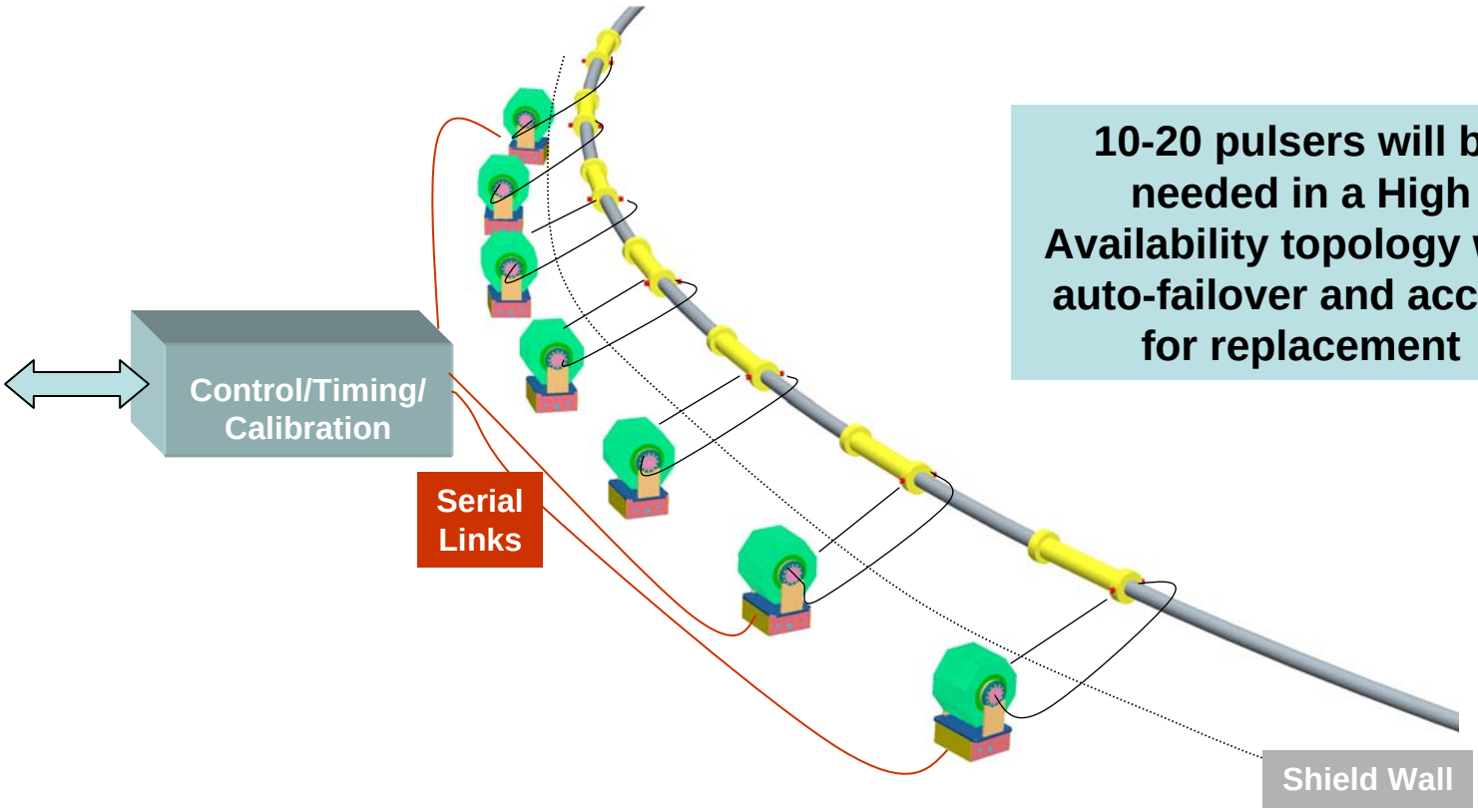
III-4. Damping Ring Kickers

- Damping Ring pulser performance directly related to size of the rings.
- Currently assuming can operate with 6 km circumference largely based on extrapolations of pulser performance.
- Architecture requires a large number of stripline pulsers to develop total kick.

III-4. Damping Ring Kickers

- Goals:
  - *Reduce size, cost of damping rings with 20 nsec beam interleave performance.*
  - Limit size of DR to ~ 6 km circumference.
- Specifications:
  - *Tr, Tf 1ns to +/-5-10 kV,*
  - *3 MHz constant beam extract rate*
  - *Amplitude matching, timing to <0.1% stability long term*
  - *Multiple units needed in tandem*

III-4. Kicker System Topology



10-20 pulsers will be needed in a High Availability topology with auto-failover and access for replacement

Dwg by C. Brooksby BN/LLNL

III. Power Systems Architectures

- 1. Crate & Card-Level Power Systems
- 2. DC Magnet Constant Current Power Supplies
- 3. Marx Klystron Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer (DIL)

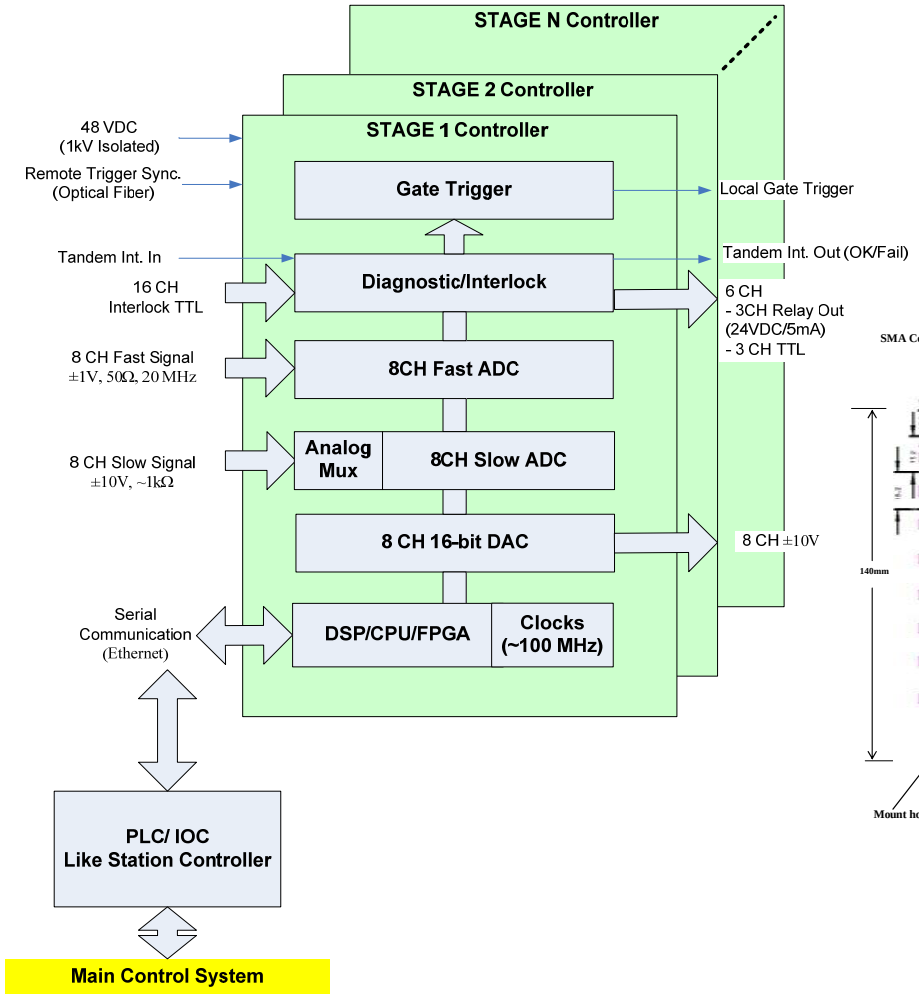
III-5. Diagnostic Interlock Layer

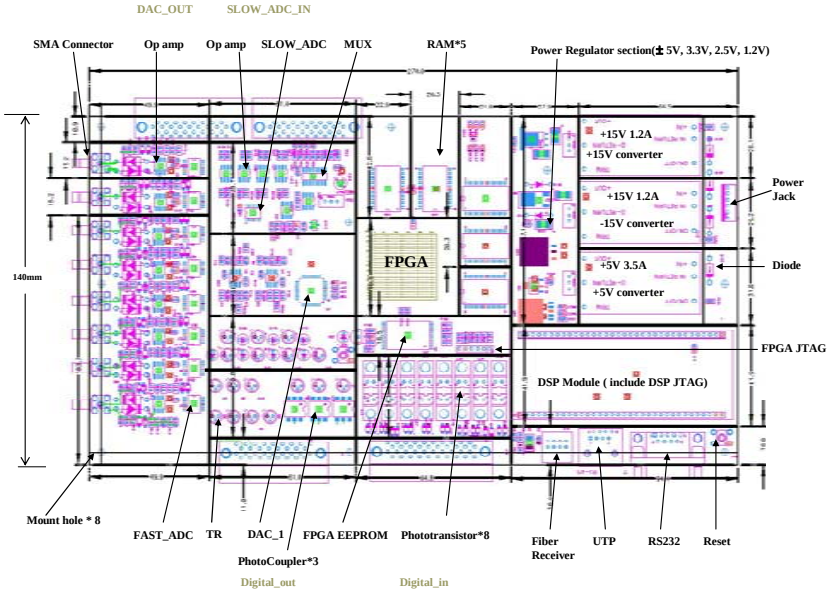
- DIL Goal: Help achieve near-zero MTTR
  - *All power systems will have a "DIL" card or hybrid circuit in each power cell.*
    - Similar in function to ATCA Shelf Manager for Controls crates but with added controls features such as interlock management, waveform capture and memory.
  - *Gathers diagnostic information to view in control room: Interlock set points vs. actual levels; fast and slow waveforms.*
  - *Enables evasive action to avoid trips: Reduces load, adjusts set points if permitted; "safes" system in case of failure.*
  - *Manages Hot-Swap operation if feasible or module swap operation in case of trip.*

III-5. Diagnostic Interlock Layer Concept

- DIL Functions (Typical)
  - *Combination digital controller and memory of small size imbedded into power circuits such as power supplies, modulators*
  - *Captures power conversion waveforms in ADCs to detect early failures in switching circuits*
  - *Captures fast & slow waveforms, stores recent results to local memory*
  - *Monitors interlocks, controls trip settings*
  - *Monitors temperatures of critical components*
  - *Provides fast timing and trigger control & monitoring*

III-5. DIL Prototype Functional Design





Courtesy S. Nam, Pohang Light Source

IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV-1. ATCA Collaboration R&D

- Hardware/software tests of starter kit, shelf manager, auto-failover of controllers, VME adapter development
  - *SLAC with University of Illinois*
- Control system architecture, hardware & software modeling, commercial product search, integrated system search, racks & cooling
  - *ANL, FNAL, SLAC*
- ATCA Adaptation to front end instruments for LLRF, Detectors
  - *DESY, FNAL, BNL, Yale*
- Overall system cost estimates
  - *ANL, FNAL, DESY, KEK, SLAC*

IV. Ongoing HA R&D Programs

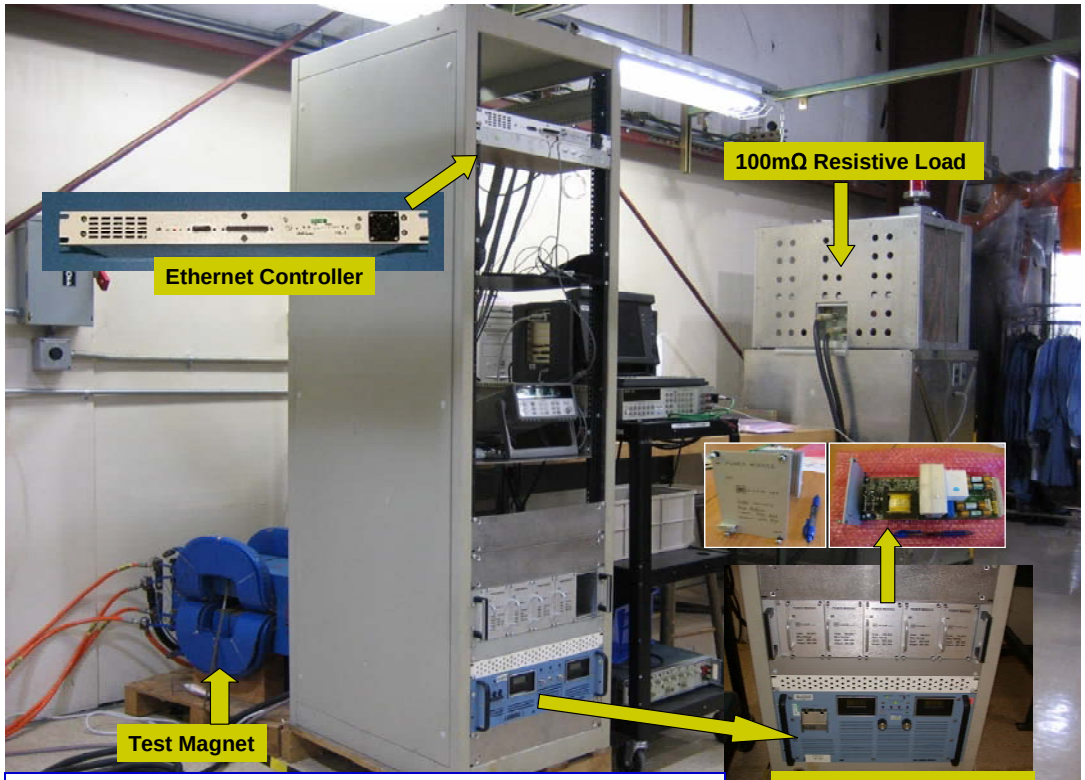
- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV-2. DC Magnet Power Systems

- Study of commercial products in prototype 5kW system to demonstrate redundant N+1 architecture, auto-failover, current sharing stability
  - *SLAC*
- Application to system of 41 magnet supplies for ATF2 at KEK
  - *SLAC with KEK, due to complete in 2008*
- Development of dual redundant diagnostic controller for magnet supplies
  - *SLAC*
- Study of low voltage commercial products for crate, board level applications
  - *SLAC, RW Downing Inc.*

IV-2. Magnet PS Prototype R&D

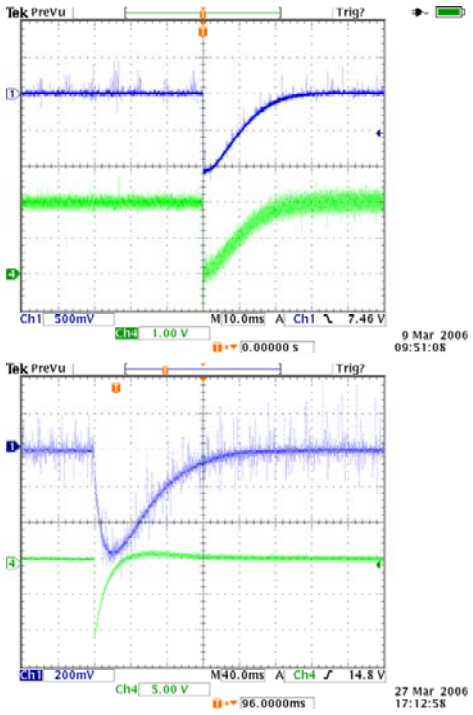
- Approx. 18,000 magnets & supplies in all systems
- FY07-09 Goals: Demonstrate all HA features on multiunit test system in KEK ATF2.



Prototype Test n/N Auto-Failover

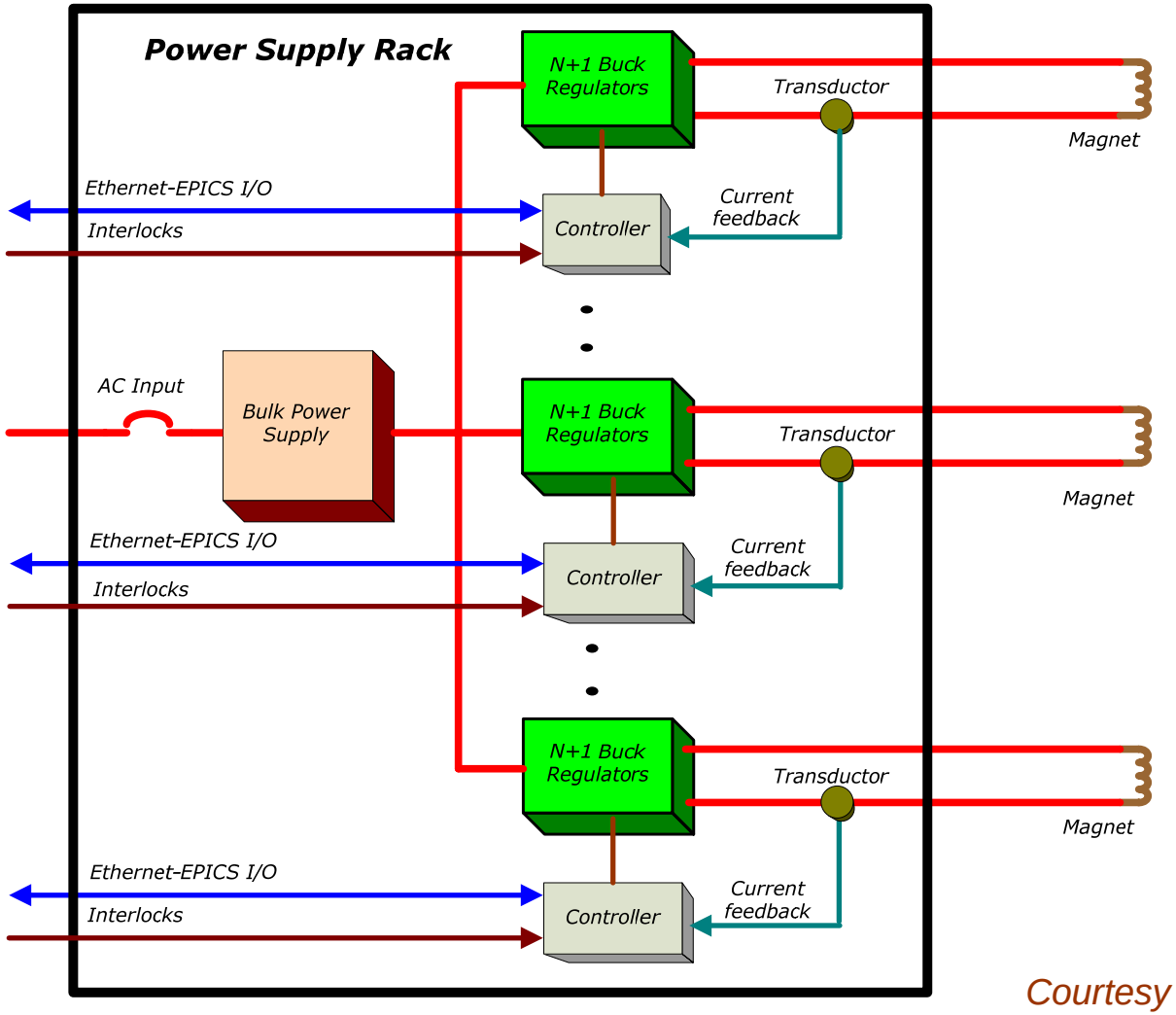
P. Bellomo & B. Lam

Transient Recovery
1 Module Switched Off



Top: Resistive Load, 10 ms/cm
Bottom: Magnet Load +100mΩ, 40 ms/cm

Typical System Block Diagram



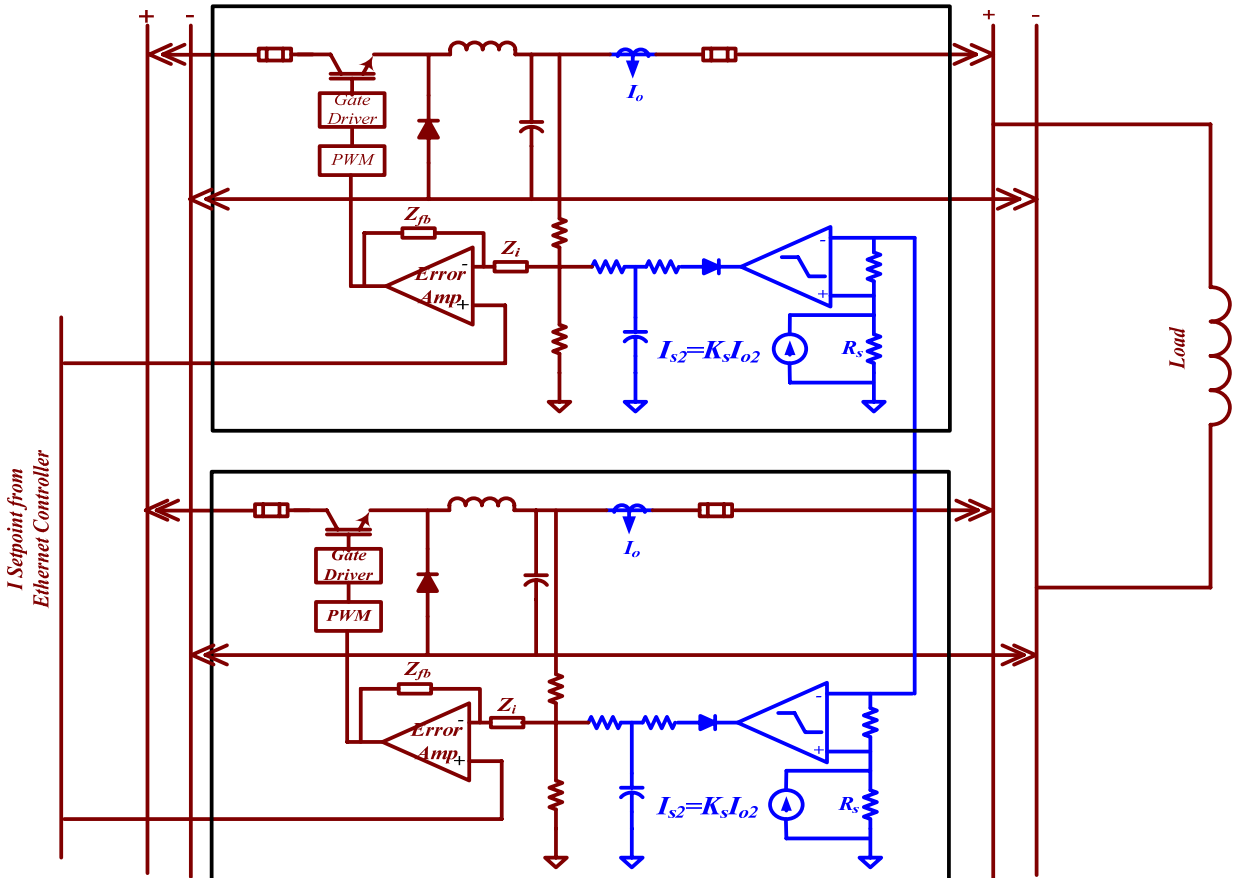
Courtesy P. Bellomo & B. Lam, SLAC

Bulk Power Supply Mfgrs

Elgar Electronics Corporation
9250 Brown Deer Road
San Diego, CA 92121
Website: www.elgar.com
IE Power
12 Falconer Drive, Unit 15
Mississauga, Ontario
Canada L5N 3L9
www.iepower.com
Lambda-EMI
Aroma Square Bldg 5F
Kamata, Ohta - Ku
Tokyo 144-8721 Japan
www.densei-lambda.com
***Matsusada** - Shiga Headquarters*
745 Aoji-Cho,
Kusatsu -City, Shiga, 525-0041
Japan
www.matsusada.com

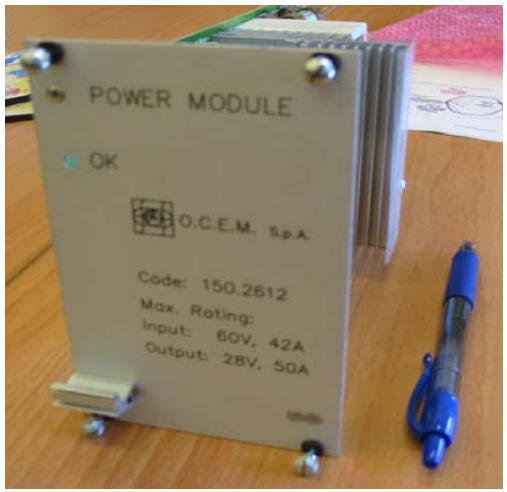
Courtesy P. Bellomo & B. Lam, SLAC

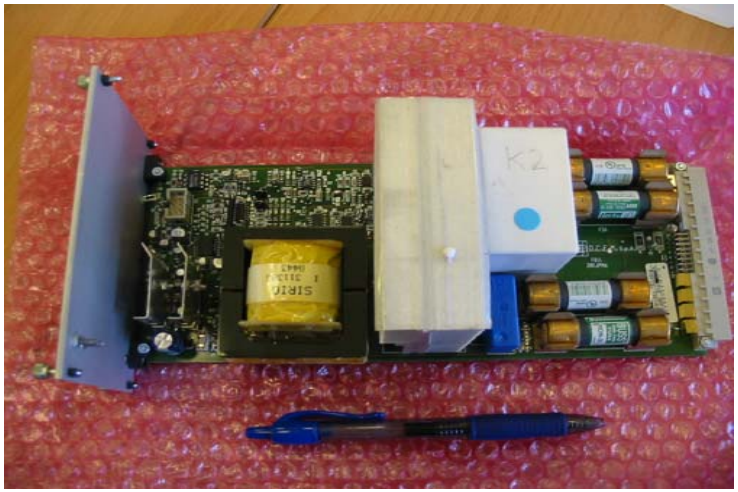
Democratic Current Share Circuitry



Courtesy P. Bellomo & B. Lam, SLAC

Commercial Power Modules





- *Purpose – current regulation of magnet current*
- *All 20V, 50A*
- *Parallel for current share and redundancy*
- *OCEM Italy IE Power Canada*

Courtesy P. Bellomo & B. Lam, SLAC

Ethernet Power Supply Controller

Note: Dual Redundant Controller with DIL features development started 2007

Purpose

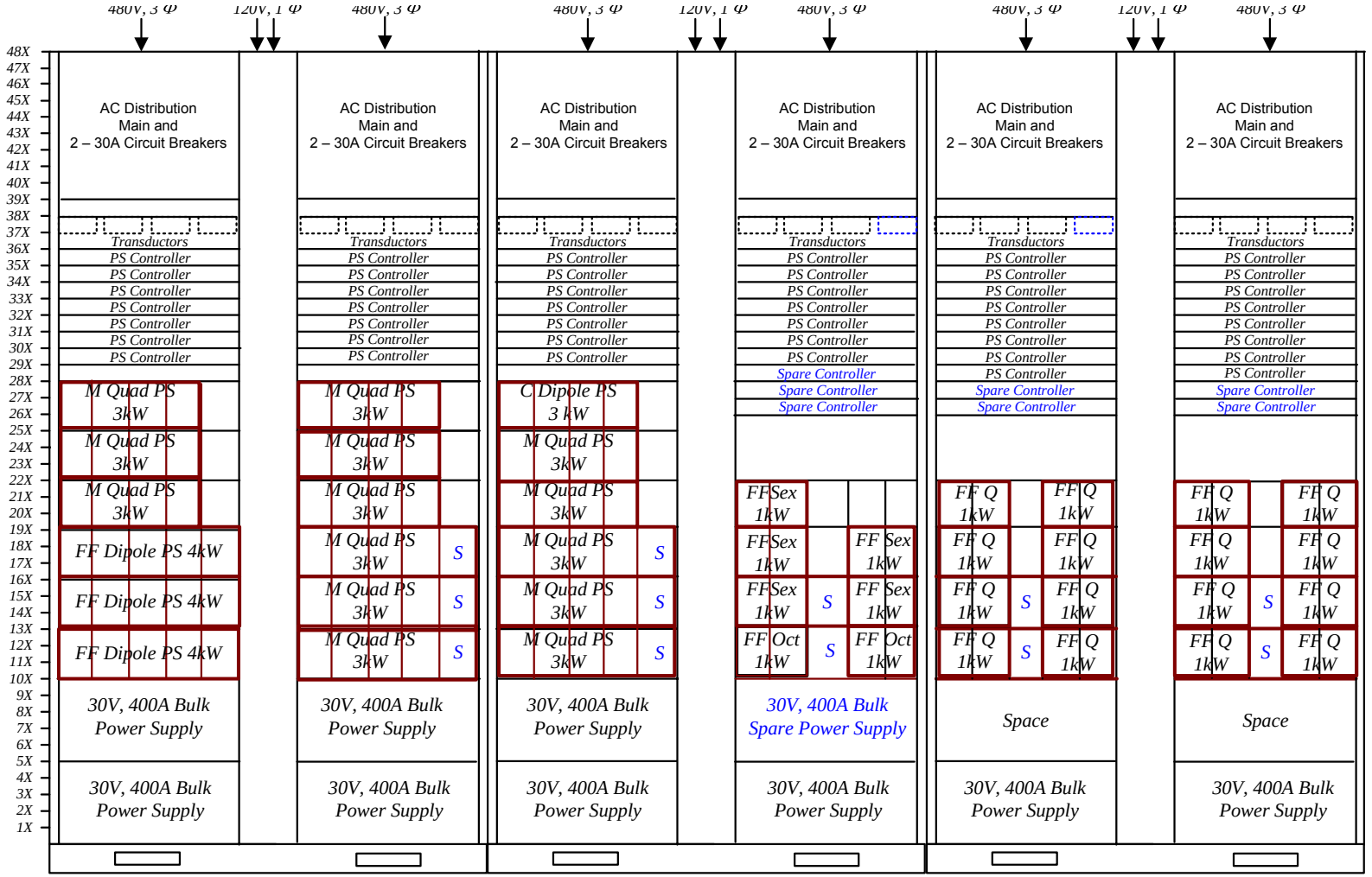
- *Interfaces remote computer to power supply*
- *Closed loop control for current setting and regulation*

Features

- *Integrated EPICS IOC*
- *100Mbps TCP/IP communications via UDP protocol*
- *SLAC-Built for PEP and SPEAR, ≥300,000h MTBF.*
- *Controllers slated for LCLS project use.*

Courtesy P. Bellomo & B. Lam, SLAC

Configuration of 41-Supply System



Courtesy P. Bellomo & B. Lam, SLAC

IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV-3. First Marx Assembly Underway

IV-3. 8-Cell Output Waveforms

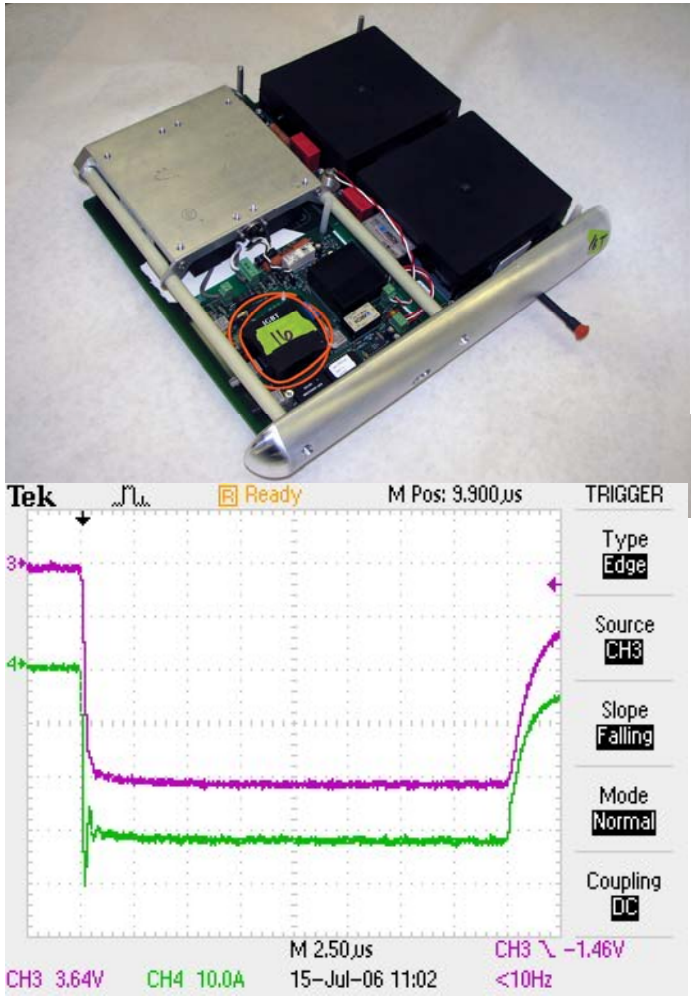
Goal: 120 kV
Reached:
80kV
1/25/07.

Courtesy G. Leyh, SLAC

Industrial Marx Efforts

- Two industrial SBIR's underway (Phase I).
- One company received contract for military agile radar application & successfully lab-tested first unit.
- Similar in power to ILC Marx, but shorter (variable width) pulse, higher (variable) trigger rate, lower voltage (90 kV max c.f. 120 kV for ILC.
  Significant demonstration of viability of Marx.

Commercial Marx Demonstration



•Output Specifications:
Resistive Load
90 kV 50A
100µsec 125 kW

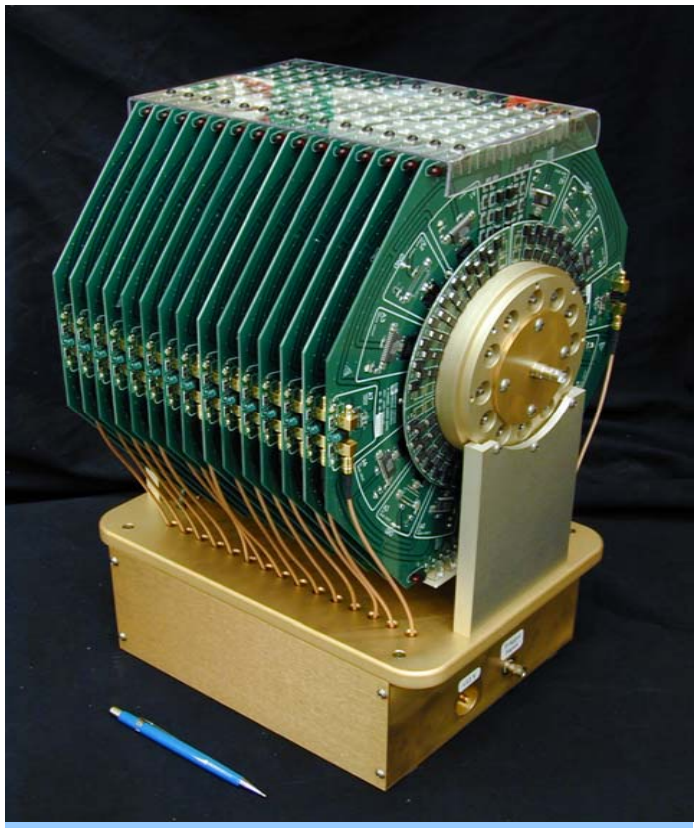
•Waveforms shown:
Klystron Load
81kV ~30A
20µsec

Courtesy R. Cassel, SLAC & Stangenes Industries, Palo Alto CA.

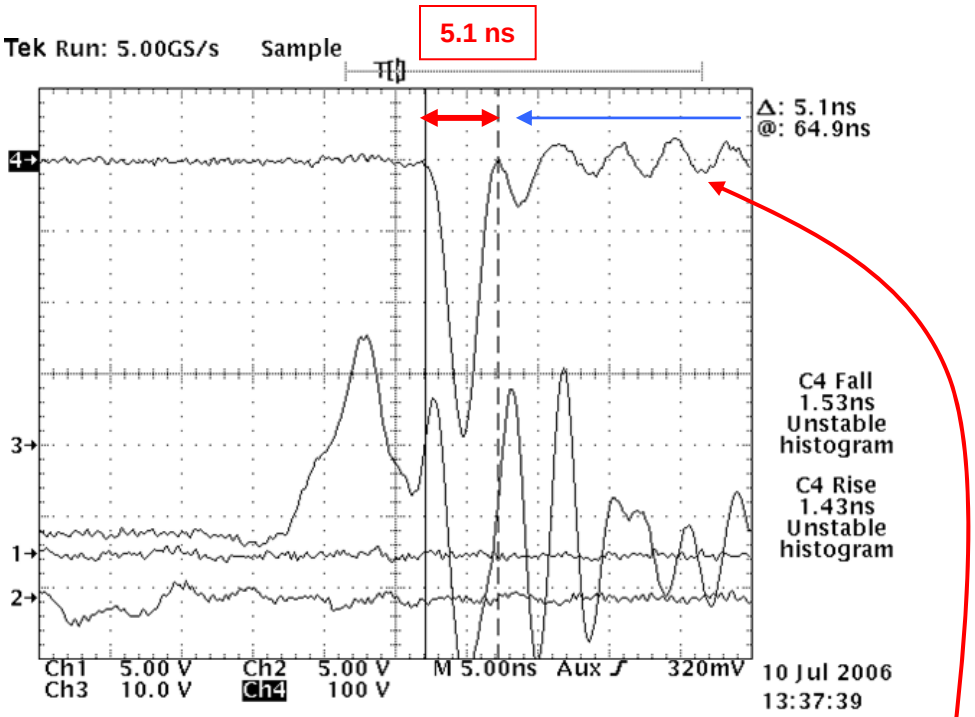
IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

IV-4. LLNL Induction Kicker



LLNL Kicker Tested at KEK ATF



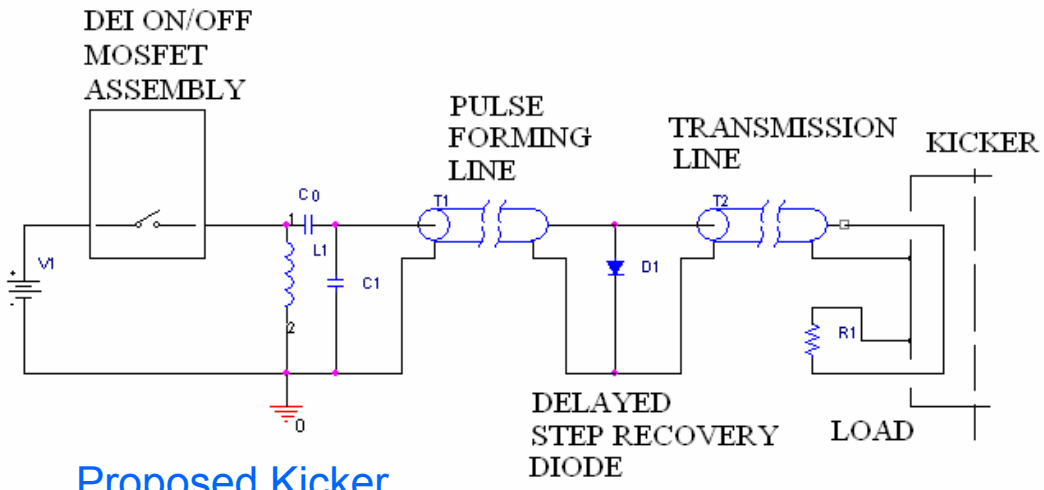
- Unit has 15 MOSFET-driven induction cells
- Type C Coax cables connected to each side produces +/-8 kV bipolar pulses
- Does not yet achieve desired Tr, Tf, clean tail

Courtesy E. Cook LLNL

IV-4. DSRD R&D

- Parallel R&D started on *Drift Step Recovery Diode (DSRD)* circuit, possibly using Induction unit as "pump."
- Tr, Tf of 1-2 nsec 5 kV into 50 Ω demonstrated on bench.
- Note- DSRD's used are samples. Commercialization is in progress.

Packaged Unit
Ioffe PTI,
St. Petersburg

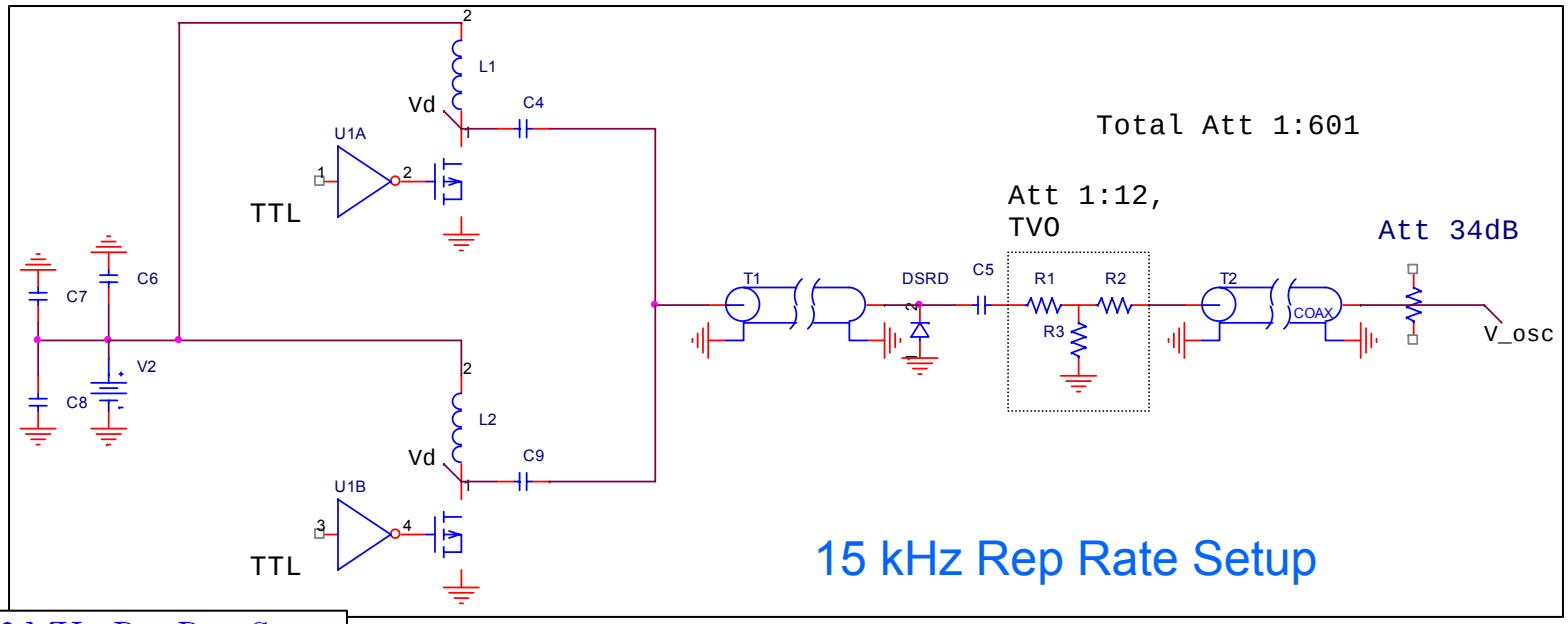


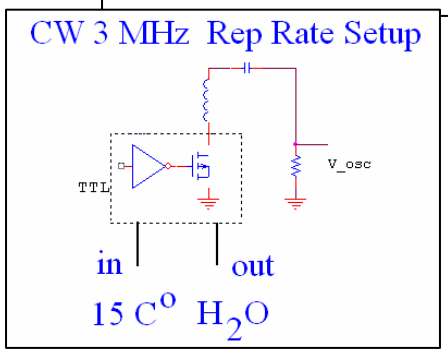
Proposed Kicker
(one side shown)

Courtesy A.Krasnykh, SLAC &

A. Kardo-Sysoev, Ioffe PTI

IV-4. DSRD Test Circuits

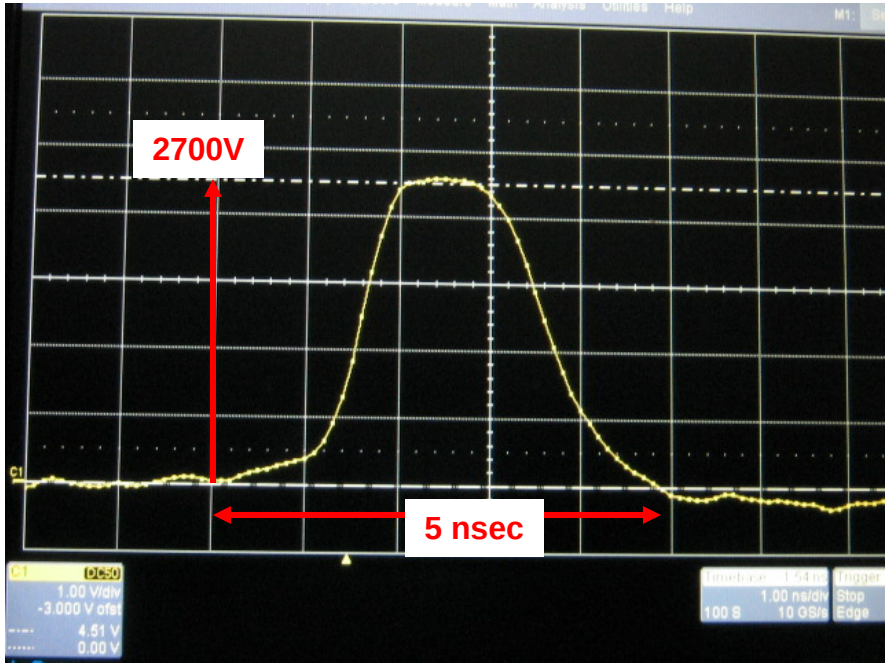


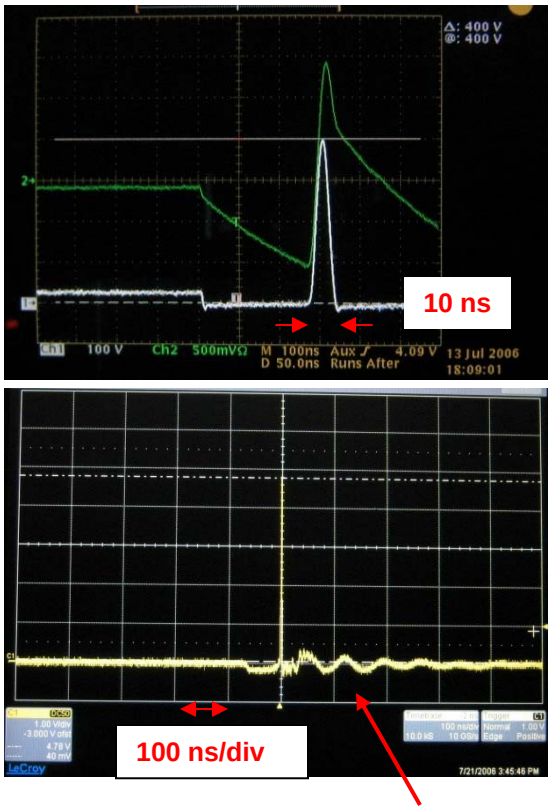


Courtesy A.Krasnykh, SLAC

A. Kardo-Sysoev, Ioffe PTI

IV-4. Test Circuit Waveforms





A_out = 4.5 x 600 = 2,700 V H=1 ns/cm

LeCroy @ 10GS/s

Tail effects need to be reduced

Courtesy A.Krasnykh, SLAC

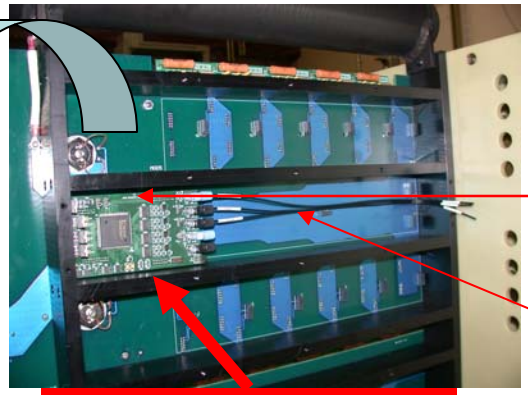
A. Kardo-Sysoev, Ioffe PTI

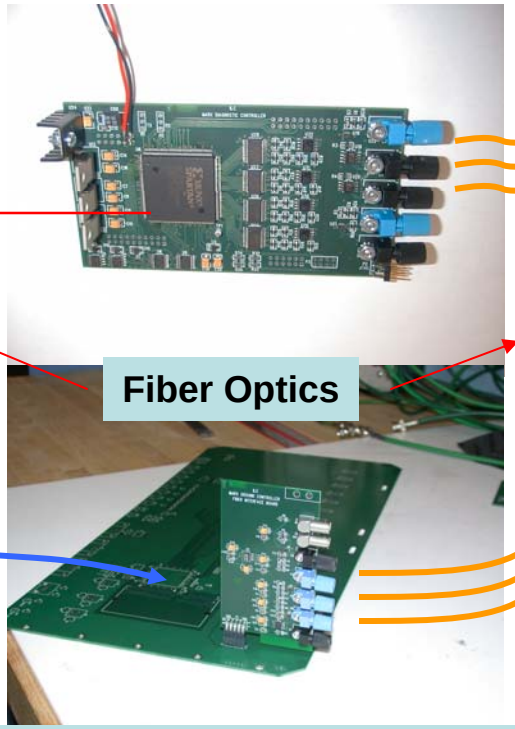
IV. Ongoing HA R&D Programs

- 1. ATCA Evaluation
- 2. DC Magnet Power Systems
- 3. Marx Modulator
- 4. Damping Ring Kickers
- 5. Diagnostic Interlock Layer

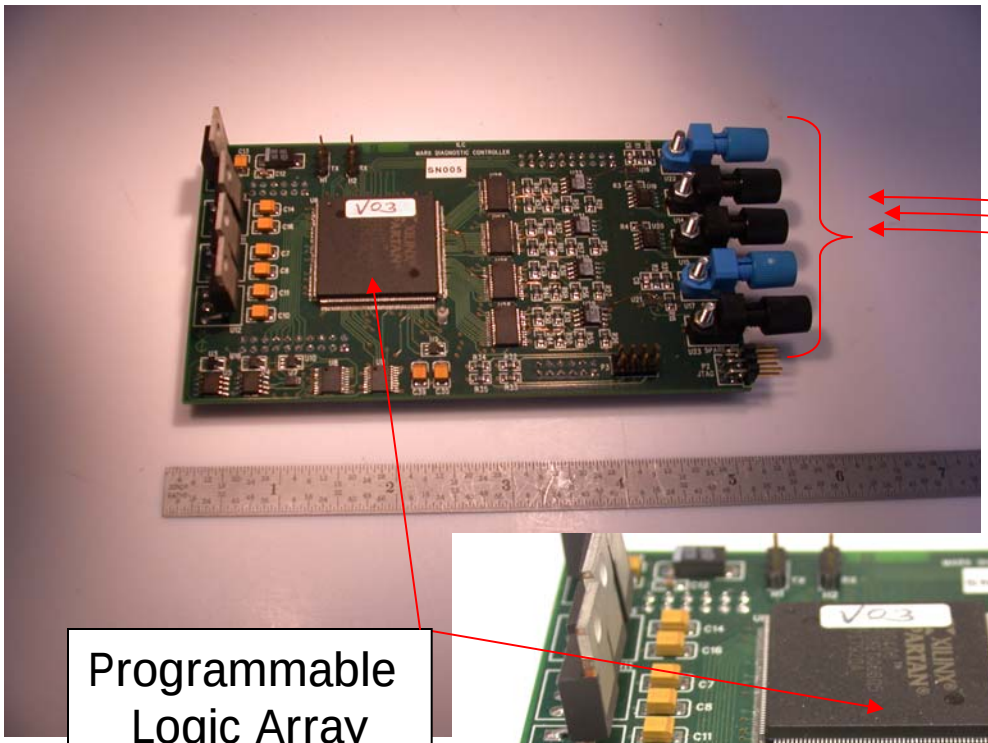
IV-5. Marx DIL Controller

- DIL had to be designed for very low power
- Operates on cell control power from charged capacitor
- Board floats up to 120 kV at output (*80 kV achieved to date*)



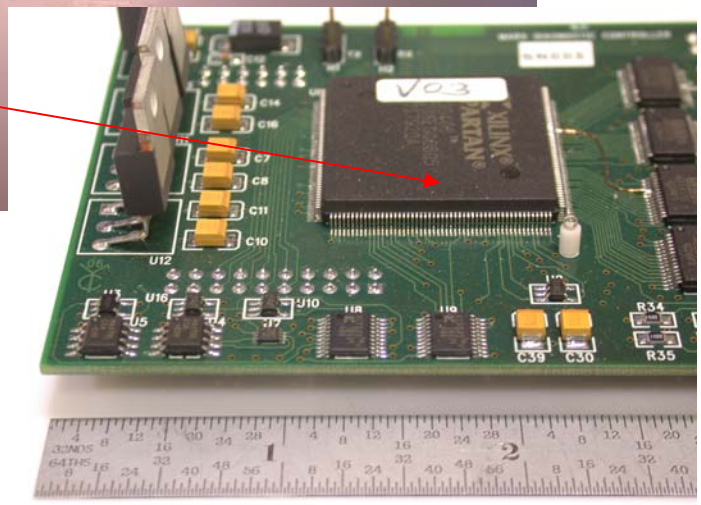


IV-5. DIL Controller Details

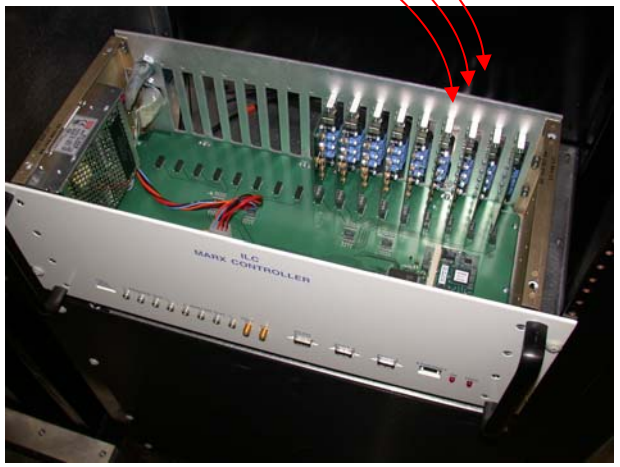


Dual Fiber Optic Timing & Data Links

Programmable Logic Array



Duplex Timing & Data Channels Each Cell (Mounted on Rear)



16 Ch Ground Station

V. Conclusions-1

"Design and build systems that do not interrupt machine operation when components fail."

- HA design strategy well accepted in the ILC
  - *ILC 10 times larger than largest comparable machine (SLAC)*
  - *Cannot meet machine up-time goals without HA, ~10X improvement.*
  - *Full machine goal of A>0.85 requires all electronics subsystems to strive for → 0.999*
  - *HA applies to all systems, not just electronics*
- *A → 0.999 is achievable* with combination of strategies
  - *N+1 redundancy tolerates faults without immediate interruption*
  - *Modular design for quick replacement of faulty unit (minimize MTTR)*
  - *Auto-failover for networks carrying critical control, RF and timing signals*
  - *Hot-Swap of modules using shelf manager or DIL to detect, isolate, quickly repair.*
  - *Improved, pervasive diagnostics through DIL crucial to overall success*

V. Conclusions-2

- Evaluation of ATCA Platform is Critical
  - *ATCA platform offers ready solution to many controls, instrument applications.*
  - *Industrial effort to design ATCA could never have been undertaken by labs as in past standards efforts.*
  - *Advances in chip technologies, rapid change demand a modernized platform for physics*
  - *Large Telecom market for ATCA promises affordable core product solutions for labs.*
  - *Shelf manager, HA software design pose largest problem for controls and instrumentation.*
  - *Industrial software and hardware solutions growing rapidly, will offer useful solutions to physics systems.*

ATCA Workshop – IEEE RT2007 Conference

Fermilab - 4/29-5/6/2007

V. Conclusions-3

- ILC offers exciting opportunity to frame the next- generation challenges. However:
  - *Engineering needs to develop effective collaborations due to size of challenges and relative shortage of experts.*
  - *Collaboration needs to evolve with other large projects such as ITER, ATLAS Upgrade (starting).*
- The Laboratory HA Challenge
  - *Need R&D to decide feature set, evaluate suitability of ATCA as instrument platform, prototype all critical hardware-software applications.*
  - *Labs need to build strong international collaboration of electronics experts to meet future challenges in both machines and detectors.*
  - *Learning to take advantage of ATCA features requires large investment especially in software systems.*

Acknowledgment

- Besides those acknowledged on the slides, a large team has actively contributed to the High Availability electronics program. The laboratories involved besides SLAC are Argonne, Fermilab, Lawrence Livermore, KEK, DESY, Pohang, University of Illinois (UIUC). R. W. Downing formerly of UIUC is a consultant for the program.