

Power distribution R&D for ATLAS sLHC upgrades

Maurice Garcia-Sciveres
Lawrence Berkeley National Lab

SiD tracking meeting

Power lines



- Problem of “long” distance electrical power distribution is not new
- The novelty is that “long” is getting shorter
- The relevant distance scale turns out to be the load operating voltage
- Wrong units? Voltage is driven by oxide thickness inside the IC: units of length.
- => Miniaturization inside IC also affects distances outside IC!
- Eventually all power distribution distances become “long” => can only be solved at IC level

ATLAS pixel detector cable plant

- Built in the traditional way

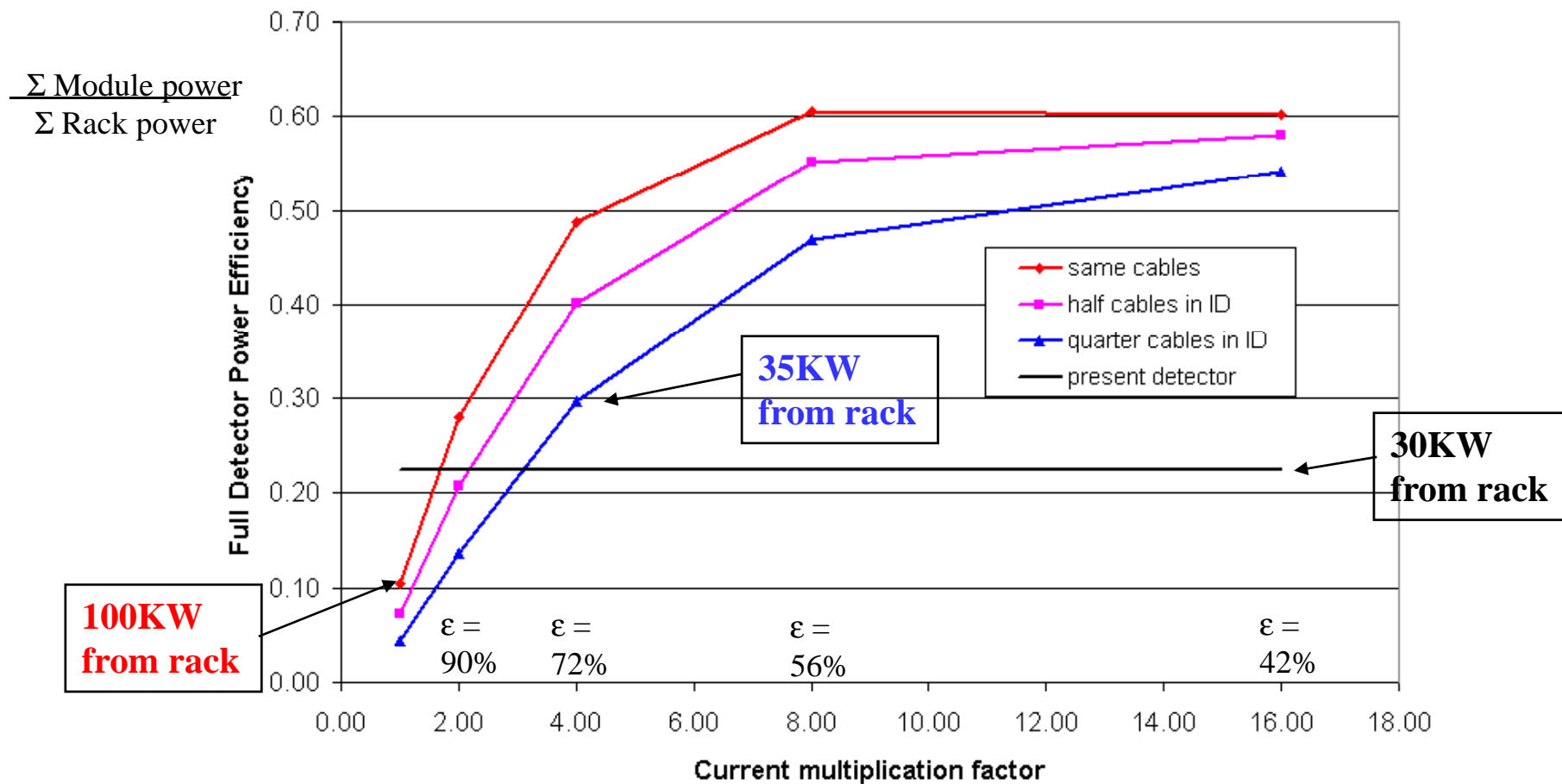


**10% of detector
(147 modules)**



Scaling from present pixel detector with same cable plant down to PP2

Power efficiency for pixel with 2x channels and 1.5V electronics



Existing efforts

- There is a combined ATLAS R&D proposal:
- Serial power:
 - SP demonstrator pixel modules have been produced at Bonn some time ago
 - Plan to make realistic serial power stave prototype in the near term
 - SCT implementing serial power with external regulators
 - More recent but also more prototyping work in SCT at present (RAL, LBNL)
- DC-DC
 - **Switched capacitor development at LBL**
 - 2 version of ASIC submitted 1 month ago
 - This should produce a real regulator ready to power SCT stave prototypes and pixel modules but late summer.
 - **Magnetic “buck” converter**
 - Work started by Satish Dawn of Yale >1 year ago. Evaluate commercial parts and options for industry partnership
 - Parallel effort started at CERN in 2006. Significant manpower. Plan is to design a magnetic regulator controller and build a regulator from the ground up
 - Need to evaluate AC magnetic field issues.

Why switched capacitors?

- Commercial DC-DC down-converters for power applications are all inductive.
 - (Switched capacitors used to step-up voltage at low power to drive displays, etc.)
- Why then study switched capacitors for power?
 - Cannot use ferrites in magnetic field => performance penalty for magnetic converters
 - Fringe AC magnetic fields may produce pickup in detectors (must study case-by-case)
 - Ceramic capacitor miniaturization makes great advances year after year (air-core inductors cannot be improved).
 - Over-voltage safety considerations

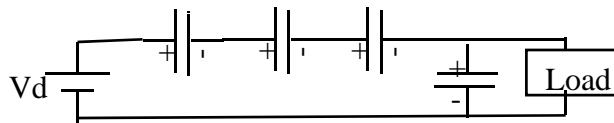
Switched capacitor credits

- IC design: Peter Denes
- Simulation: Bob Ely, Peter Denes
- Testing (so far only first prototype): Bob Ely, Seung Ji, Sami Hynynen, M. Garcia-Sciveres

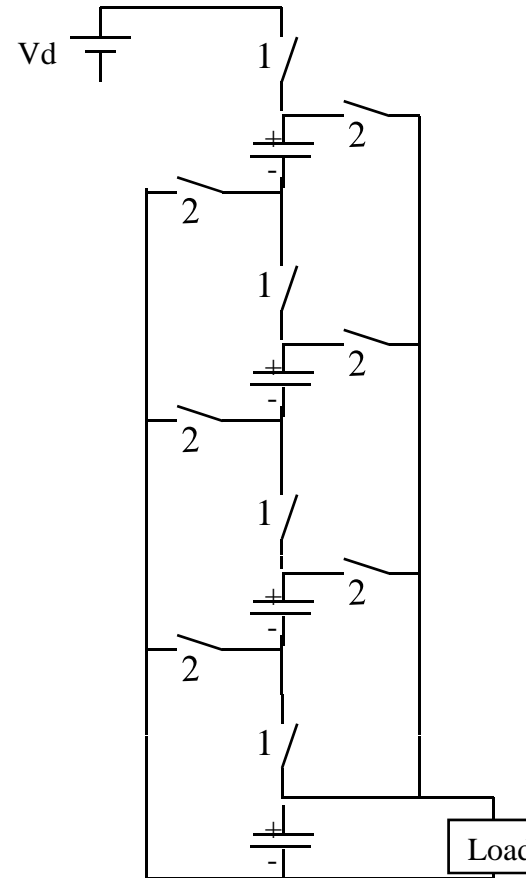
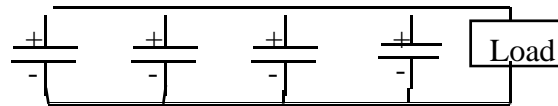
Test configuration used: divide-by-4 stack

4 capacitors – 10 switches

- Phase 1 - Charge



- Phase 2 - Discharge



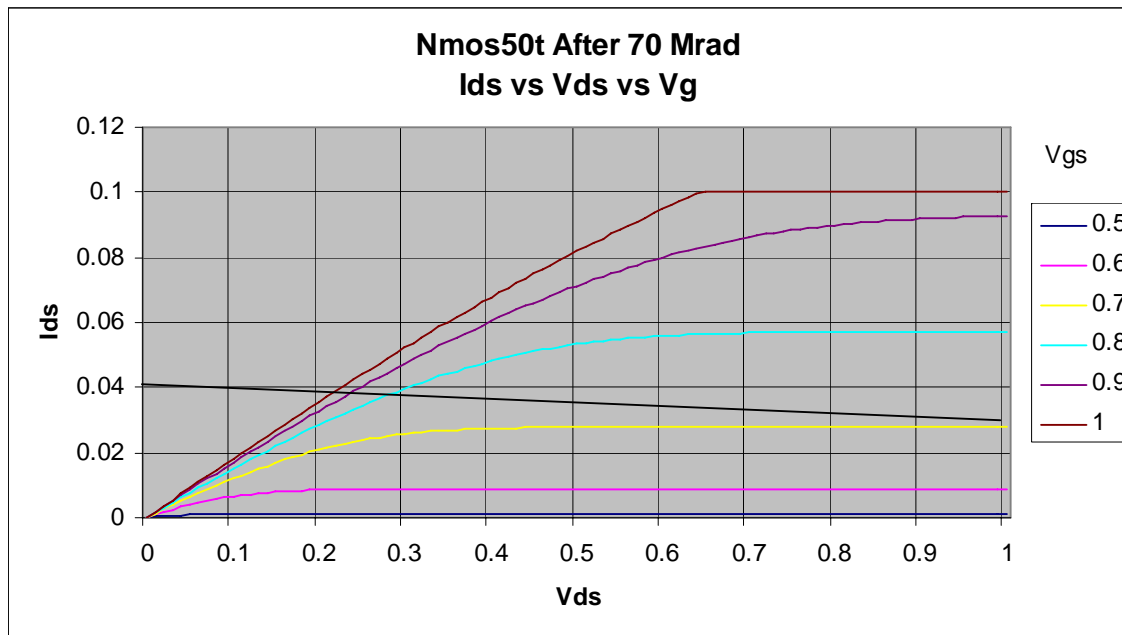
Other configurations

- Many capacitor arrangements are possible with different advantages
 - Minimum number of capacitors for a given ratio (less than for stack)
 - Minimum voltage drop across switches (more than for stack), etc.
- Problem has been solved in general:
Makowski, D. Maksimovic, "Performance limits of switched capacitor DC-DC converters," IEEE PESC, 1995 Record, pp. 1215-1221)

First prototype test chip

- 50V (s-d) 0.35 μ m HV CMOS process
- Minimum size (adequate for \sim 100mA)
- Switch transistors only- no auxiliary circuitry
- Learned about process simulation, radiation hardness, and bulk isolation
- Did not work as a useful converter due to bulk isolation problems
- Results presented at 12th Workshop on Electronics for LHC and Future Experiments, <http://ific.uv.es/lecc06/>

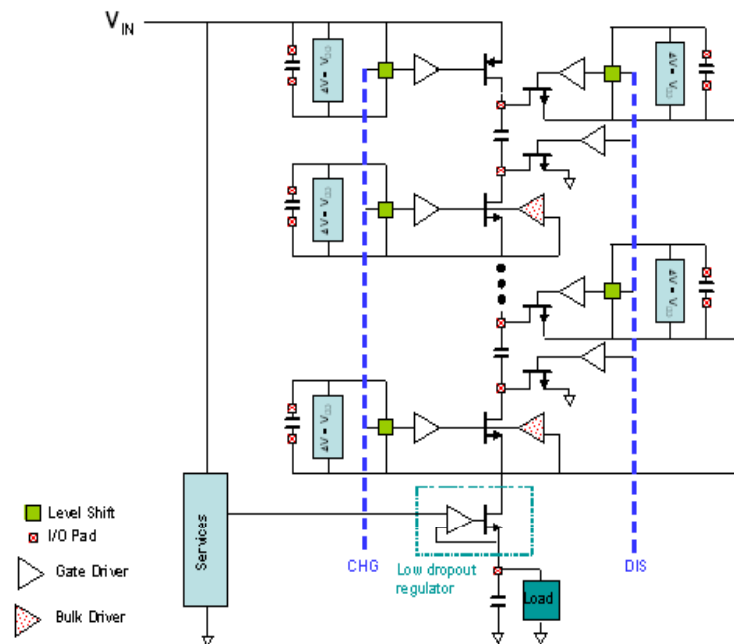
HV Transistor characteristics after irradiation



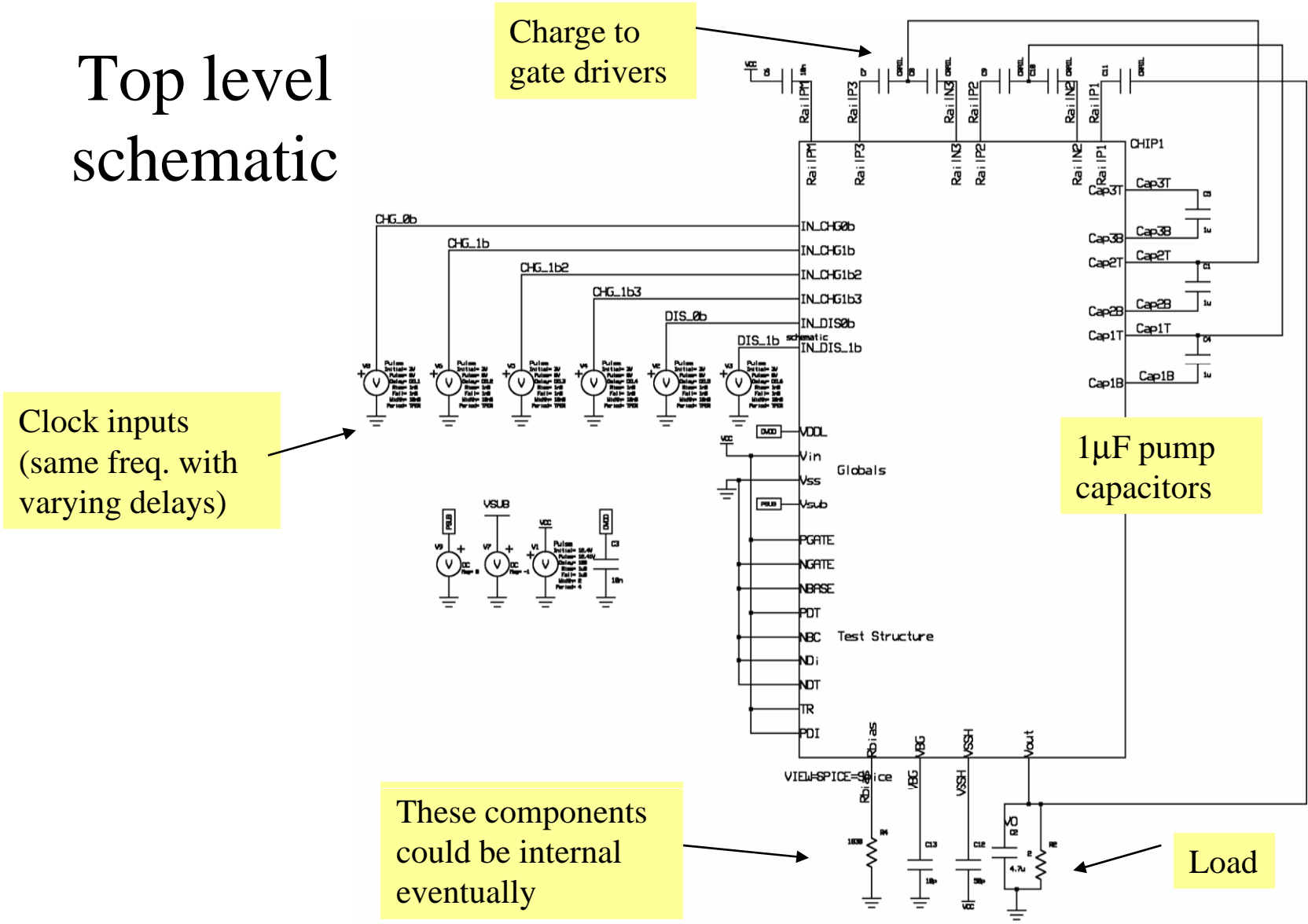
- The most important result is that the drain source resistance has increased by about 10%
- Measured R_{ds} also exceeded model predictions even before irradiation.
- => Increased switch size.

Second prototype

- Same 50V 0.35 μ m HV CMOS process
- Submitted February 2007 (expected back in May)
- Sized for 1A output.
4.3 x 4.9 mm
- Contains auxiliary circuits
- All capacitors external
- All clocks external



Top level schematic



Charge to gate drivers

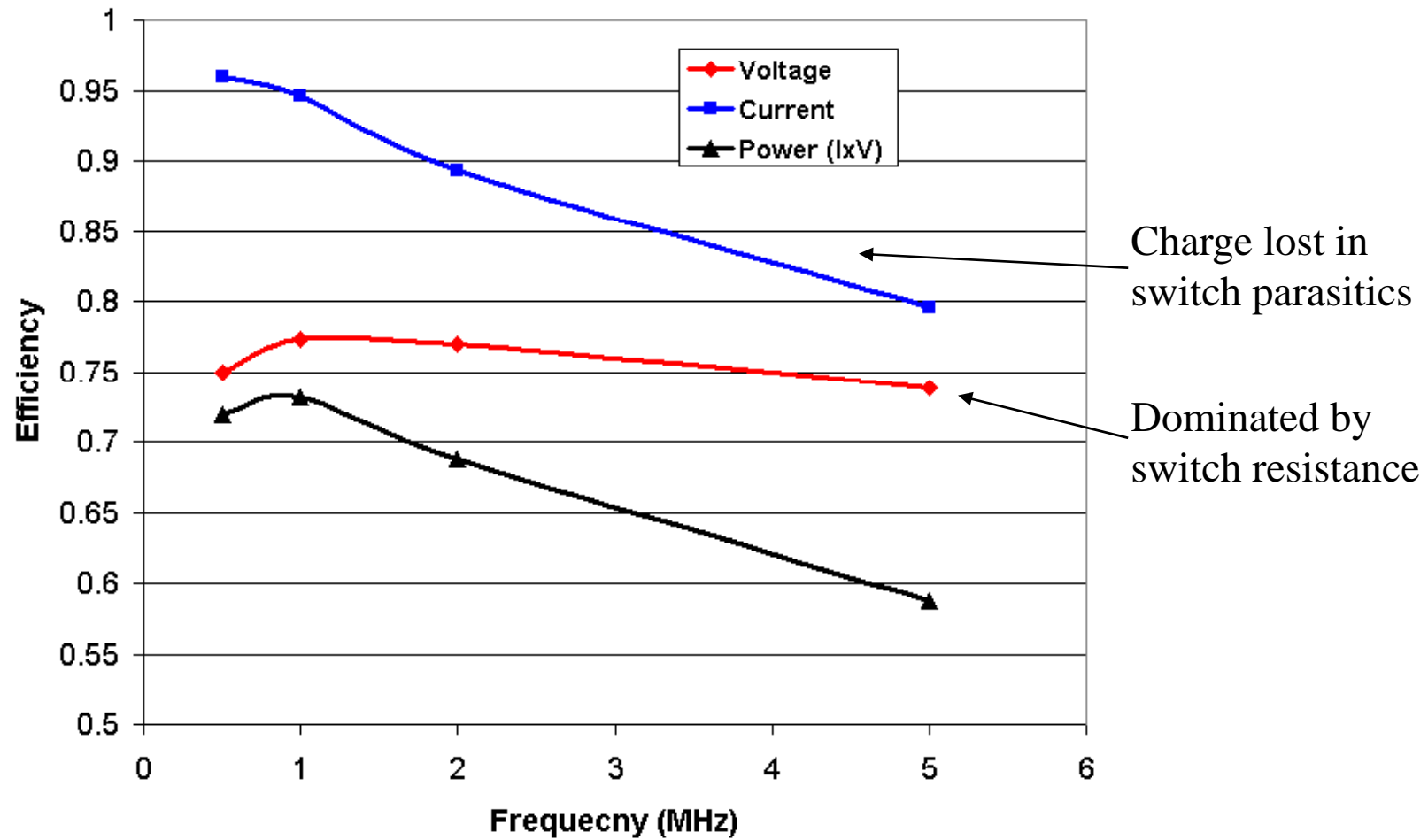
Clock inputs (same freq. with varying delays)

1µF pump capacitors

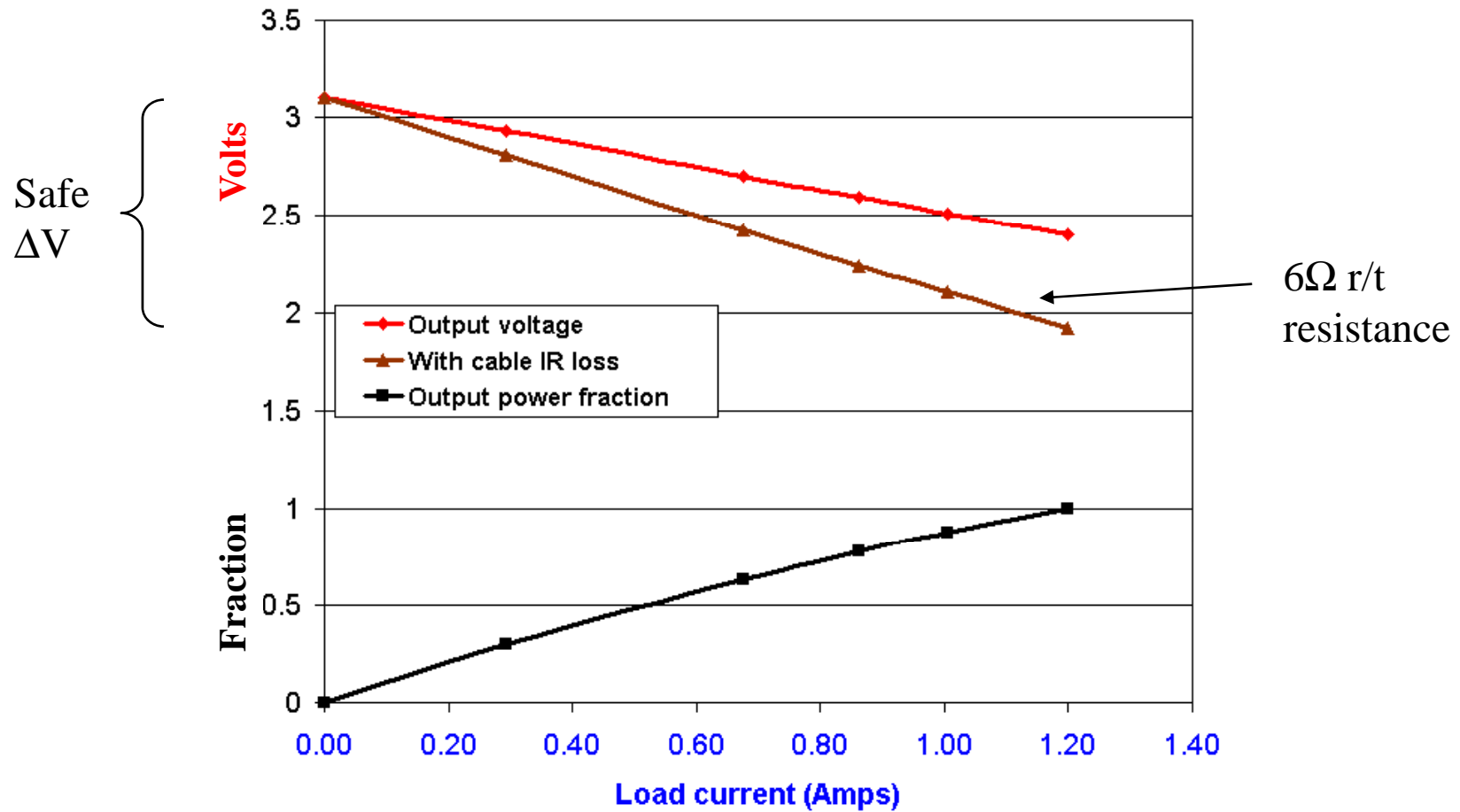
These components could be internal eventually

Load

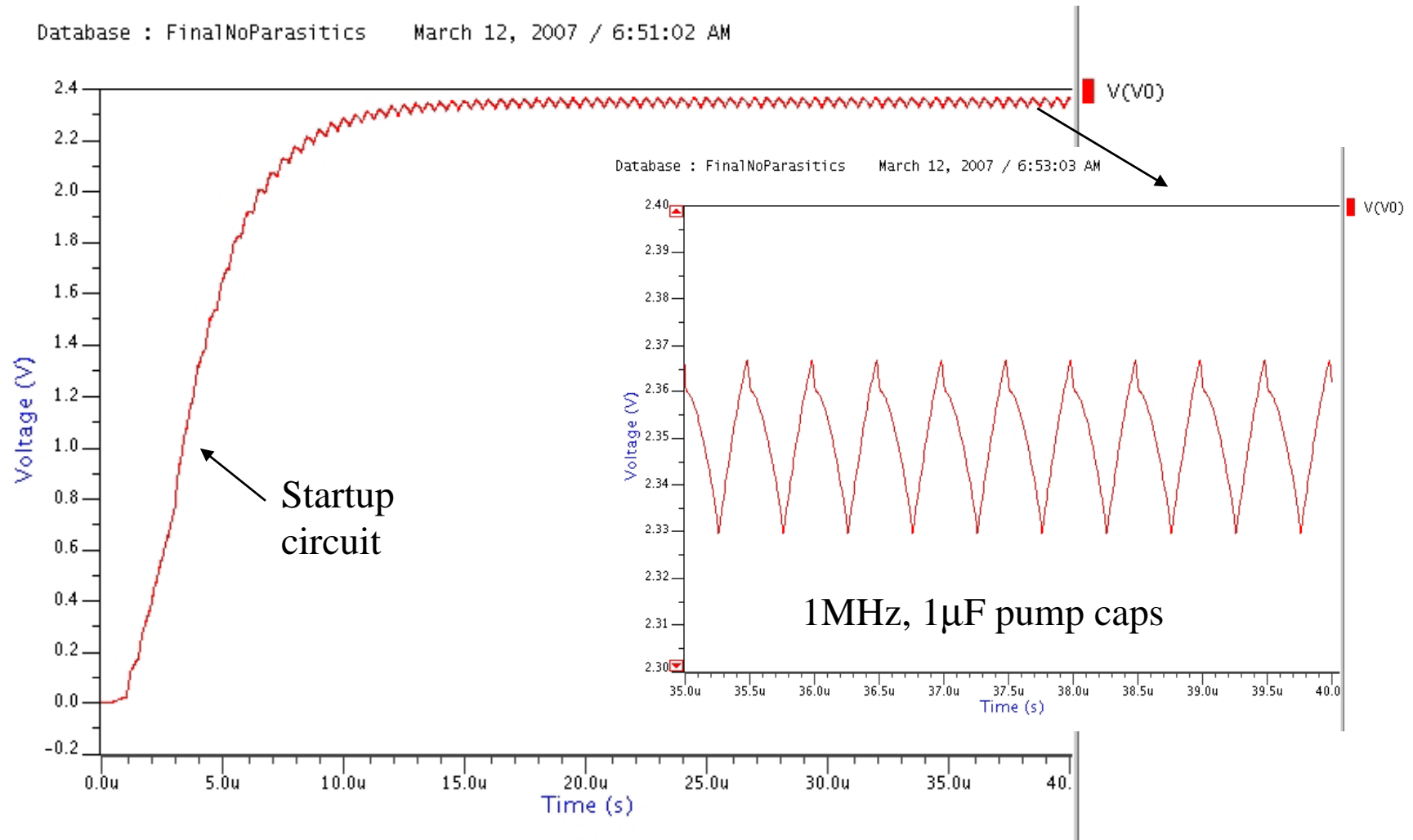
Simulation results 1



Simulation results 2



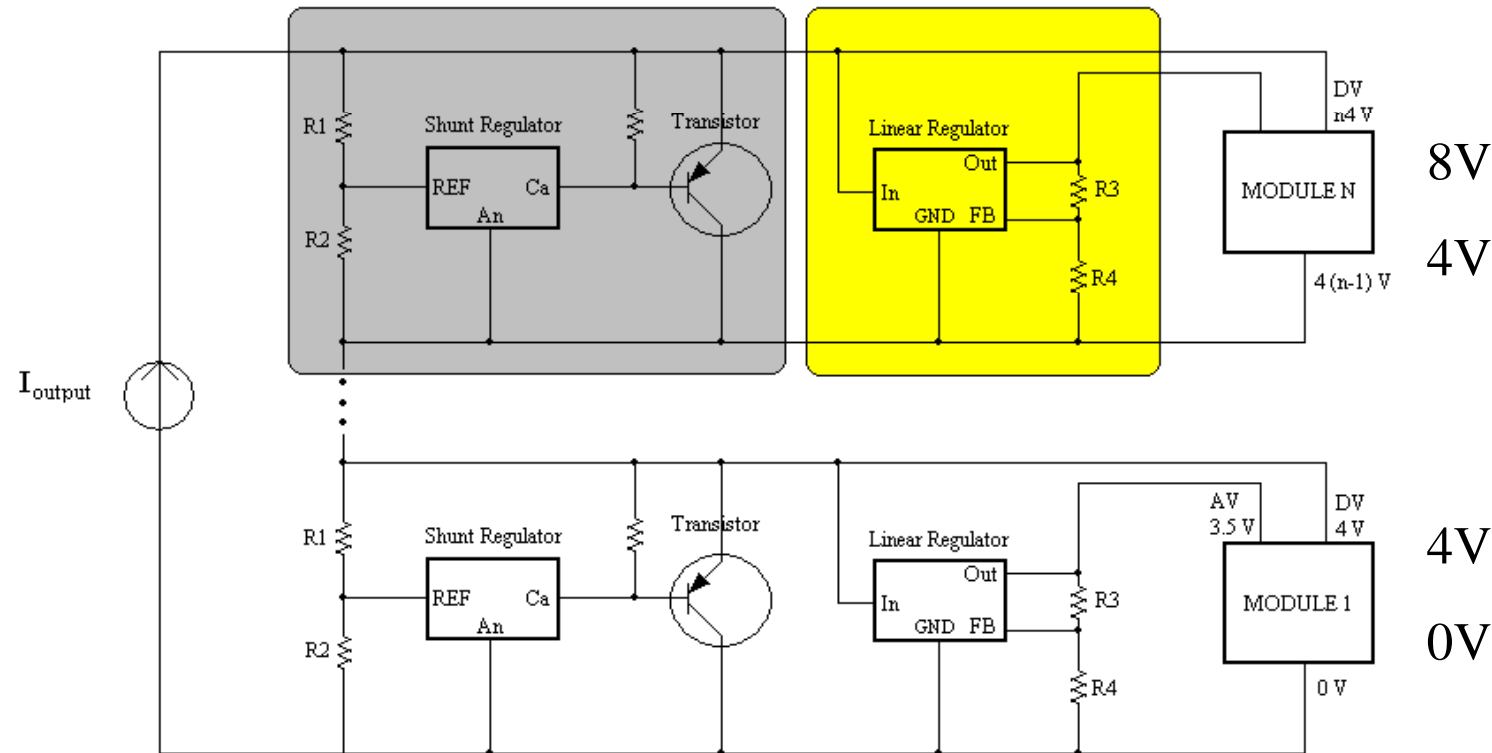
Simulation results 3



Serial power vs. DC-DC trade-offs

- **Power:** Both increase power at/near the module by a similar amount
- **Mass:** Serial power is in principle less massive because regulators can be built into chips.
- **Radiation:** SP naturally rad-hard if regulators built into chips. DC-DC not yet rad-hard enough
- **Generality:** DC-DC can be an off-the-shelf solution. A given converter can be used in several applications
- **Complexity:** With SP the detector basic unit is a super-module. With DC-DC the basic unit is still a module.
- **Control:** individual module control is simple with DC-DC, not with SP. With DC-DC module voltages are adjustable- not easily with SP.
- **Cable reduction:** Both reduce copper mass by same amount. SP also reduces the cable count by default. DC-DC allows trade-off between cable count and control granularity.

Serial power implementation



- Regulators can be external or inside readout chips
- Production pixel readout chips already have internal regulators built-in (but not used).
 - This shows that the serial power pixel R&D has a long history by now

Why is there no conductive interference (noise) between serial powered modules?

- What about **current fluctuations**?
 - a) modules cannot sink current, current is conserved \Leftrightarrow no problem

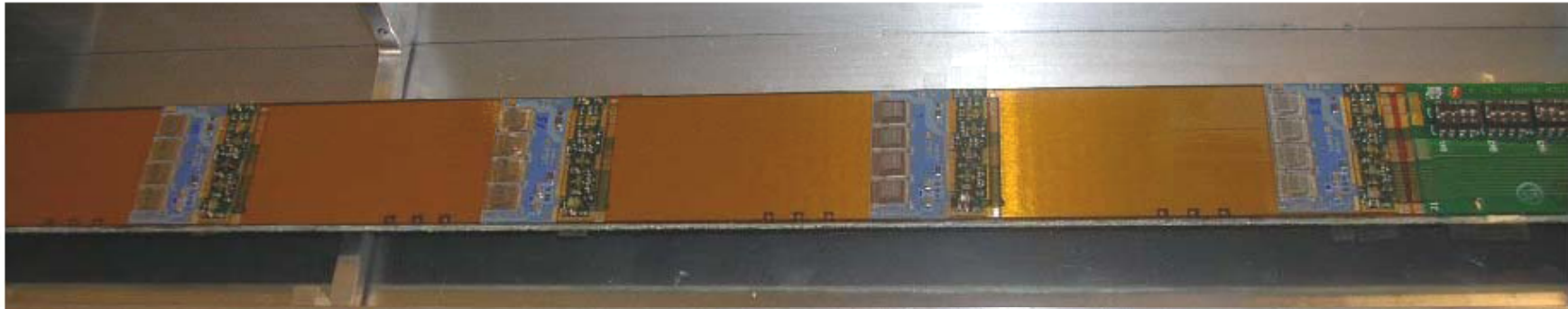
(shunt regulators can cope with current fluctuations under normal conditions)

- What about **voltage fluctuations**?
 - a) IR drops are minimum (since current is constant) \Leftrightarrow no damage to regulators, minimum pick-up from power lines

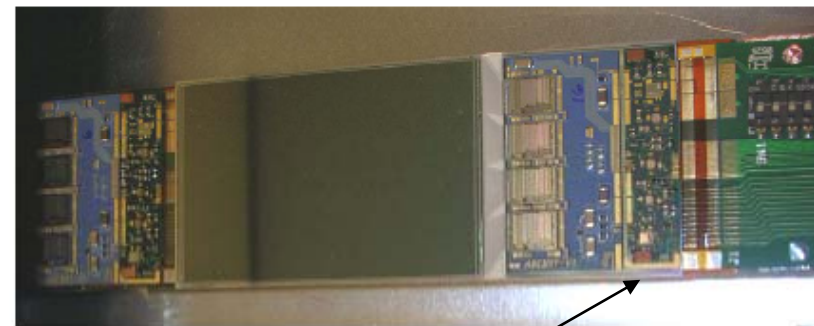
 - b) Module voltage fluctuations do not influence neighbouring modules since voltages are derived by local shunt regulators

Serial-powered strip sensors

LBNL SP supermodule with 6 hybrids (no sensors)



same LBNL SP supermodule with 5 hybrids
and 1 module



Can replace with DC-DC converter
for direct performance comparison →

SP adapter “hybrid” with
regulators and signal level shifters.

Serial power references

First pioneering work was done by Bonn group for pixels

T. Stockmanns, P. Fischer, F. Hugging, I. Peric, O. Runolfsson, N. Wermes, “Serial powering of pixel modules”, Nucl. Instr. & Meth. A511 (2003) 174–179; D. B. Ta, T. Stockmanns, F. Hugging, P. Fischer, J. Grosse-Knetter, Ö. Runolfsson, N. Wermes, “Serial Powering: Proof of Principle demonstration of a scheme for the operation of a large pixel detector at the LHC”, Nucl. Instr. Meth. A557 (2006) 445-459

RAL picked it up 2 years ago for strips

Marc Weber, Giulio Villani, Mika Lammentausta, Proceedings of the 11th workshop on electronics for LHC and future experiments, CERN-LHCC-2005-038, (2005) pp. 214-217; Marc Weber, Giulio Villani, “Serial Powering of Silicon Strip Detectors at SLHC”, Proceedings of the 6th “Hiroshima” conference on Silicon detectors (2006); Carl Haber, “A Study of Large Area Integrated Silicon Tracking Elements for the LHC Luminosity Upgrade”, Proceedings of the 6th “Hiroshima” conference on Silicon detectors (2006).

Conclusion

- Powering has become a hot topic with lots of work going on
- Expect usable prototype DC-DC converters by year's end
- Focus tends to be on powering existing chips, because that's what people can make tests on
- Reduction of current at the source (chip) has NOT YET received nearly as much attention within HEP. It should
- How do we reduce the analog current keeping good performance?
- How do we reduce the digital current?
 - An extreme is stacked logic domains- serial power inside the chip. Reference: <http://www.bioee.ee.columbia.edu/>
 - Less aggressive approaches are possible. I/O protocol. Clock distribution. Architecture.