SPIROC status
Silicon Photomultiplier
Integrated Read Out Chip

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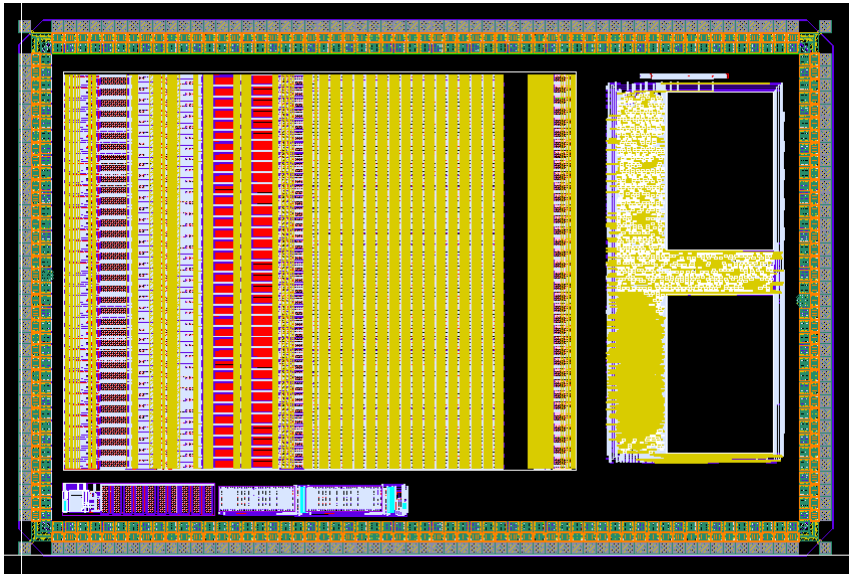
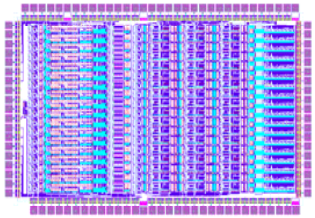
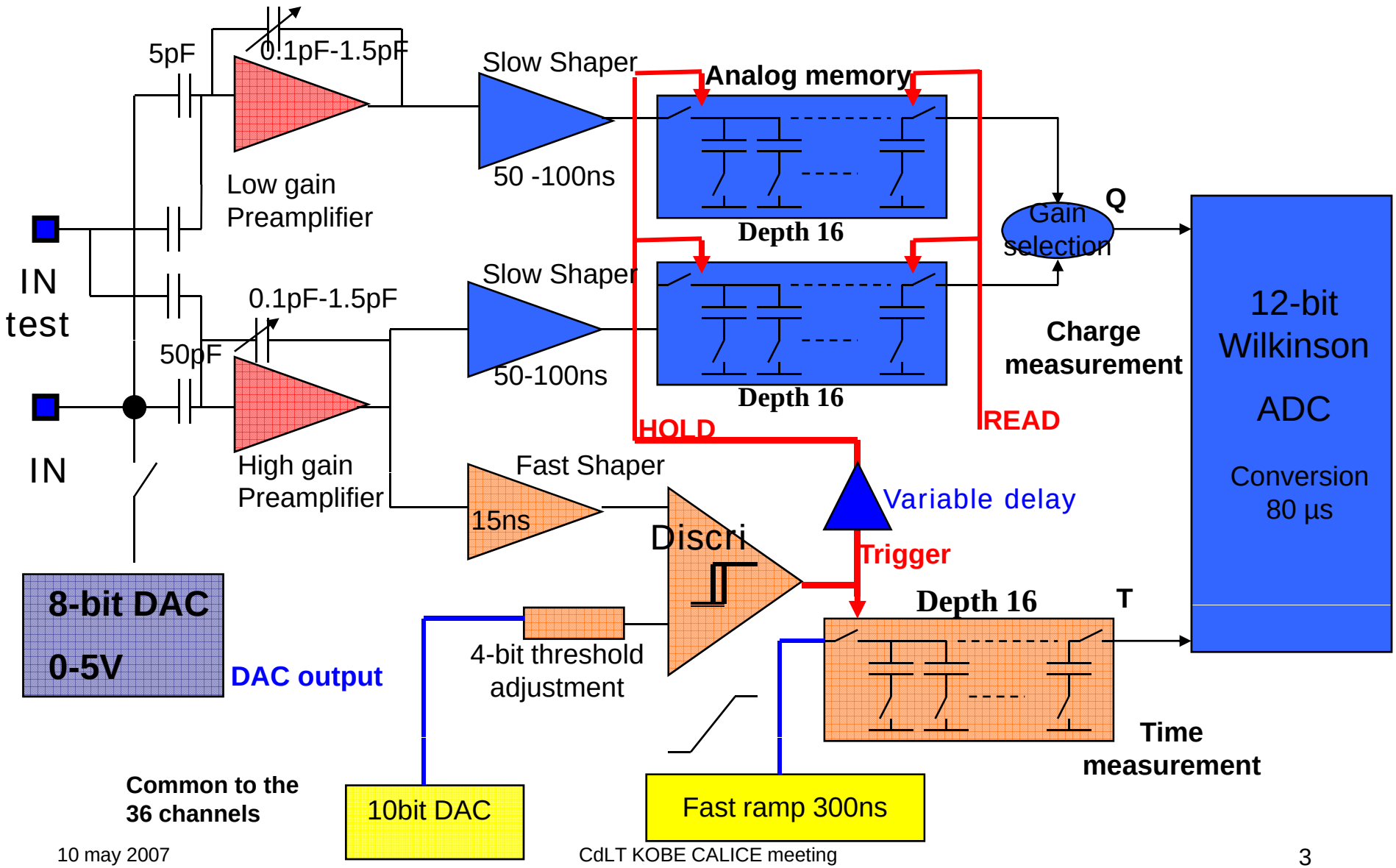
SPIROC overview

- A-HCAL read out
- Silicon PM detector
  - G = 3 E5 to 1 E6
  - Same biasing scheme as TB
- 36 channels
- Compatible with old & new DAQ
- Many SKIROC, HARDROC, and MAROC features re-used
- Area = 30 mm2 -> 30 k€ !
- Submission foreseen june 11th



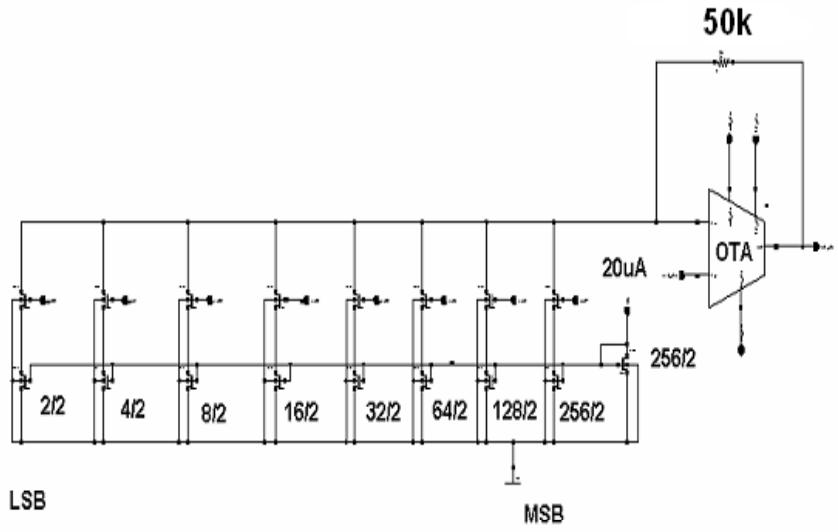


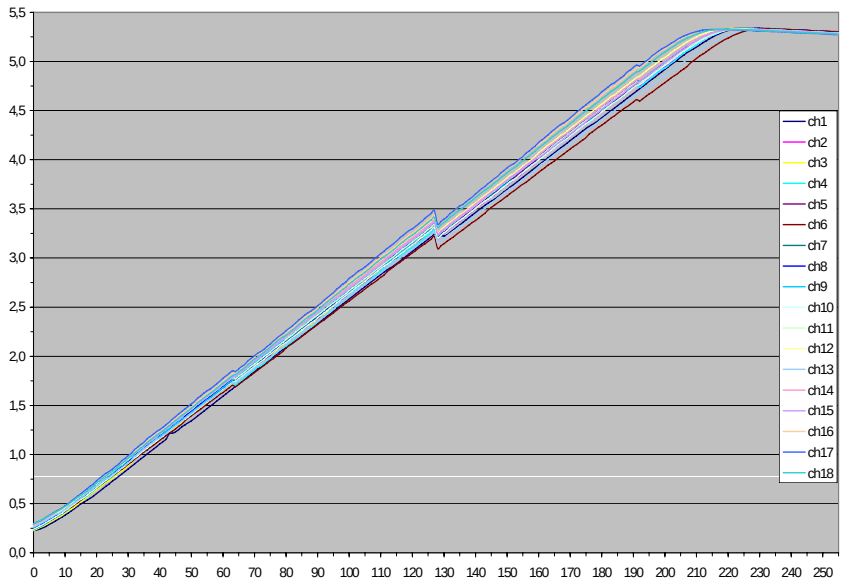
SPIROC: One channel schematic



Input DAC

- **New, but same principle as FLC_SiPM**
  - 36 DACs : one per channel
  - Ultra low power : no power pulsing
  - 0 to 5 Volts output
  - +5V by default
  - 8 bits : LSB = 20 mV
  - Scaled current mirrors now PMOS
  - Reference current now 100nA
  - New output OTA : 2 stages, power dissipation 180nA*5V = 1 µW
  - OTA feedback now 5 Meg
  - Can be switched off
  - Can sink 10 uA leakage current
  - Linearity not known, presumably better than FLC_SiPM (beside ->)
  - Uniformity between the 36 channels possibly several %

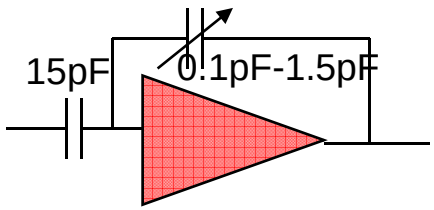


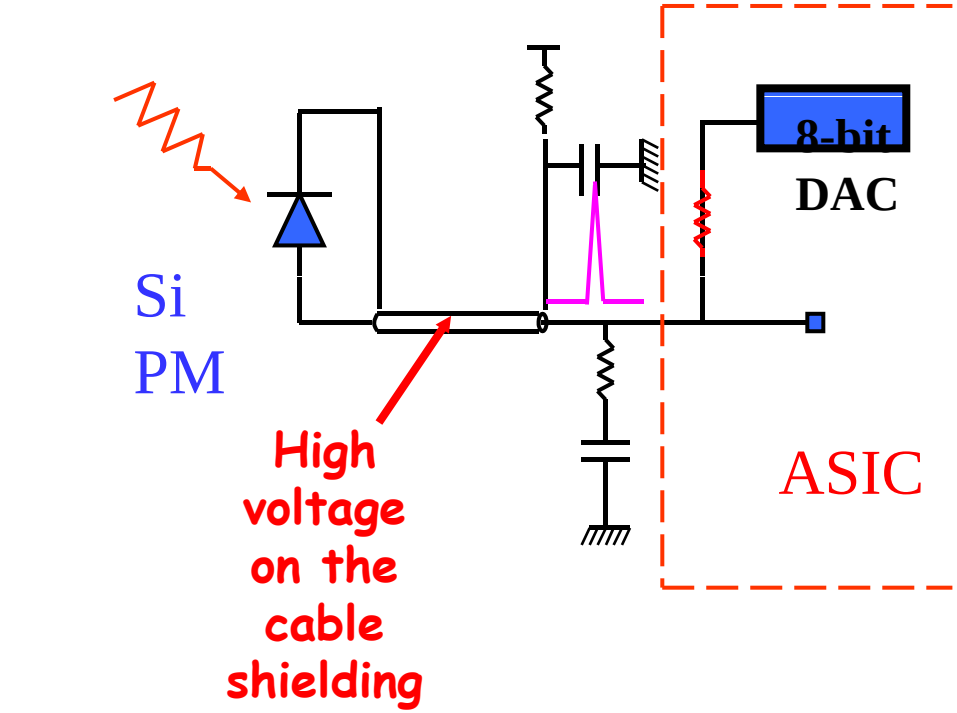


Input preamp

- **Same as SKIROC**
  - Low noise charge preamp capacitively coupled = voltage preamp
  - Gain adjustable with 4 bits common to all preamps
  - Preamp can be switched off individually
  - 8 mV/pe in HI Gain
  - Noise : 1.4 nV/sqrt(Hz)
  - Power : 2 mW

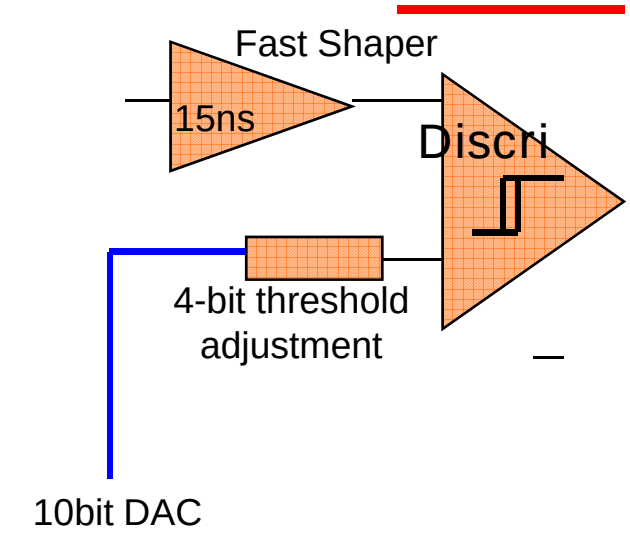
- **Low gain at preamp level**
  - 1.5pF coupling capacitor



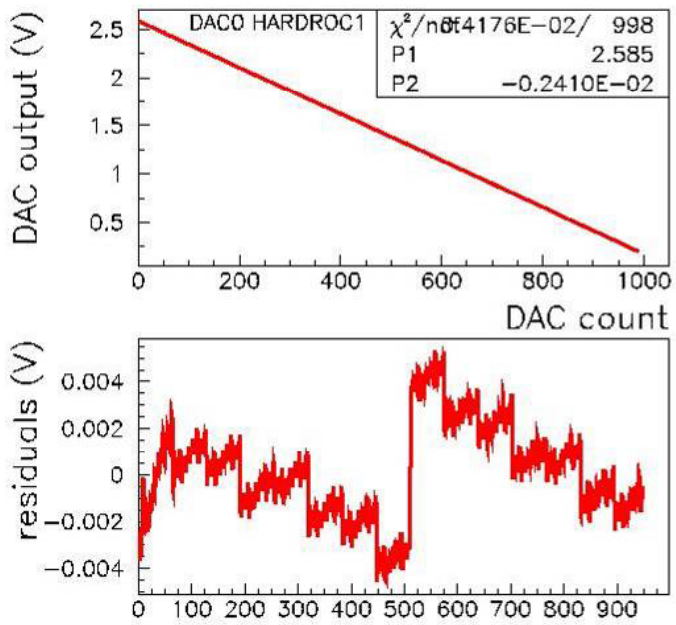


Fast shaper and discriminator

- **Totally new block, high speed => risky**
  - CRRC shaper : tp = 15ns
  - OLG=50dB GBW=
  - Gain = 50 : 120 mV/pe
  - Noise
  - Power :

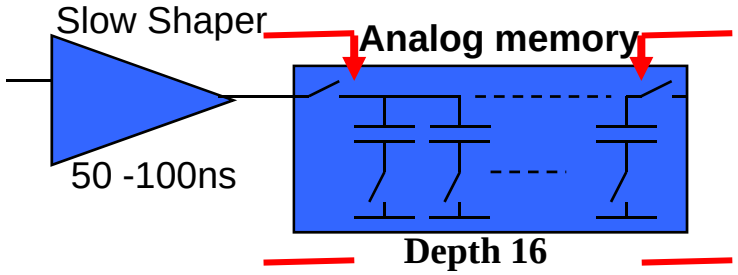


- **Discriminator = HaRDROC**
  - 10 bit overall DAC from HARDROC
  - 4 bit fine adjustment/channel
  - Max range : +/- 40mV
  - Power : 300 μW

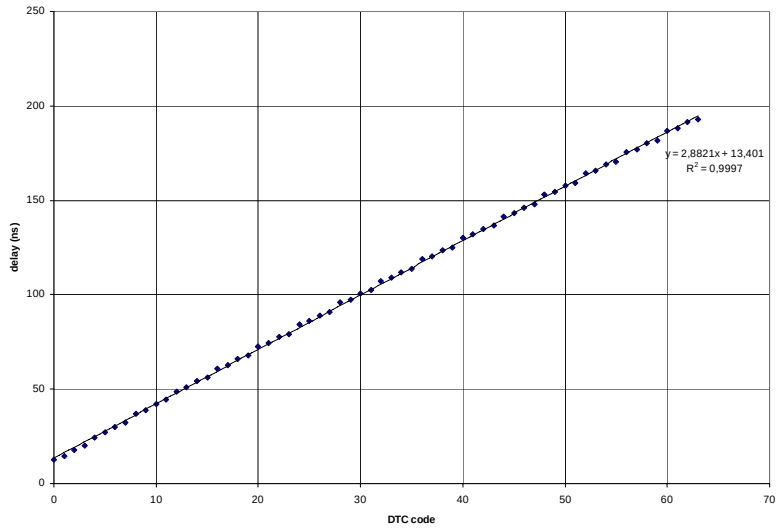


Slow shaper & SCA

- **Slow shaper from HaRDROC**
  - Variable peaking time : 50-150 ns
  - 3 bits common to all channels
  - High Gain = 10 mV/pe
  - Noise = 900 µV
  - Low gain = 1 mV/pe



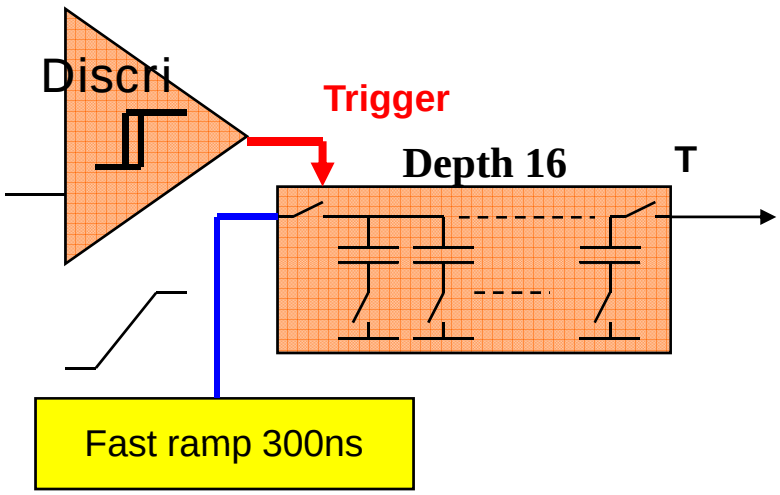
- **Backup : analog T&H from HaRDROC**
  - Hold capacitor : 2pF -> 0.5 pF
  - Needs external hold signal
  - Multiplexed analog output @ 5MHz
  - Allows readout with DAQ0



- **SCA : new block**
  - = multiple T&H
  - Depth = 16
  - Droop < 1 mV/ms (measured on HaRDROC)
  - Hold signal generated internally with adjustable delay (new block)

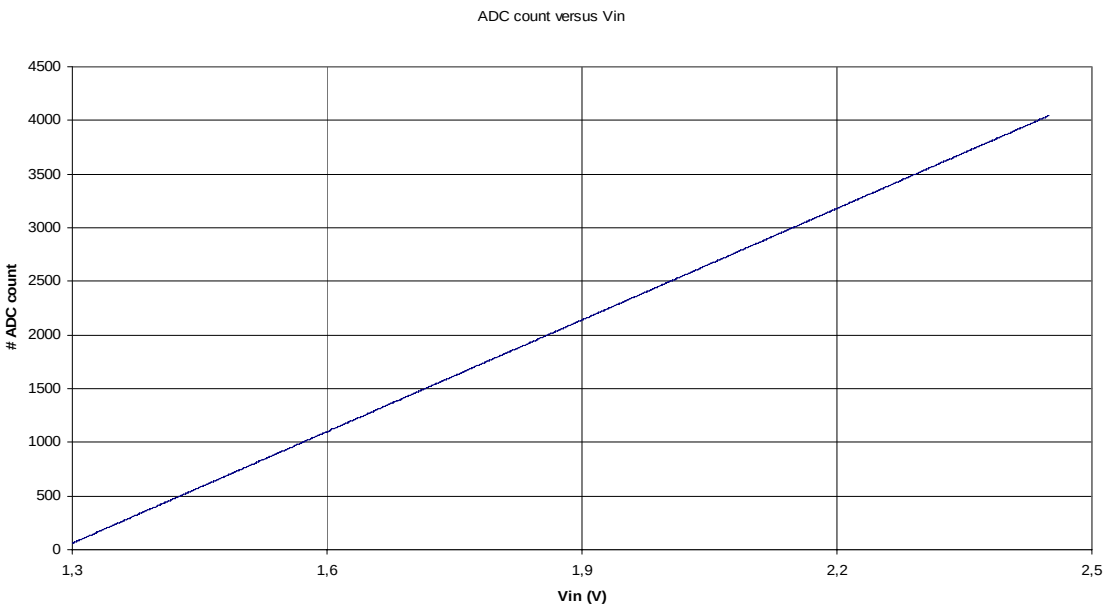
TDC

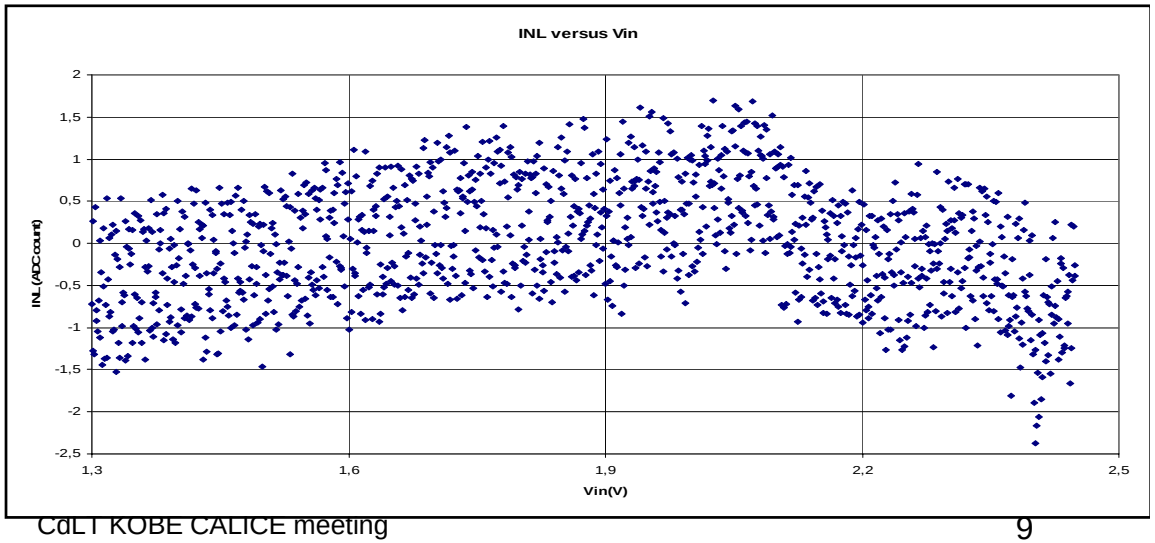
- **New block**
  - 12 bits
  - 300 ns full scale
  - 100 ps LSB (not accuracy !)
  - « common start » = BC
  - Time stored in SCA together with charge
  - Can also be readout with backup analog



Wilkinson ADC

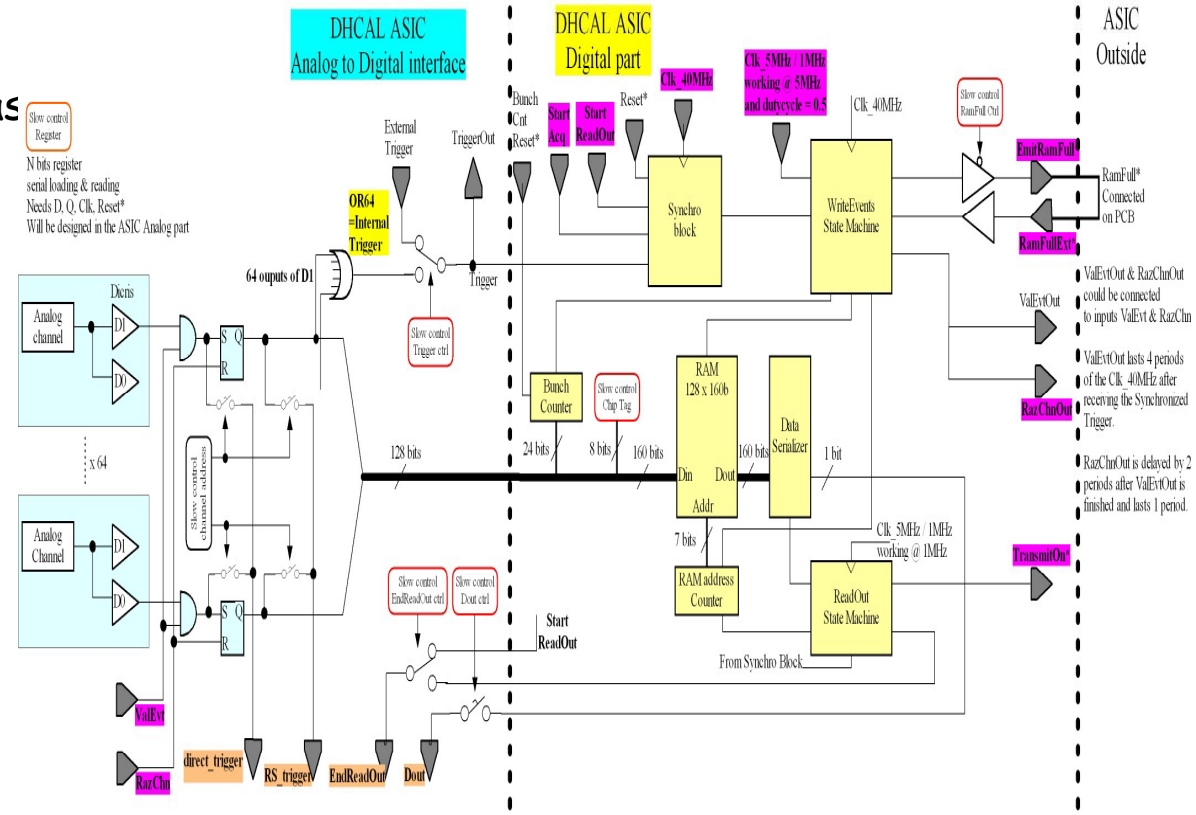
- **Taken from MAROC**
  - New : adjustable resolution : 8 - 10 or 12 bits
  - 40 MHz clock
  - 6-100 μs conversion time
  - Power dissipation : 350μW





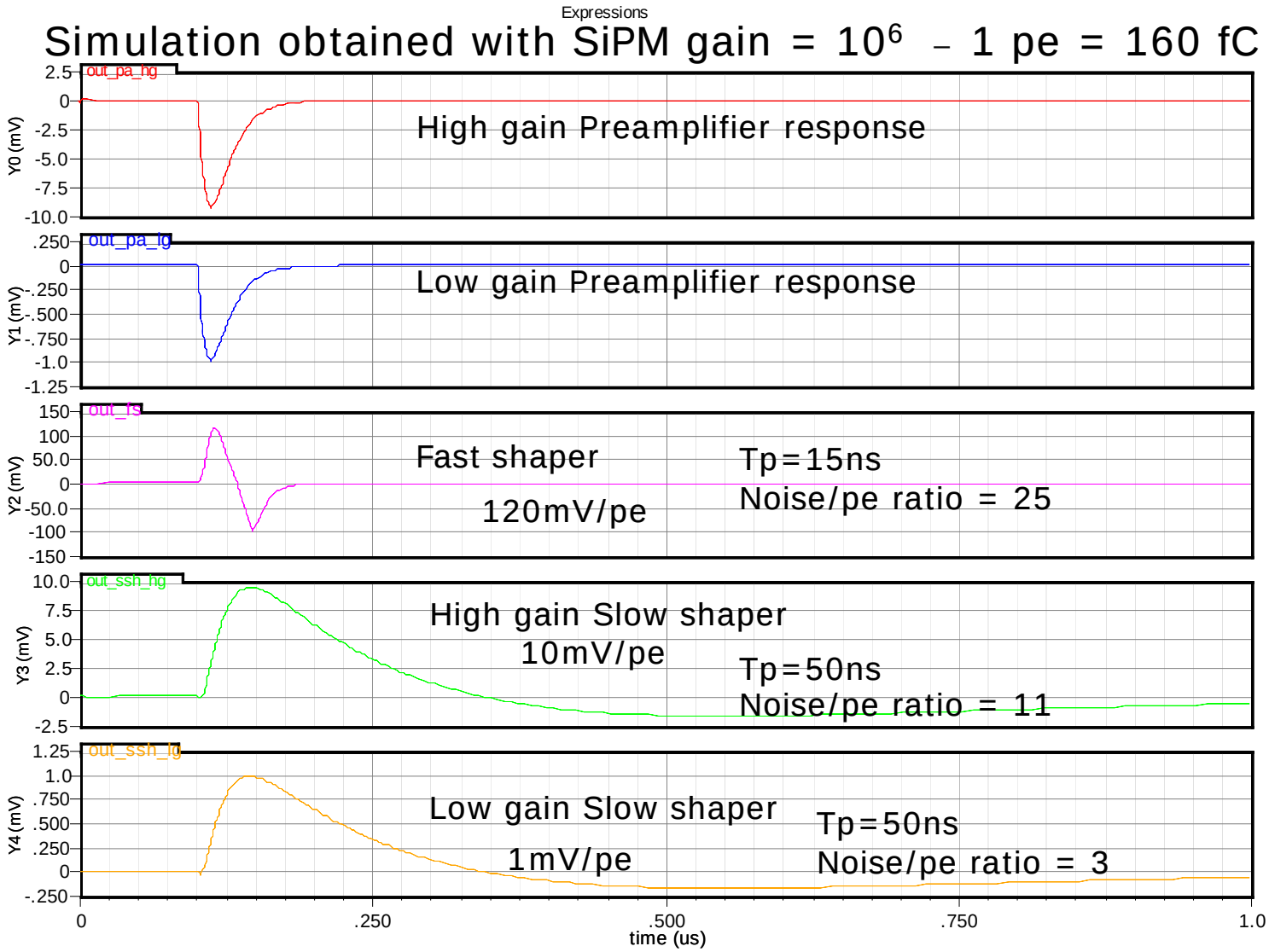
Digital part

- **Inspired from HaRDROC**
  - Internal or external Trigger
  - OR36 output
  - Discriminator Validation fast input
  - 4kbyte RAM
  - « Open collector » output signals
  - LVDS clocks
  - Start conversion
  - Start/end readout

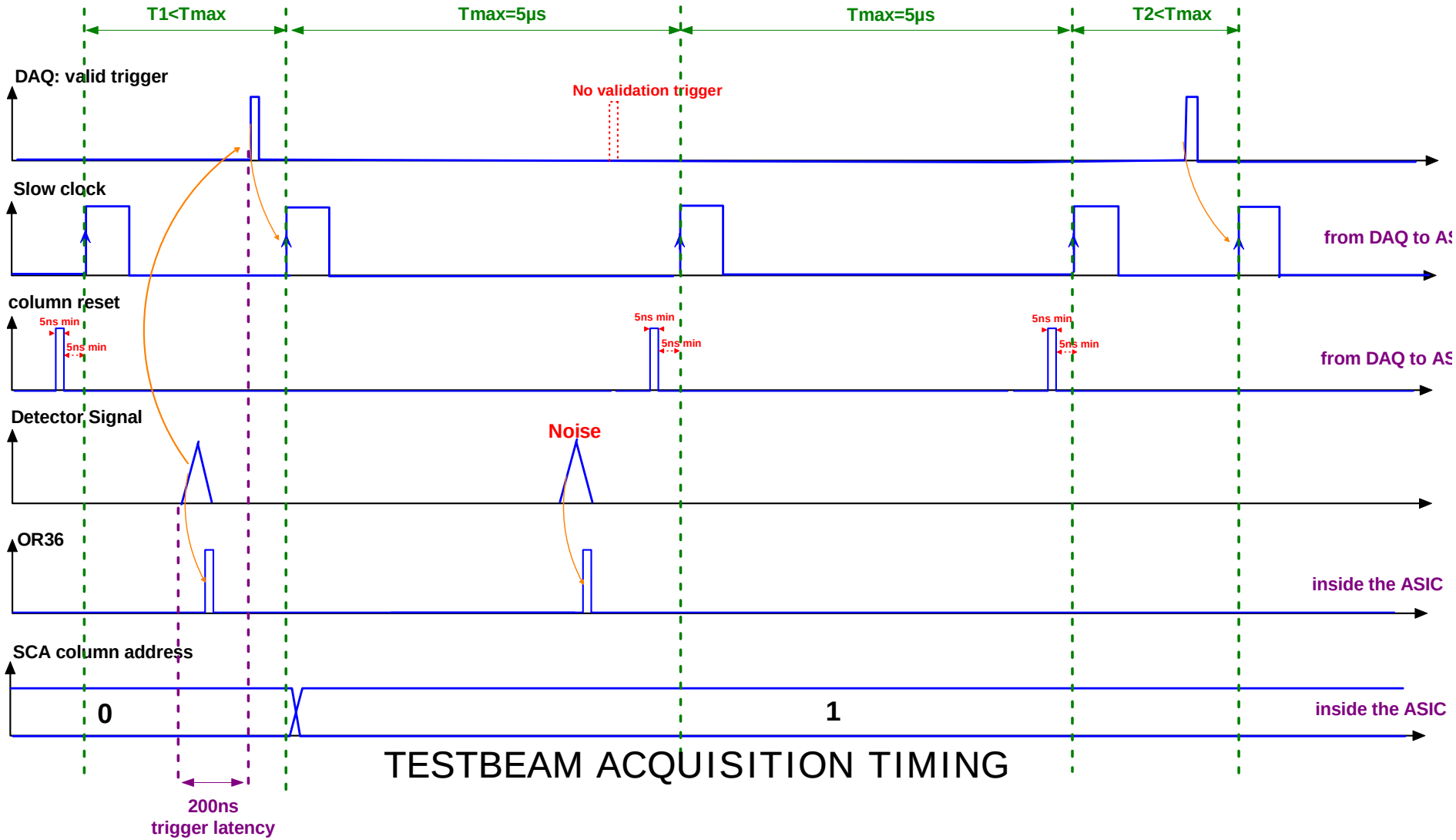


SPIROC : Photoelectron response simulation

Simulation obtained with SiPM gain = 10^6 – 1 pe = 160 fC

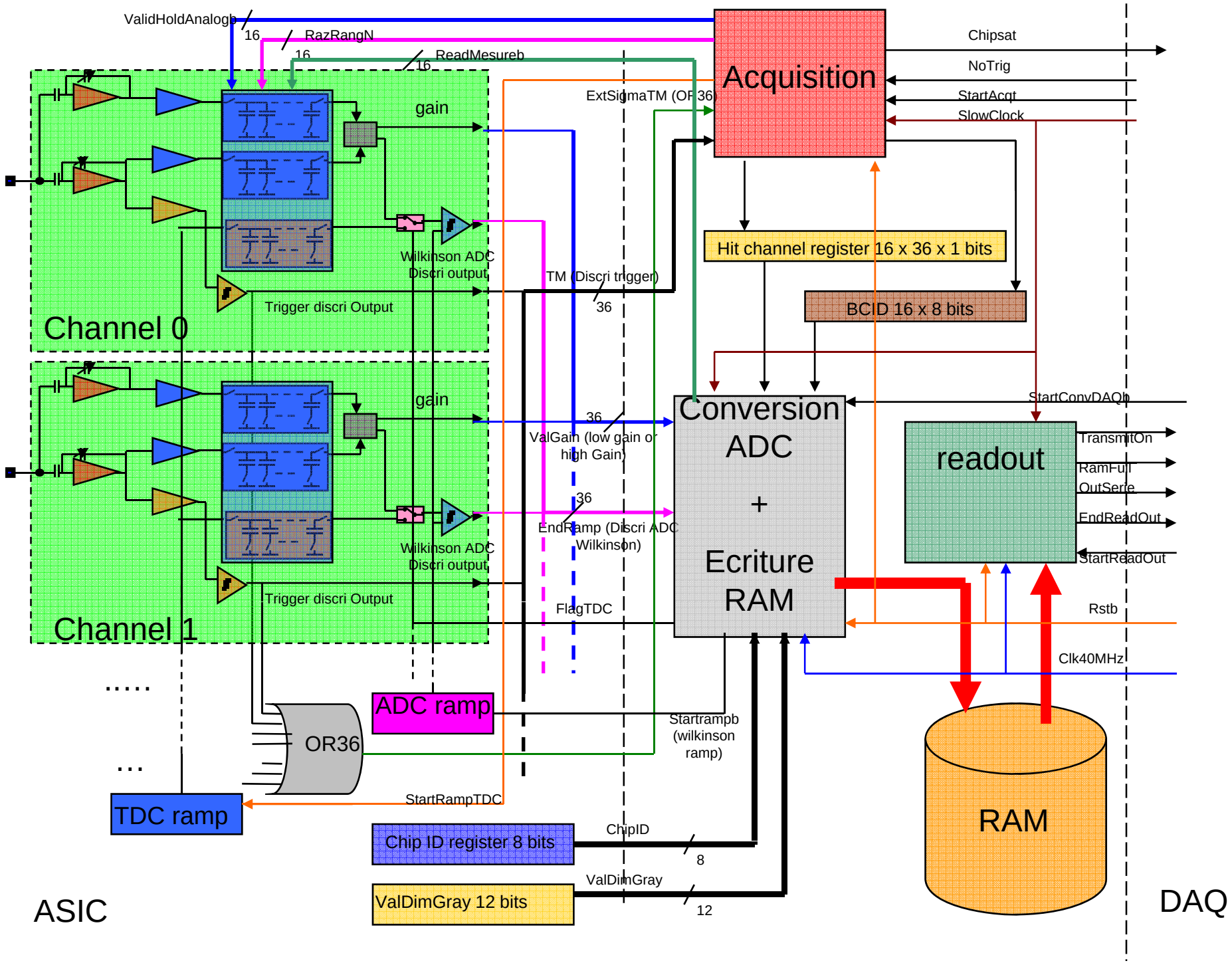


Timing overview

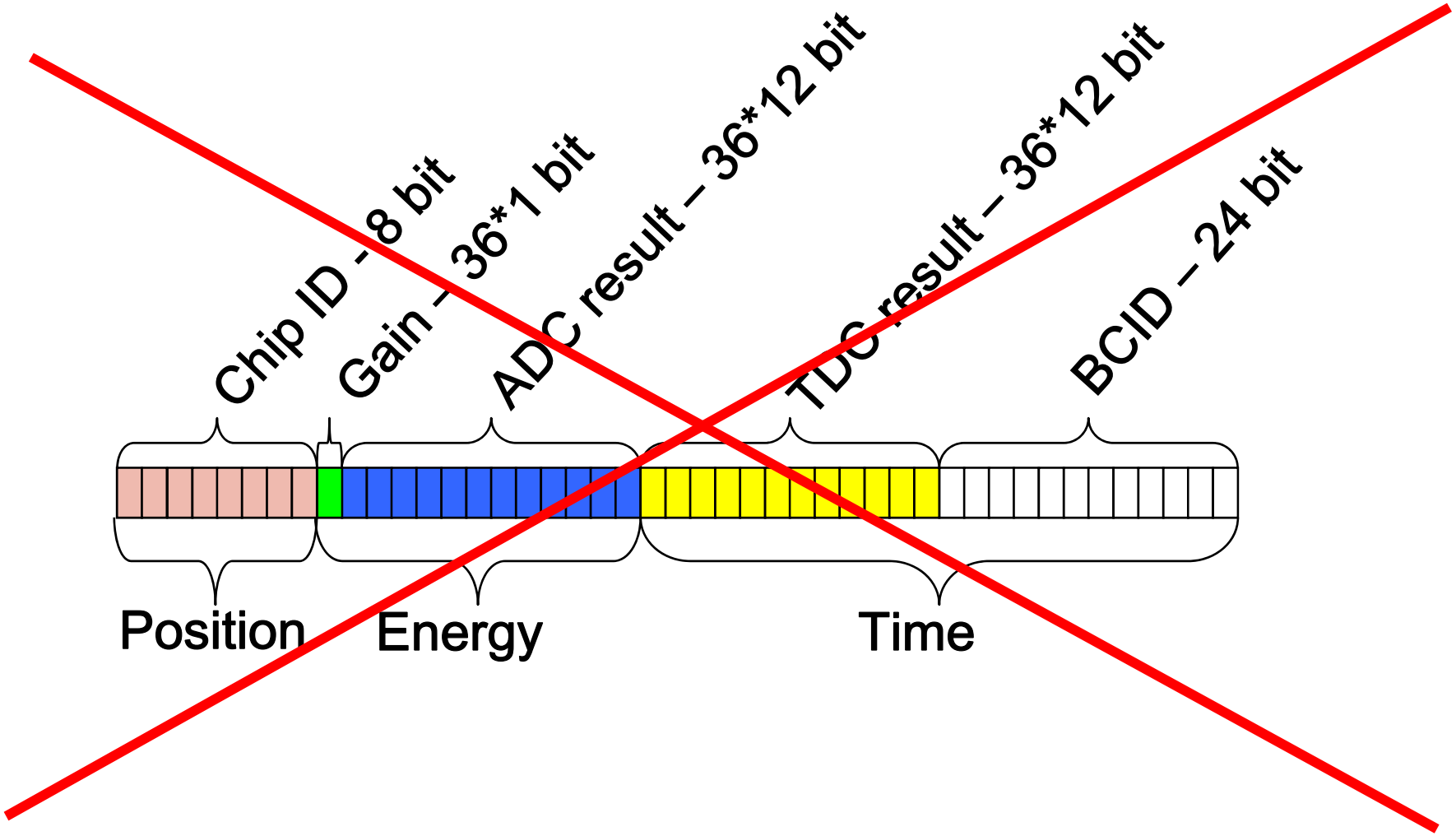


SPIROC main features

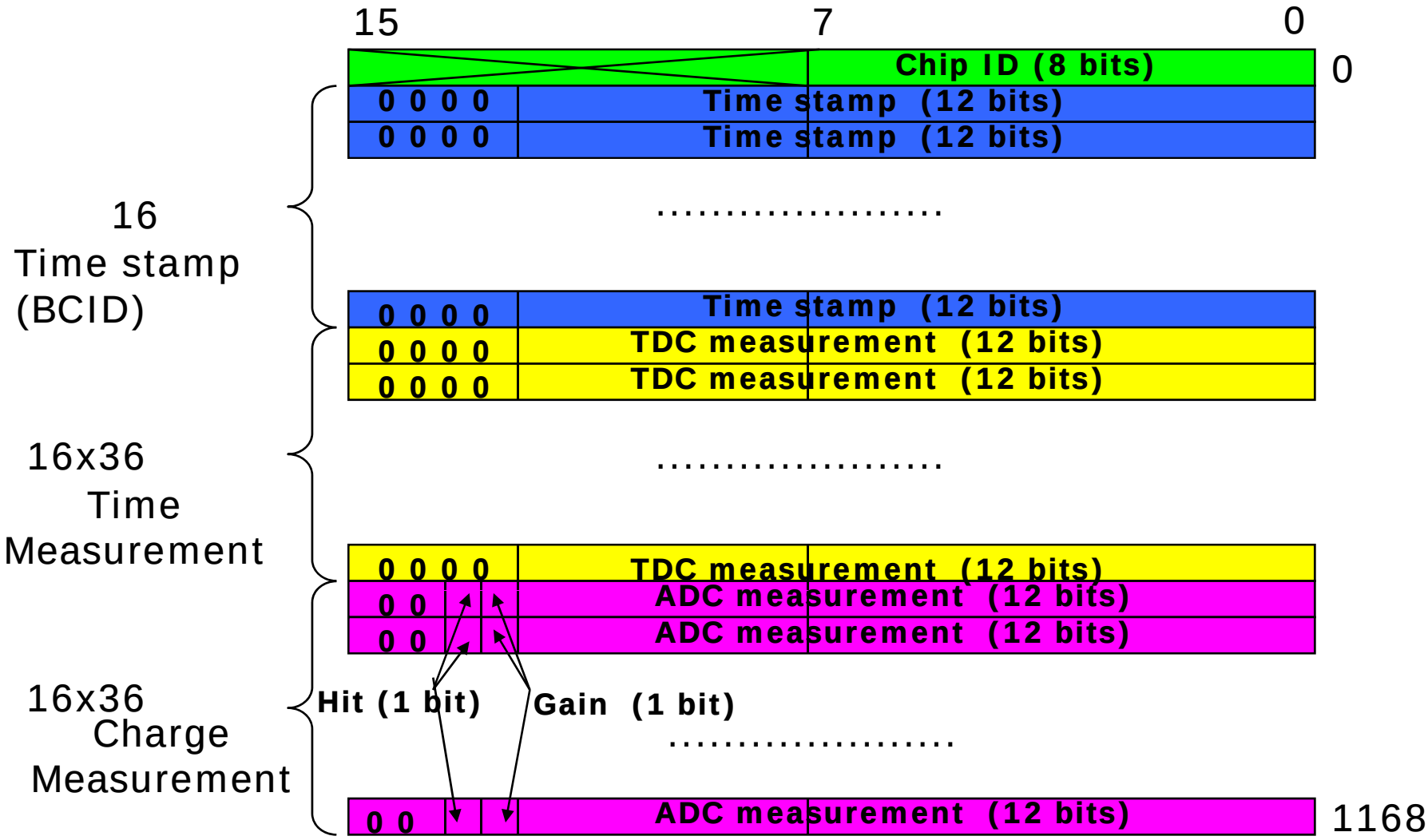
- **36-channel readout chip**
- **Internal input 8-bit DAC (0-5V) for SiPM gain adjustment**
- **Energy measurement :**
  - 2 gains / 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 50ns to 100ns
  - pe/noise ratio : 11
- **Time measurement :**
  - 1 TDC (12 bits) step~100 ps
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~15ns
  - Auto-Trigger on $\frac{1}{2}$ pe
- **Analog memory for time and charge measurement : depth 16**
- **Power pulsing integrated**
- **Low consumption : ~25µW per channel (in power pulsing mode)**
- **Calibration injection capacitance**
- **Embedded bandgap for voltage references**
- **Embedded DAC for trigger threshold**
- **Compatible with physic prototype DAQ**
  - Serial analogue output
  - External "force trigger"
- **Probe bus for debug**
- **12-bit Bunch Crossing ID**
- **SRAM with data formatting 2 x 2kbytes = 4kbytes**
- **Output & control with daisy-chain**


ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
TM (Discri trigger)
36
Trigger discri Output
Channel 0
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
36
ValGain (low gain or
high Gain)
Conversion
ADC
+
Ecriture
RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
36
EndRamp (Discri ADC
Wilkinson)
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
FlagTDC
Rstb
Clk40MHz
.....
ADC ramp
Startrampb
(wilkinson
ramp)
OR36
...
TDC ramp
StartRampTDC
RAM
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
ASIC
DAQ

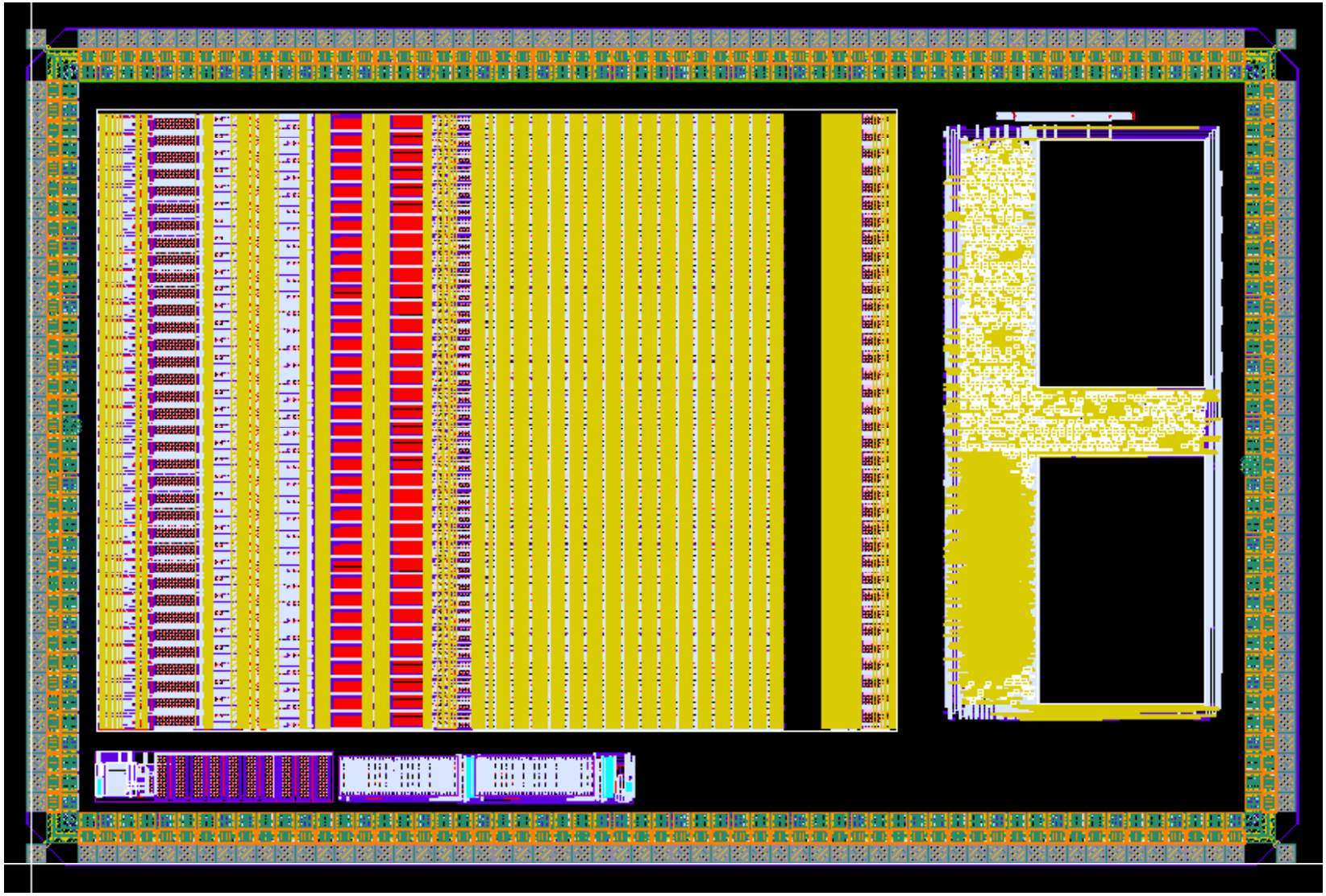
One SPIROC event



SPIROC : RAM Mapping



SPIROC layout



Schedule

- First Prototype submission : 11th june 2007
- Expected delivery : September 2007
- SPIROC Characterization : End of Year

Next steps

- **HaRDROC in hand since jan 07, can be used for EUDET module**
- **SKIROC : in hand since apr 07. Cannot be used for EUDET module**
- **SPIROC : foreseen sept 07. Can (in principle) be used on EUDET**

- **Next SKIROC prototype : need SPIROC results**

- **Could have a production of thousands ASICs by a dedicated run**
  - Cost : 150 k€
  - Share this cost on several chips : MAROC (ATLAS), HaRDROC,