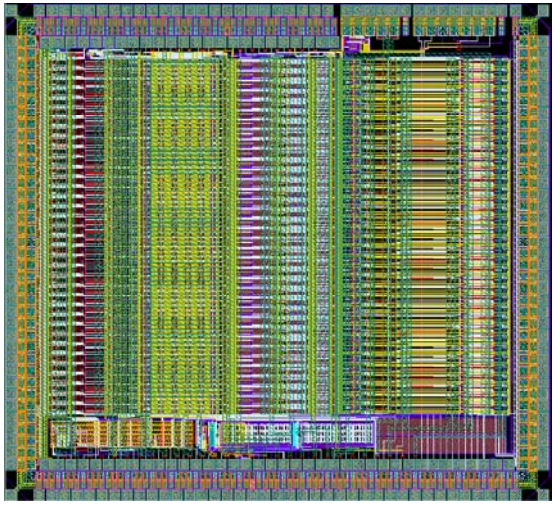
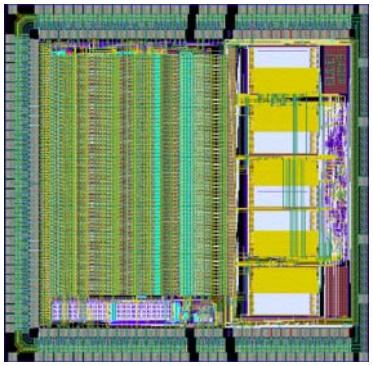
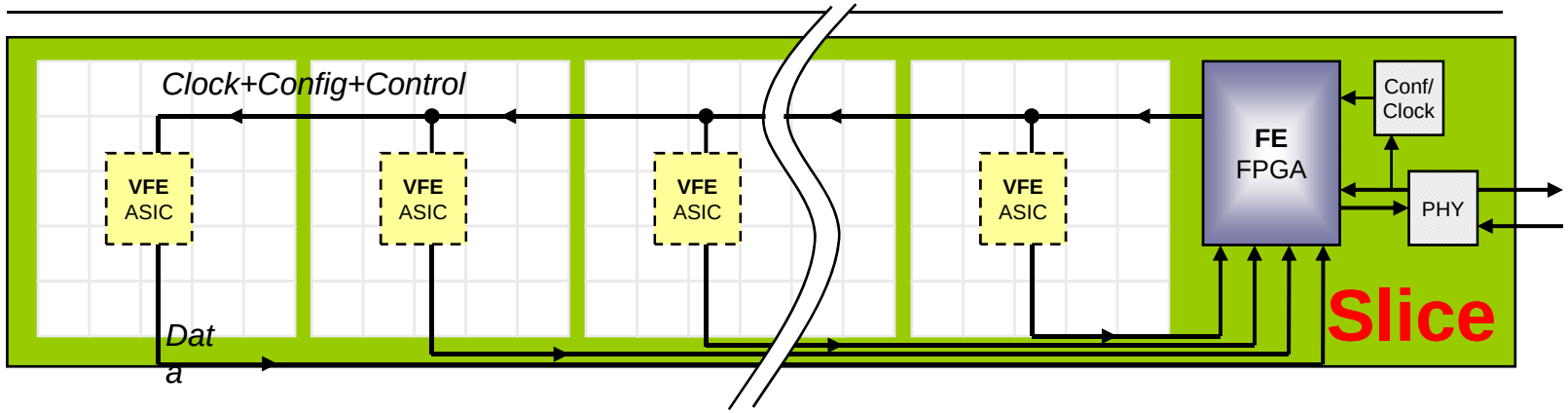
SKIROC status

Calice meeting – Kobe – 10/05/2007

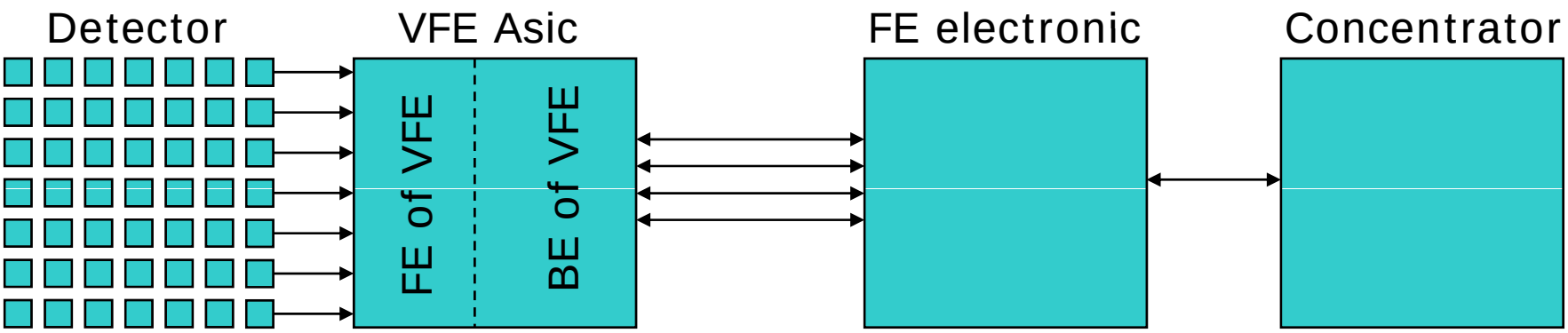




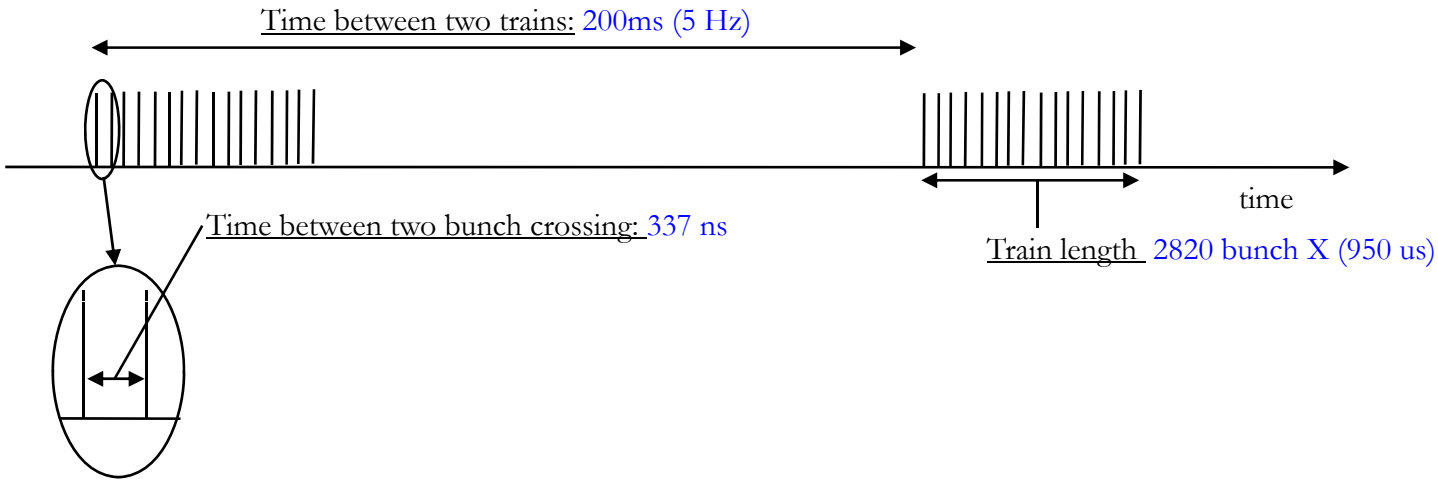
Common DAQ

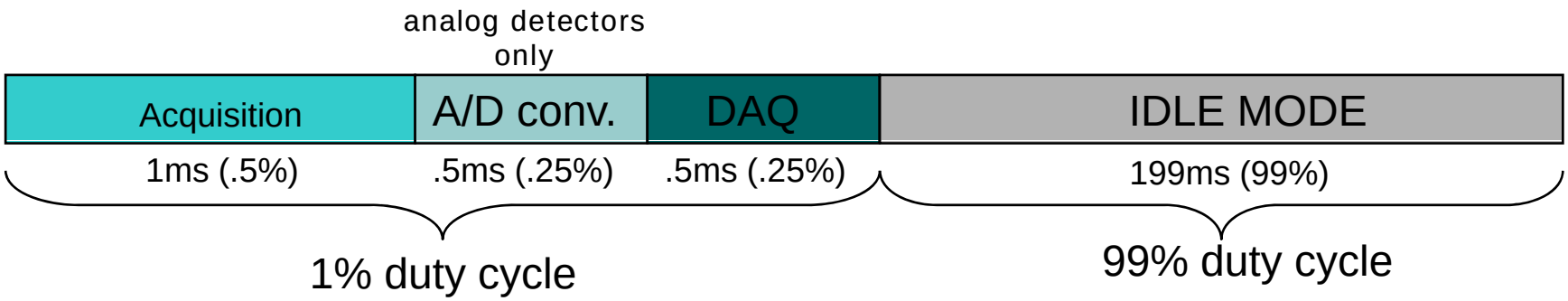


- Timing is the same for all detectors
- Number of channels involves embedded electronic for all detectors
-Outputting of data is done the same way for all detectors
→ Back-end of very-front-end shall be common for all detectors

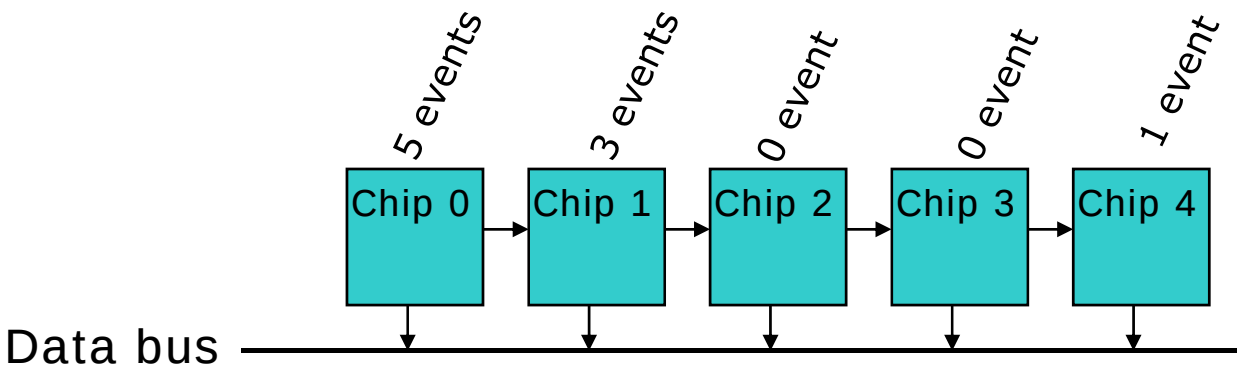


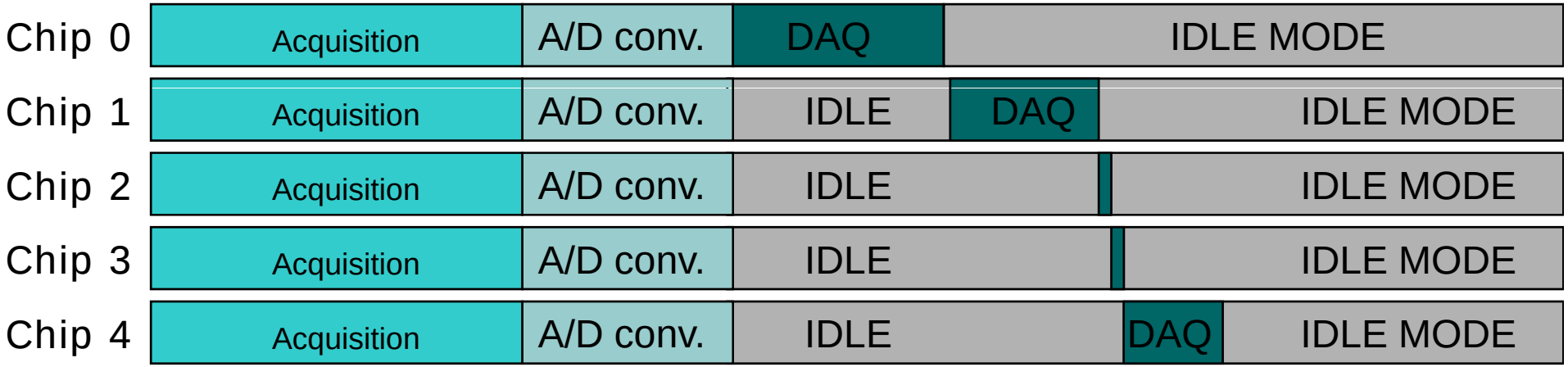
Time considerations





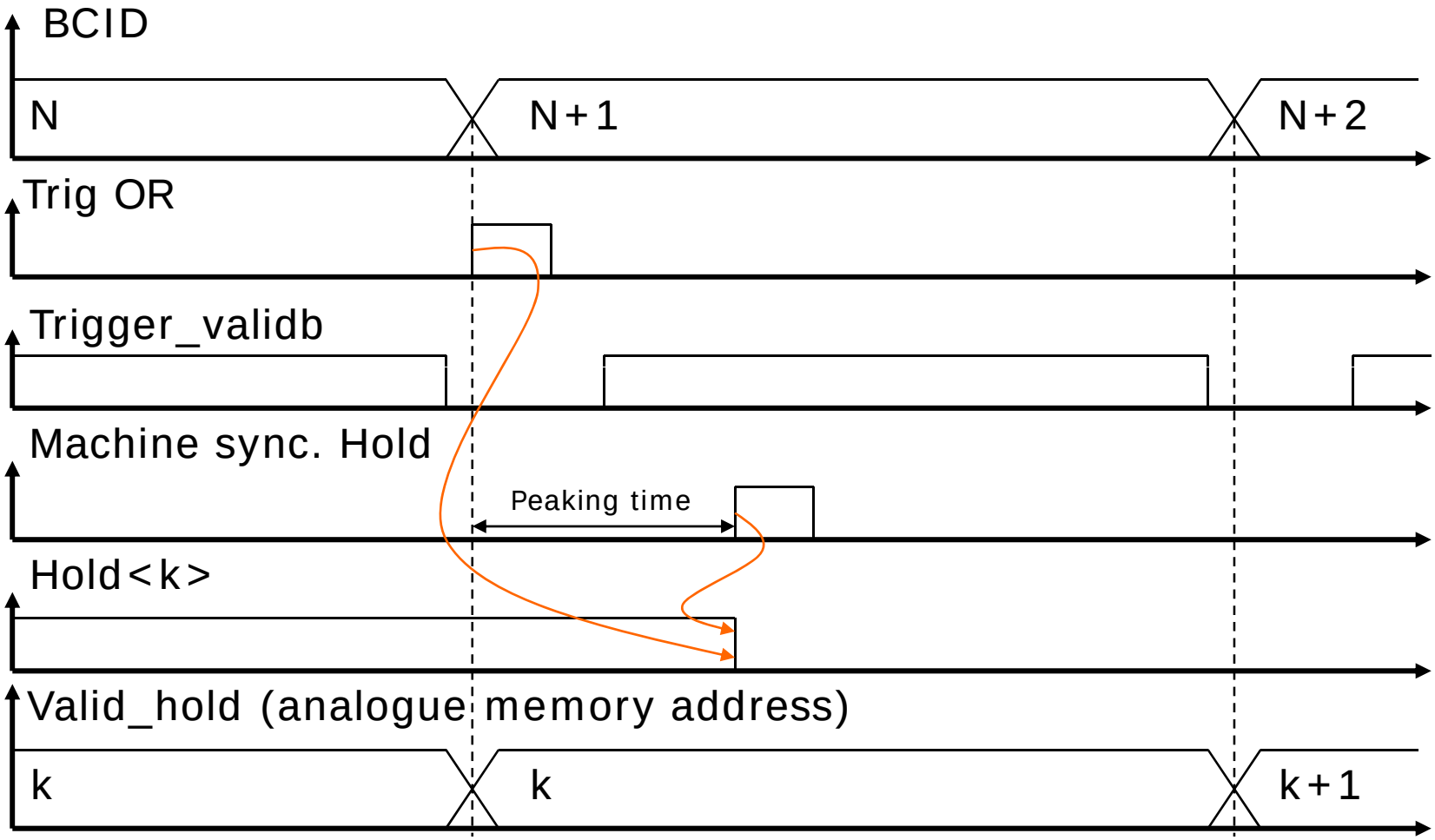
Read out : token ring



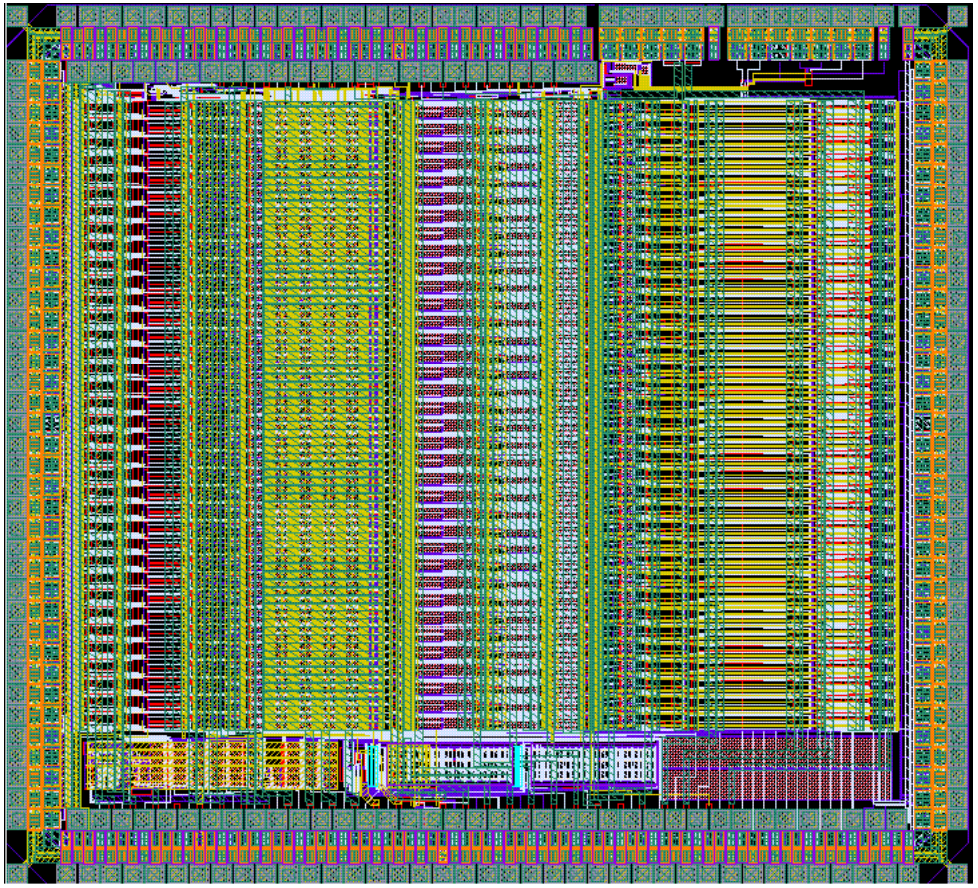


Acquisition mode in test beam

- No time measurement
  → Synchronous hold validated by internal trigger



SKIROC presentation



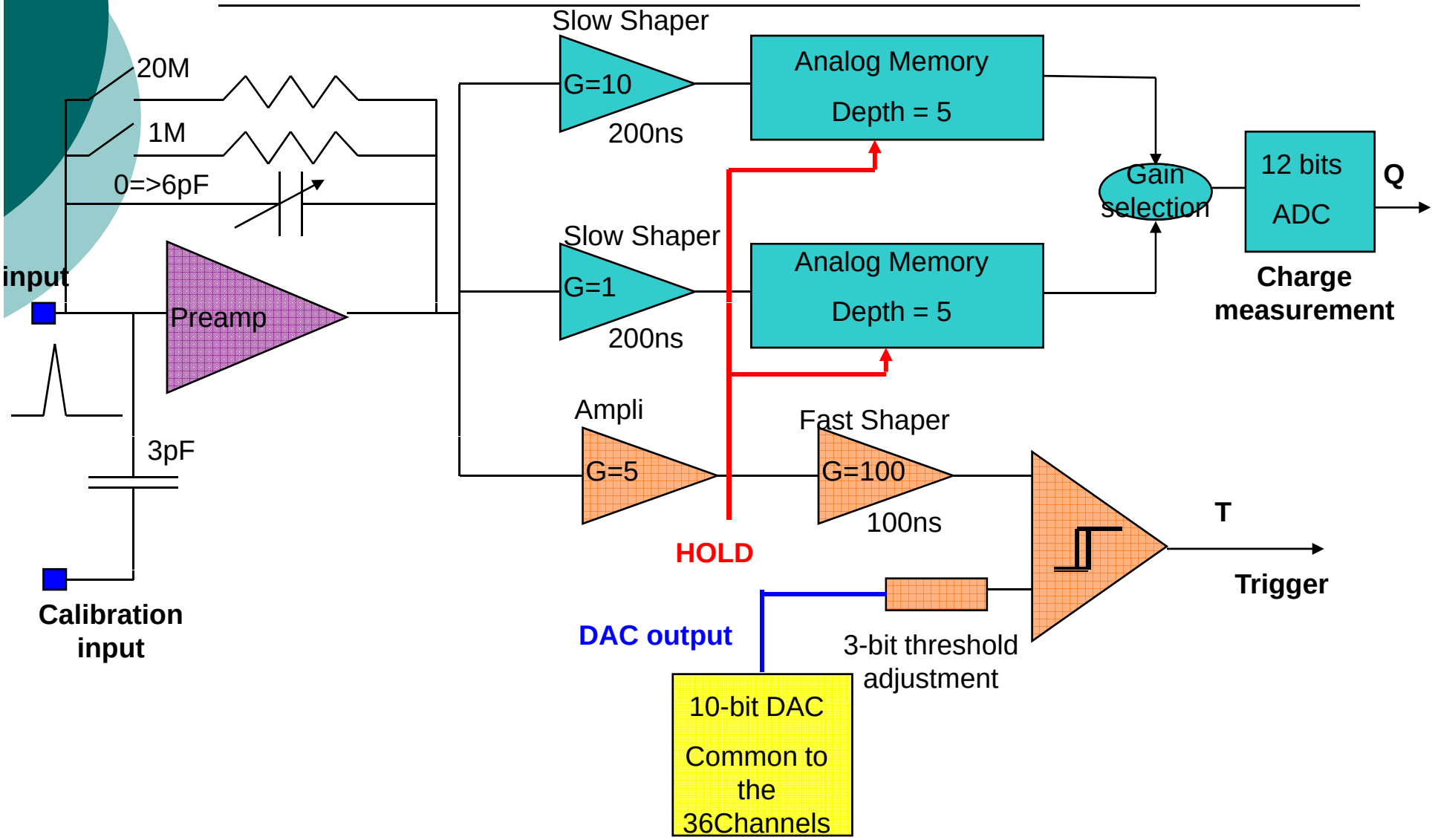
- ECAL read out
- Silicon PIN detector
- 36 channels
-Compatible new DAQ

Main features

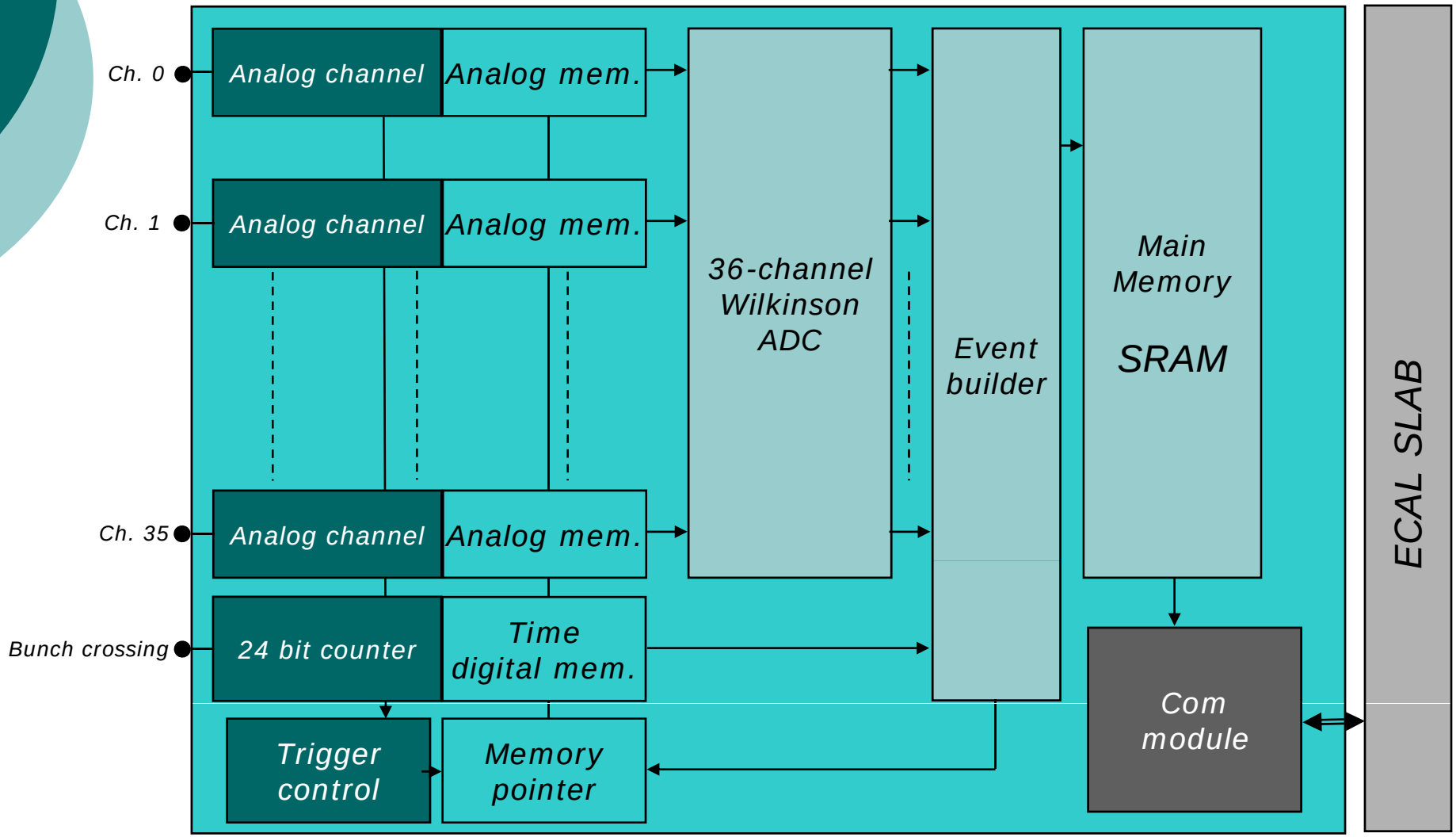
- Designed for 5*5 mm² pads
- 36 channels (instead of 72 to reduce cost of prototype)
- Detector AC/DC coupled
- Auto-trigger
  - MIP/noise ratio on trigger channel : 16
- 2 gains / 12 bit ADC → 2000 MIP
  - MIP/noise ratio : 11
- Power pulsing
  - Programmable stage by stage
- Calibration injection capacitance
- Embedded bandgap for references
- Embedded DAC for trig threshold
- Compatible with physic proto DAQ
  - Serial analogue output
  - External “force trigger”
- Probe bus for debug
- 24 bits Bunch Crossing ID
- SRAM with data formatting
- Output & control with daisy-chain

} Digital on FPGA for debug

One channel


Slow Shaper
G=10
200ns
Analog Memory
Depth = 5
20M
1M
0=>6pF
Gain selection
12 bits
ADC
Q
Slow Shaper
G=1
200ns
Analog Memory
Depth = 5
input
Preamp
Charge measurement
Ampli
G=5
Fast Shaper
G=100
100ns
3pF
HOLD
T
Trigger
Calibration input
DAC output
3-bit threshold adjustment
10-bit DAC
Common to the 36Channels

Block scheme of SKIROC



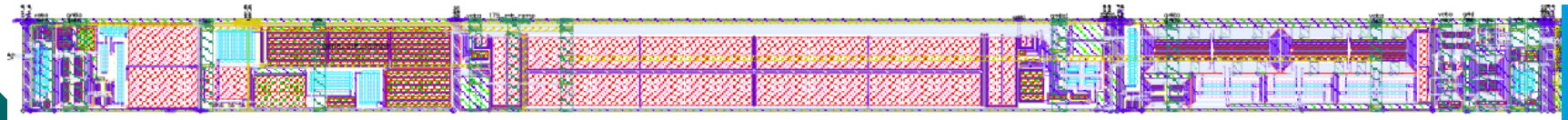
SKIROC status

- Chips in hand
- Test board debugged
- Consumption OK
- Chip alive
- Slow control loading checksum OK

→ First test are conducted now

ADC design

Work done at LPCC (Clermont Ferrand)

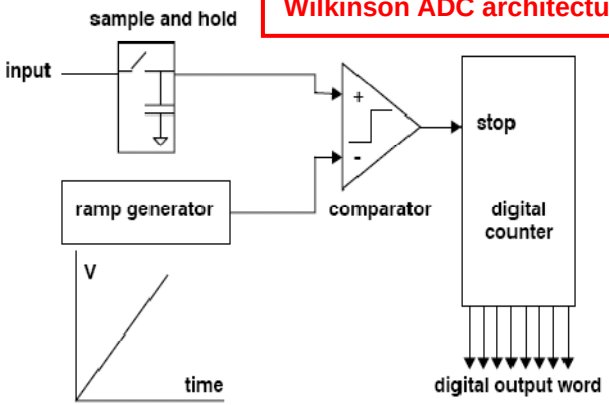


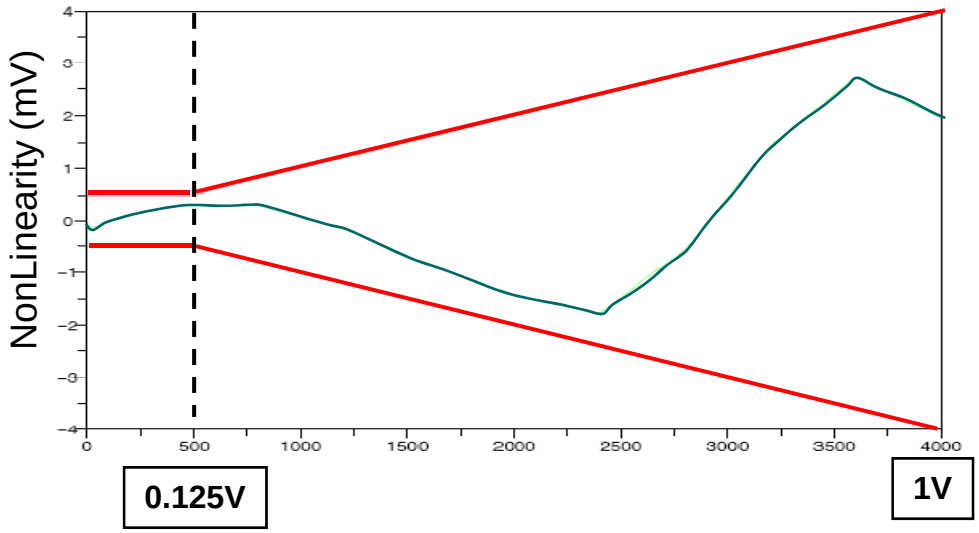
Wilkinson ADC in SKIROC

- **Characteristics:**
  - Technology: BiCMOS SiGe 0.35µm
  - Power supply: 3.5V (digital: 2.5V)
  - Clock frequency: 50 MHz
  - Differential architecture
  - Gray counter
  - Die area: 0.12 mm²

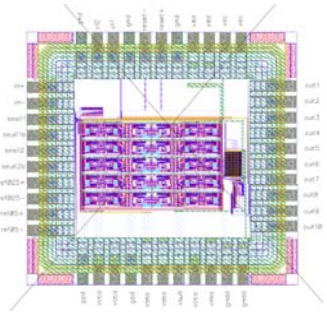
- **Performance (simulated):**
  - Resolution: 12 bits
  - Consumption: 3 mW
  - Conversion time: 80 µs (@ 50MHz)
  - Integrated cons.: (3mW * 80µs)/200ms= 1.2µW
  - Current source (ramp generator):
    - Input dynamic signal: 1V Common Mode
    - 2V differential ramp generator
    - T° sensitivity : 40 ppm/°C max (20 to 50°C)
    - Power supply sensitivity: 5 ppm/°C (±50 mV)

Wilkinson ADC architecture





NonLinearity (simulated):
< ± 500 µV up to 125mV
< 0.1% from 125mV to 1V

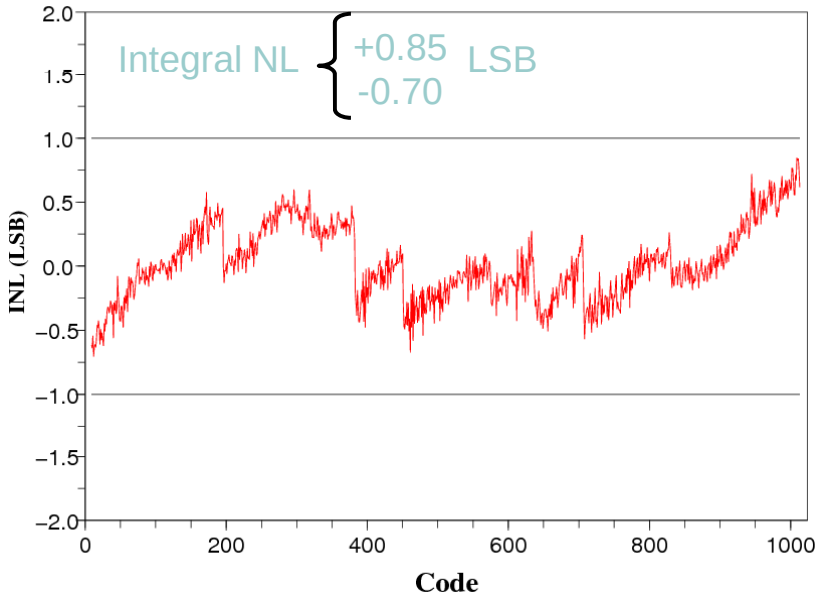


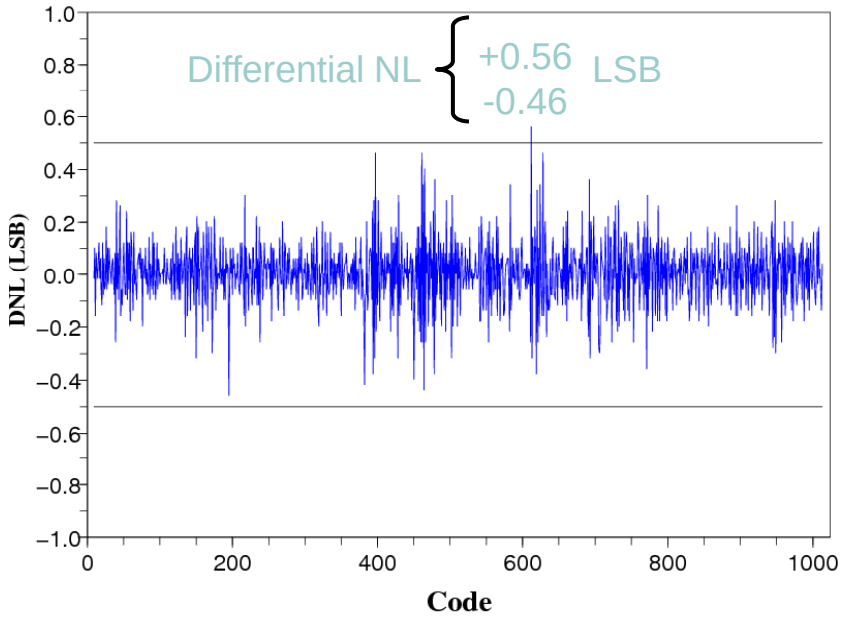
Next step: Pipeline ADC

- Performance (measured):
  - Resolution: 10 bits
  - Consumption: 35 mW
  - Conversion time: 0.25 µs (@ 40MHz)
  - Integrated cons.: (35mW * 0.25µs)/200ms= 0.044µW

- Characteristics:
  - Technology: CMOS SiGe 0.35µm
  - Power supply: 5V (digital: 2.5V)
  - Clock frequency: 40 MHz
  - Differential architecture
  - 10 stages - 1.5 bit/stage
  - Die area: 1.2 mm^2

Noise (measured):
< 0.47 LSB @ 68% C.L.

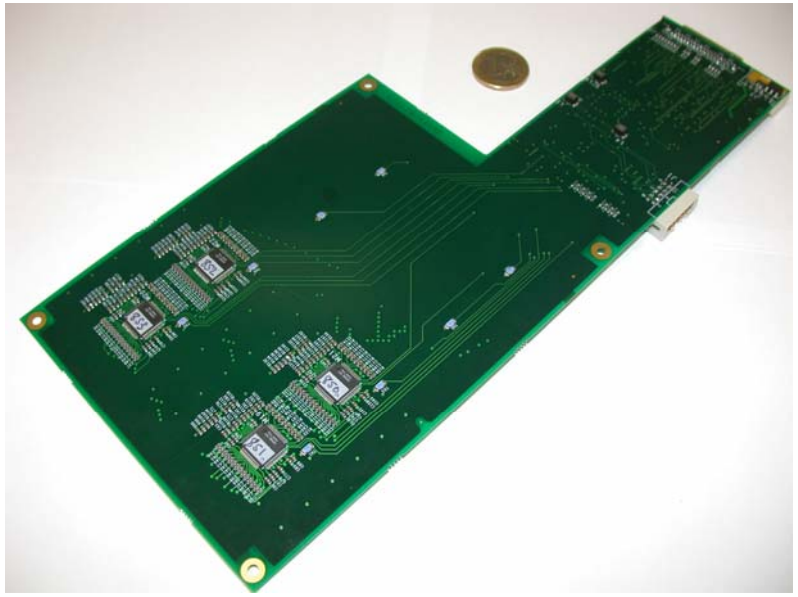




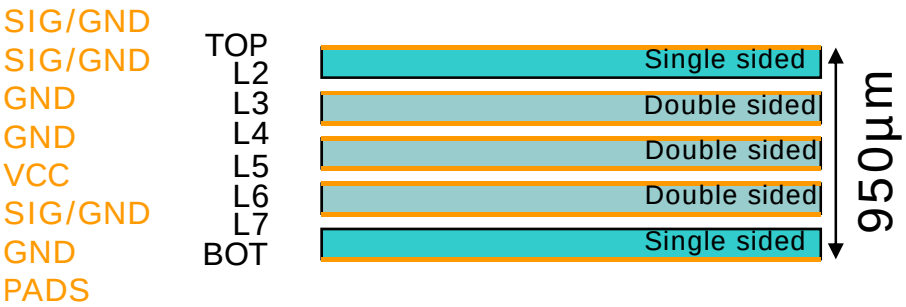
PCBs

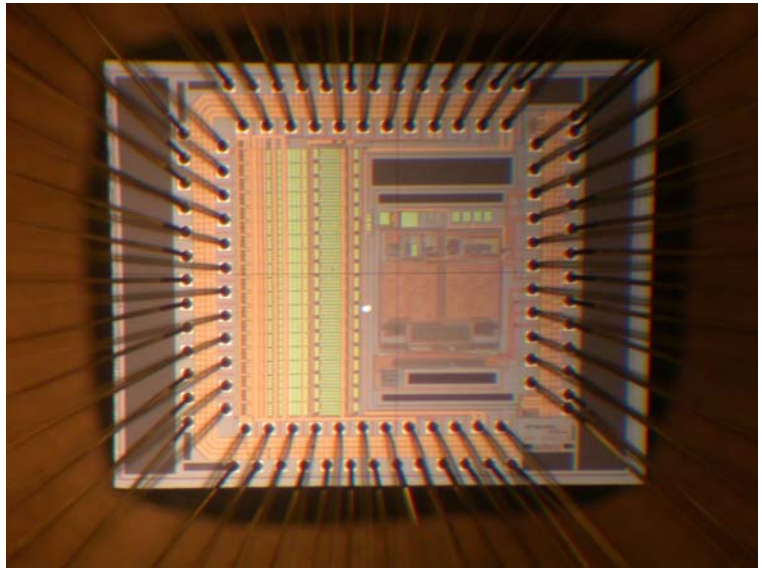
FEV4 : New PCB description

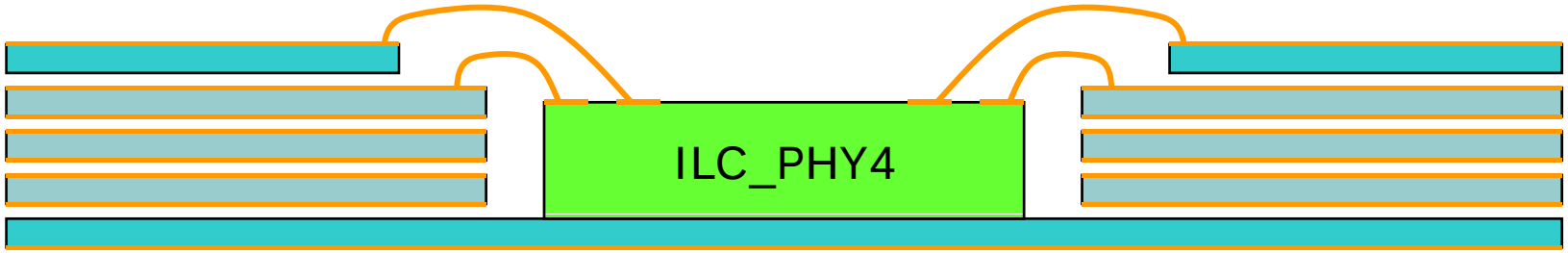
- Compatible physics prototype
- Same size as FEV3
- 1 active wafer (instead of 2 for FEV3)
- Chip buried in the PCB



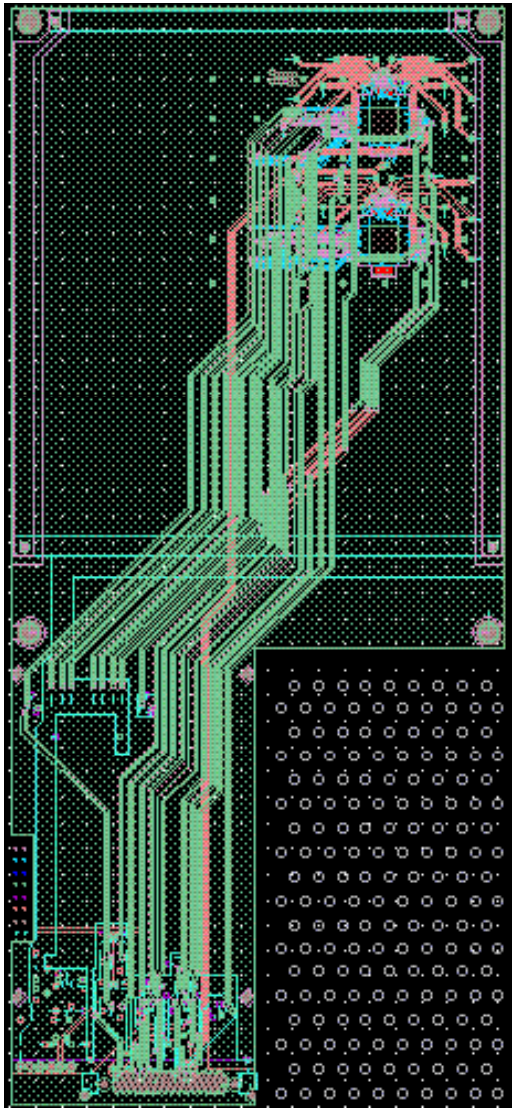
FEV4 – stack up description



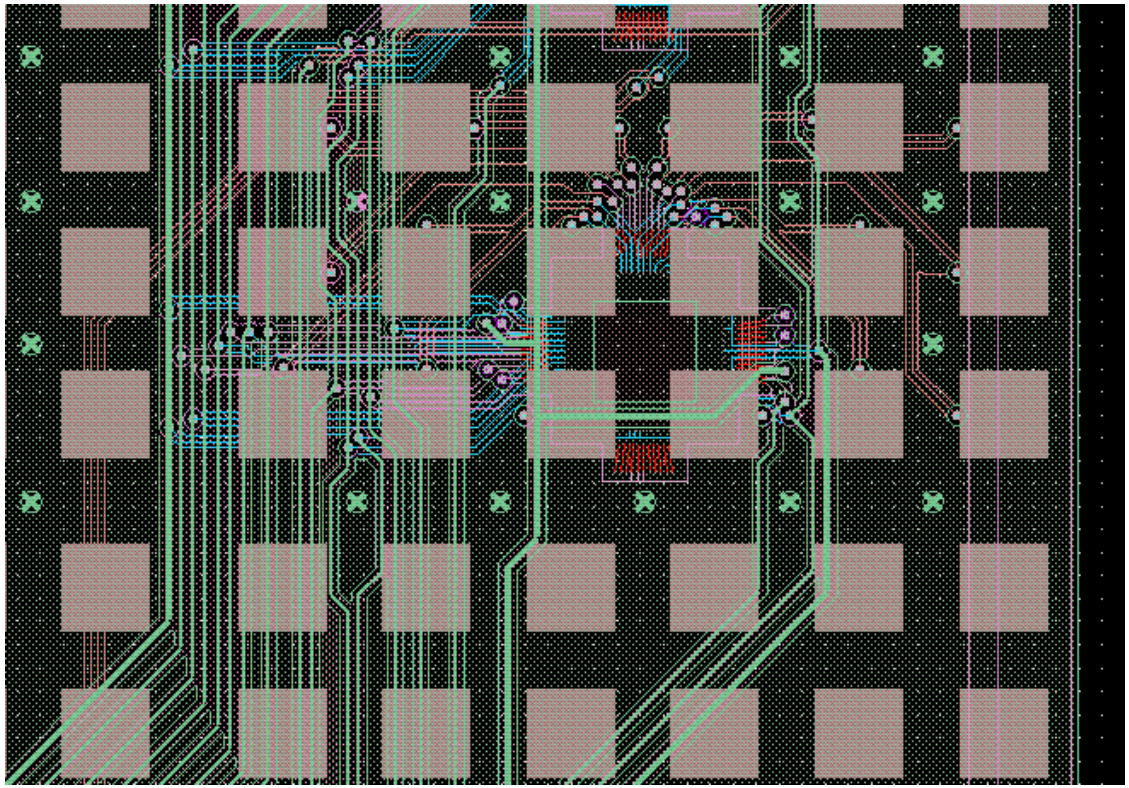




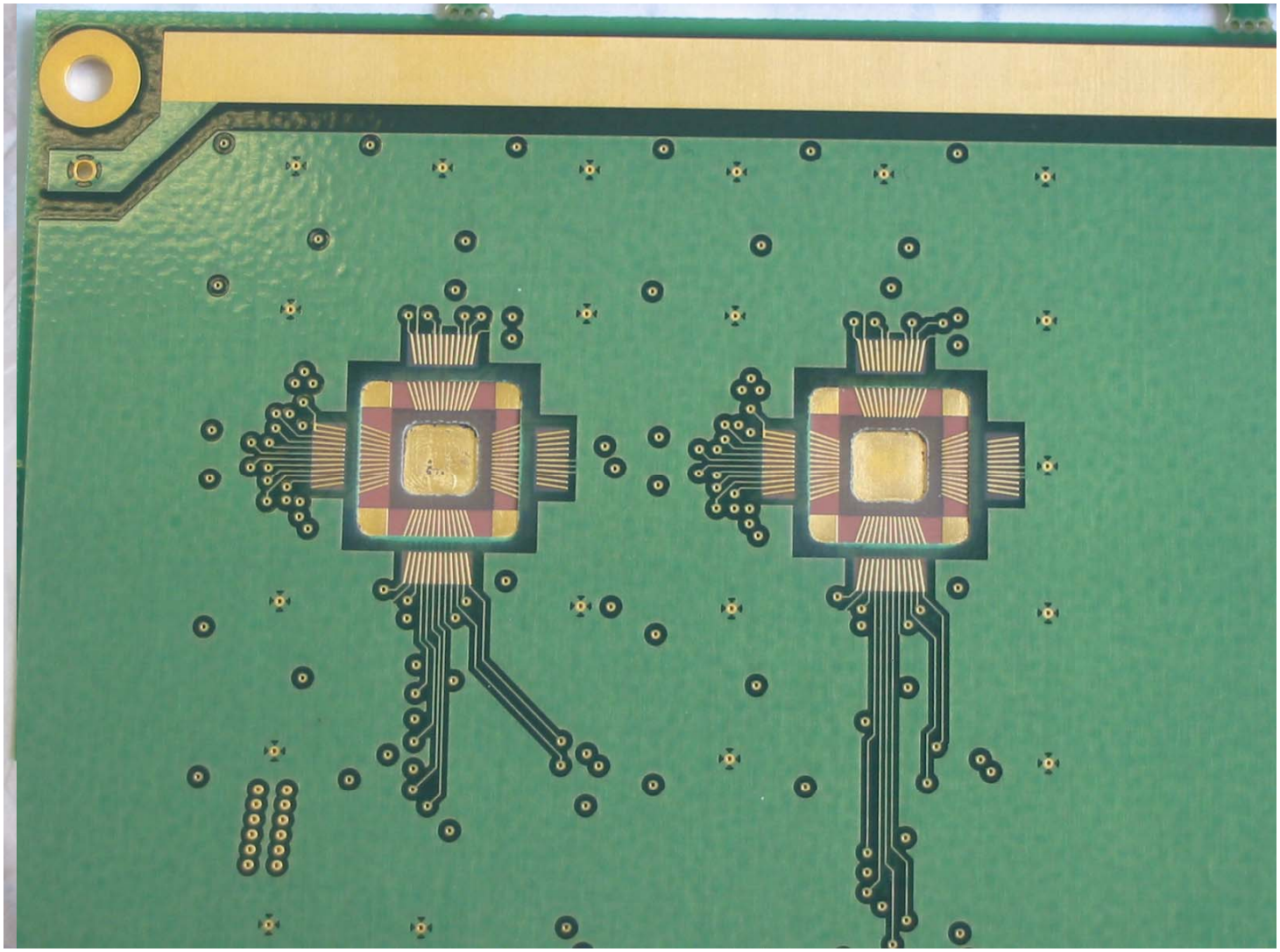
FEV4 – signal density



Difficulty are already foreseen to carry signals from one stitchable PCB to another



FEV4 pictures

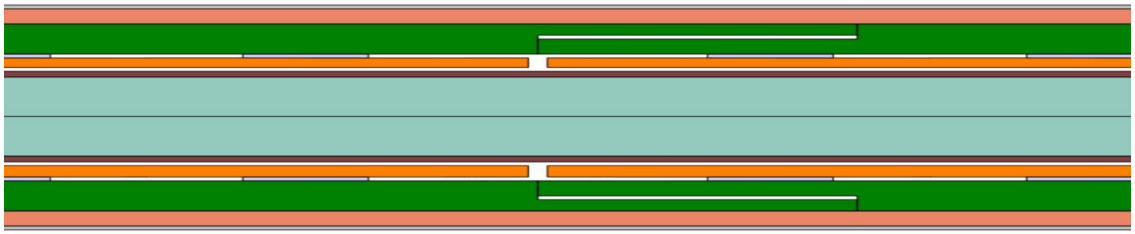


FEV4 duty

- Chip on board test
  - First prototype of chip in board
- Thin PCB coupling measurement
- Chip in beam test
  - Technology is 0.35µ
  - Analog part is very close to final version
  - Digital missing
- Power pulsing test

FEV4 – missing features

- 5*5 mm² pads
- Stitching
- Daisy chain
- Flat buried chip



Conclusion

- Chips are in test
  - MPW has been delayed by a couple of weeks
- 1 Test board is ready
  - 3 more PCBs are due
  - Firmware is in developpment, slow control OK
  - Labview software is in development, SC OK
- First results delayed due to late chip delivery but analogue measurement soon