Status of UK Work on FE and Off-Detector DAQ

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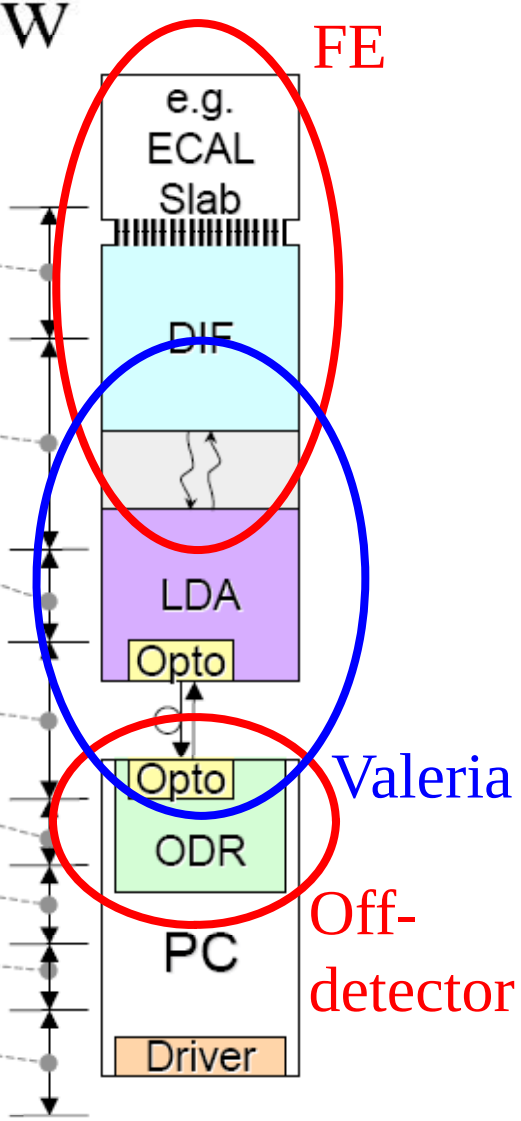
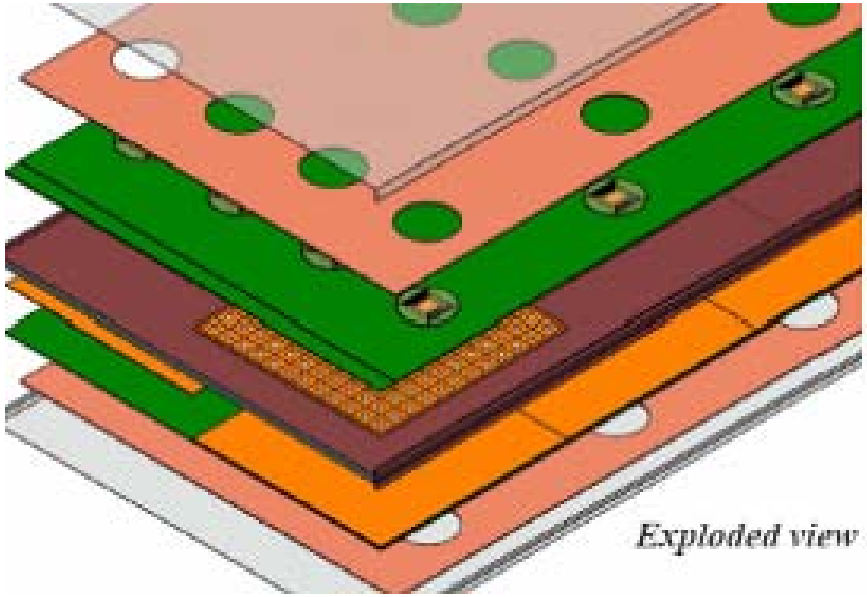
DAQ Overview

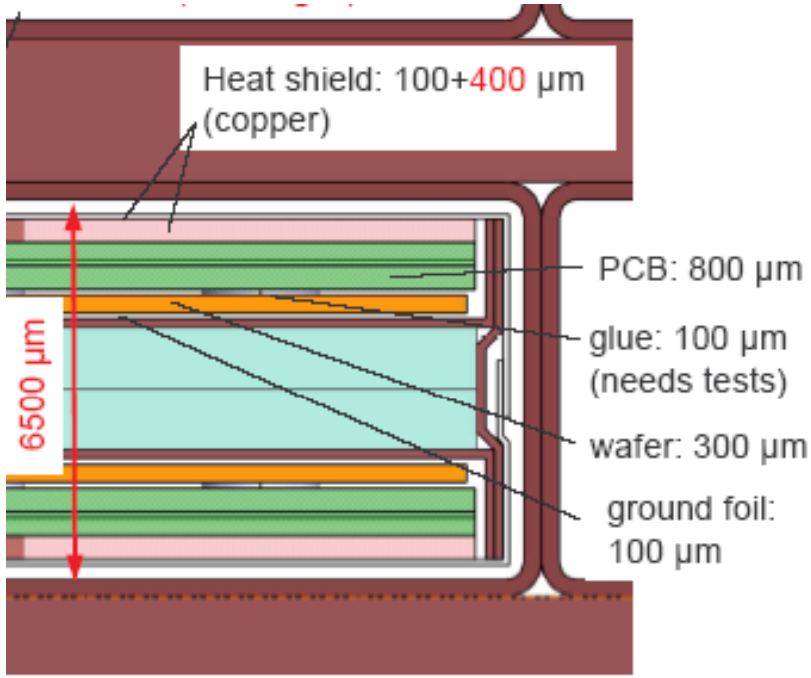
- **Detector Interface (DIF)**
  - Sub-detector specific, in conjunction with detector groups
- **DIF to LDA**
  - Generic, Copper links (25Mbit)
- **Link/Data Aggregator (LDA)**
  - Data format
  - Clock/Commands fan-out
- **LDA to ODR opto-links**
- **Off-Detector Receiver (ODR)**
- **ODR to disk**
  - PCI-Express driver software
- **Local Software DAQ**
- **Full blown Software DAQ**



ECAL slab design



- Constraints on data paths:
  - Limited space (800 µm PCB thickness)
  - Tight power budget («0.3W)
  - Long slabs (~1.6m)

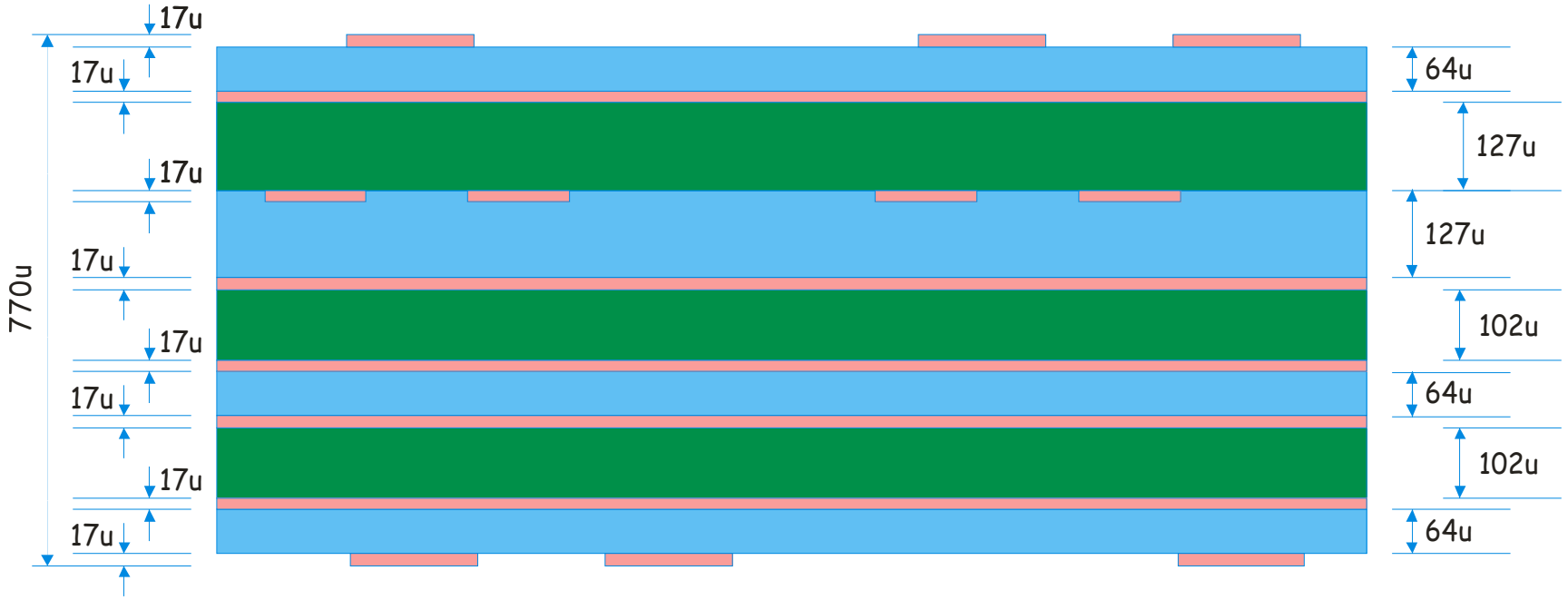


- Technology choices:
  - VFE chip on board; build slab in segments (panels) to conserve yield
  - Joint between PCBs must be zero height; novel interconnect needed
  - CMOS signalling where possible for low power consumption

Slab panel PCB

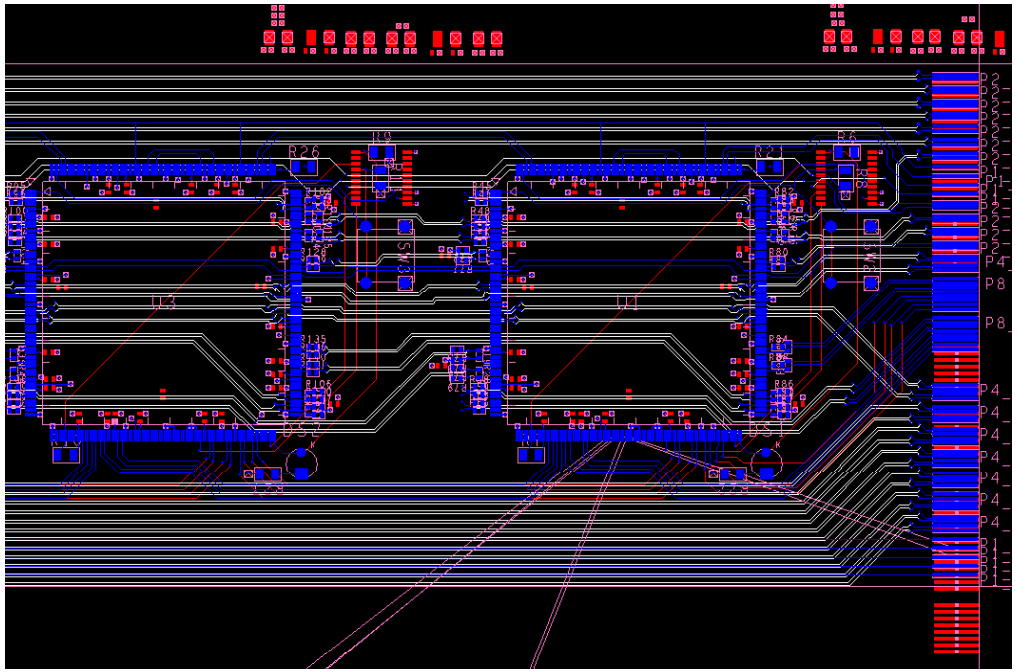
- Target slab PCB thickness = 800µm
- Expected thickness ~ 770µm + resist + text
- Top, bottom and differential signal layers
- 5 power and ground planes
- Transmission line parameters from traces important for noise and power

Trace width (µm)	C_0 (pF/m)	Z_0 (Ω)
200	373	16.5
150	305	20.3
100	229	27.1
75	160	32.8

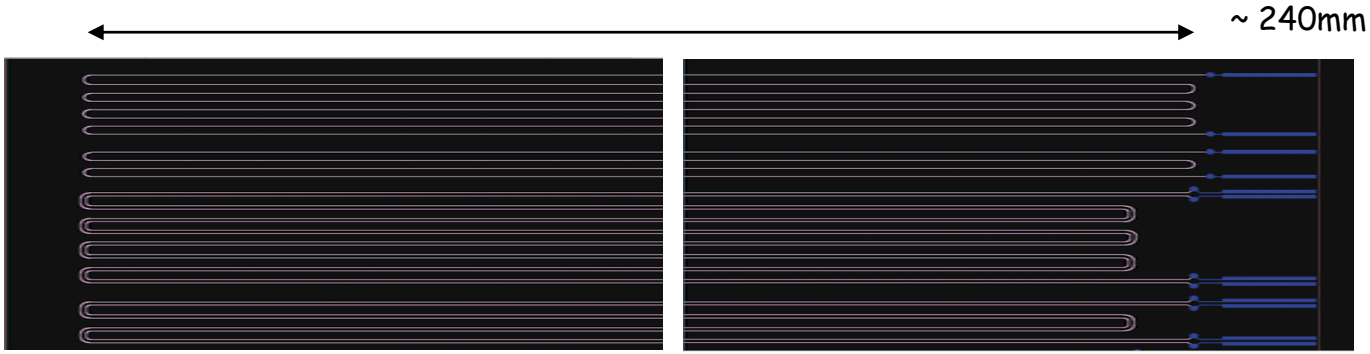


Slab panel model

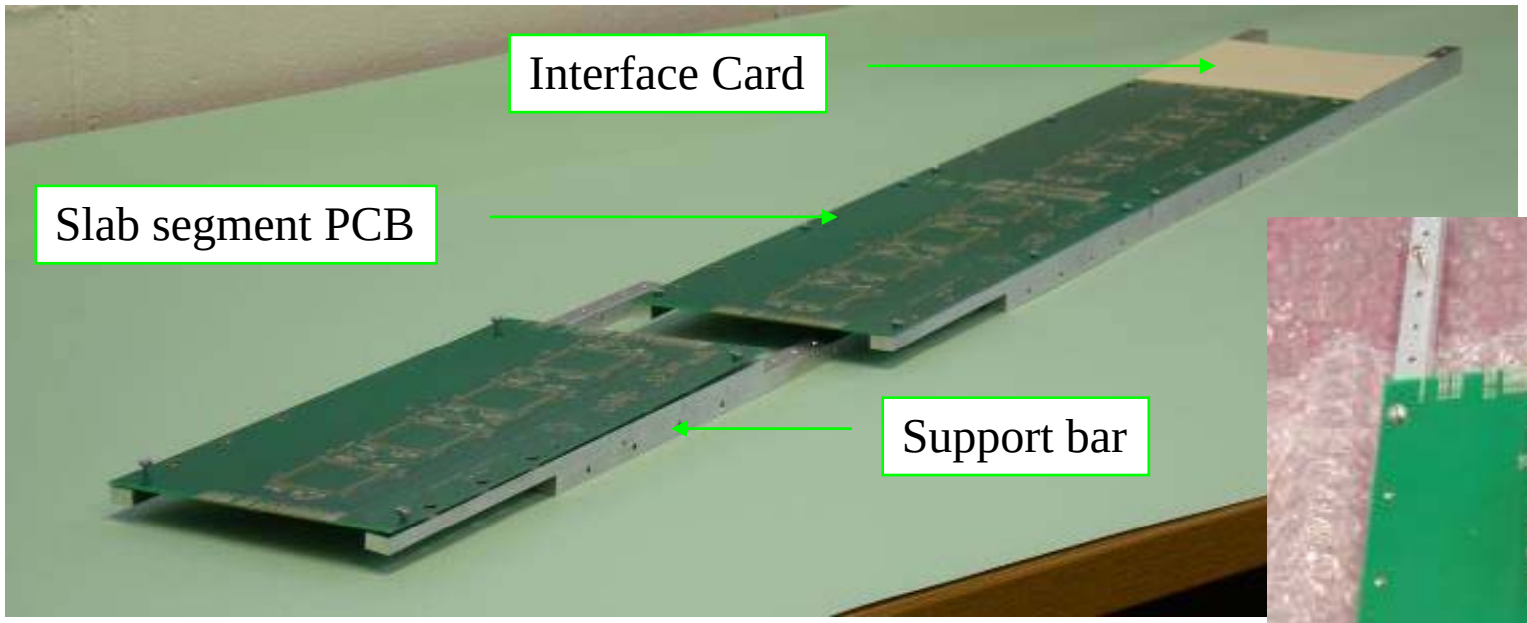
- FPGAs instead of VFE chips; "pseudo-VFE" (pVFE)
- 1 FPGA mimics 2 VFE chips
- HCAL in VHDL serves as VFE



- Many signal distribution/routing options incorporated in PCB
- Many output standards and speeds supported by FPGA
- Includes long, folded lines for measurements on transmission lines

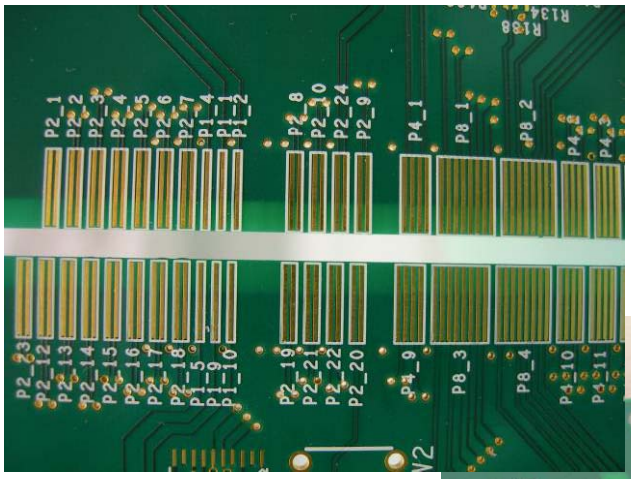


Slab model: current status

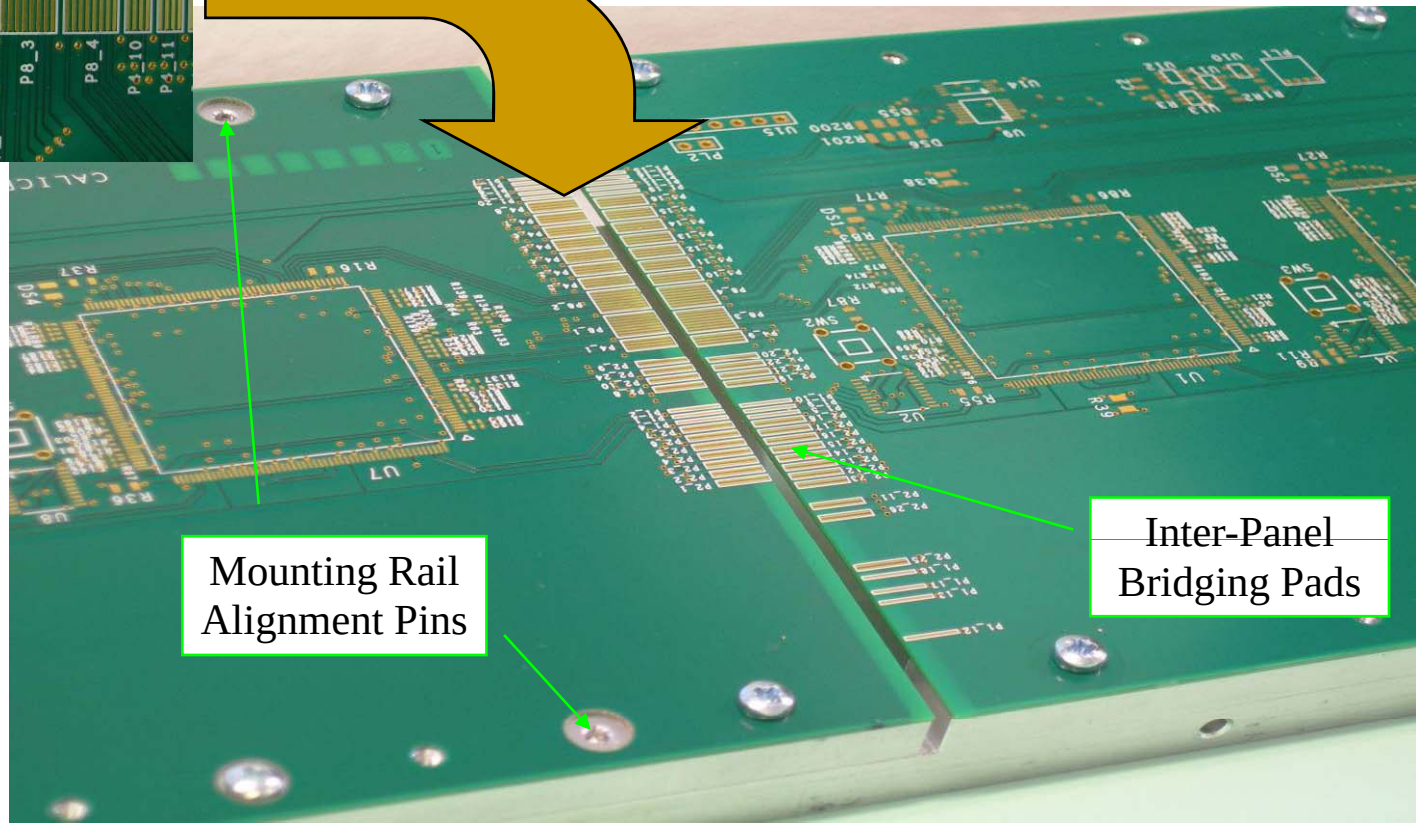


- 10 PCBs manufactured
- PCB support bars for slab assembly
- 1 PCB populated, powered and tested

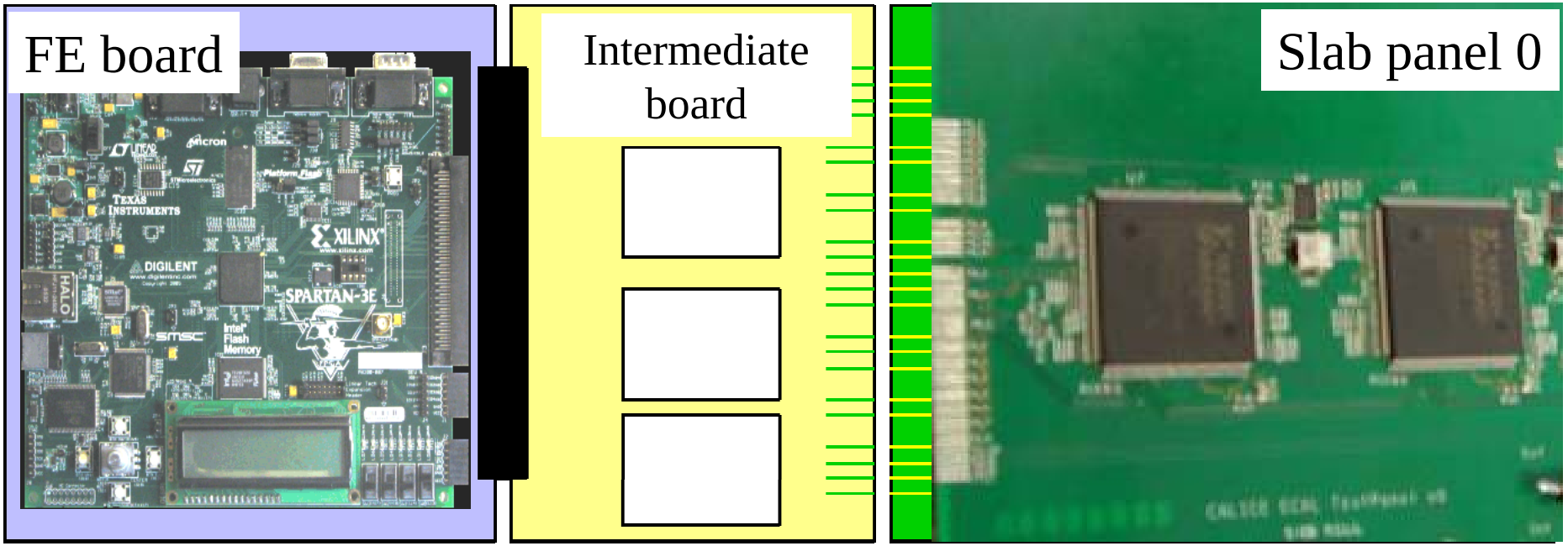
Slab panel PCB interconnects



- Test methods for interconnect



Slab panel test setup



- Clock generation
- Control signals (token,etc.)
- Data reception & buffering
- Interface with outside world

- Clock distribution
- Power distribution
- Interface with slab

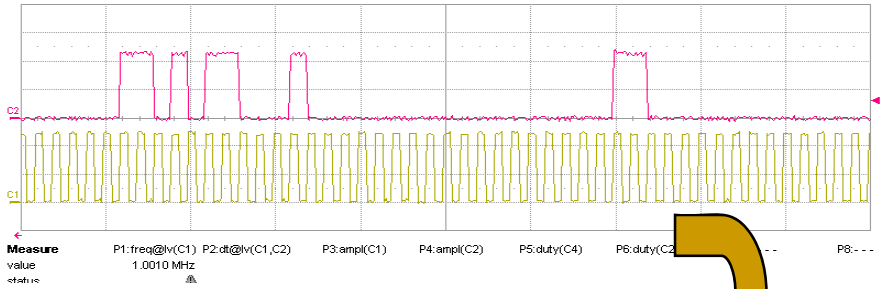
Digilent FPGA development board starter kit serves as FE board for tests

- Combines functions of LDA and system-dependent DIF of “real” system

Test slab current status

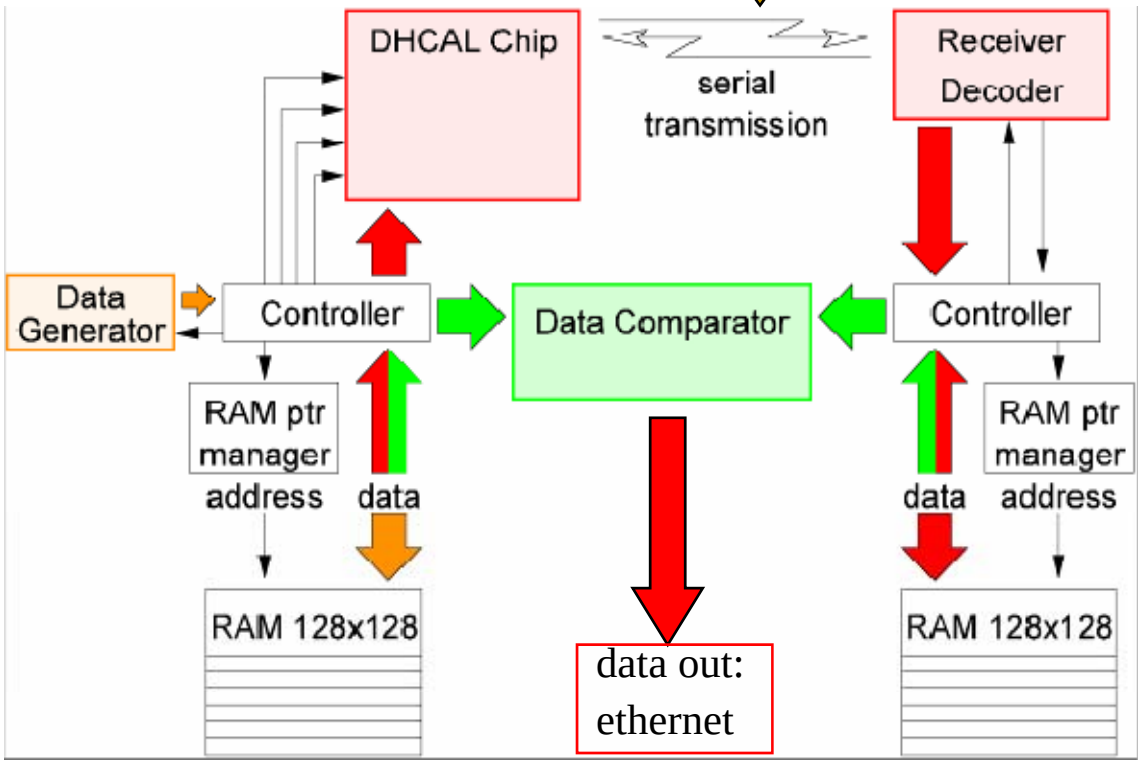
- Slab panel
  - One panel populated and tested
  - Firmware for pVFA FPGAs is effectively ready
- Intermediate board
  - Powered up OK, currently being tested
- FE board
  - Firmware: clock management, deserialiser, data buffer and ethernet communication works
- Slab $\leftrightarrow$ intermediate board $\leftrightarrow$ FE board
  - Connected, ready for commissioning
  - Assembling automated measurement system

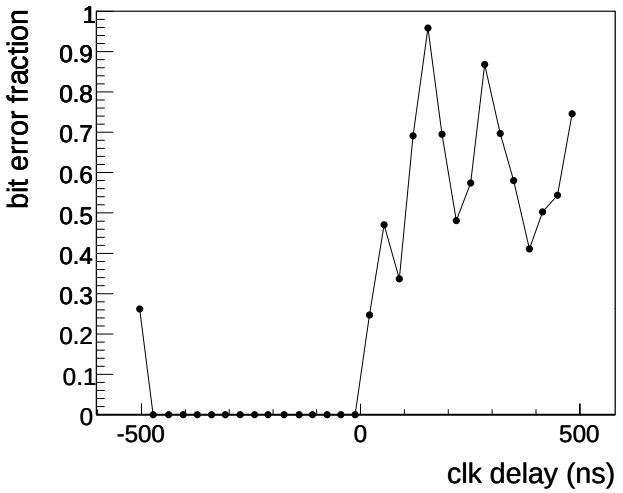
pVFE and FE firmware: BER test



First Bit Error Rate (BER) test:

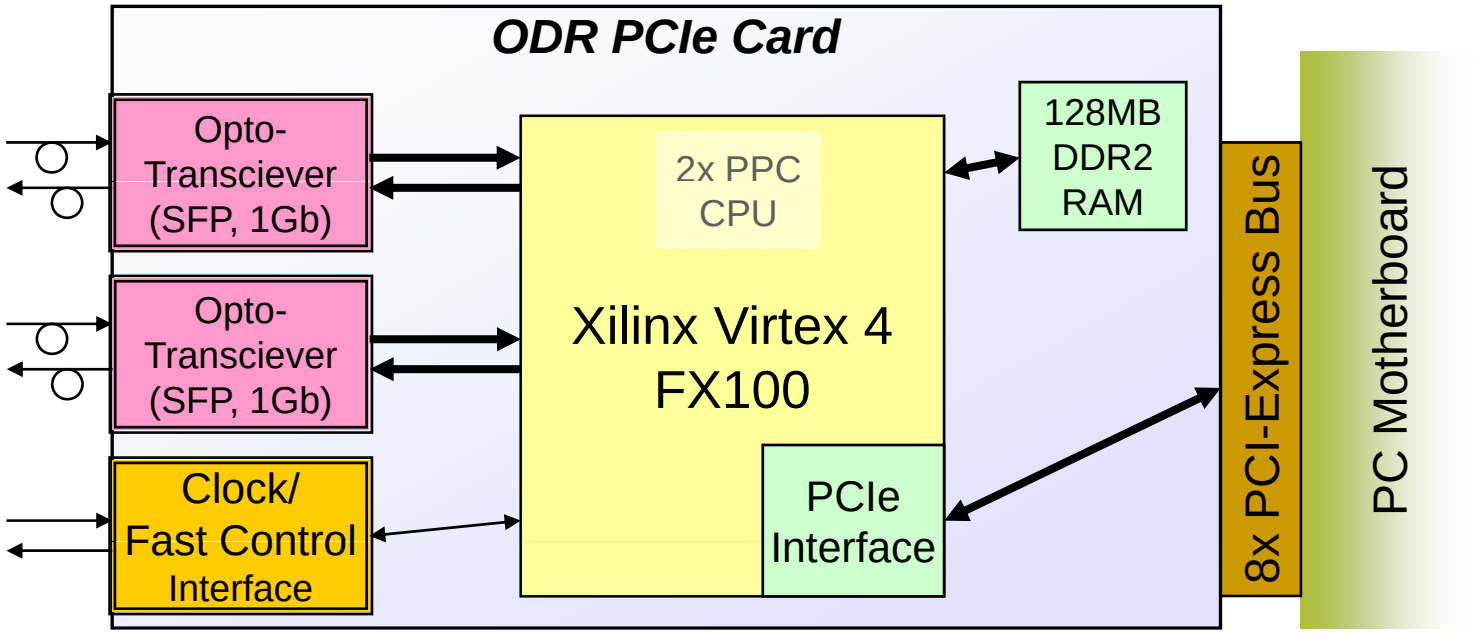
- ✓All logic in single FPGA
- ✓Separated Tx/Rx blocks
- ✓Signals routed through external wires





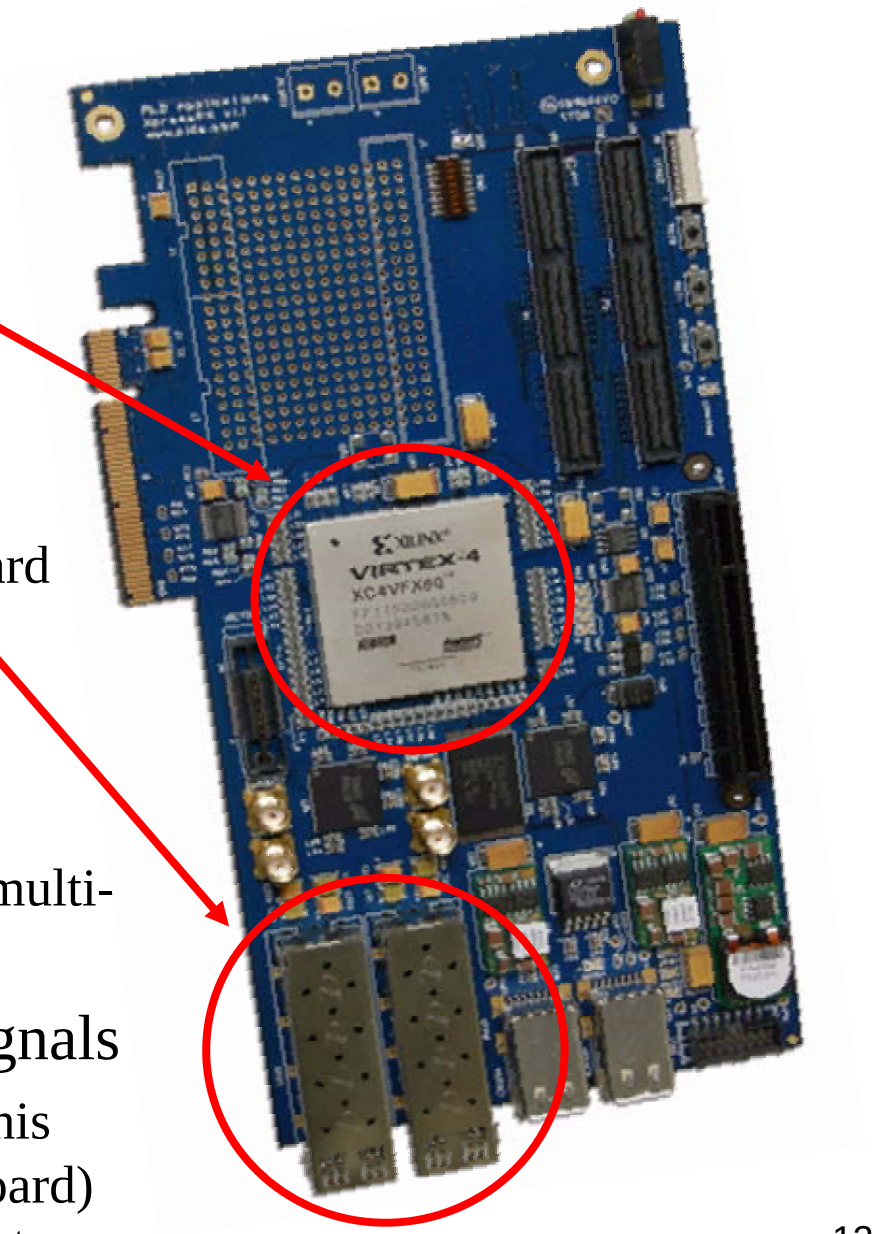
Off-Detector Receiver (ODR)

- Want readout optical fibres to go directly into PCs
  - No crates/custom electronics off-detector
  - Preferably off-the-shelf, commercially available
- "Straw-man" choice of card for data collection into PCs
  - Will be used for EUDET but specs expected to improve in near future



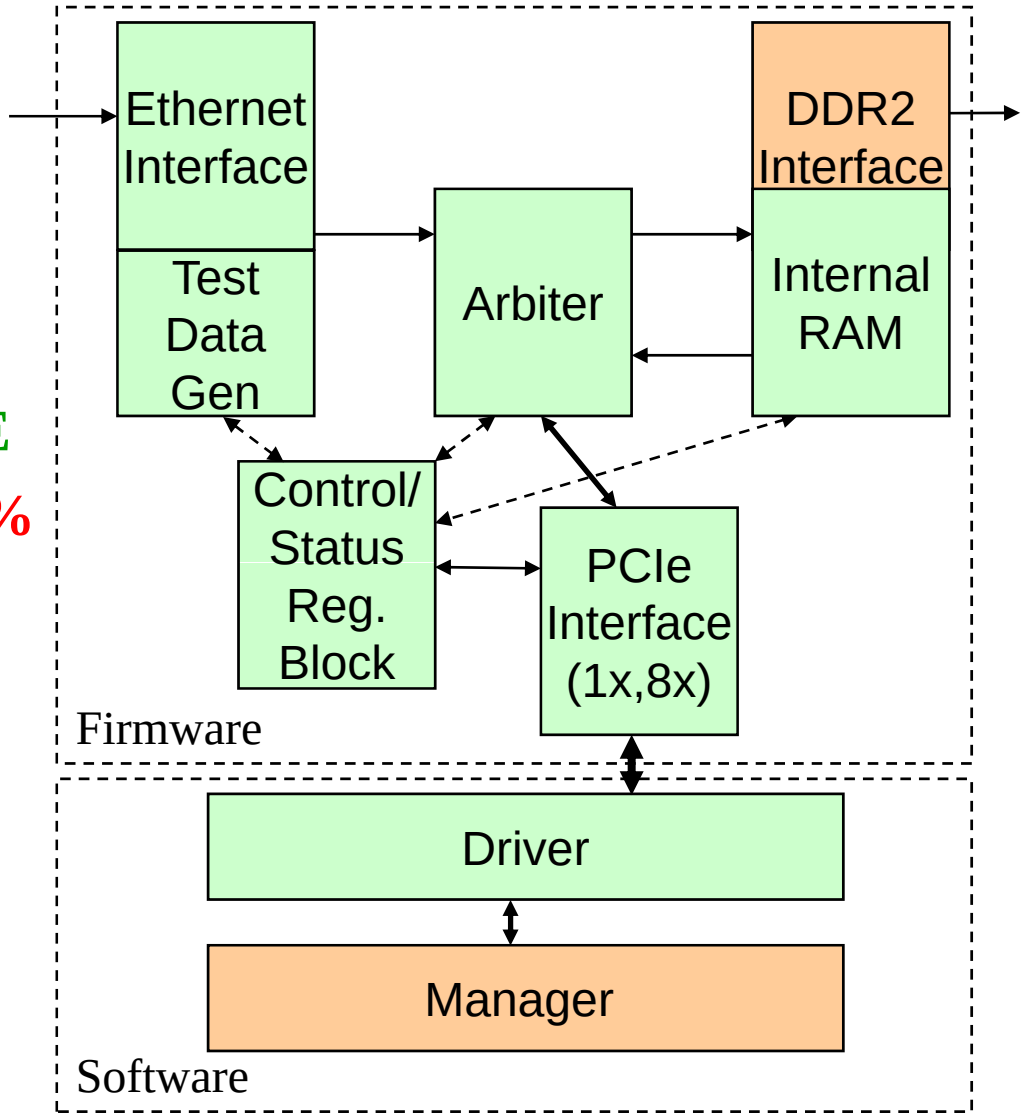
PLDA XpressFX

- PCI-Express Card
  - 8 lanes to PC
- Virtex 4, FX100 FPGA
  - Large FPGA; easily sufficient
- Hosts opto-links
  - 2×SFP on board
  - 3×SFP via commercial expansion board
  - 1.0–2.5Gb/sec optical inputs
- Distribution of clock and control
  - Initially copper (LVDS); later fibre
  - External clock and synch signals for multi-board synchronous operation
- Control may need fixed latency signals
  - Work needed to see if possible with this board (or if needs custom daughter board)

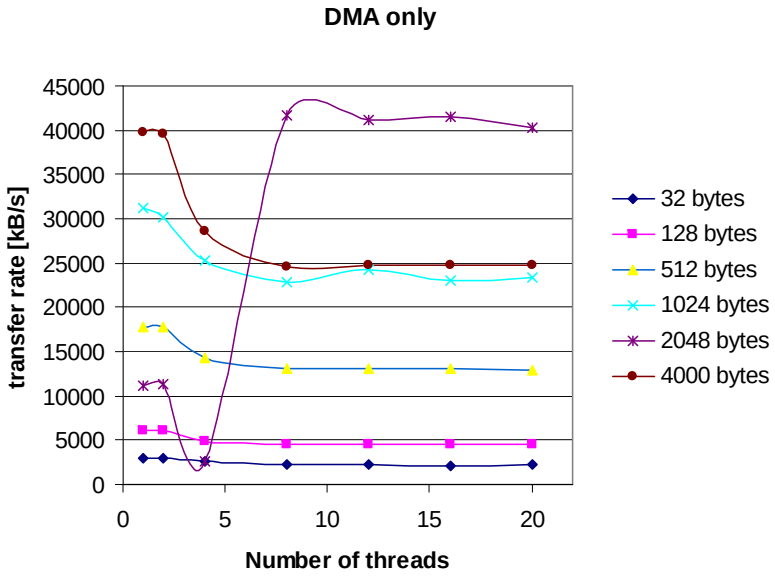


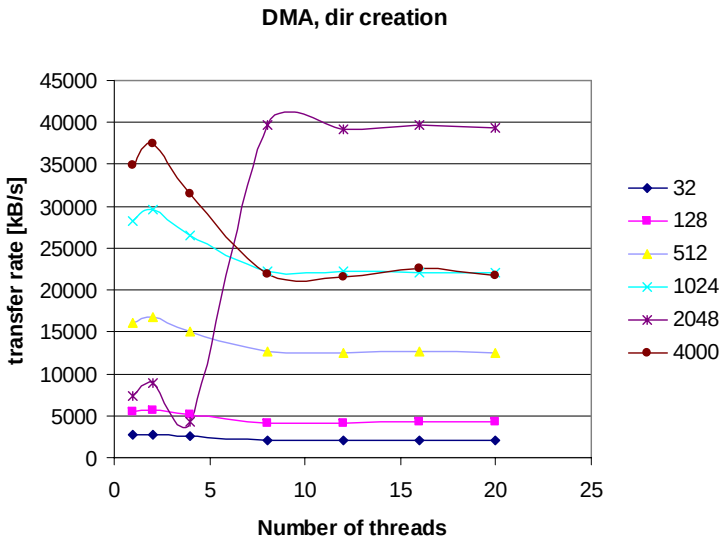
ODR status

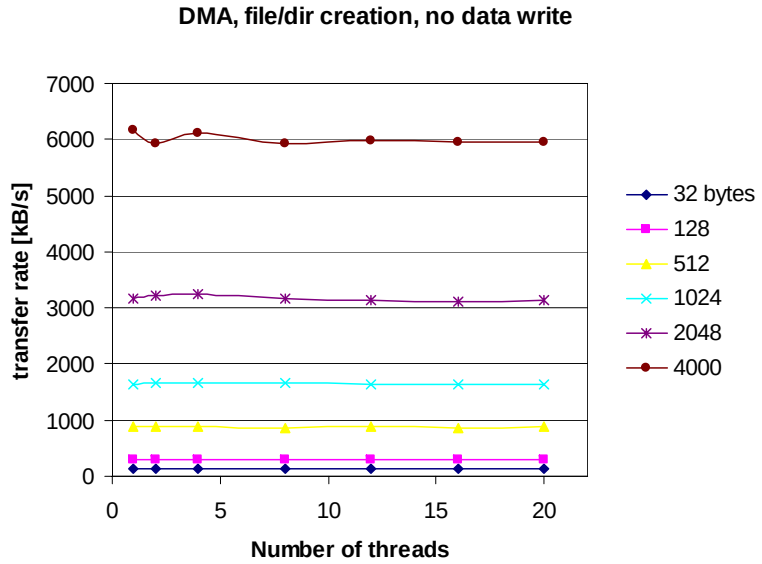
- PCI-Express interface (1x,8x) **DONE**
- Register read/write **DONE**
- DMA access **DONE**
- Gbit (Ethernet) interface **DONE**
- Gbit (fixed latency) interface **0%**
- DDR2 interface **50%**
- Linux driver **DONE**
- Optimised disk store **50%**
- Manager software **50%**
- Performance profiling **50%**
- Clock and control uplink **20%**
- Fast controls interface **0%**

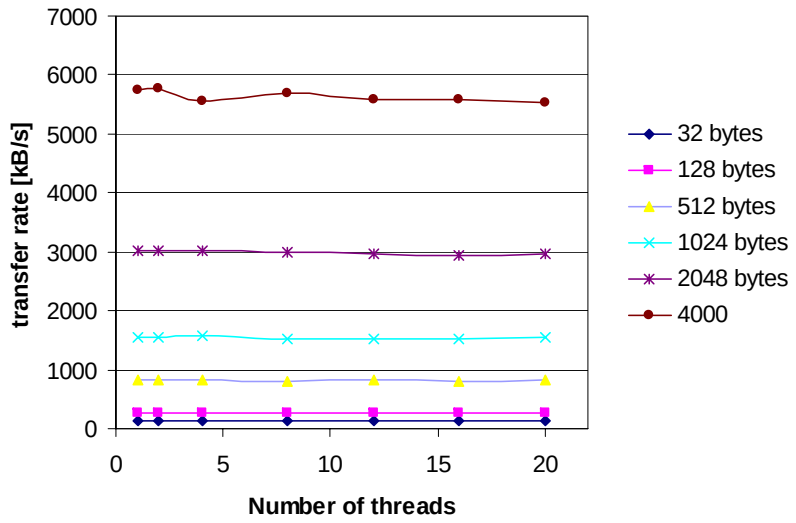


ODR performance



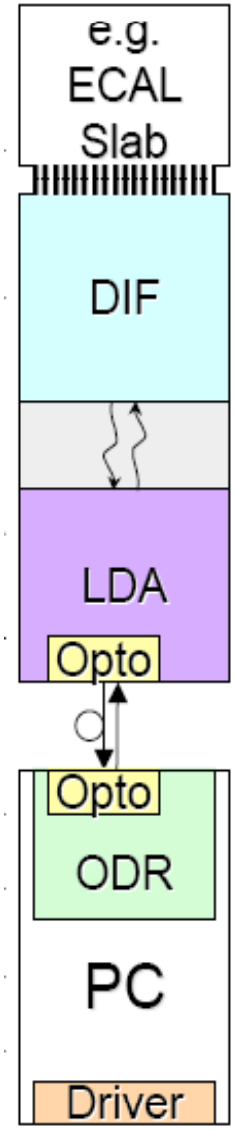






LDA-DIF interface

- ODR is most expensive part of system
  - Minimise number of ODRs and optical links
- LDAs controlled directly from ODR
  - Two optical links = two LDAs per ODR
- The major fanout will be at LDA-DIF connection
  - Simple serial I/O interface; up clock/data, down data?
  - Could have ~50 DIFs per LDA
  - Resulting DIF data rate (1Gb/sec)/50 ~ 20Mb/sec; enough?
- LDA-DIF interface is current focus
  - Must define this clearly soon to allow work on both sides to continue in parallel
  - Need to know requirements for data rates, fan-out numbers, clock frequencies, clock jitter, fixed latency, etc.
  - Hope to firm all this up within the next month



Summary

- Significant effort ongoing to understand how to build an ECAL slab PCB for EUDET and/or a final ILC detector
  - Getting a PCB to meet all the specs will be a major task…
  - …but we are developing the expertise within CALICE to do this
- Straw-man off-detector receiver being tested
  - Will be used for EUDET; technology will move on for final detector
  - Much of the required firmware and software are ready
  - One outstanding issue is ability to run with fixed latency for clock and control
- LDA-DIF interface is a hot topic
  - Input needed from the various subdetectors over next few weeks