Objectives of LLRF Development
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Advance RF Control Technology in the areas of hardware and software to meet the requirements for linear collider and X-ray FEL.

- develop LLRF implementation as HA ATCA System
- develop concept for modular system
- develop multi-channel ASIC version of downconverter
- develop multi-channel downconverter board based on ASIC and standard component
- develop other necessary control systems
- high degree of automation for large scale system, operability
- reliability and availability optimization and cost reduction
- technical performance, pushing the envelope of performance

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Collaborating Institutions:
DESY - Deutsches Elektronen-Synchrotron
DMCS – Department of Microelectronics and Computer Science, Technical University of Lodz, Poland
ISE - Institute of Electronic Systems, Warsaw University of Technology, Poland
INP - Niewodniczanski Institute of Nuclear Physics, Krakow, Poland
IPNO - Orsay
INFN - Padova
PSI

Proposed coordinator: S.Simrock

	Personyears	hardware [KEuro]	travel	
O HA (High Availability) LLRF Implementation in ATCA	21.0	680	150	
- Architecture (incl. standardization), ATCA and uTCA	1.0	20	20	DESY
- Development of ATCA carrier boards with FPGA, DSP	3.0	130	20	DESY,IPNO
- Fast analog IO and digital IO (100 MHz, 14-bit)	2.0	70	10	ISE
- Ultra fast analog IO (2 Gs, 10 bit)	1.0	50	10	DMCS,INFN
- Neutron detector board with customized ASIC	4.0	100	20	DMCS
- Gamma detector board	1.0	30	10	DMCS
- Integration of downconverters and upconverters	1.0	40	10	DESY
- Digital signal processing	2.0	30	10	DCMS
- Communication	2.0	80	20	IPNO
- Redundancy and self diagnostics	2.0	40	10	DMCS
- HA Design (HW, SW), QA and QC	2.0	90	10	DESY
o High precision Timing and Synchronization for LLRF	7.0	250	65	
- Integration MLO, MO, Timing	1.0	70	10	ISE
- Integration pulsed optical with RF	1.0	30	10	DESY
- Precision temperature stabilization of the reference frequency coax cables	2.0	30	15	INP
- Cal. Reference and LO to downconverters	1.0	50	10	DESY
- Clock synthesizer for LLRF ADCs	1.0	30	10	ISE

- Int. with ultrast. timing and clock, event, (data ?)	1.0	40	10	ISE
o Software Architecture and Implementation Strategies	16.0	430	90	
- Software architecture	3.0	20	20	DESY
- Software development tools	1.0	50	10	DMCS
- Software documentation tools	1.0	40	10	DMCS
- Distribution of Algorithms (FPGA, DSP, CPU)	2.0	20	10	ISE
- Software/hardware co-design	2.0	80	10	DMCS
- Communication protocols	1.0	60	10	ISE
- Algorithm development	5.0	100	10	DESY
- Diagnostics (HW & SW)	1.0	60	10	DESY
o Precision RF Field Measurement	5.0	190	30	
- Low noise, low drift downconverter (field detector)	2.0	60	10	INFNP
- Low cost, low real estate, multi-channel downc. (ASIC)	2.0	80	10	DMCS,ISE
- Transient detection (low cost multichannel)	1.0	50	10	DMCS,DESY
o Other control systems	4.0	`120	30	
- RF Gun temperature stabilization	1.0	40	10	INP
- WGT control system	3.0	80	20	INP
o Procedures for Commissioning and Operation	10.0	320	60	
- Commissioning and Operation Procedures	2.0	80	10	DESY
- Automation of Operation	2.0	20	10	DMCS
- Cavity simulator including rf front end	2.0	90	10	ISE
- Interfacing to other accelerator subsystems	2.0	40	10	DESY
- Interlocks	1.0	20	10	ISE
- Monitors	1.0	70	10	ISE
o Fast Frequency tuner	4.0	160	30	
- Piezo driver	1.0	50	10	DMCS
- Increased stroke of PZT	?	?	?	?
- Segmented fusing of piezostacks	1.0	40	10	DMCS
- Microphonics control	2.0	70	20	DMCS
O Beam feedbacks for LLRF	6.0	160	30	
- Beam feedback Concepts	1.0	20	10	PSI
- Beam diagnostics and monitors (Int. with LLRF)	3.0	60	10	PSI
- Beam feedback prototype impl. At FLASH	2.0	80	10	PSI
	73.0	2310	485	

HA (High Availability) LLRF Implementation in ATCA

The demand for high availability, modularity, standardization and long time support favors the choice of the ATCA and uTCA standards with carrier boards and AMC modules. This technology is basis for the ILC technical design. Presently none of the required AMC boards for ADCs, DACs, downconverters, clock synthesizers etc. are available. Therefore a development of these boards using state-of-the-art technology is necessary.

Architecture (incl. standardization), ATCA and uTCA

The LLRF system architecture based on ATCA and uTCA can be structured in several ways. The wide application of commercially available components is highly desirable since it allows reducing costs. On the other hand many features of the LLRF control system are unique and components realizing these functions not exist in other systems. It is necessary to design the LLRF control system in a way that optimize the total costs while keeping high commercial standards on reliability, availability, maintainability and others.

Deliverables:

- Report on system architecture and standardization.

Development of ATCA carrier boards with FPGA, DSP

The LLRF control system will be build using modular approach basing on ATCA and uTCA architecture. The input signals will be processed by AMC plug-in modules hosted by carrier board. The required carrier boards are not commercially available and must be developed.

Deliverables:

- Design and manufacturing of the carrier board prototypes.
- Report on characterization of the system.

Fast analog IO and digital IO (100 MHz, 14-bit)

The LLRF control system will be build using modular approach basing on ATCA and uTCA architecture. The input signals will be processed by AMC plug-in modules hosted by carrier board. The AMC modules featuring required functions are not commercially available and must be developed.

Deliverables:

- Design and manufacturing of the AMC modules with required functionality.
- Report on characterization of the system.

Ultra fast analog IO (2 Gs, 10 bit)

The sampling rate of analogue to digital converters is constantly increasing. Soon this will create possibility to remove some obsolete hardware such as downconverters and sample higher frequency signals directly. The main purpose of this project is to test existing fast ADC (sampling parameters, connection to processing units, etc.) and to determine the possibility of direct sampling of RF signals. The AMC board will be designed and tested. It will be also evaluated in industrial version of the transient detector.

Deliverables:

- AMC board with fast ADC
- firmware for the board

- performance tests report

Neutron detector board with customized ASIC

Two main types of radiation are produced during the operation of high-energy linear accelerators: bremsstrahlung photons and photoneutrons, like XFEL or FLASH. Radiation sensors are required to monitor and control radiation environment of a linear accelerator. Presence of mixed gamma and neutrons radiation requires selectively sensitive dosimeters. A distributed system should allow to monitor radiation in real-time.

Various neutron dosimeters are available on the market. However, real-time dosimeters have insufficient sensitivities to monitor radiation in the XFEL tunnel. Performed research proved that Static Random Access Memory can be applied as a neutron dosimeter. Un-moderated SRAM chips are ideal thermal neutron detectors. Unlike other dosimeters' chips (TLD 600) the SRAMs are insensitive to gamma rays. Memories available on the market have rather poor sensitivities (in range of 1·108 n·cm-2). The main advantage of dosimeters is high insensitivity to gamma radiation. High background gamma present in the XFEL tunnel cannot generate any SEUs in the memory.
Neutron-sensitive memory arrays will be designed and fabricated in the customised application-specific integrated circuit (ASIC). Different methods can be applied to improve memory cell's sensitivity to neutron-provoked Single Event Effects (SEUs). Radiation-sensitive cells will be developed during the first phase (sub-task 1). Various memory cells will be tested with SPICE and NanoTCAD simulators. The most sensitive cells will be used to design the first ASIC with test arrays of static memories. Memory arrays will be fabricated as integrated circuits in technology allowing applying boro-phosphate-silicate-glass (BPSG) layer with 10B boron to improve sensitivity of designed detectors. The fabricated dosimeter will be evaluated with 241AmBe neutron source and tested in the FLASH accelerator tunnel. The most sensitive cells will be used to design the final integrated circuit, second ASIC. The final dosimeter will be composed of a higher capacity memory array than ASIC 1. The final dosimeter will be calibrated. A dedicated readout system is required to evaluate neutron fluence measured by SRAM-based dosimeters. A digital portable reader will be developed and built to perform tests of the first integrated circuit with test memory arrays. Finally, the system equipped with CAN or EIA RS 485 interface will be developed and built for a real-time neutron detector. The fabricated final neutron fluence dosimeter (ASIC 2) will be calibrated in-situ in the FLASH/XFEL tunnel.

List of subtasks

- Study, comparison and simulation of various radiation sensitive SRAM cells
- Selection of optimum radiation-sensitive cells for the neutron dosimeter array
- Design of a test integrated circuit ASIC 1
- Design and fabrication of a prototype board for initial tests of dosimeters
- Fabrication of the test integrated circuit ASIC 1 in the silicon foundry
- Tests in the radiation environment and selection of final cells and the detector structure
- Design of the final integrated circuit ASIC 2 of the neutron fluence dosimeter
- Fabrication of the final integrated circuit ASIC 2 in silicon foundry

- Tests and calibration of the neutron dosimeter

Gamma detector board

Gamma radiation monitoring in a linear accelerator requires an application of real-time gamma dosimeter. Various dosimeters are available for gamma measurement. However, available dosimeters have different sensitivities, linearities, temperature coefficients and time stabilities. Radiation sensitive Field Effect Transistors (RadFETs) fabricated by different companies and Optically Stimulated Luminescence (OSL) dosimeters will be tested. Finally, the most suitable dosimeter will be selected (good sensitivity and long-term-temperature stability). All mentioned dosimeters generate an analogue signal. The signal must be amplified and then digitalized before the measured dose is evaluated. A simple data acquisition system (DAQ) will be designed and built for initial dosimeters tests. Finally, a detector board equipped with temperature a compensation system will be designed and fabricated. The detector board equipped with the selected dosimeter will be finally calibrated.

List of subtasks

- Study and comparison of available gamma dosimeters
- Design and fabrication of prototype board for initial tests of dosimeters
- Radiation sensitivity tests of selected gamma dosimeters
- Design of detector board
- Fabrication of detector board
- Tests and calibration of gamma dosimeter

Time schedule, deliverables and milestones

Task Name	Milestone	Main Deliverables	Months
WP 1.1			
Study, comparison and simulation of various radiation sensitive SRAM cells		Report	3
Selection of optimum radiation-sensitive cells for neutron dosimeter array		Design of sensitive Cell	1
Design of test integrated circuit ASIC 1		I.C.design ASIC 1	6
Design and fabrication of prototype board for initial tests of dosimeters		Test board	3
Fabrication of test integrated circuit ASIC 1 in silicon foundry	ASIC 1		6
Tests in radiation environment and selection of final cells and detector structure		Report on tests results	3
Design of final integrated circuit ASIC 2 of neutron fluence dosimeter		I.C.design ASIC 2	6
Fabrication of final integrated circuit ASIC 2 in silicon foundry	ASIC 2		6
Tests and calibration of neutron dosimeter	Detector		3
WP 1.2			

Study and comparison of available gamma dosimeters		Report	3
Design and fabrication of prototype board for initial tests of dosimeters		Test board	6
Radiation sensitivity tests of selected gamma dosimeters		Report on tests results	6
Design of detector board		Board design	6
Fabrication of detector board	Board	Detector board	3
Tests and calibration of gamma dosimeter	Detector	Report	3

Integration of downconverters and upconverters

The analogue downconverters and upconverters circuits must be integrated with digital control system operating in ATCA or uTCA crate. Therefore special countermeasures have to be provided to secure analogue parts from disturbing influence of digital signals. It would also very convenient to put downconverters and upconverters on Rear Transition Module of the ATCA crate and connect the cables from the back side of the crate avoiding cables mesh at the front side.

Deliverables:

- Design of downconverters and upconverters in RTM
- Performance test report.

Digital Signal Processing

During last years fast progress on FPGA market is observed. New generation FPGA chips are equipped with such features as dedicated DSP blocks, embedded processors and fast serial links. From the viewpoint of parallel calculations they left traditional DSP chips behind. To accommodate all this features, the new approach to digital signal processing needs to be developed. During this task flexible processing block will be designed. They can be used as a firmware for FPGA based Low Level Radio Frequency system. This will help to achieve better field stability and much more features in comparison with existing DSP system.

The developed techniques will be used in various applications improving their performance, flexibility, reliability, testability. The open list of possible application areas includes:

- field detection module
- feedback module
- linearisation module
- digital upconversion module
- communication module
- embedded system integration
- DSP system integration

Deliverables:

- the firmware for ATCA system (Cavity Field Controller)

Communication

The LLRF control system will be highly modular and therefore the inter-module communication will be crucial for machine operation. The hardware layer of communication links must be designed and optimized for the particular interface, aiming required communication parameters (e.g. latency, throughput, noise susceptibility, electromagnetic compatibility etc.). For long distance communication optical communication can be the most effective. In case of systems located in close proximity, fast electrical communication can be suitable. Especially, Low Voltage Differential Signals (LVDS) can be used in many different applications, like chip-to-chip (on-board) communication, interface with optical transceivers, board-to-board cable communication, and the ATCA backplane and AMC modules communication.

Deliverables:
Designs of communication links hardware between system components.

Redundancy and self diagnostic:

The basic objectives of the proposed research activity are:

- to identify the critical parts of the system, that must be available during operation
- to develop control strategy when parts of the system are not available
- to develop software techniques improving the reliability of operating system and user applications
- to develop methods for hardware and software faults detection in the digital control systems
- to develop methods for detection of faults and deterioration of analogue parts including also power supplies
- to implement the developed techniques in the control system based on ATCA

Deliverables:
Report on developed methods, techniques and algorithms.
Implementation of these methods, techniques and algorithms in LLRF control system.

HA Design (HW, SW), QA and QC

The developed hardware must be reliably operated in harsh environment of linac tunnel. Therefore the procedures of circuit design, manufacturing and testing must be worked out, that will allow to keep high quality.

Deliverables:
Requirements, design and tests procedures.

High precision Timing and Synchronisation for LLRF

Precision timing signals in form of clocks and event triggers are required for digital control system to guarantee synchronicity of ADC data with the electron bunches and allow for digital rf field detection. The clocks signals are in the 100 MHz range require stabilities of the order of a few picoseconds. Also available must be rf reference signals as local oscillator signals for downconverters and as rf calibration signals with a long stability of the order of 100 femtoseconds. Although the development of system components is quite advanced, it will be necessary to integrate all this systems for accelerator operation.

Integration MLO, MO, Timing

The reference signals from Master Oscillator and timing synchronization signals must be available in LLRF system. Since the system must be highly reliable and available the redundant reference and timing boards must be present in the crate and switched on request while providing required quality (jitter and drift) of the signals.

Deliverables:
The designed and manufactured AMC modules with reference signals and timing functionality.

Integration pulsed optical with RF

The reference and timing signals can be distributed in electrical and optical form. For the optical fibers the AMC modules featuring optical receivers and transceivers must be developed and integrated in AMC module.

Deliverables:
The designed and manufactured AMC modules with optical signals transceivers.

Precision temperature stabilization of the reference frequency coax cables

The temperature changes influence the RF cables causing phase drifts in reference signals. Therefore the cable temperature should be stabilized. The cable temperature monitoring and stabilization system must be developed; installed in accelerator and integrated in existing control system.

Deliverables:
Temperature stabilization system for RF cables.

Cal. Reference and LO to downconverters

The precise field detection in LLRF system requires high quality LO and calibrated reference signals at downconverter (10^{-4}, 0.01 degree). The local RF distribution box for the DWC's signals from fiber link featuring:

- RF and Clock distribution to DWC and Upconverter for all modules
- Drift compensation setup of DWCs
- Reference box for amplitude and phase linearization or using cavity decay
- Monitor quality of the field detection (RF distribution, drift, jitter, linearity)

must be designed and integrated with LLRF system.

Deliverables:

- Local RF distribution box for the DWC's signals from fiber link.

Clock synthesizer for LLRF ADCs

Integration with ultrastable timing and clock, event, (data ?)

Software Architecture and Implementation Strategies

The performance and functionality of the digital rf control system is largely dominated by the implemented software. For the LLRF system for the XFEL about 50% of the LLRF system cost will be invested in software. Most future upgrades will be made in software. It is therefore essential to define a software architecture which is modular and allow collaborator to contribute from their home institutes. In an early stage the distribution of algorithm should be specified to determine the necessary resources (FPGA, DSP, CPU).

Software architecture

Software development tools

Software documentation tools

Every big project needs to have standardized documentation management policy. It is especially important with projects, where particular parts of the system must closely cooperate with each

other. Unified documentation system allows for retrieving interesting information very fast and without necessity of communication with other persons or teams. The system should be easy accessible, easy searchable, should store history of changes and should be easy to use.
Various documentation management tools are available on the market. Most known are e.g. Doors, Rhapsody and there is also set of much simpler and usually free to use such as CVS or SVN. None of them is easy to integrate with other software tools and usage of them is usually quite complicated. They are universal systems, so in the same time they cannot be tuned to exact needs of unusual needs.
The idea of the research is to find documentation management strategy matching unusual needs of the proposed project and similar ones. After requirements gathering stage, the universal system structure will be proposed. The structure of the system will have to match complicated and universal addressing mechanisms related to documentation localization and complicated role/groups/privileges/authorization schema related to security/availability issues. The other research will have to be done on implementation technique and development type. There are a lot of possible programming platforms (PHP, Java EE, .NET, others) and a lot possible implementation solutions in the platforms. There is also a lot of other issues, which need to be solved: centralized versus distributed system, data persistence layer implementation (SQL based versus ORM techniques), programming interface development (if distributed: CORBA, WebServices, native one), view layer implementation (XHTML-based or AJAX).

Time schedule, deliverables and milestones

Task Name	Milestone	Main Deliverables	Months
WP 3.3			
Study and comparison between existing documentation tools		Report describing possible solutions	2
Requirements gathering		Report describing requirements	2
Universal architecture development		UML system structure	3
Database development	Database implementation		1
Programming interface methodology choice and development		API	2
Graphical user interface development		GUI	1
Tests development	Documentation system		1

Distribution of Algorithms (FPGA, DSP, CPU)

Software/hardware co-design

Communication protocols

The LLRF control system will be highly modular and therefore the inter-module communication will be crucial for machine operation. The communication protocols organize data transfer between elements of LLRF system like electronics components, chips, boards and crates. All protocols must be efficient – use all advantages of hardware implementation. Moreover, protocols must fulfil all required parameters for each tasks like transfer bandwidth, error correction, etc. Based on hardware equipment, software level of communication must provide easy establishment of the connection, transmission and closing the connection. Software level of communication protocols will include user tools for using and checking status of transmission.

Algorithm development

Diagnostics (HW & SW)

Build in diagnostic is required to provide online troubleshooting capability during regular machine operation. During maintenance periods the dedicated test signals extend range of the detection capability. Diagnostic features include hardware and software components for testing functionality and failure/degradation detection.

Deliverables:

Development of diagnostics for LLRF system with following features:

- online hardware performance monitoring
    - concept of the system, architecture, source of test signals, monitor performance of field detection, calibration, klystron drive change, timing, piezo drive, temperature, power consumption all electronic boards, modules, and crates.
- online software functionality monitoring
    - monitor quality of the field detection, signal integrity, quality of regulation
- internal and external interfaces checking
    - detect communication errors, including signal (analog& digital) connections, timing signals
- hardware characterization during maintenance day
    - Locate damage hardware (board, connection, power supplies), list of connected boards to selected board, system and subsystems linearity (down and up - converters, klystron), data base of electronics modules and interconnection between them.
- performance/failure statistics tracking
    - count defined events in the system, e.g. number of SEU, error rate in communication channels, hands-up, time with regulation with given stability

Precision RF Field Measurement

Achieving an rf field stability of the order of 2e-4 for amplitude and 0.01 deg. requires highly stable field detectors. Different approaches for low noise and low drift must be combined to achieve the required short and long term stability. Precision detection of single bunch induced transients is necessary to determine the beam phase without risk of vacuum loss and beamline activation.

Low noise, low drift downconverter (field detector)

Low cost, low real estate, multi-channel downconverter (ASIC)

The multichannel low hamonics synchronous downconverter from 1.3 GHz to the intermediate frequency in range 1-250 MHz will be designed and the prototypes manufactured. The downconverter will be designed using one of the technologies available via Europractice (feature size 0.35 um or less). Before delivering the final designs, at least two test chips containing components of the final chip are to be fabricated and measured.

Deliverables:
Design report of test chip 1: 6 months
Fabricated test chip 1: 9 months
Measurements report of test chip 1: 12 months

Design report of test chip 2: 15 months
Fabricated chips after test chip 2: 18 months
Measurements report of test chip 2: 21 months

Design report of final project: 24 months
Fabricated chips (final): 27 months
Final report: 30 months

Transient detection (low cost multichannel)

There is a need to precisely calibrate the RF field in respect to the beam in order to optimize the machine operation and achieve safe and stable operating conditions. This is particularly important during machine commissioning and startup. The calibration idea is based on beam induced transients measurements in respect to the beam. During last few years the single bunch induced transient detection system was build and operated, however the system costs are high and its precision is limited due to the fact, that beam excites not only the base mode oscillations but also other pass-band and higher order modes. The limitations of the transient detection system must be overcome to obtain the accuracy of few percent in amplitude and few degrees in phase. Also the cost of the transient detection system must be reduced in order to enable its installation in all accelerating module.

Deliverables:
Industrial version of the single bunch transient detection system with improved accuracy. Integration of the single bunch transient detection system into current control system.

Other control systems

RF Gun temperature stabilization

The RF Gun operation depends strongly on gun temperature. Therefore precise temperature stabilization for the gun is needed.

Deliverables:

- Gun temperature stabilization system

WGT control system

The RF power is distributed to the accelerating cavities through the waveguides. The RF signal phase in the cavity is regulated by motorized waveguide tuners (WGT). For automated tuning the control system for WGT must be developed.

Deliverables:

- WGT control system

Commissioning and Operation Procedures

The knowledge of commissioning and operation procedures is necessary to develop the required applications. These are used to automate the operational procedures. A cavity simulator is required for the development of the llrf electronics and to allow only debugging of hardware and software.

Commissioning and Operation Procedures

Modern large accelerators projects like ILC or XFEL make use of a highly collaborative approach which involves people from many countries operating the accelerator. As not all of them must be experts for machine operation it is important to equip them into clear and compact description how they should proceed to achieve desired accelerator operation state. It is necessary to develop procedures like e.g. "Self Tests", "Turn on RF", "Signal Calibration", "Tune Cavities", "Establish Accelerating Field", "Turn on Beam", "Establish Correct Beam Phase" and many others. The worked out procedures will be also used in the automation engines that will make use of experts knowledge embedded in the procedures. High degree of automation is necessary to relieve the operators from complex but well understood tasks, in particular when the large number of RF stations must be operated (as it is in case of XFEL and ILC). Set of procedures will be developed and described for various types of machine operation; maintenance and service.

Deliverables:

- **Operation procedures**
  The operation procedures covers collection and description of any action performed during the machine operation. That includes procedures changing the machine state when the experiment condition changes (beam / no beam, different gradient or beam parameters settings, etc.) or temporary access activity or starting up the system work after shut-down.
- **Maintenance procedures**
  They organize the maintenance work for the LLRF subsystems. These procedures will contain description of steps needed for running of the system diagnostic and regular maintenance activities performance. There will be different routine procedures defined by the subsystems experts that will have to be executed in order to check and maintain high level of the system performance.
- **Service and exception handling procedures**
  An operator of RF station has to observe various different parameters in order to recognize current system status. When the machine behaviour differs from expected one the experts knowledge is needed. Basing on aforementioned information operator is able to react in well defined way to the known system failures and glitches. Well documented procedures will provide this ability to new users and can be implemented in automated exception handling.

Automation of Operation

This work package aims at providing the software for automation of the LLRF system. Its functionality will encompass automation of routine operation procedures like startup, shutdown, calibration and auto-recovery from recoverable operation glitches. Previous attempts to solve the problem were directed towards design of FSM statecharts describing the automation process. Unfortunately existing designs are still not up to the challenge.

To make the implementation more efficient and dependable one proposes to employ and extend tools and methods which were proposed for automation of the RF-power station for the FLASH. At present there are guidelines and tools supporting software specification, implementation and formal verification. They proved to work in practice, but they are still not flawless. Effectiveness of crucial planning algorithms must be improved. Moreover full integration with the distributed control system DOOCS has not been yet accomplished. There is still no remote GUIs for automation software supervision from operator's dashboards.

To complete the whole design process a method for deriving the specification from the experts practice is needed. We want to elaborate complete step-by-step guide of preparing the specification for automation of LLRF subsystem (or any other accelerator subsystem), which can then be used for implementation, testing and verification.

Set of auxiliary applications for common system operators actions is also required. There are different operation, maintenance and commissioning procedures which require coordination of various system parameters. This can be automated in order to facilitate the system operator's work.

One of the control application that also requires management this auxiliary is linearisation tool for high power amplifiers in RF stations. This tool have been developed and tested during the CARE activities. Main activities was focused on the klystron and its pre-amplifier characteristics measurement and linearisation – to decrease dependency between power level and loop gain and loop phase. This will provide overall device availability increase.

Tool functionality extension by the adaptation to varying system conditions is needed. Additionally optimal cooperation of the tool with the cavity field feedback controller have to be developed (in order to achieve low FPGA resources consumption and minimize computation time by using PowerPC and DSP for placement of the algorithms). Other challenge is development of the HPC diagnostic setup for more precise field detection. Signal detection hardware modification for signal levels adjustment, noise suppression.

Eventually the evaluation of the tool in the FLASH accelerator and Module Test Stand is planned. Aforementioned tests will help in making a decision about optimal implementation in all FLASH modules and MTS.

Deliverables:

● Step-by-step methodology for automation specification and design

● Improvements of software design framework elaborated for RF-power stations automation

● Installation of the automation software for the LLRF system

- HPC linearization tool automation
- Linearization tool implementation in the LLRF controller and other hardware layer
- Evaluation and installation of the tool in the MTS and FLASH RF stations.

4.3.1 Requirements analysis and prototyping

4.3.1.1 Preparation of main use-cases

4.3.1.2 Preparation of the activity diagrams describing each use-case.

4.3.1.3 Preparation of the scripts

4.3.1.4 Revision 1 – scripts revision

4.3.1.5 Modeling the state-based behavior of the operator

4.3.1.6 Revision 2 - automation model revision

4.3.2 Implementation of automation for the LLRF system

4.3.2.1 Preparation of the specification for the planner

4.3.2.2 Preparation of the specification for the exception handler

4.3.2.3 Formal verification of completeness and safety properties.

4.3.2.4 Operator assisted evaluation of the software.

4.3.2.5 Revision 3 – Implementation revision

4.3.3 Development of global LLRF supervisor

4.3.3.1 Preparation of chief use-cases

4.3.3.2 Preparation and revision of the scripts

4.3.3.3 Modelling the state-based behaviour of global supervisor

4.3.3.4 Implementation

4.3.3.5 Implementation revision and testing

4.3.4 Design framework improvements

4.3.4.1 Integration of general automation with current control system infrastructure (DOOCS)

4.3.4.2 Performance optimization

4.3.4.3 Testing and formal verification support

Cavity simulator including rf front end

Interfacing to other accelerator subsystems

In accelerator design the interfaces between various subsystems are crucial for successful operation but are usually not specified very well. It is therefore necessary to study the requirements and implementation for these interfaces in great detail.
Interlocks
Monitors
Controls

Fast Frequency tuner

Piezo driver
Increased stroke
Segmented fusing of piezostacks
Microphonics control

Fast frequency tuners are necessary for Lorentz force compensation. Their potential for control of microphonics and the possibility of using time varying detuning to increase the acceptable gradient spread require further investigation.
The piezoelectric tuners demonstrate the ability to compensate the Lorentz Force for field gradients up to 35 MV/m. The driver used for this purpose suffers from the over-heating. Moreover, there is a pressure to combine 8 drivers in one board to minimize the cost of the system. As a result there is need to redesign the current driver used for piezostacks. Additionally, the active elements are mounted inside the cryomodule and they cannot be exchanged in case of failure. We aim to develop a segmented piezostack with dedicated fuses for each section. Then, in case of breakdown of one segment the others will work properly. This WP will also cover the further investigation dedicated to microphonics compensation. Advance correction of the phase and the amplitude during the RF pulse will decrease the additional RF power needed for field control. At least but not least, the further development of techniques used for Lorentz force will

be performed. These include stroke improvements, new elements characterization, investigation of mechanical cross-talk between the nearest cavities, wiring improvement.

Deliverables: 1) new driver for piezoelements
2) fuse set for piezostack protection
Milestones: 1) report about the microphonics compensation
2) report about the cross-talk of the fast tuners

Beam feedbacks

Beam based feedbacks are necessary to correct long term drift of rf amplitude and phase in rf gun, injector and main linac. The concepts for the beam based feedback must be developed and prototype implementations evaluated at the 'FLASH'.

Beam diagnostics and monitors

Beam feedbacks