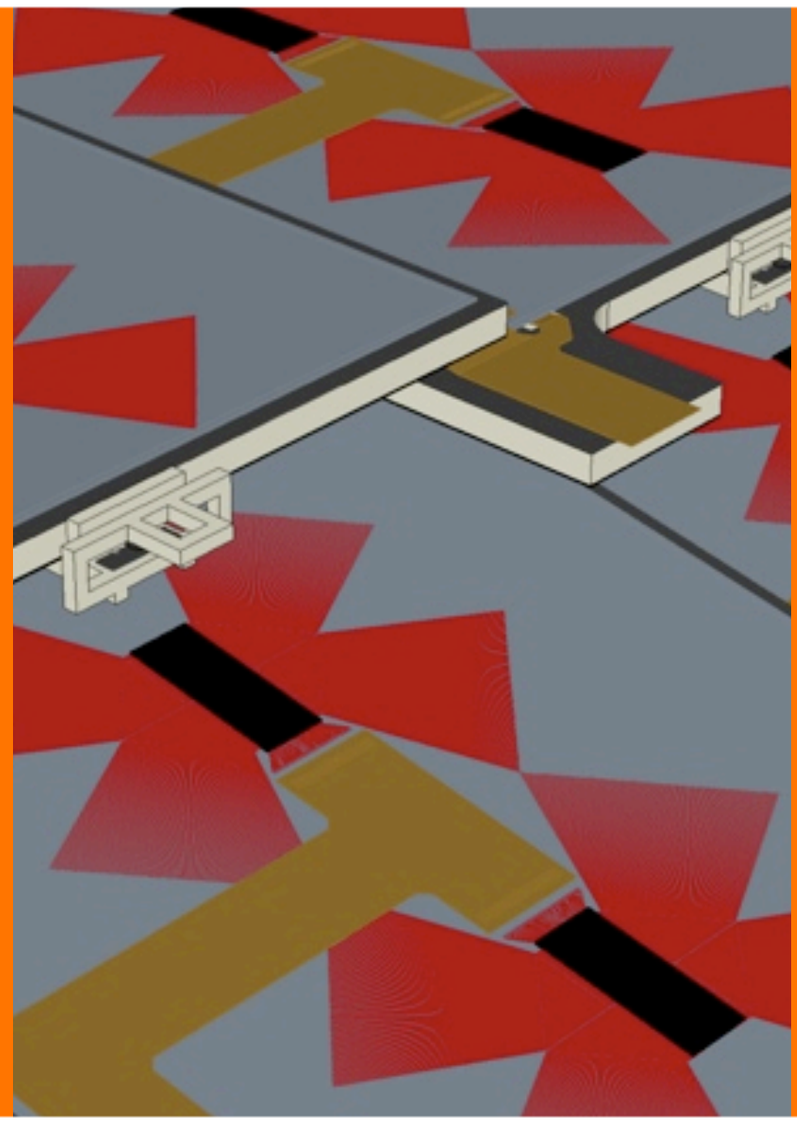


ILC Silicon Tracking R&D

Tim Nelson - SLAC

Review of the US Program of Detector R&D for the ILC

Argonne National Laboratory - June 19, 2007

R&D Summary

- US R&D revolves around development of SiD concept
  - Also applicable to silicon layers in other concepts
  - Stringent demands of SiD all-silicon tracking inspire most aggressive R&D
- Most effort funded through labs and LCDRD
- Labs play a central role
- High degree of cooperation among groups
- Cooperation with vertex R&D groups here and in Europe and with SiD ECal group

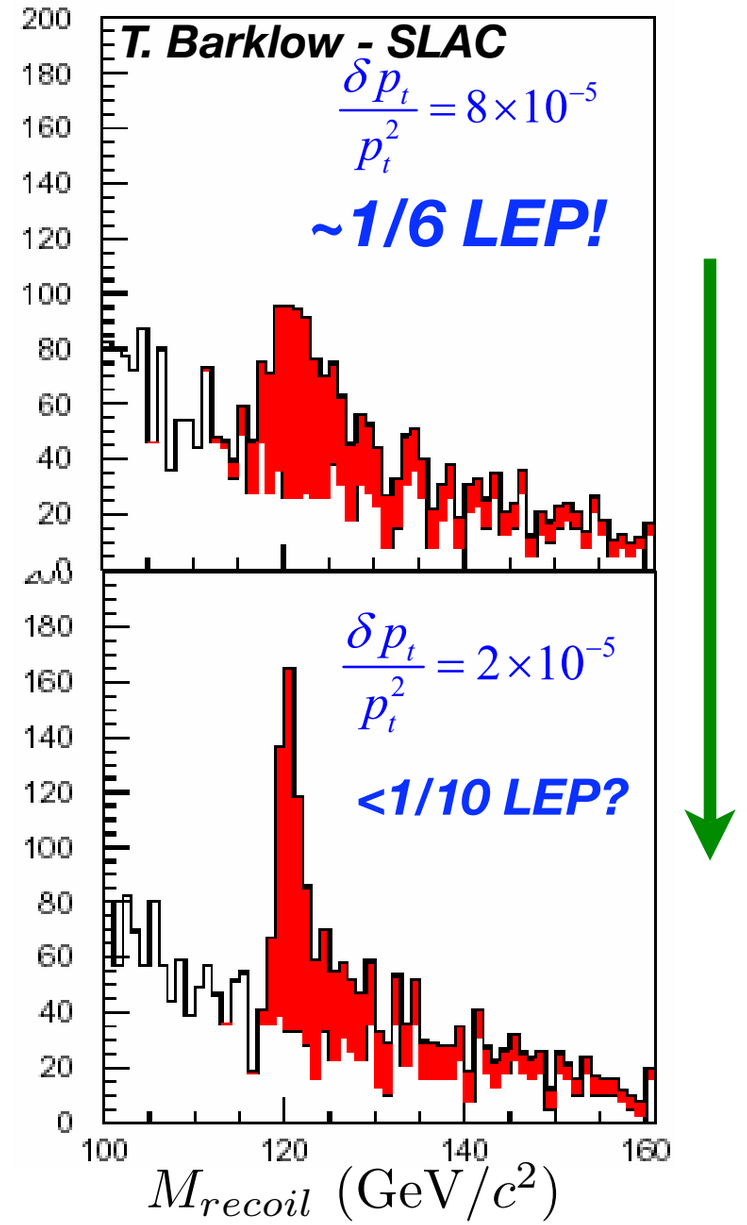
ILC Silicon Tracking R&D in the US

System	Work Package	Institutions
Mechanical	Support Design	FNAL, SLAC, Washington
	Module Design	FNAL, SLAC
	FSI Alignment	Michigan
Sensor	Double Metal Sensor	FNAL, SLAC
	Thin Silicon	Purdue
	Characterization and testing	New Mexico, SLAC
Readout	KPiX	BNL, Davis, Oregon, SLAC
	Long Shaping Time Front End	Santa Cruz
	Charge Division	Brown, Santa Cruz
Cables	KPiX Cable	New Mexico, SLAC
Simulation and Reconstruction (see N. Graf's presentation)	Simulation Infrastructure	Oregon, SLAC
	Vertex Seeded Tracking	Brown, Colorado, FNAL, Oregon, Santa Cruz
	Standalone tracking	FNAL, Santa Cruz, SLAC
	Calorimeter Assisted tracking	Kansas State
	Fitting and Resolution	Oregon, Santa Cruz, SLAC

Why Silicon?

- Allows emphasis on phi resolution:
  - superior asymptotic P_T resolution for given B-field and Δr
  - a prime ILC example:

$$e^+e^- \to Z^0 H^0 \to \mu^+\mu^- + X$$
$$\text{Given } \sqrt{s}, M_Z, M_{\mu\mu} \Longrightarrow M_H$$



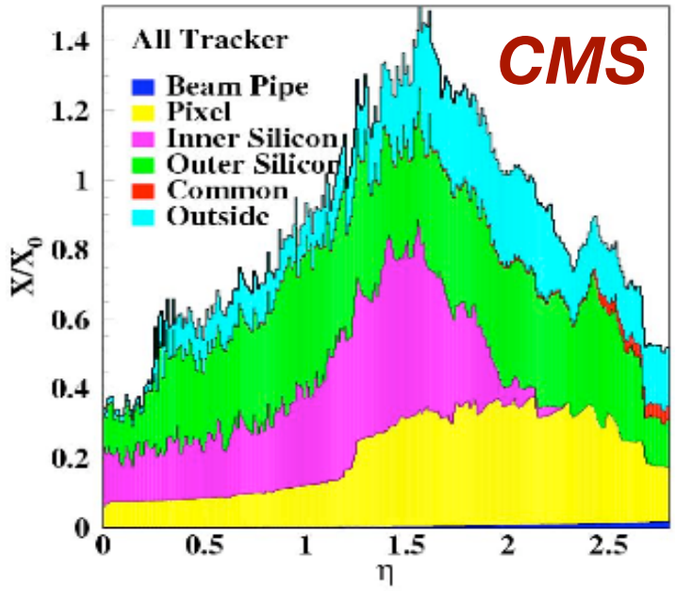
- Fast response allows single-bunch timing:
  - number of voxels/bunch train similar to TPC
- Sensors required are technologically mature
- Robust against aging and beam accidents

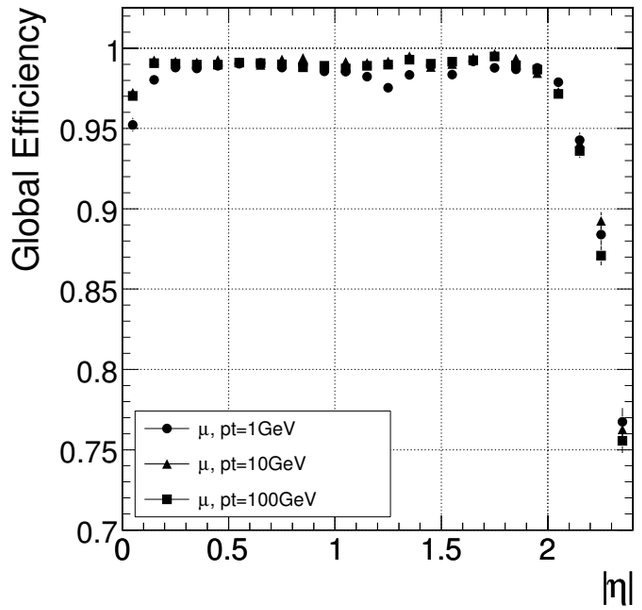
Key R&D Drivers

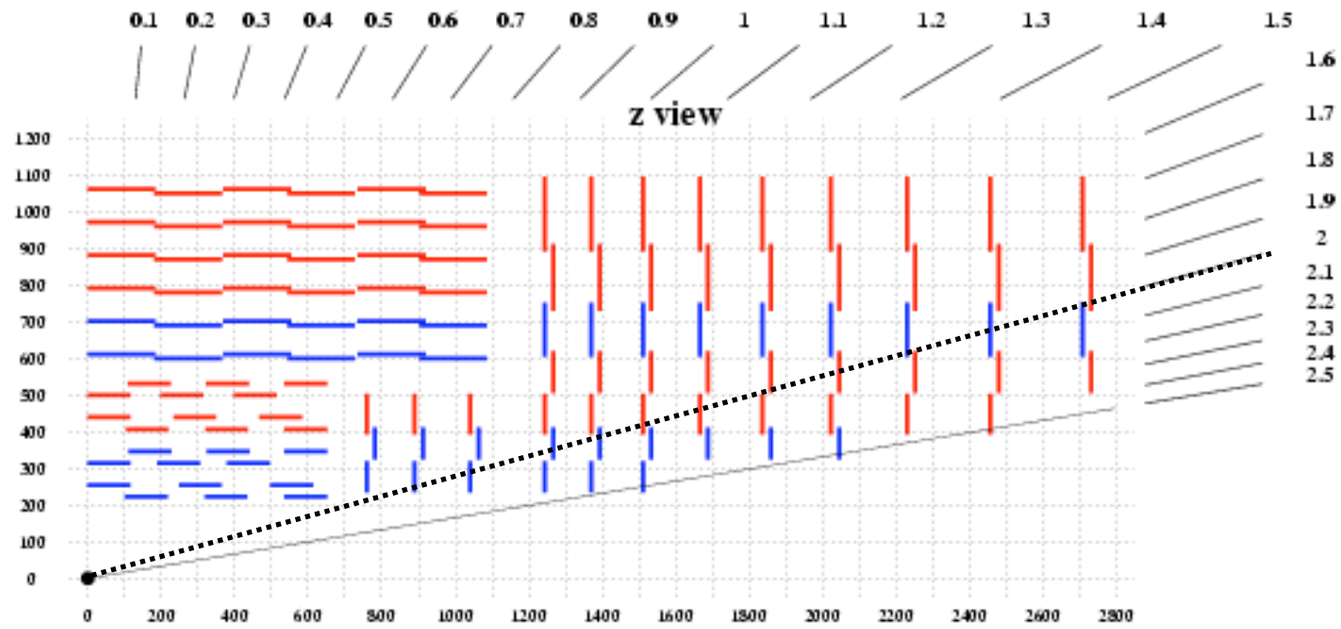
So, where is the R&D challenge?

- Large silicon trackers (ATLAS, CMS) have been too massive
- Excellent forward tracking has eluded previous efforts

These are the key issues to be resolved by the R&D program

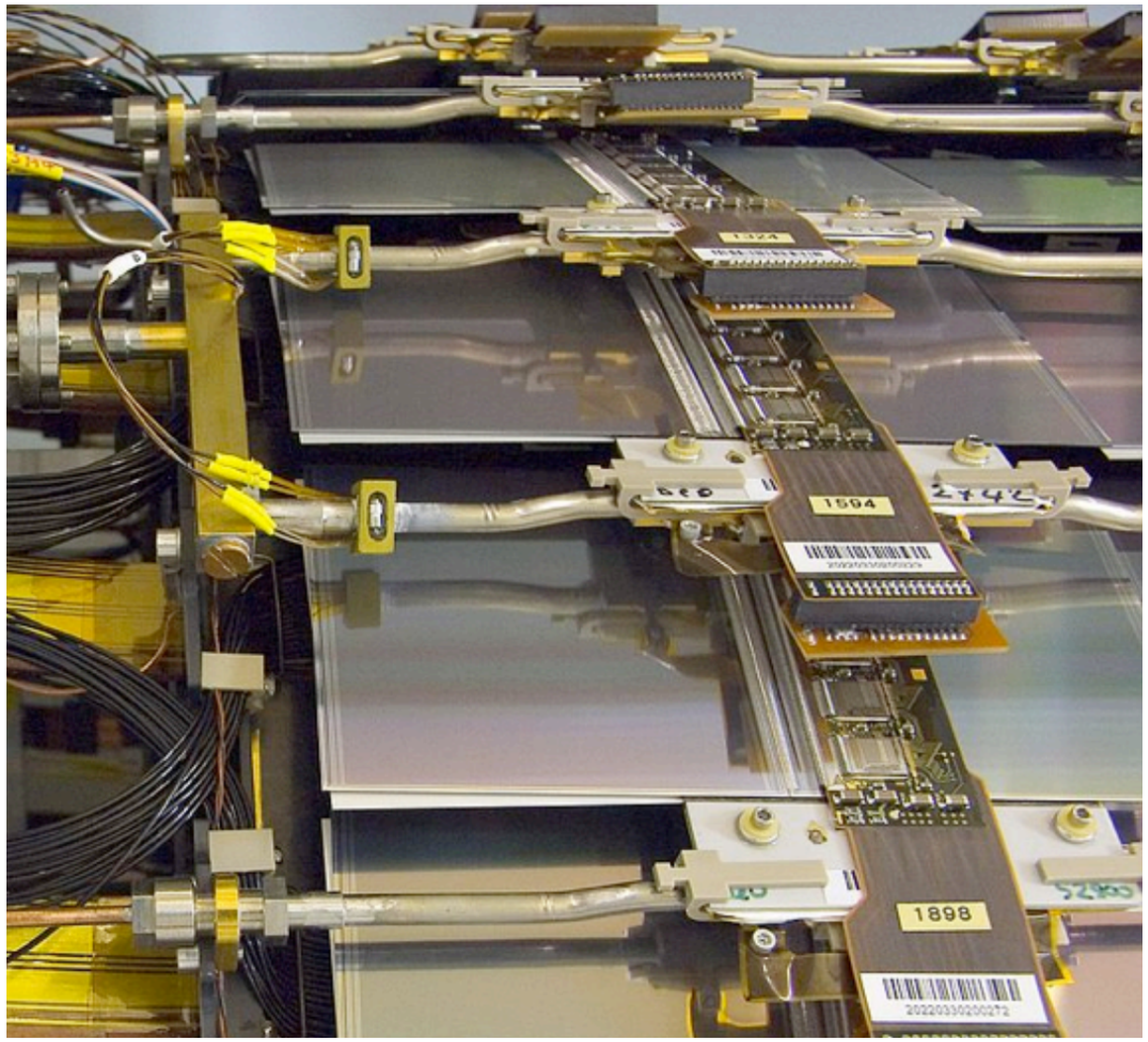






Reducing Material

- Cooling: eliminate
- Readout: reduce
  - Chips
  - Hybrids
  - Cables
- Support: minimize
- Sensor: thin?
- avoid extra unnecessary redundancy



Eliminate Liquid Cooling

- Pulsed operation of front end results in ~100X reduction in dissipated power
- Designs under consideration can be gas cooled

Pulsed power is a common element of all readout chip efforts, in particular:

- Long Shaping Time Front End (LSTFE) - *SCIPP/UCSC*
- KPiX - *SLAC, Oregon(ECal)*

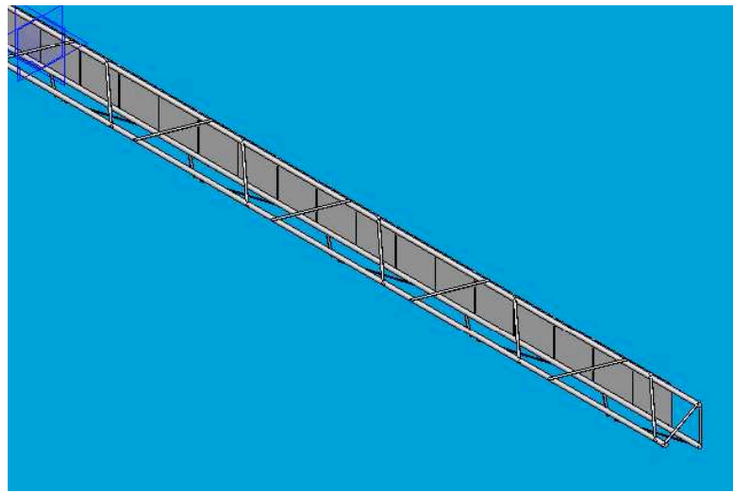
These efforts differ primarily in approach to reducing readout material

LSTFE

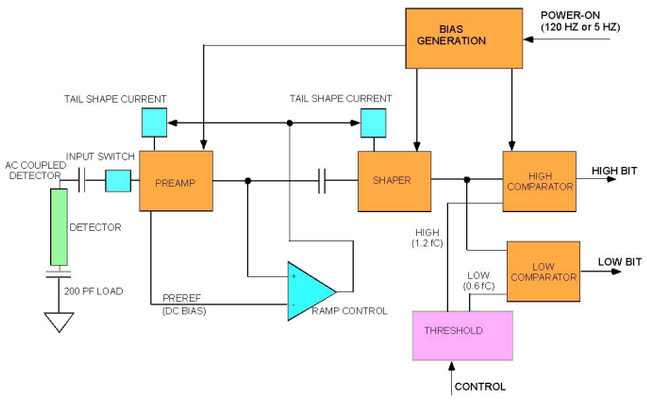
SCIPP/UCSC

Simple approach to reduction of readout material

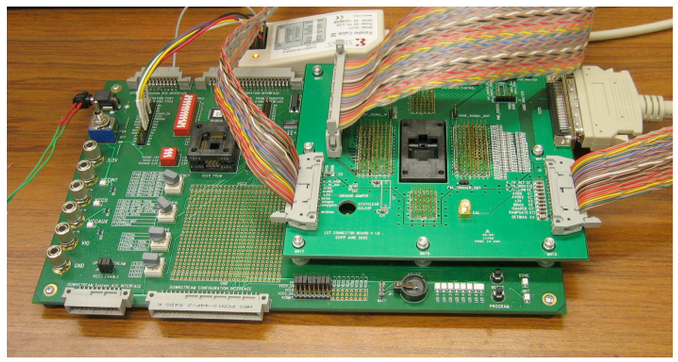
- design tracker with very long strips
- ultimate goal: ladders 1/2 length of SiD barrels (up to 1.7m)
- Simulation developed at UCSC indicates a feasible operating point for readout
- Requires a carefully designed front end optimized for low noise in this regime

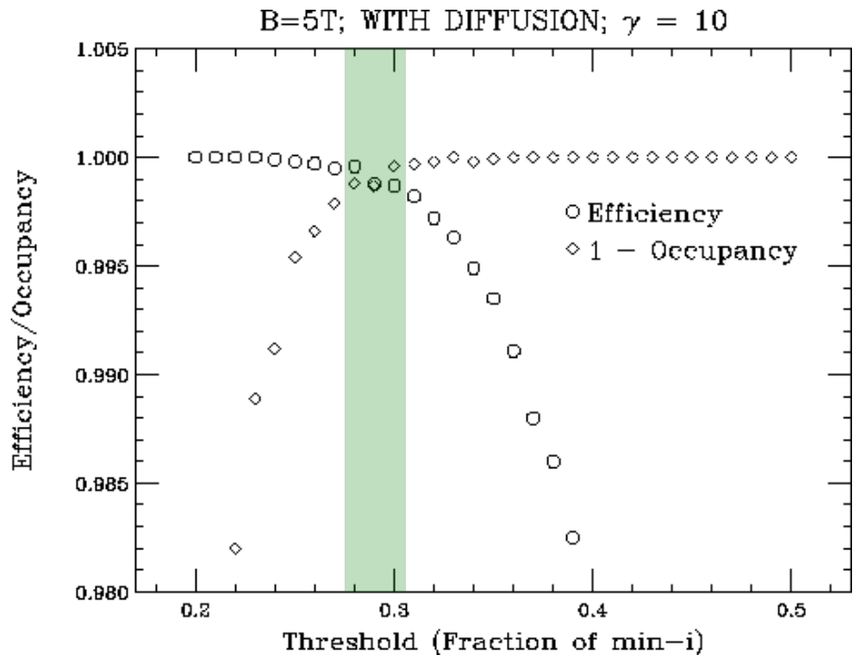


LSTFE



FPGA-based digital section

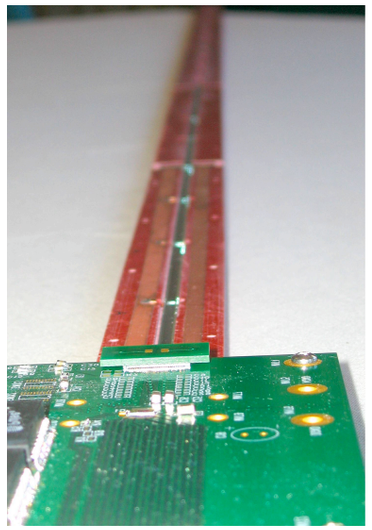


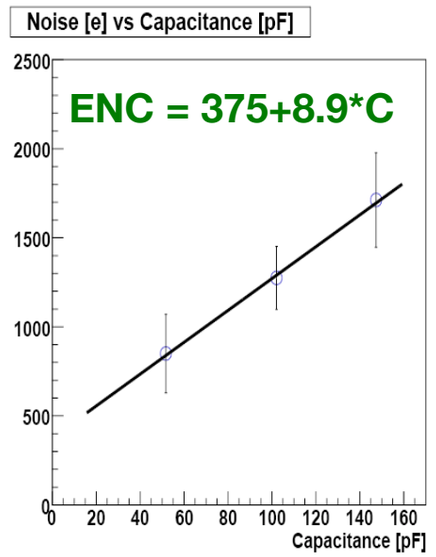


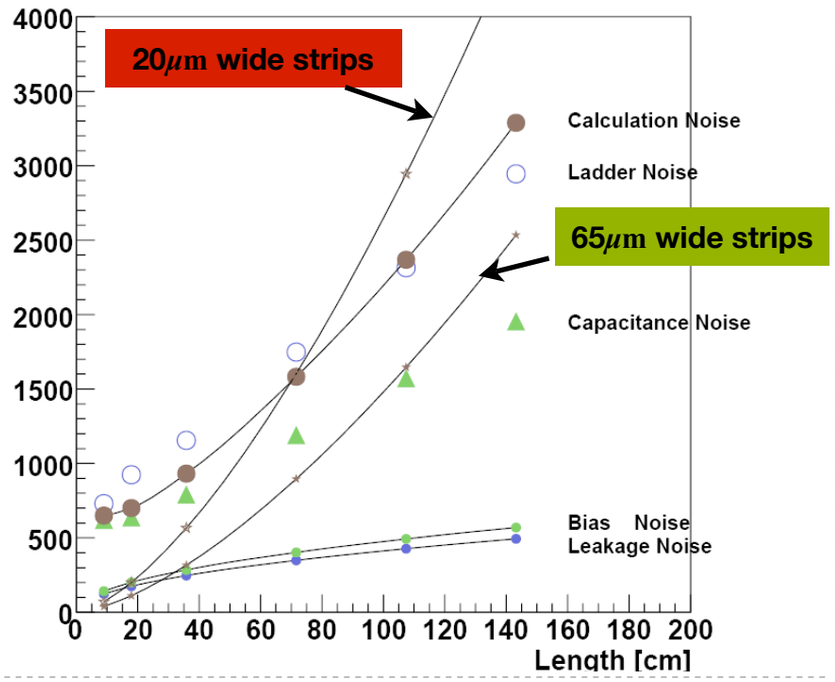
LSTFE

SCIPP/UCSC

- Testing with long strips of GLAST sensors encouraging: noise performance of front end is excellent.
- Challenges remain for ultra-long ladders
  - series resistance of long strips at finer pitches required may be problematic for longest ladders
  - manufacturing/handling/installation is difficult
  - stereo ladders in barrel difficult to accommodate
- Re-optimize chip for strips ~10-80cm in length
- Continue development of digital logic





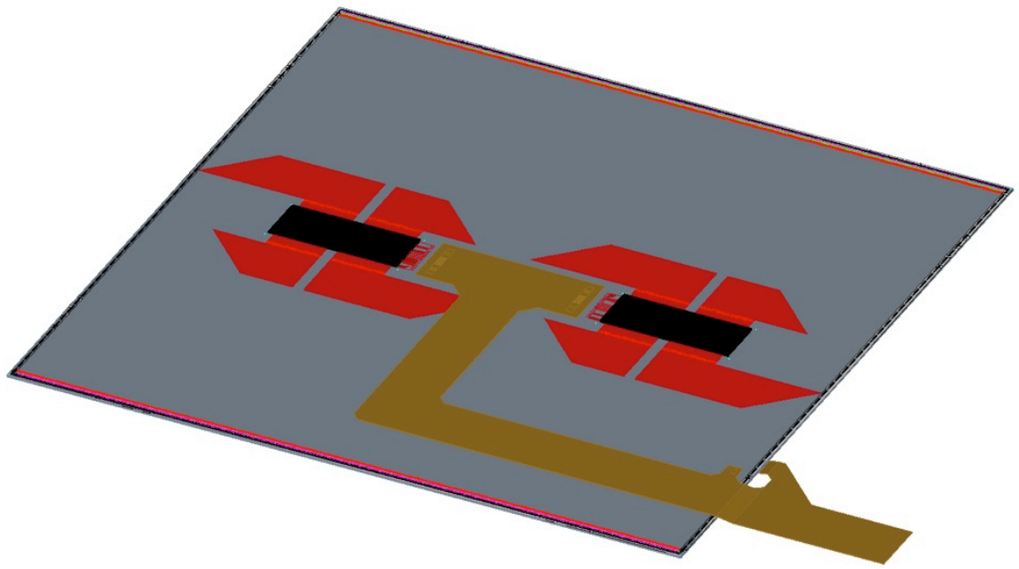


KPiX

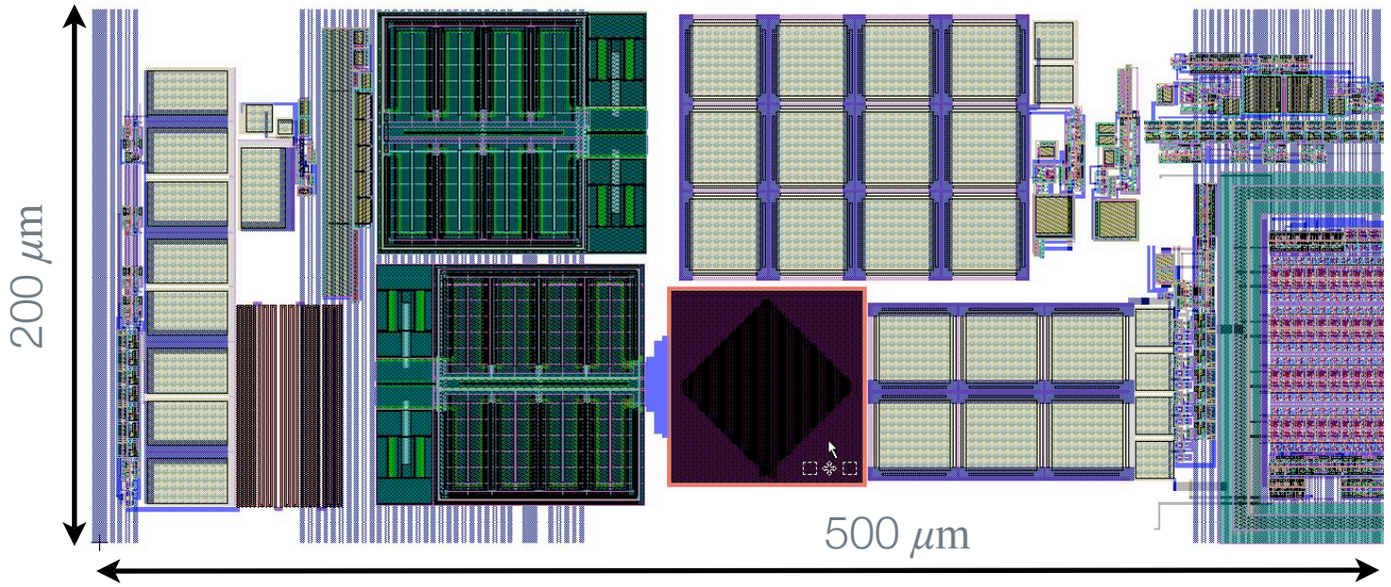
BNL, UC Davis, SLAC, Oregon

More radical approach to reduction of readout material

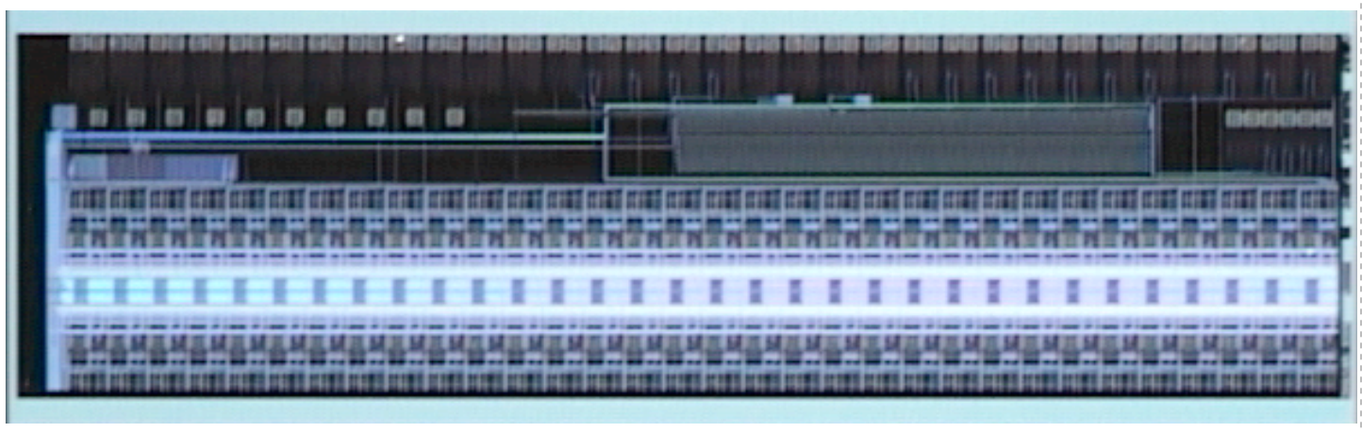
- Store readout in 4 analog buffers, digitize and read out chip between bunch trains
- complete elimination of hybrid circuit board
- chip is bump-bonded directly to sensor: read out each sensor individually through double metal traces and low-mass cable



a single cell of KPiX



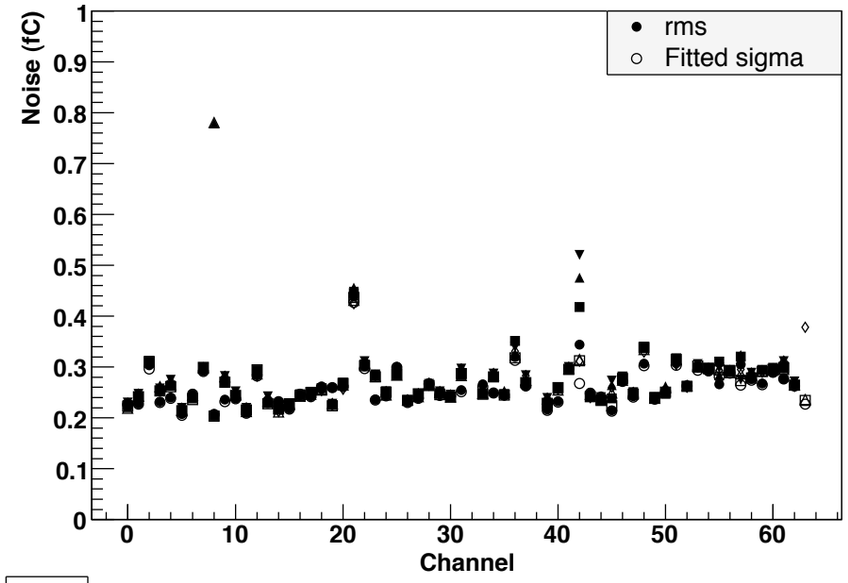
KPiX64

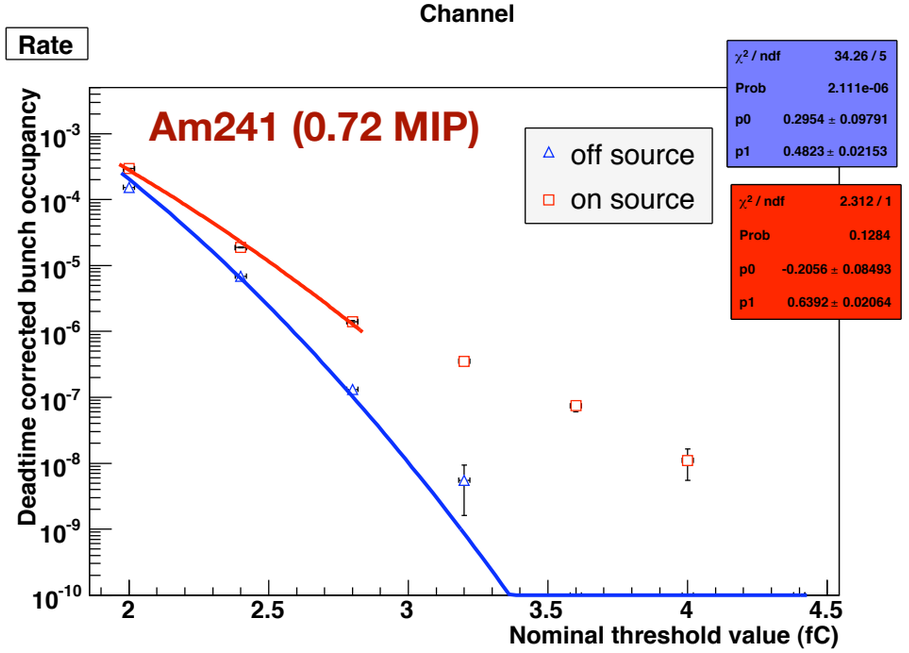


KPiX

BNL, UC Davis, SLAC, Oregon

- 64-channel prototype, KPiX64-4 has undergone extensive testing
  - All major features working, some operational quirks remain
  - Current noise measurement: 1100+30*C, expectation is 300+30*C
  - Source testing with Layer 00 sensor producing encouraging results
- KPiX64-5 just submitted, includes several significant enhancements
- Key is proof of bump-bonded readout concept



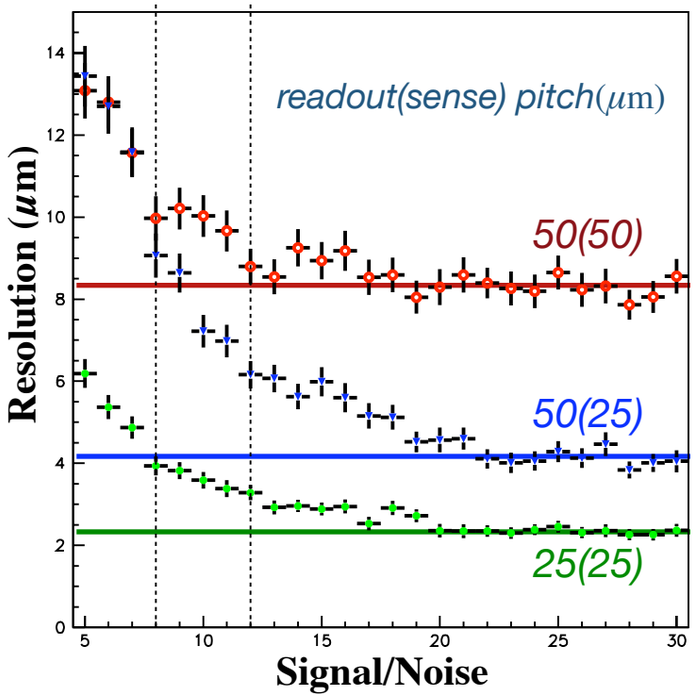


Sensor Prototype

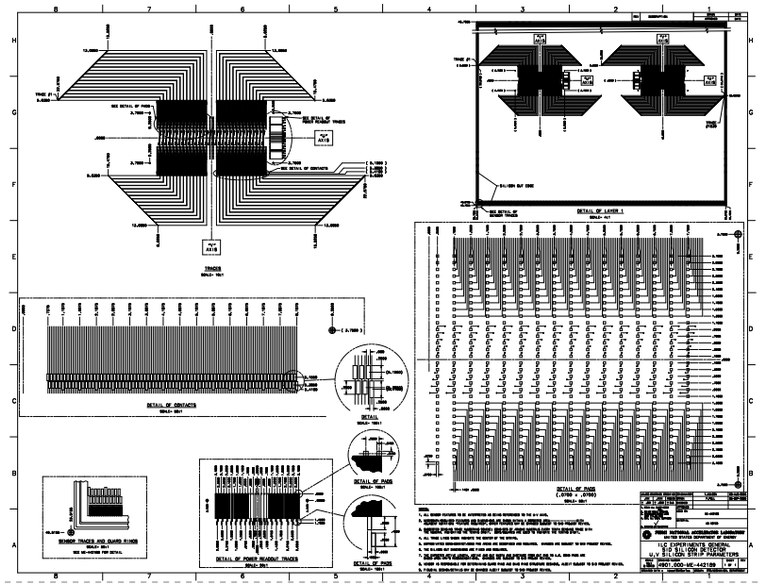
FNAL, SLAC

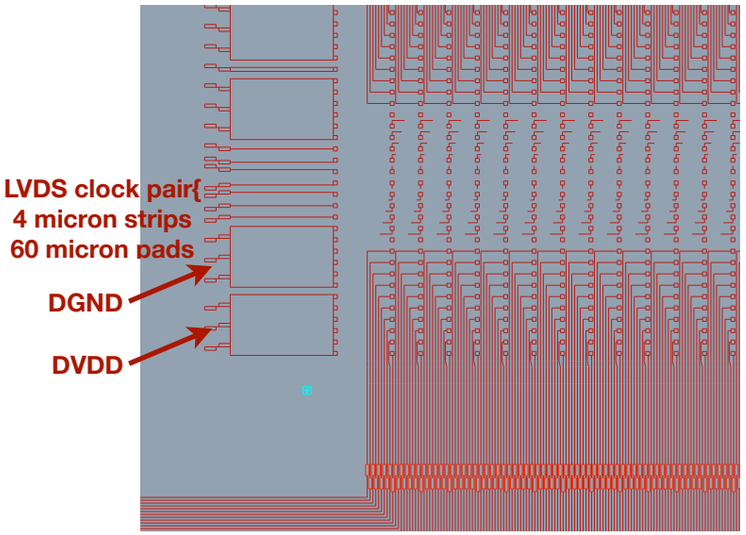
Prototype double-metal sensors submitted to HPK

- Should achieve <5 micron resolution for short modules
- Configured for both bump-bonding and wirebonding
- Can be daisy-chained to read out longer modules
- Refinement through independent review of design and specifications, extensive FEA capacitance calculations



Parameter	Specification
Wafer size	6-inch
Active area	92.031 mm X 92.031 mm
Number of readout (sense) strips	1840 (3679)
Depletion voltage	<100V
Junction breakdown	>200V
Leakage current	< 4μA at 150V
Strip width	8-9 μm
Coupling capacitance	>10pF/cm
Interstrip capacitance	<1.2pF/cm
Polysilicon bias resistor value	20-40 MΩ
Not working strips	<20 readout strips / sensor



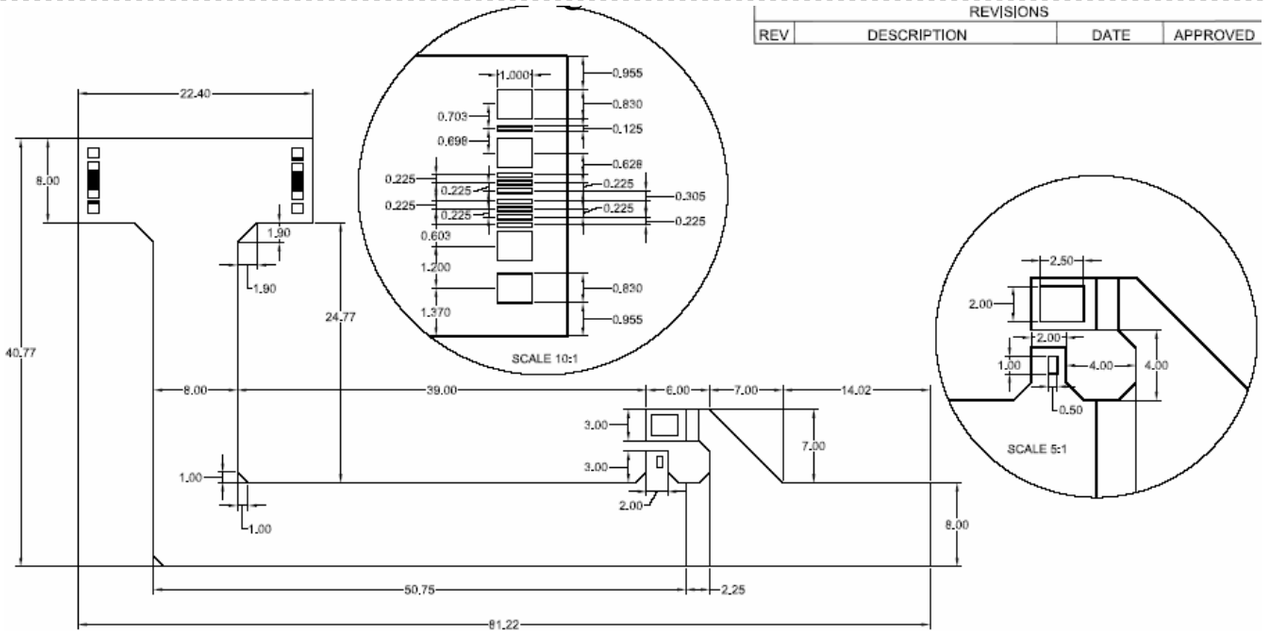


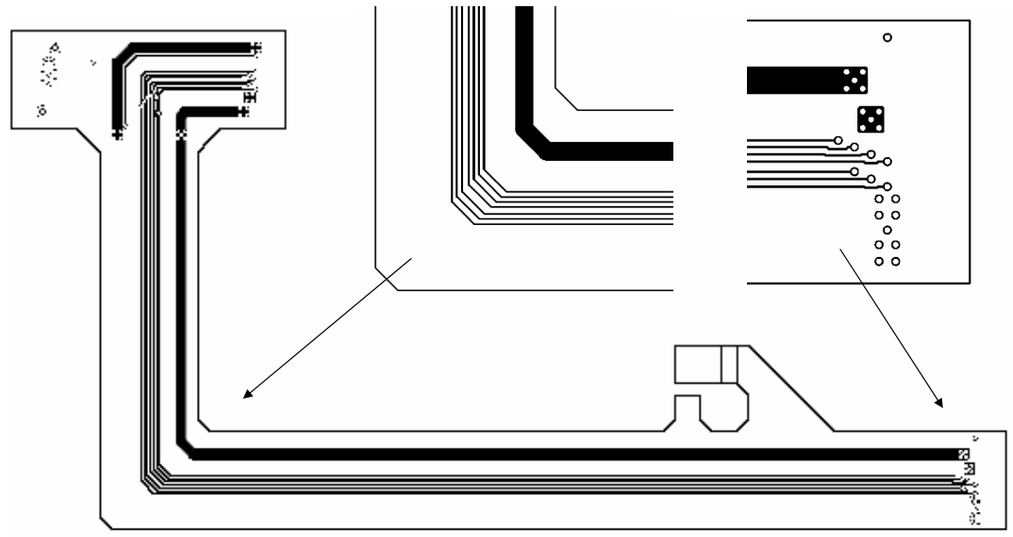
Cable Prototype

UNM, SLAC

Layout for prototype cable produced from basic SLAC mechanical design

- ¼-ounce copper on 50μm Kapton
  - 2 power+ground pairs <0.5Ω/trace
  - 8 narrow control/readout lines
  - HV pair for sensor bias
  - ➡ cable width ~1cm
- Working cable could be delivered on same timescale as prototype sensors





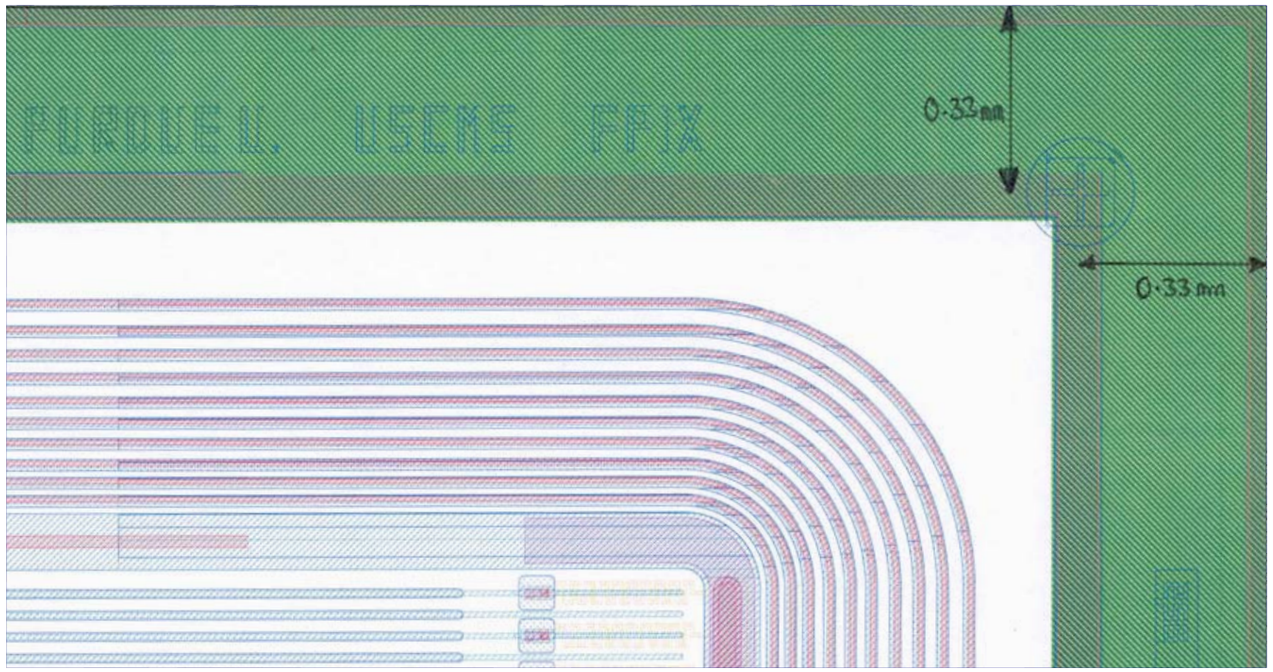
Thinned Sensors

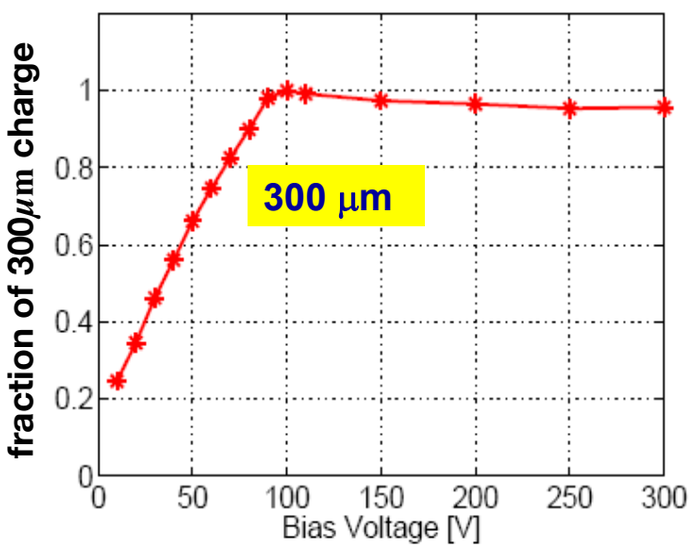
Purdue

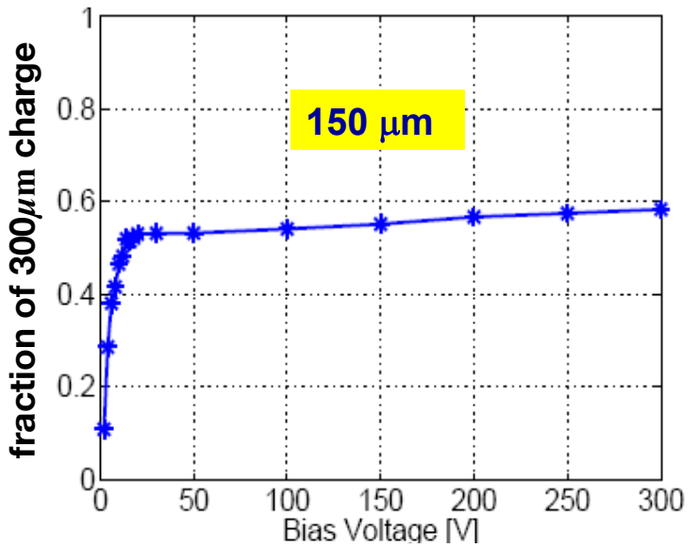
Prototyping sensors on thinned silicon

- CDF Layer 00 mask design
- 150, 200, 300 μm thickness
- Only yield issue occasional breakage of entire wafer
- Bias voltage, charge collection, etc. as expected
- Tested successfully with SVX4 readout: *KPiX* next

For short modules, 200 micron silicon will not compromise resolution



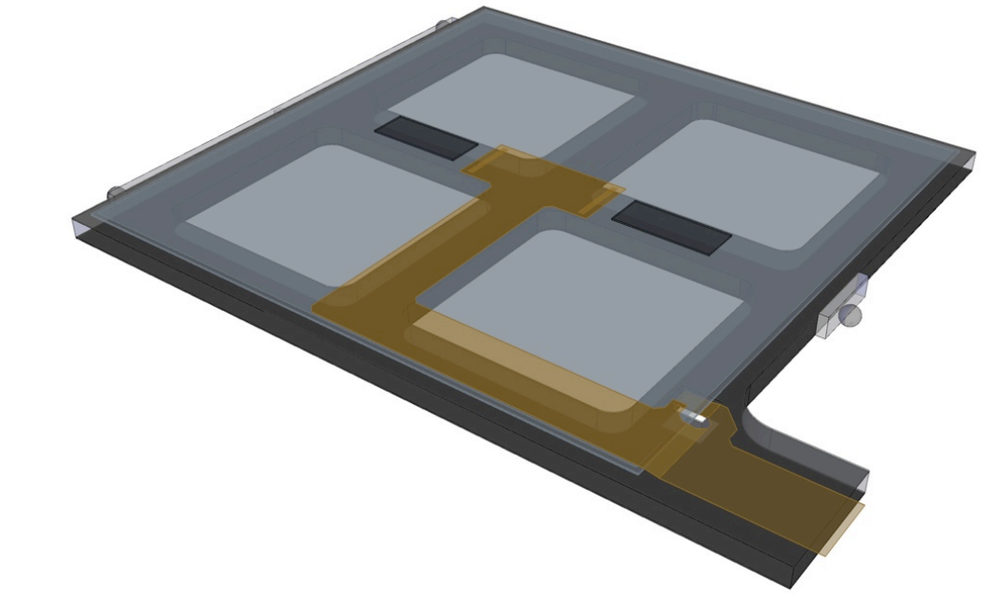


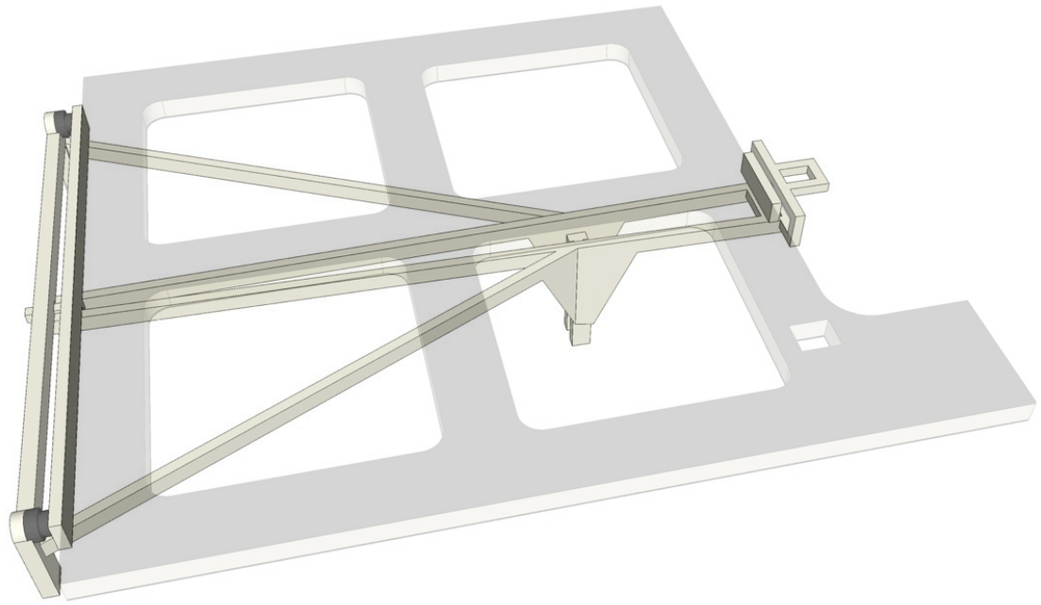


SiD Module Design

FNAL, SLAC

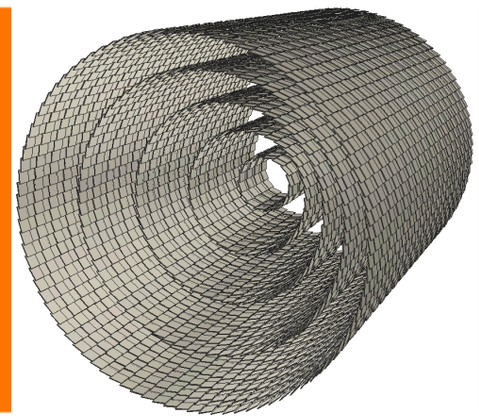
- Support frame is minimal: holds silicon flat and provides precision mount
  - CF-Rohacell frame
  - CF-filled injection-molded Torlon
  - Si_3N_4 mating parts
- Molded mounting clips glue to large-scale supports
- Designed for ease of assembly, handling, installation and replacement
- Can be made double-sided with addition of same silicon on other side
- Plan rapid prototyped supports and mounting clips to test concept, first test beam
- Full prototypes needed for large-scale mockup





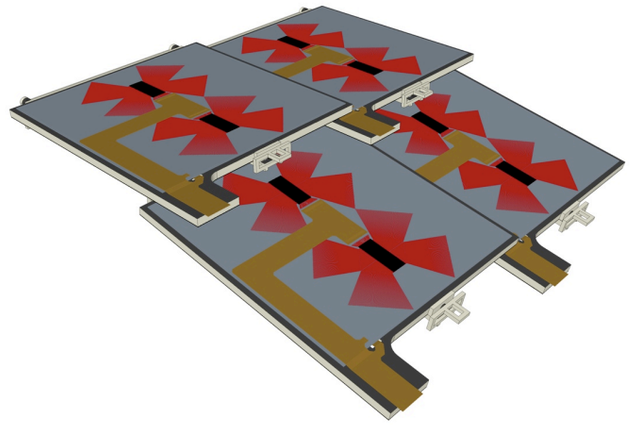
*Si*D Tracker Design

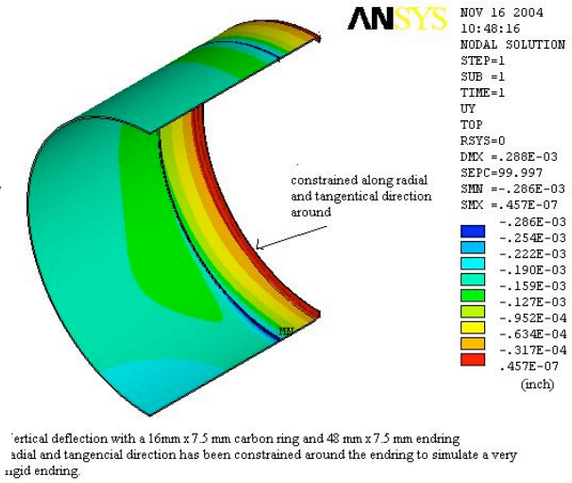
FNAL, SLAC

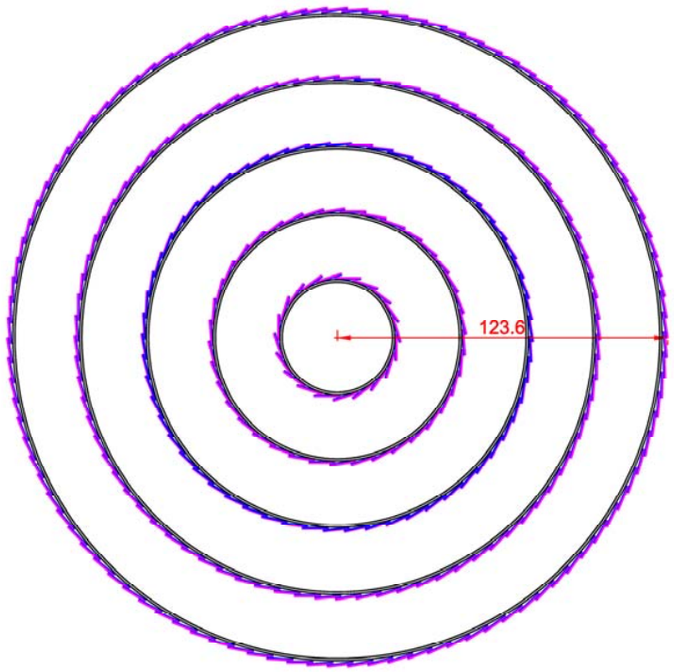


Barrel modules tile CF-Rohacell cylinders

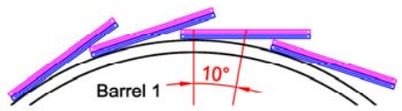
- Module tilt corrects for Lorentz drift
- Similar cylinders fabricated for D0, ATLAS
  - FEA results: 7um deflection fully loaded
  - 0.3% X_0 for solid cylinders: could be made up to 50% void
- More engineering and, ultimately, full scale prototypes will be required

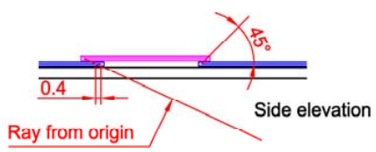






Sensors:
Cut dim's: 9.35 cm x 9.35 cm
Active dim's: 9.20 cm x 9.20 cm
Modules:
Outer dim's: 9.65 cm x 9.65 cm x 0.3 cm
Support cylinders:
OR: 21.5, 46.5, 71.5, 96.5, 121.5 cm
Number of phis: 20, 38, 58, 80, 102
Tilt angles: 6.6 to 10 degrees
Radii normal to silicon (mm):
Barrel 1: 2.175, 2.215 cm
Barrel 2: 4.675, 4.715 cm
Barrel 3: 7.175, 7.215 cm
Barrel 4: 9.675, 9.715 cm
Barrel 5: 12.175, 12.215 cm
Blue and magenta sensors are at different Z's to provide longitudinal overlap.
Within a given barrel, cyan sensors overlap in phi, as do magenta sensors.

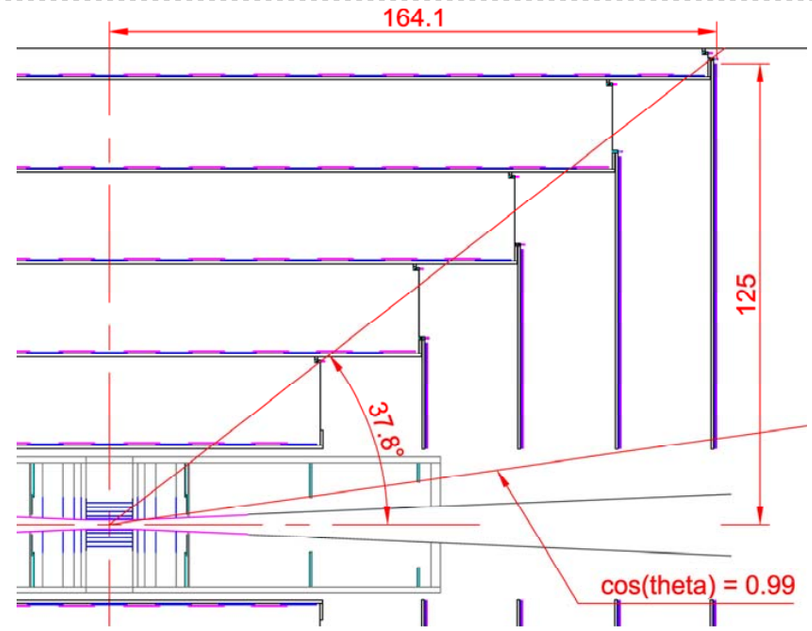


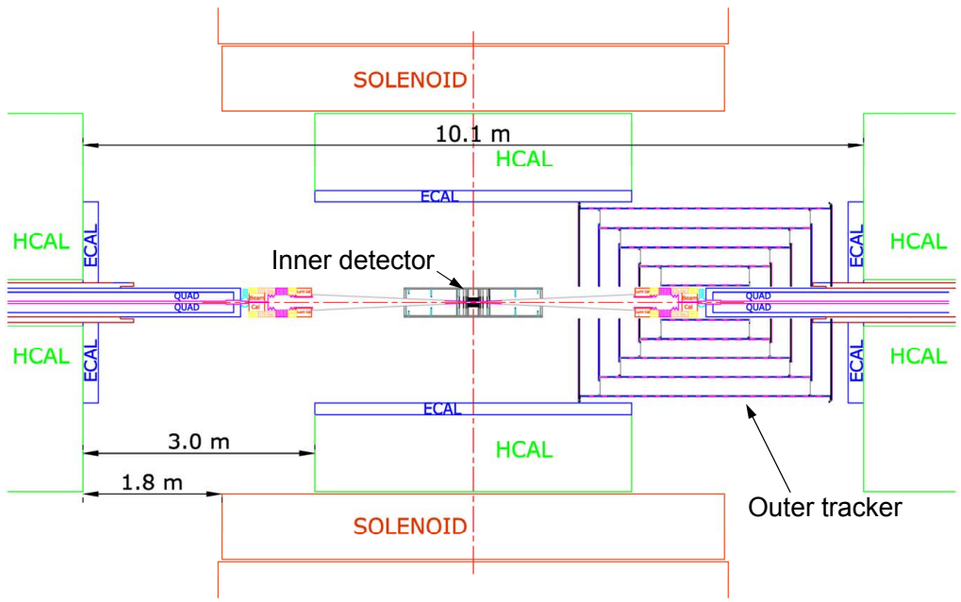


*Si*D Tracker Design

FNAL, SLAC

- Nested cylinders supported by annular rings that also host power distribution and data concentrators
  - Existing optical transceivers can easily meet our requirements
  - DC/DC conversion or serial powering assumed to reduce cable plant
- Cylinders closed with CF-Rohacell forward disks of similar fabrication: tiled with similar modules of as-yet undetermined shape
- Inner portion of disks supported with VTX to allow servicing





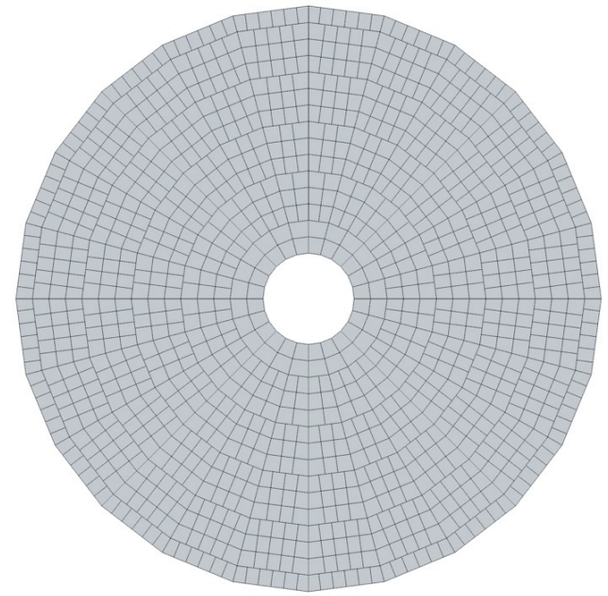
Outstanding Questions

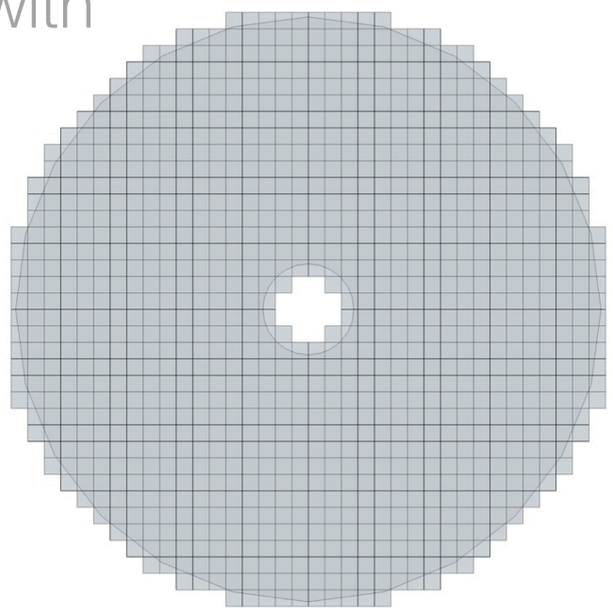
- What is required for robust forward tracking?
- Are stereo measurements required forward? elsewhere?
- What technology is needed for small radius portions of forward disks?
- How is instantaneous current for pulsed power delivered?
- How problematic are Lorentz forces from pulsed currents?

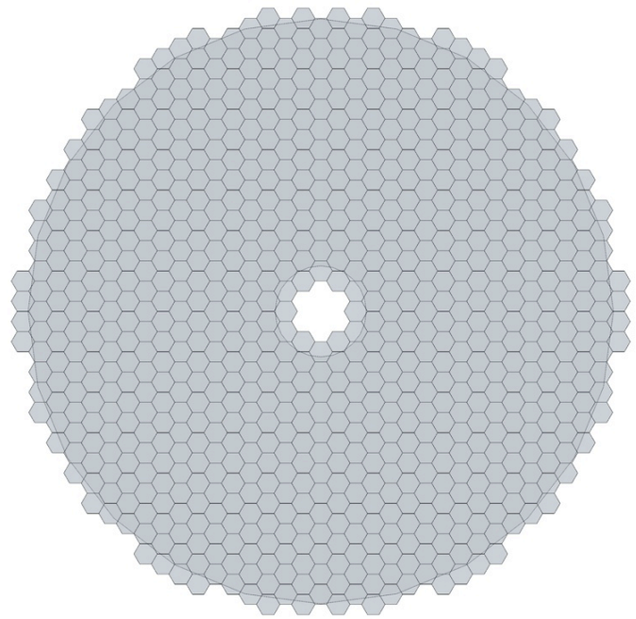
Forward Tracking

- Forward layout still in question: more simulation effort required
- Issues demanding hardware R&D independent of module shape
  - Short module concept designed with double-sided modules in mind
  - Long-module mechanics may exclude some options

We must have an answer soon!





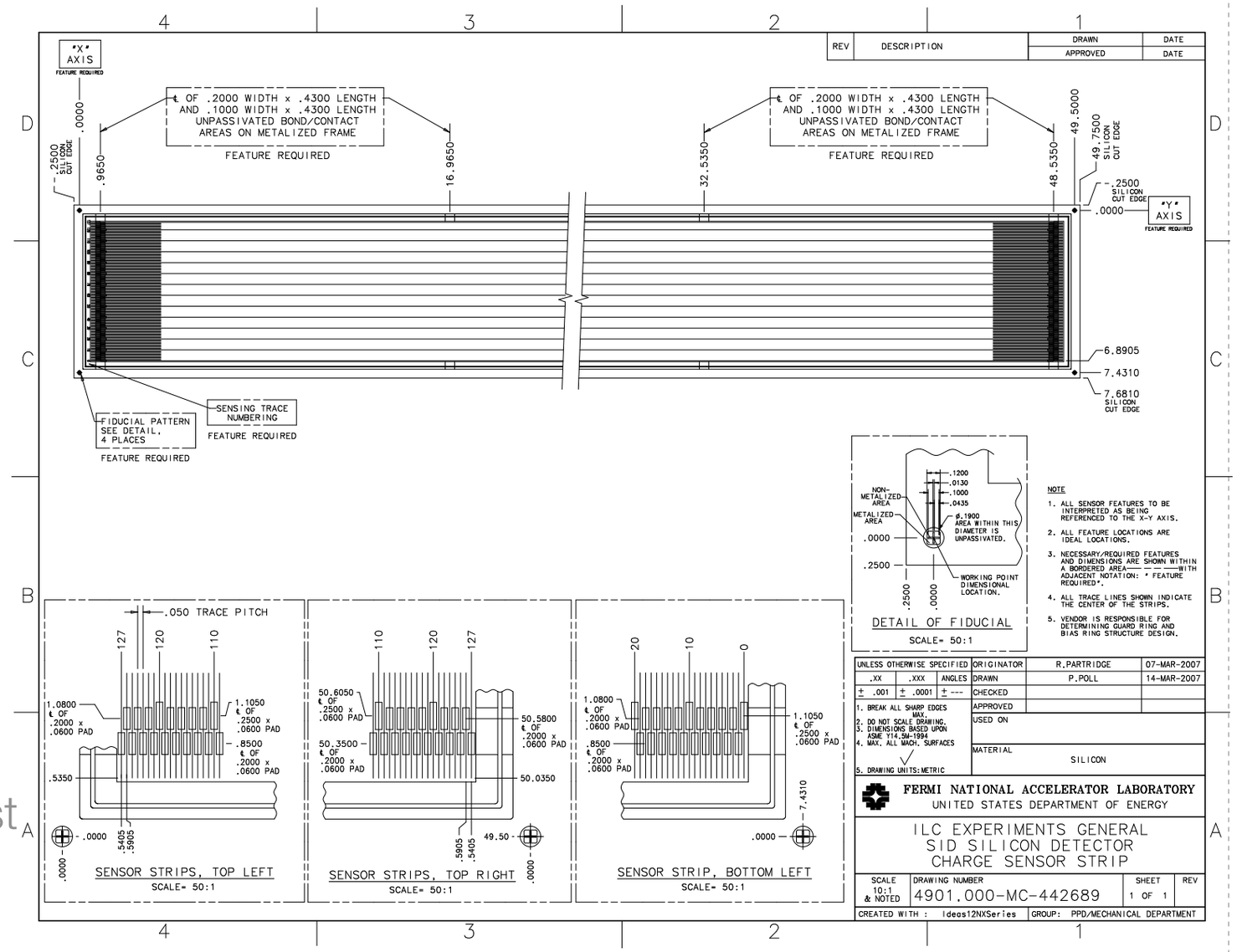


Charge Division Readout

Brown, SCIPP/UCSC

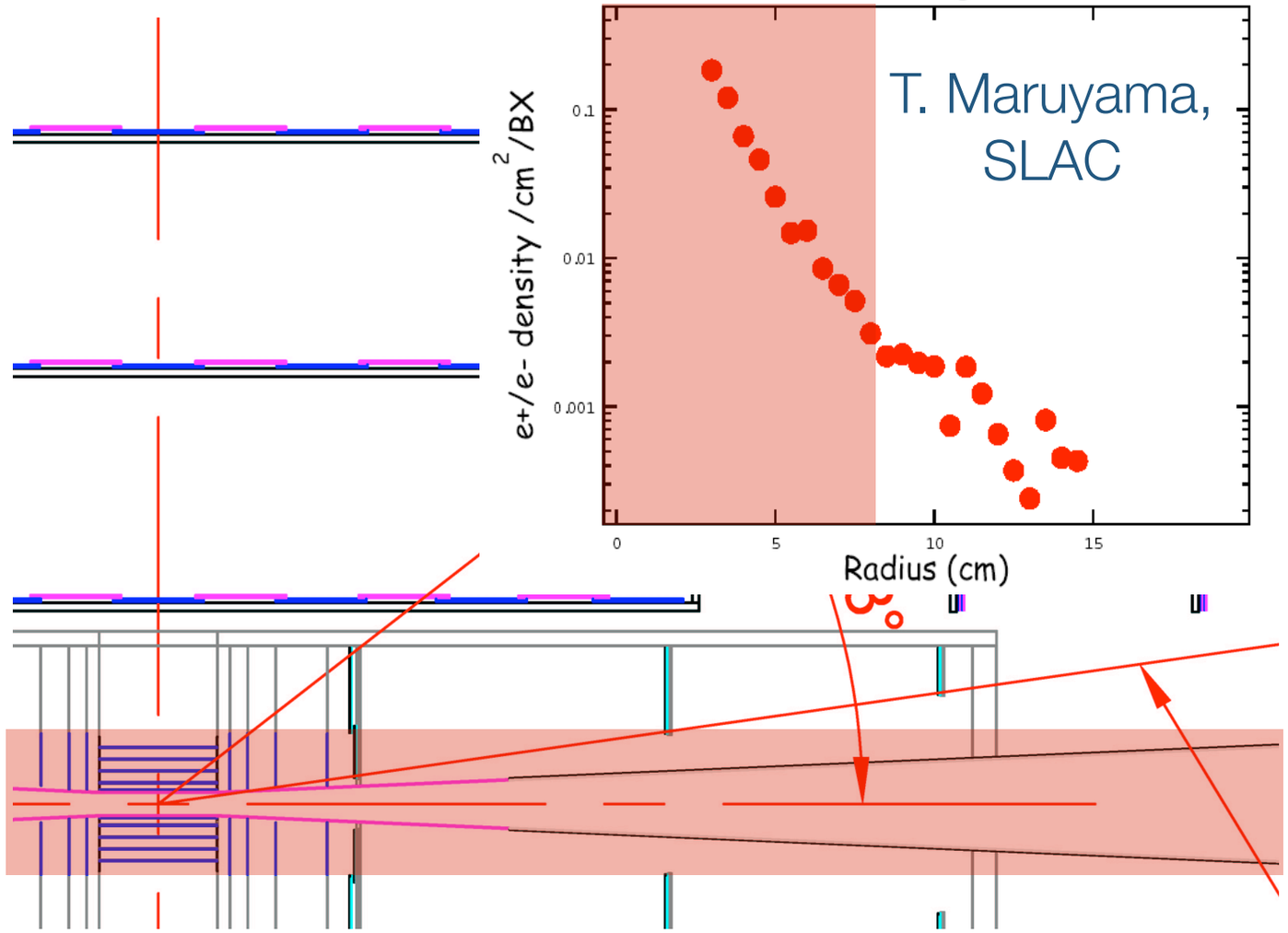
Obtain 3-d measurement by instrumenting both ends of strip

- Like double-sided modules, could be used forward, in barrels if necessary
  - No second sensor: less material, cost
  - Somewhat less precision: ~5mm along strip in best case
- Test sensor included with double-metal sensor submission
- Will design and fabricate optimized test chip to evaluate technique



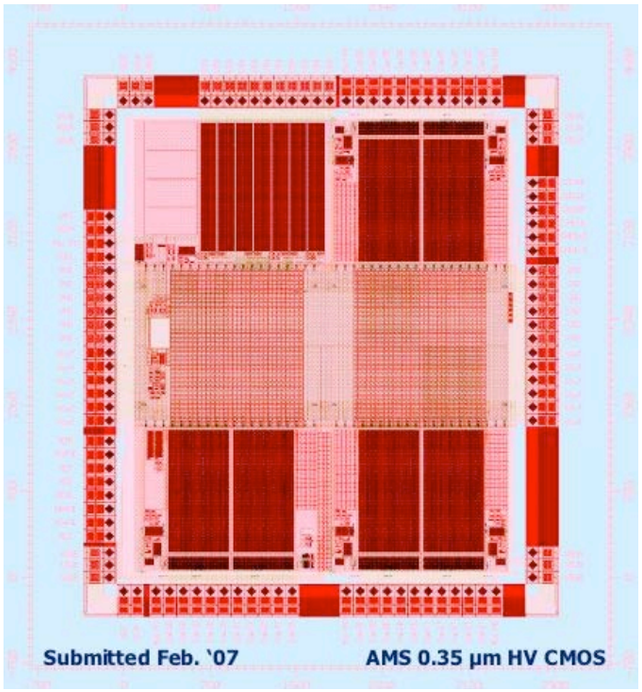
Far Forward

- Occupancies at smallest radii are quite large
- One small piece of forward disks will be problematic for 4-buffer KPiX
- Could require modified KPiX, continuous readout (LSTFE) or pixels of some kind
- This requires a significant new effort

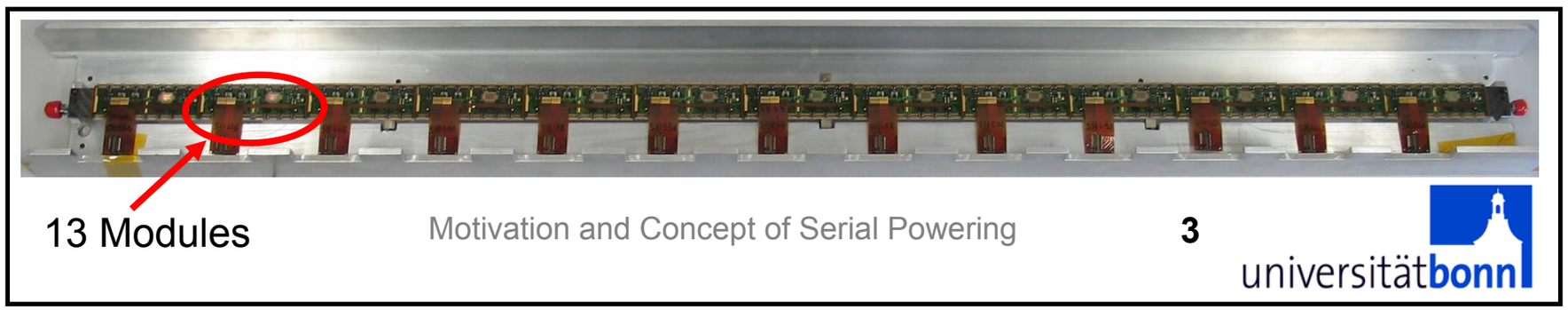


Powering

- DC/DC conversion, serial powering are hot topics
  - Significant work done for LHC, continuing for SLHC
  - We are learning, but a major new effort is required
- Pulsed power an issue for many ILC subdetectors
  - Instantaneous current for tracker 5000 amps
  - Lorentz forces could be problematic
  - Letting VTX take the lead but effort for tracker is needed

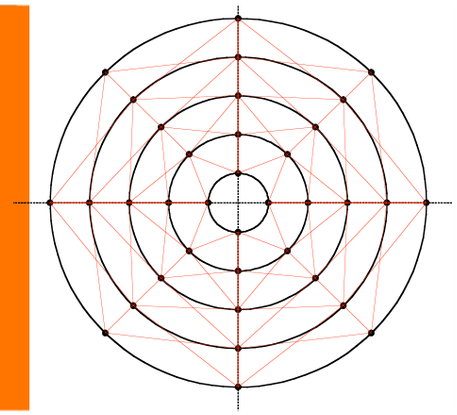


DC/DC ASIC (P. Denes, LBNL)



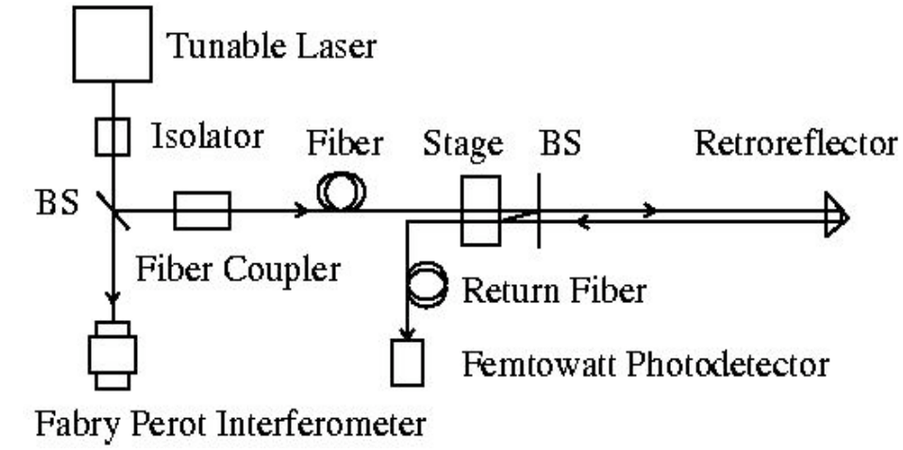
Dual Laser FSI

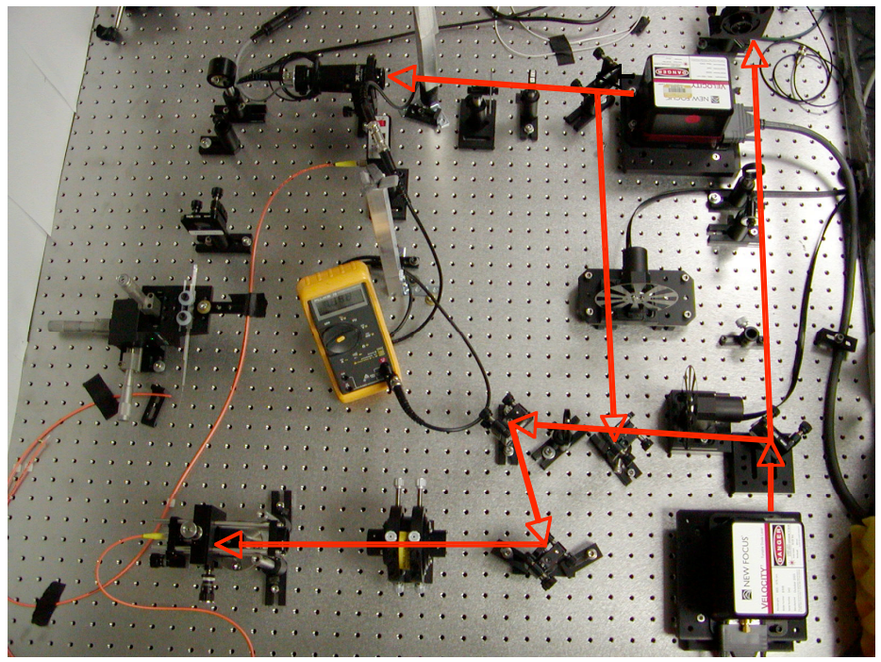
U. Michigan



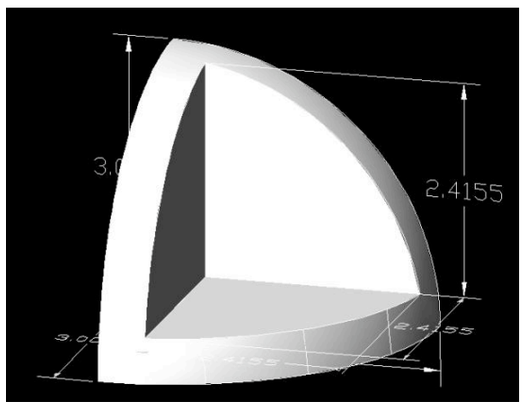
Aggressive material trimming, pulsed-power and push-pull may create need for alignment monitoring

- Absolute distances measured to ~200nm in real-world conditions with commercial optics
- Working on miniaturization: initial testing achieved 70nm precision with corner cube array
- Also applicable to VTX, TPC





hep-ph/0609187 - NIM A, Volume 575, Issue 3, p. 395-401.



SiD Material Estimates

FNAL, SLAC

Scrupulous attempt to account for material

- Included: sensors, chips, cables, connectors, bypassing, glue, module supports, module mounts, overlaps, power distribution boards, DAQ for baseline design
- Not included: alignment monitoring, mounting to ECAL, voids in large scale support structures

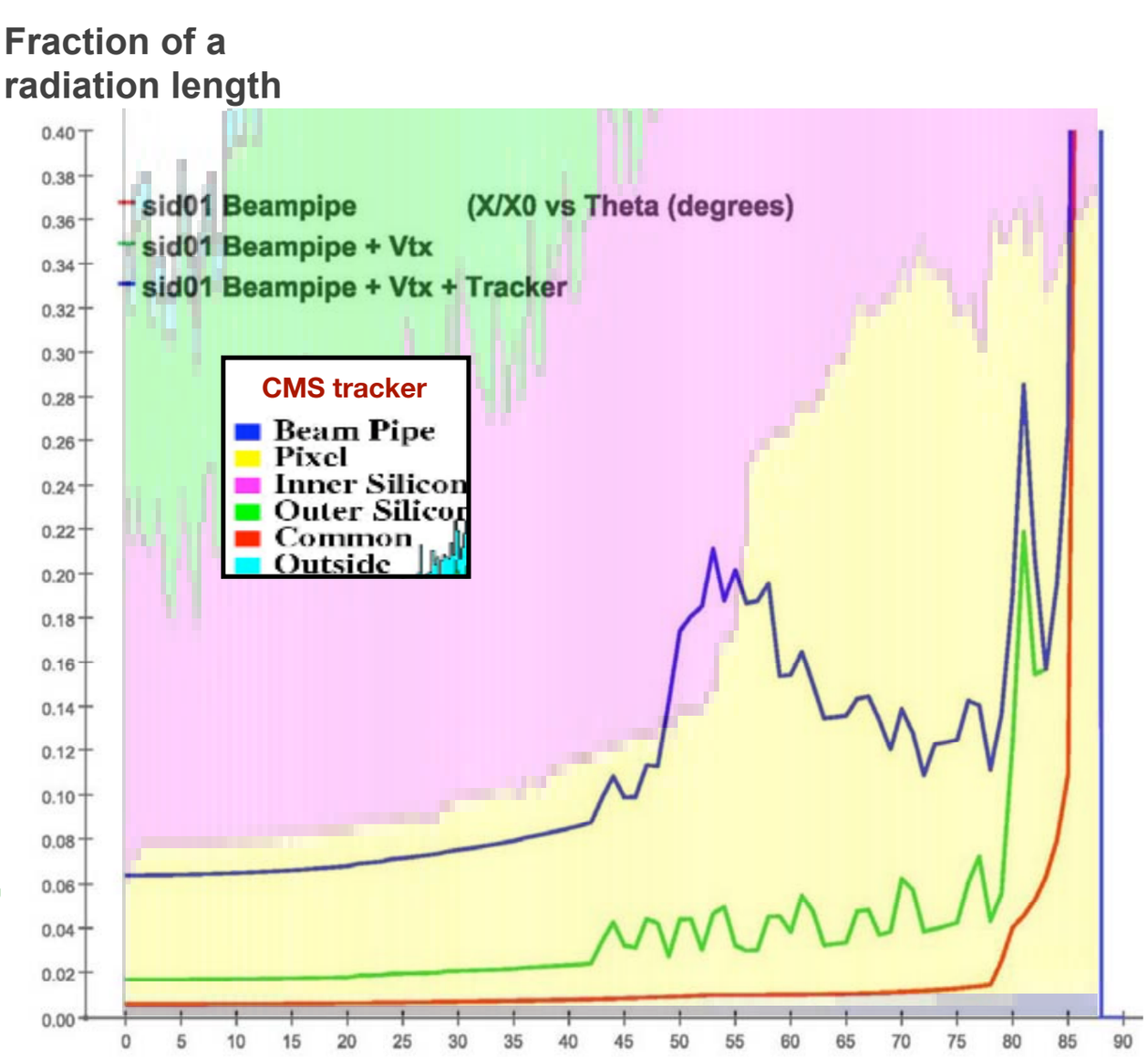
SiD Tracker Material
V0.23

Tim Nelson

January 14, 2007

1 Introduction

This document describes the current understanding of material necessary for an ILC tracking detector based on the SiD detector concept and utilizing short silicon readout modules. While no description of detector material is ever complete or perfectly precise, a reasonable model of



Getting There From Here

- Discussion of deadlines, timelines and important milestones

Summary