DIF for ECAL

some Technical aspects
- Mechanics
- Signals

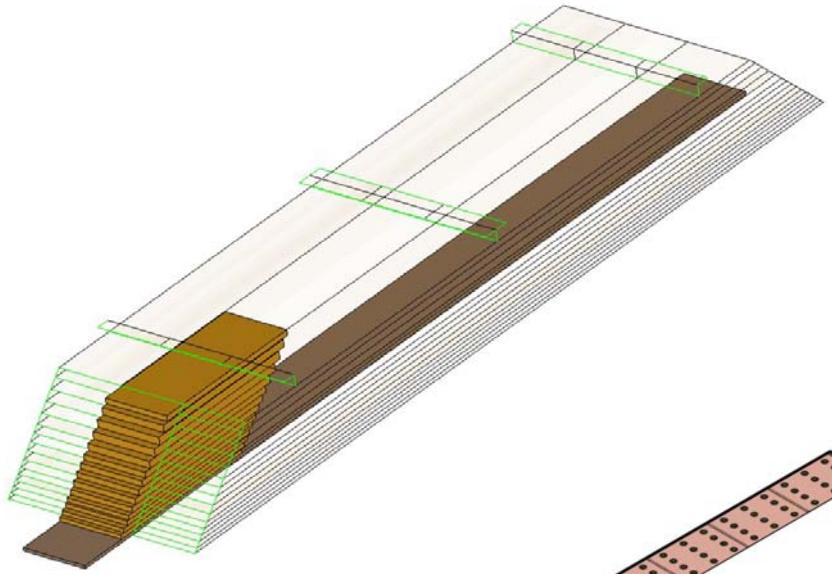
DIF working group

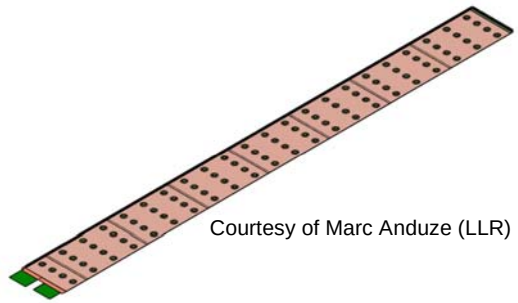
R. Cornat - LPC

EUDET Module (ECAL)

Concept : to be the most representative of the final detector module

- 15 Detector slabs with FE chips integrated
  - 1 long and complete slab (L=1.5m)
  - 14 short slabs to obtain a complete tower of detection (typ. L=30 cm?) and design of compact outlet.

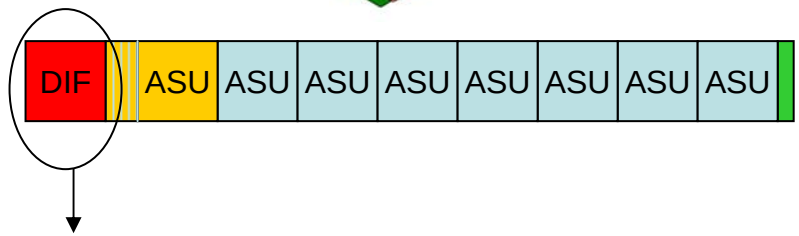




Courtesy of Marc Anduze (LLR)

SLAB :

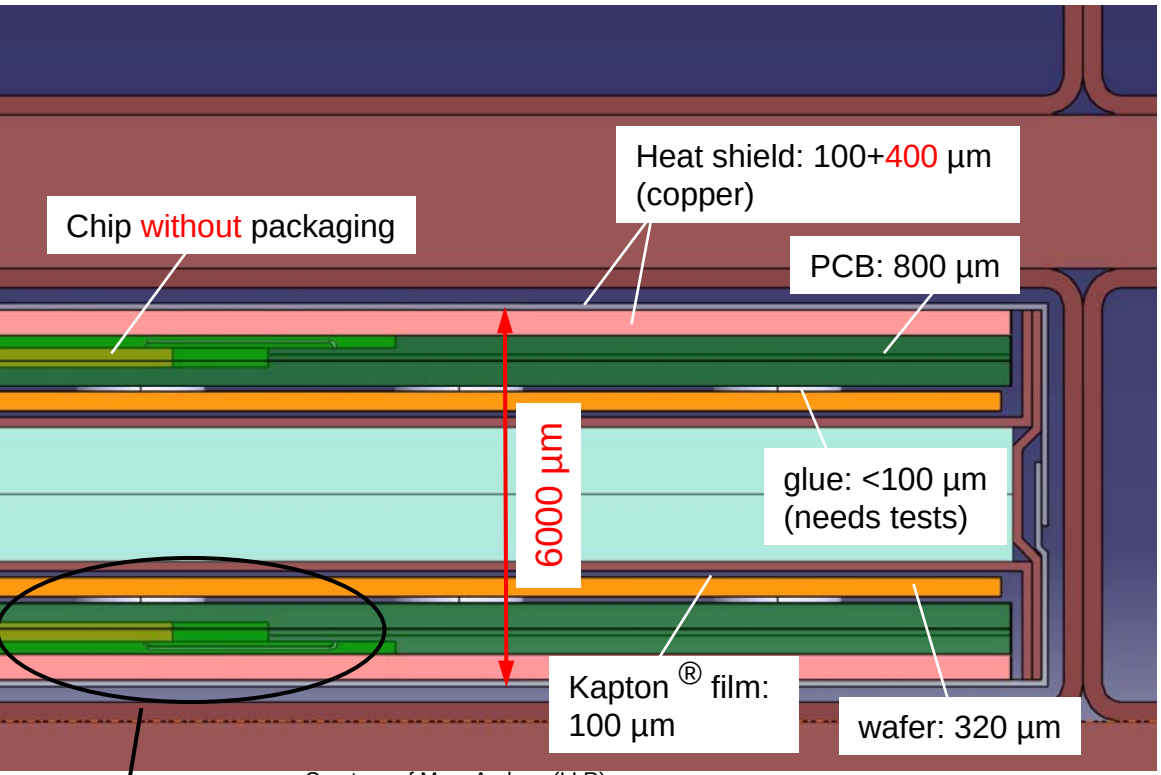
- 1 termination cap
- 7 stadard ASUs (Active Sensor Unit)
  - 18.5 x 18.5 cm2
  - 4 wafers of 18x18 pixels
  - 4 SKIROC chips per wafer (81 channels each)
- 1 termination ASU
  - variable length according to the layer
  - 15 layers
- 1 DIF



Connexion ?
Layout ?

Mechanical constraints for the DIF

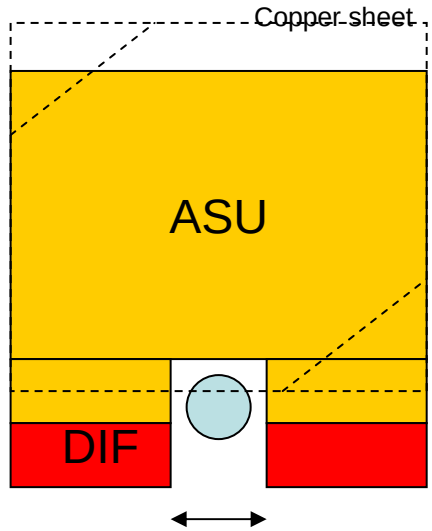
The expected alveolar thickness is 6.5 mm



Courtesy of Marc Anduze (LLR)

Design EUDET Slab

Heat shield has to be connected to a cold pipe
This pipe crosses DIF and/or termination ASU
A 20 mm hole must be foreseen at the end of the SLAB

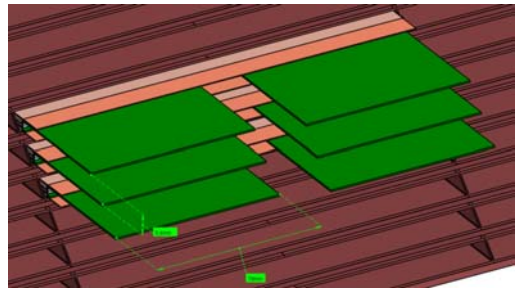


Very thin space is allowed for DIF components

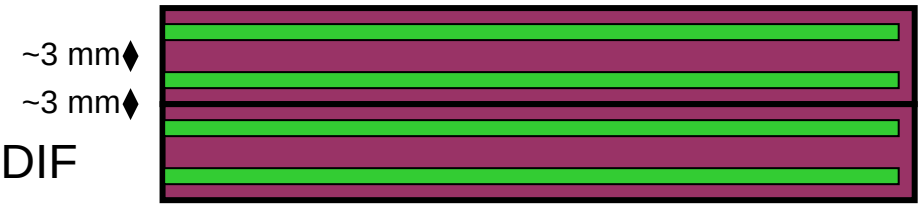
- 50 mm x 80 mm x ~6 mm (final)
- X mm x 180-80 mm x Z mm (EUDET relaxed constraints/options)

Last ASU of SLAB - DIF

- DIF options
  - Common DIF with additional adapter specific to the detector (power, …)
    - Adds a connector
    - Differs from “ILC” version
    - Rigidity of the end of the SLAB not ensured
    - But…common DIF
  - Mostly common DIF
    - Shared designs
    - But remains specific to detector

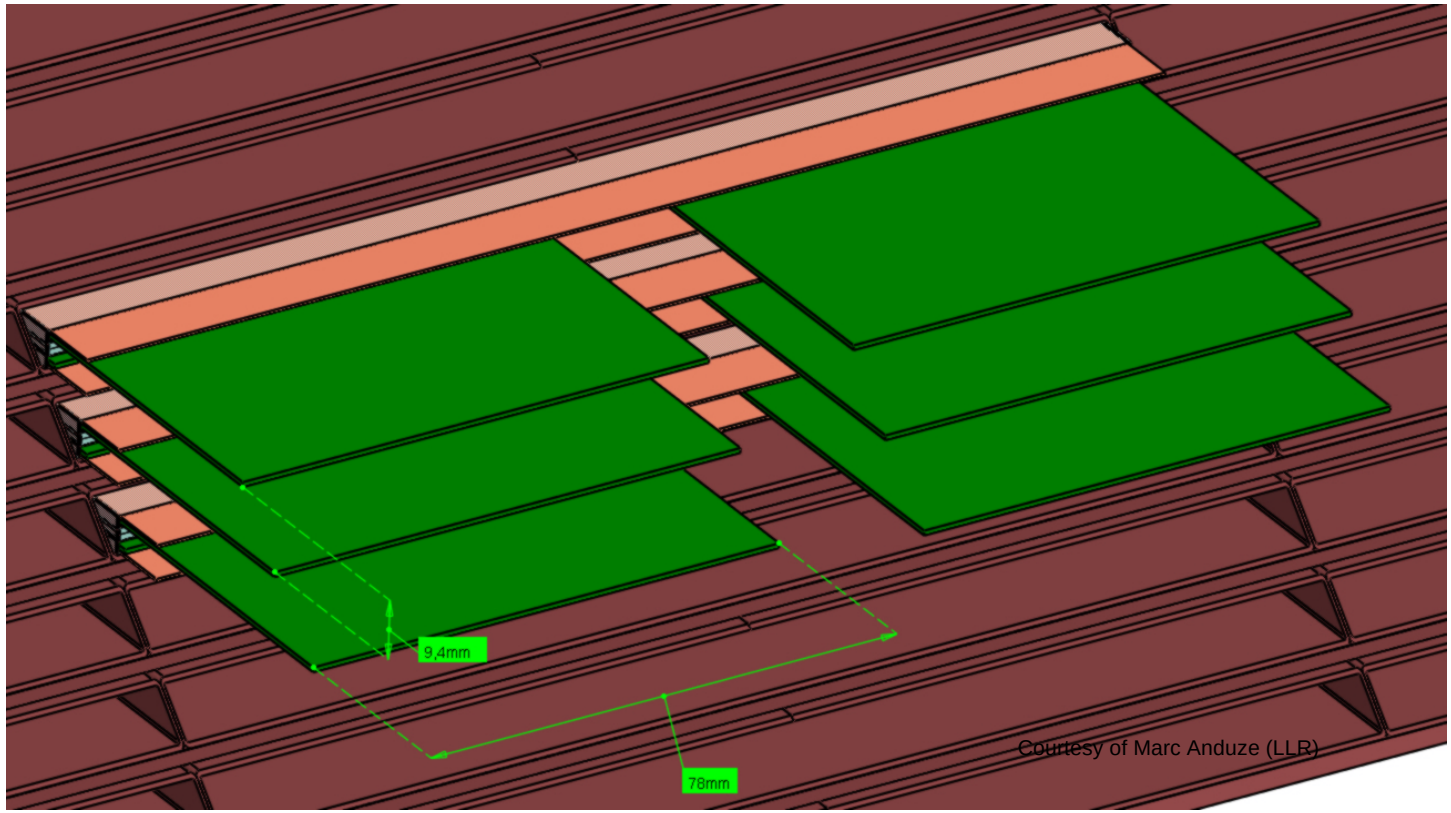


- DIF location
  - Full width
    - Poor 3 mm space allowed for DIF components



  - Half width (see next transparency)

Mechanical constraints for the DIF



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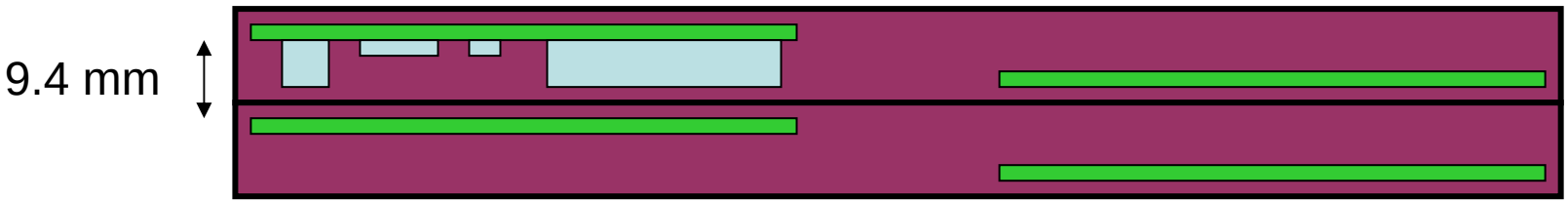
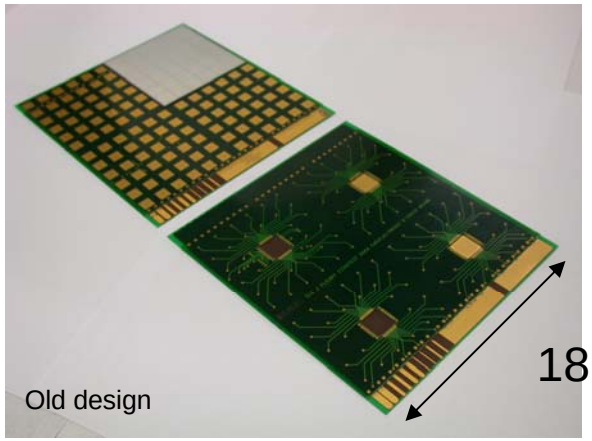


6 to 7 mm allowed for components but reduced width

ASU edge connector

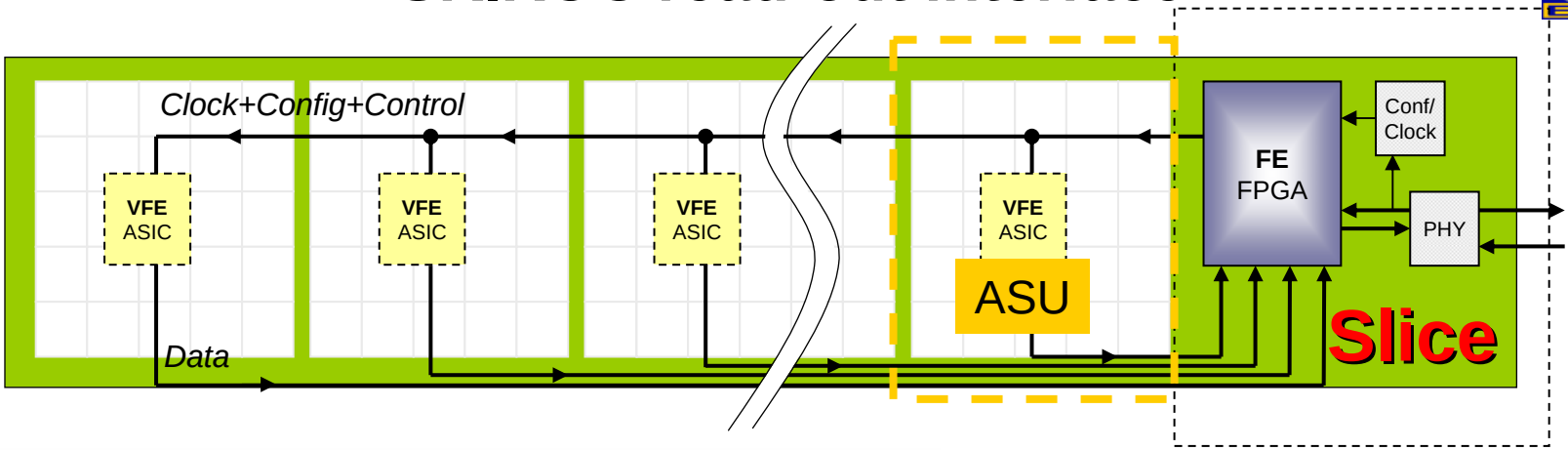


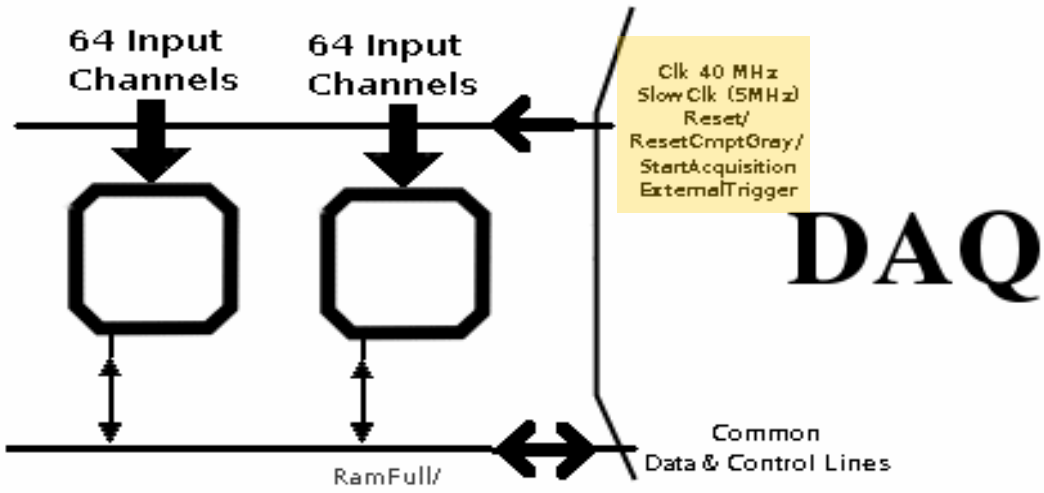
ASU will be glued edge to edge
Glue provides electrical contact

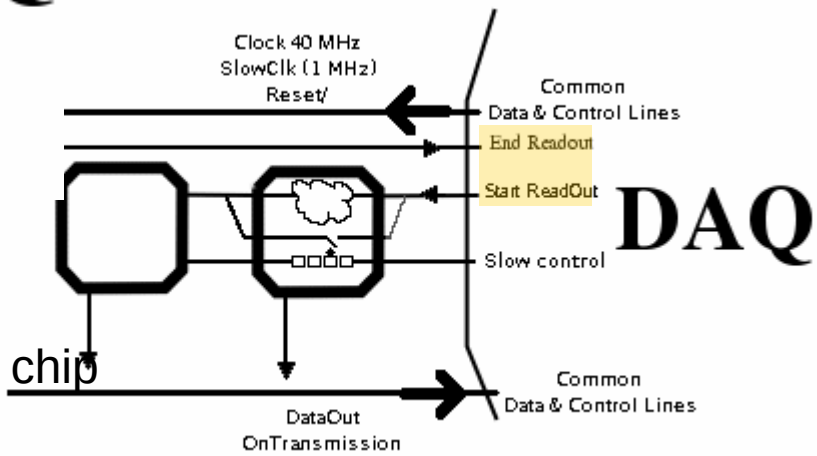
Glue dot diameter reach 2 mm
allowing a maximum number of contacts of about 3/cm.

Power supplies contacts extend by about 8 cm
25 to 30 signal contacts are allowed for a whole SLAB

SKIROC read-out interface







Design based on buses

Chip selected by a token circulating from chip to chip

SLAB-DIF connector System requirements

- High Voltage
- Power
- Bias
- Clock, Control and Commands (CCC)
- Slow control
- Read-out
- Probe

- Reliability
- Power dissipation
- Testability
- Signal integrity
- Timing
- Mechanical constraints
- Successive versions of ROC chips

ASU-DIF
ASU connector

ASU/SLAB connector I/O — LPC 22/06/07

CAT	NAME		
HV			
POWER	GND		1
	3.3V		1
BIAS			0
REFERENCE			0
CCC	clkp 40MHz	1 LVDS	O

Category	Signal	Function	I/O for slab	Validon	ECAL (SKIROC)	DHCAL (HARDROC)	AHCAL (SPIROC)
operation control							
	reset*	global reset of complete ASIC	I	low	LVCMOS	LVCMOS	LVCMOS
	pwr_on	power-cycling control	I	high	LVCMOS	LVCMOS	LVCMOS
	StartAcq	start data acquisition	I	high	LVCMOS	LVCMOS	LVCMOS
	start_conv_DAQ	start ADC conversion	I	high			LVCMOS
	no_trig	erase active analogue column	I	high			LVDS
	Val_Evt	external validation of event	I	high	LVDS	LVDS	LVDS
	trig_ext	external trigger	I	high	LVCMOS	LVCMOS	LVDS
	RAZ_Chn	reset for internal RS flip flops (discriminator outputs)	I	high	LVDS	LVDS	
slow control							
	clk_sc	slow-control shift-reg. clock 1MHz	I	rising	LVCMOS	LVCMOS	LVCMOS
	srin_sc	data input of slow control shift-reg.-chain	I	high	LVCMOS	LVCMOS	LVCMOS
	srout_sc	output of slow-control shift-	O	high	LVCMOS	LVCMOS	LVCMOS
	SCASat	analogue pipeline full	O	high			open coll
	RamFull	digital RAM full	O	high	open coll	open coll	
	RamFull_ext	stops current acquisition if an HC RAM is full	I	high		LVCMOS	
	bypass_in	bypass for token signal for readout	I	high			LVCMOS
readout	bypass_out	bypass for token signal for readout	O	high			LVCMOS
debugging							
	hold_ext	external channel trigger	I	high		LVCMOS	LVDS
	Raz_chn_int		O			(4)	
	Out_Trig_int		O			(4)	
	RS_trig0	spy RS outputs	O	-		LVCMOS (4)	
	RS_trig1	spy RS outputs	O	-		LVCMOS (4)	
	Trig0	spy discrim. outputs	O	-		(4)	
	Trig1	spy discrim. outputs	O	-		(4)	
Power							
	positive supply	+3.5V (digital + analog)	I	-	power	power	power (?)
	additional supply	+5V (DAC)	I	-			power (?)
	common ground	GND	I	-	power	power	power (?)
	detector bias	HV	I	-	power	power	power (4)
Calibration and Monitoring							
	Sensor_Power	Power for temperature monitors	I	-			power (1)
	Temp	output of temperature monitors	O	-			analogue (6?)
	Trigger_Power	power for trigger logic	I	-			power (2)
	Charge_Power	power for charge injection circuits	I	-			power (2)
	LED_Power	power for light calibration system	I	-			power (2)
	VCALIB	analogue level of calibration signal	I	-			analogue (1)
	Trigger	fast trigger of calibration system	I	rising			LVDS
	CTest	charge injection	I	-	analogue	analogue	

This list already includes 25 signals !

- close to the limit

Discussions for optimization, reliability, … are ongoing

Next step is to finalize system level integration (architecture, …) for EUDET prototype

Conclusion

Stringent mechanicals constraints
Choices should be done to remains close to what a final version could be

DIF task force
- to identify common part of the designs (ECAL, AHCAL,DHCAL)
- to work on system level integration
- manage all constraints (feasibility, reliability, tests…)

Firsts steps to list SLAB-DIF interface signals and optimisation

Specifications document at system level by the end of this year